

VLSI Assignment #1 - Tanmay Pathak

2018102023

Question 2a)

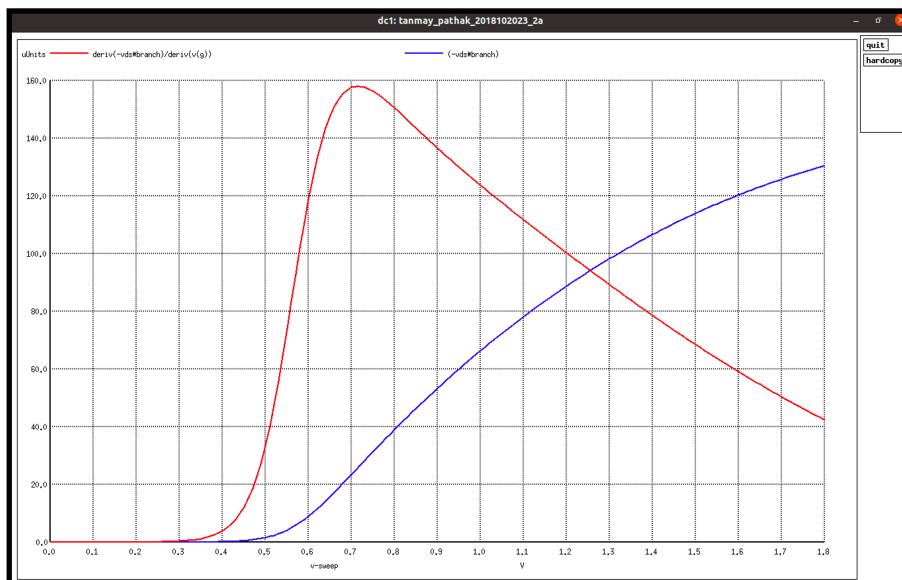
The netlist used for the question is given below

```
Netlist for 2(a) - TANMAY PATHAK - 2018102023
.include TSMC_180nm.txt
.param SUPPLY=1.8
.param VGG=1.5
.param LAMBDA=0.09u
.param width_N={20*LAMBDA}
.global gnd vdd

VGS G gnd 'SUPPLY'
VDS D gnd gnd CMOSN W={width_N} L={2*LAMBDA} AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

.dc VGS 0 1.8 0.01
.control
set hcopypcolor = 1 *White background for saving plots
set color0=white ** color0 is used to set the background of the plot (manual sec:17.7)
set color1=black ** color1 is used to set the grid color of the plot (manual sec:17.7)
run
* Plotting slope of Id vs Vgs for the linear region
set curlplottitle="Tanmay_pathak_2018102023_2a"
plot deriv(-VDS#branch)/deriv(V(G)) (-VDS#branch)
hardcopy slope_id_vg.ps deriv(-VDS#branch)/deriv(V(G)) linear_id_vs_vgs.ps (-VDS#branch)
.endc
```

Output - Graph



$$V_T = 0.5511V$$

Observations - To calculate V_T

- 1) I_d varies linearly with V_{GS} and V_{Ds} is constant
- 2) To get the values of V_T approximate the curve I_d vs V_{GS} in the triode region and find the intercept on the X- axis
- 3) We first find the point with the slope is maximum, and draw a tangent at this point. The x-intercept to this point gives us the value of V_T

Question 2(b)

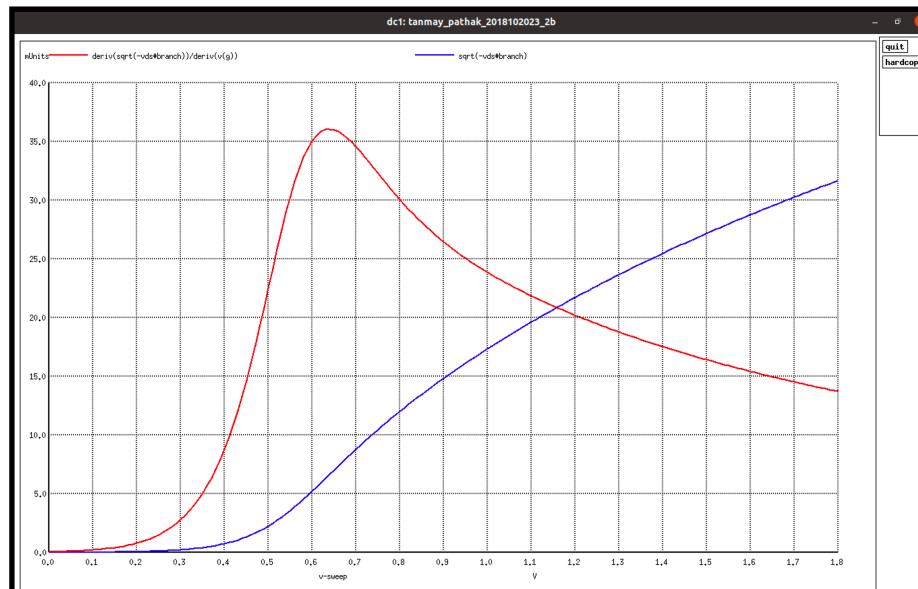
The netlist used for the question is given below

```
Netlist for 2(b) - TANMAY PATHAK - 2018102023
.include TSMC_180nm.txt
.param SUPPLY=1.8
.param VGG=1.5
.param LAMBDA=0.09u
.param width_N={20*LAMBDA}
.global gnd vdd

VGS G gnd 'SUPPLY'
VDS D gnd 1.8
M1 D G gnd CMOSN W={width_N} L={2*LAMBDA} + AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

.dc VGS 0 1.8 0.01
.control
set hcopypscolor = 1 *White background for saving plots
set color0=white ** color0 is used to set the background of the plot (manual sec:17.7)
set color1=black ** color1 is used to set the grid color of the plot (manual sec:17.7)
run
* plotting slope of Id vs Vgs for the linear region
set curplottitle="Tanmay_Pathak_2018102023_2b"
plot deriv(sqrt(-VDS#branch))/deriv(V(G)) sqrt(-VDS#branch)
hardcopy Q2_B.ps deriv(sqrt(-VDS#branch))/deriv(V(G)) sqrt(-VDS#branch)
.endc
```

Output - Graph



$$V_T = 0.4559\text{V}$$

Observations - To calculate V_T

- 1) I_d varies quadratically with respect to V_{GS} . To get a linear curve, we take square root on both sides of the equation.
- 2) Now, we can assume the slope of the linear approximation as the maximum slope of the $\sqrt{I_d}$ vs V_{GS} plot.
- 3) Again, we first find the point with the slope is maximum, and draw a tangent at this point. The x-intercept to this point gives us the value of V_T .

Question 2(c)

We observe a difference in the values of V_T in the cases (a) and (b). This can be explained by the Drain Induced Barrier Lowering (DIBL) effect. This effect is prominent in MOSFET devices with shorter channel length. This is because with shorter channel length, the drain voltage assists in formation of depletion region and thus we can achieve on condition with lower gate voltage. The equation for DIBL is given by: $V_T = V_{TO} - \eta (V_{DS})$

Question 3 - NMOS

The netlist of the question is given below

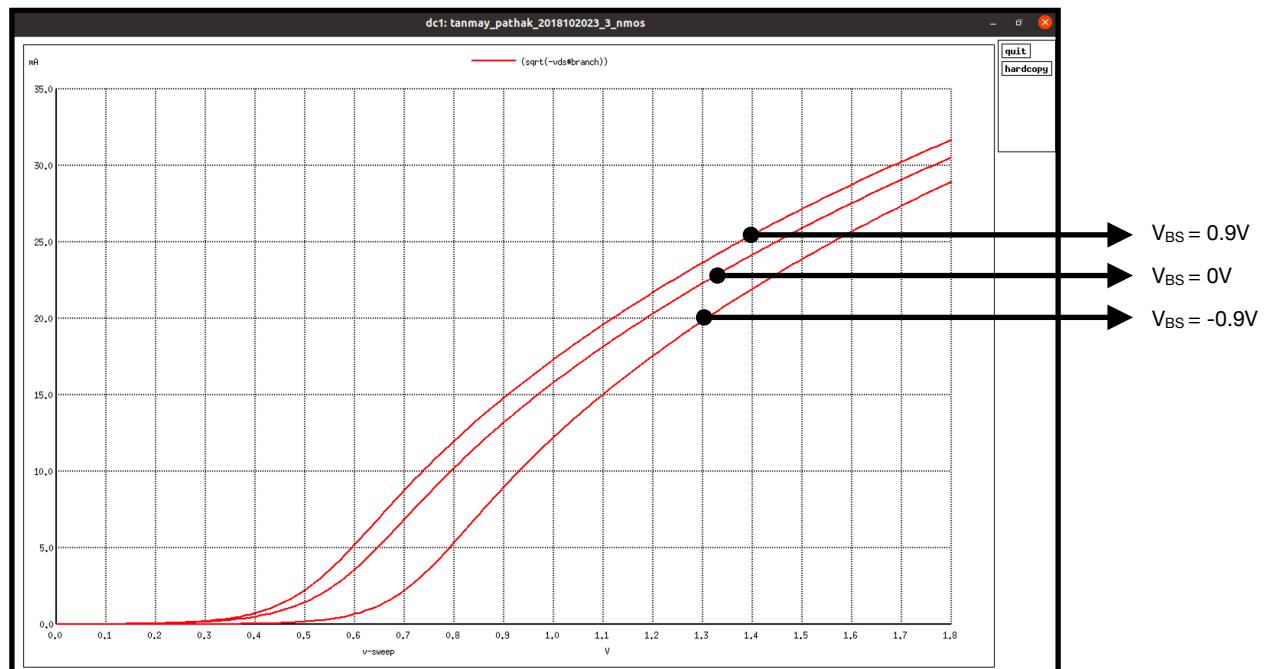
```
Netlist for 3-NMOS - Tanmay Pathak - 2018102023
.include TSMC_180nm.txt
.param SUPPLY=1.8
.param LAMBDA=0.09u
.global gnd vdd

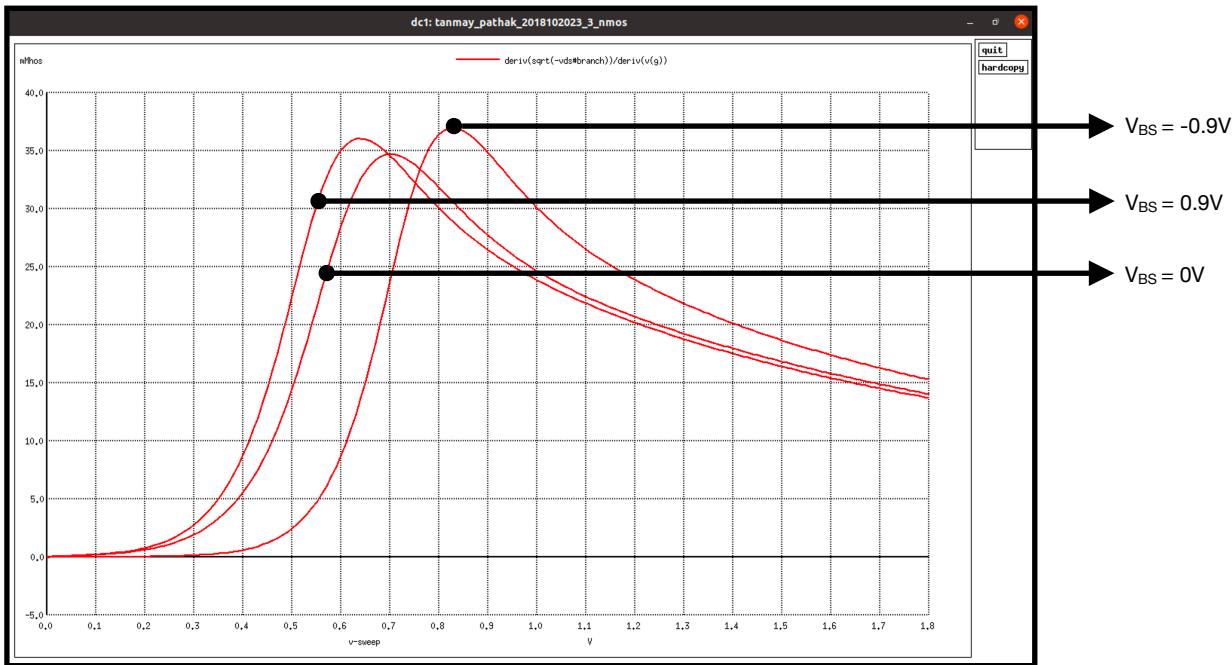
VGS G gnd 'SUPPLY'
VDS D gnd 1.8
VBS B gnd 0
.param width_N=[20*LAMBDA]

M1 D G gnd B CMOSN W={width_N} L={2*LAMBDA} + AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}
.dc VGS 0 1.8 0.01 VBS -0.9 0.9 0.9

*.dc VGS 0 1.8 0.01
.control
set hcopypscolor = 1 *White background for saving plots
set color0=white ** color0 is used to set the background of the plot (manual sec:17.7)
set color1=black ** color1 is used to set the grid color of the plot (manual sec:17.7)
set color2= red
set color3 = blue
run
* plotting slope of Id vs Vgs for the linear region
set curplottitle="Tanmay_Pathak_2018102023_3_NMOS"
plot (sqrt(-VDS#branch))
plot deriv(sqrt(-vds#branch))/deriv(V(G))
*hardcopy Q2_B.ps deriv(-VDS#branch)/deriv(V(G)) sqrt(-VDS#branch)
.endc
```

Output - Graph





Observations

- 1) I_d varies quadratically with respect to V_{GS} . Again in order to get a linear form, we take the square root on both sides.
- 2) $\sqrt{I_d}$ is linearly proportional to $V_{GS} - V_{TH}$. Thus we can now calculate the value of V_{TH} by considering the x-intercept value.
- 3) The x-intercept of the linear approximation shifts for different values of V_{BS} . For negative V_{BS} , we can see the x-intercept shifts away towards right from that of $V_{BS} = 0$ V and that for positive value shifts the intercept towards left from that of $V_{BS} = 0$ V.
- 4) Calculation of V_{TH} done similarly to Q2.

V_{BS}	V_T	μC_{ox}
0.9V	0.39V	$238.8 \mu A/V^2$
0V	0.451V	$259.6 \mu A/V^2$
-0.9V	0.664V	$272.5 \mu A/V^2$

We observe different values of V_{TH} . When a positive voltage is applied at the Body of an NMOS, the potential at the body helps in lowering the energy band resulting in lowering of the threshold voltage. Thus the value of V_T for $V_{BS} = 0.9V$ is lower than that of V_T when body is grounded. Conversely, when negative potential is applied at the body, the energy band will be elevated and thus the threshold voltage will increase. Thus the value of V_T for $V_{BS} = -0.9V$ is higher than that of V_T when body is grounded.

Question 3 - PMOS

The netlist used for the question is given below

```
Netlist for 3_PMOs - TANMAY PATHAK - 2018102023

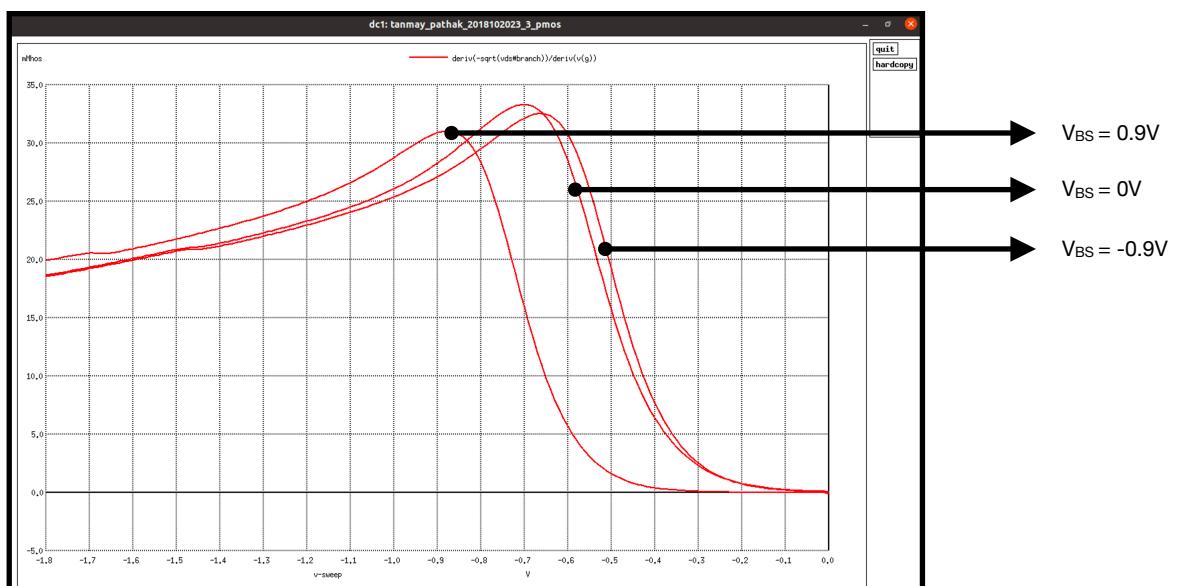
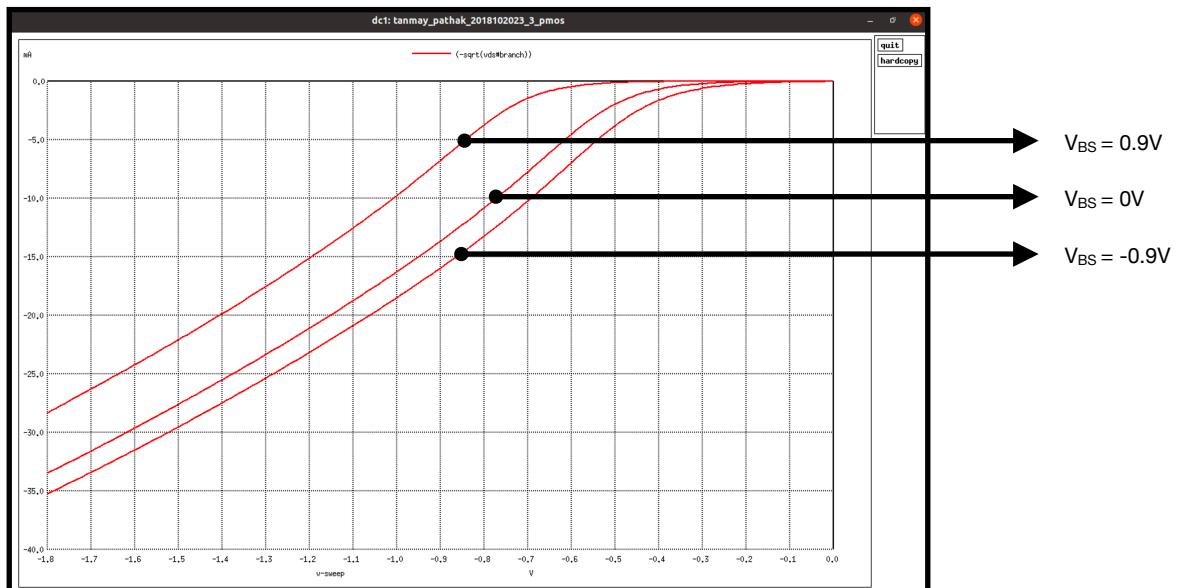
.include TSMC_180nm.txt
.param SUPPLY=1.8
.param LAMBDA=0.09u
.global gnd vdd

VGS G gnd 0
VDS D gnd -1.8
VBS B gnd 0
.param width_P={48*LAMBDA}

M1 D G gnd B CMOS P W={width_P} L=[2*LAMBDA] + AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P} AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}
.dc VGS 0 -1.8 -0.01 VBS -0.9 0.9 0.9
*.dc VGS 0 -1.8 -0.01

.control
set hcopypscolor = 1 *White background for saving plots
set color0=white ** color0 is used to set the background of the plot (manual sec:17.7))
set color1=black ** color1 is used to set the grid color of the plot (manual sec:17.7))
set color2= red
set color3 = blue
run
* plotting slope of Id vs Vgs for the linear region
*set curplottitle="tanmay_pathak_2018102023_3_PMOs"
plot (-sqrt(VDS#branch))/deriv(V(G))
plot deriv(-sqrt(vds#branch))/deriv(V(G)) sqrt(-VDS#branch)
*hardcopy Q2_B.ps deriv(-VDS#branch)/deriv(V(G)) sqrt(-VDS#branch)
.endc
```

Output



Observations

- 1) I_D varies quadratically with respect to V_{GS} . Again in order to get a linear form, we take the square root on both sides.
- 2) $\sqrt{-I_D}$ is linearly proportional to $V_{GS} - V_{TH}$. Thus we can now calculate the value of V_{TH} by considering the x-intercept value.
- 3) The x-intercept of the linear approximation shifts for different values of V_{BS} . For negative V_{BS} , we can see the x-intercept shifts away towards right from that of $V_{BS} = 0$ V and that for positive value shifts the intercept towards left from that of $V_{BS} = 0$ V.
- 4) Calculation of V_{TH} done similarly to Q2.

V_{BS}	V_T	μC_{ox}
0.9V	-0.68V	80.3 $\mu A/V^2$
0V	-0.46V	88.2 $\mu A/V^2$
-0.9V	-0.389V	92.8 $\mu A/V^2$

We observe different values of V_{TH} . The value of V_{TH} for $V_{BS} = 0.9V$ is lower than that of V_{TH} when the body is grounded this is because the positive potential at the body helps in lowering the energy band and it results in lowering of the threshold voltage. Conversely, the value of V_{TH} for $V_{BS} = -0.9V$ is higher than that of V_{TH} when the body is grounded this is because the negative potential at the body helps in elevating the energy band and as a result the threshold voltage will also increase.

Question 4)

The netlist used for the question is given below

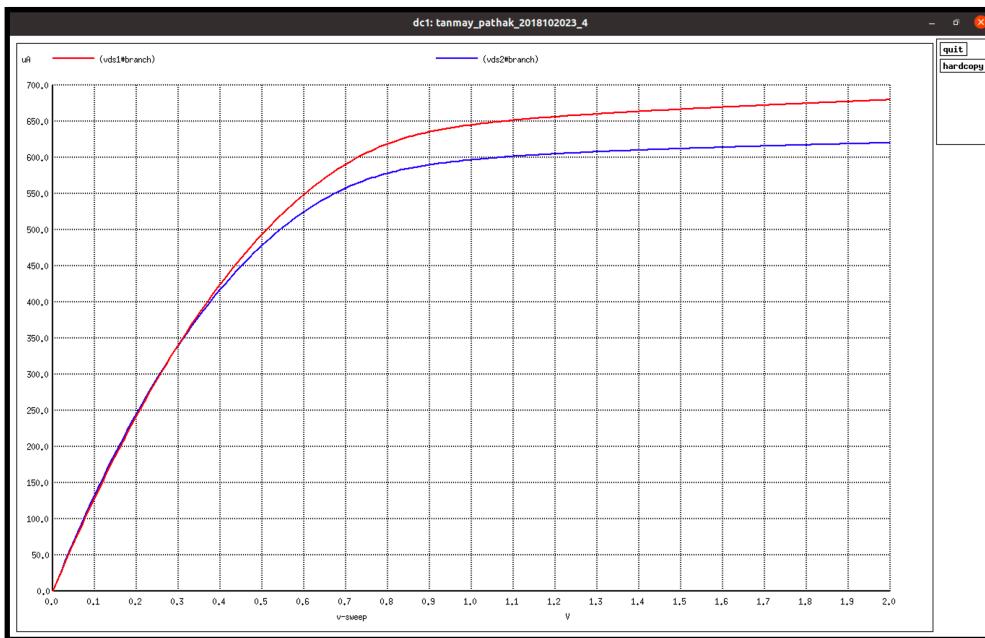
```
Netlist for 4 - TANMAY PATHAK - 2018102023
.include TSMC_180nm.txt
.param SUPPLY=1.8
.param LAMBDA=0.09u
.global gnd vdd

VGS1 G1 gnd 'SUPPLY'
VDS D gnd 1.8
VDS1 D D1 0
VDS2 D D2 0
VGS2 G2 gnd 'SUPPLY'
.param width_N={20*LAMBDA}

M1 D1 G1 A A CMOSN W={width_N} L={2*LAMBDA} + AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}
M2 A G1 gnd gnd CMOSN W={width_N} L={2*LAMBDA} + AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}
M3 D2 G2 gnd gnd CMOSN W={width_N} L={4*LAMBDA} + AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

.dc VDS 0 2 0.01
.control
set hcopypscolor = 1 *White background for saving plots
set color0=white ** color0 is used to set the background of the plot (manual sec:17.7)
set color1=black ** color1 is used to set the grid color of the plot (manual sec:17.7)
set color2= red
set color3 = blue
run
* plotting slope of Id vs Vgs for the linear region
set curplottitle="Tanmay_Pathak_2018102023_4"
plot (VDS1#branch) (VDS2#branch)
.endc
```

Output



Observations

- 1) We can see a significant increase in saturation current with V_{DS} which can be attributed to channel length. At longer channel lengths the current is slightly flatter in saturation since the channel length modulation has less impact ie. see (b).
- 2) Anomalous behaviour seen in plots: For two transistors of length L the equivalent length turns out to be 2L if the widths stay the same. So we expect the two circuits to behave in the similar manner, but from the plots we see that the two circuits behave differently at larger values of V_{DS} .
- 3) The reason for such deviation is Drain Induced Barrier Lowering (DIBL). If we connect two NMOS in series with gates connected, then we can see that one MOSFET will be in saturation region while other will be in triode region. So , DIBL will take its effect on the top MOSFET and thus reducing the threshold voltage for this MOSFET.
- 4) Since the 0.18 μm channel length MOSFET is short channel device, the second order effects will be more prominent in this device, which is the main reason for the difference in the behaviour of the two curves. Moreover, the result of CLM is an increase in current with drain bias and a reduction of output resistance. CLM is more prominent in circuit (a) and hence current is more in case (a) than (b).

Question 5)

The netlist used for the question is given below

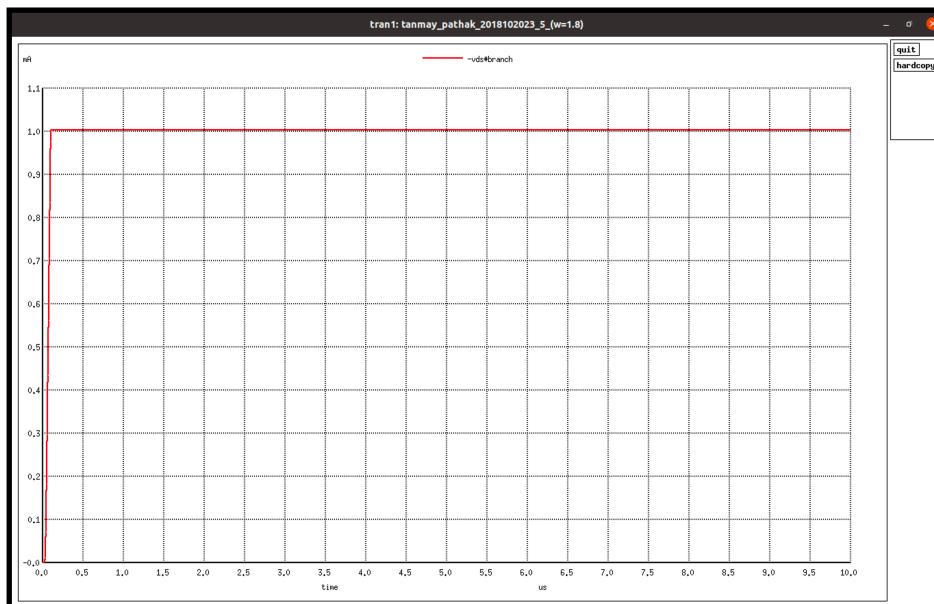
```
Netlist for 5 - TANMAY PATHAK - 2018102023

.include TSMC_180nm.txt
.param SUPPLY=1.8
.param LAMBDA=0.09u
.global gnd vdd

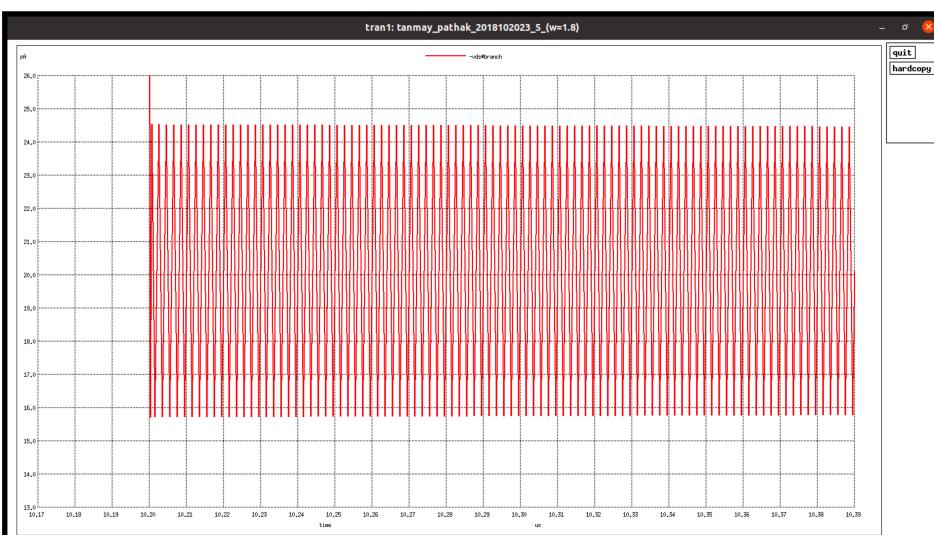
*VGS G gnd 'SUPPLY'
VGS G gnd 0
VDS D gnd 1.8

*.param width_N={20*LAMBDA} *For w = 1.8
*.param width_N={40*LAMBDA} *For w = 3.6
*.param width_N={200*LAMBDA} *For w = 18
*.param width_N={400*LAMBDA} *For w = 36
M1 D G gnd gnd CMOSN W={width_N} L={2*LAMBDA} AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}
Vgs G 0 pulse 0 1.8 0ns 100ns 100ns 10us 20us
.control
tran ins 10us
set hcopypscolor = 1 *White background for saving plots
set color0 = White
set color1 = black
run
set curplottitle="Tanmay_Pathak_2018102023_5_(w=36)"
plot -VDS#branch
.endc
```

Output: $w=1.8\mu\text{m}$

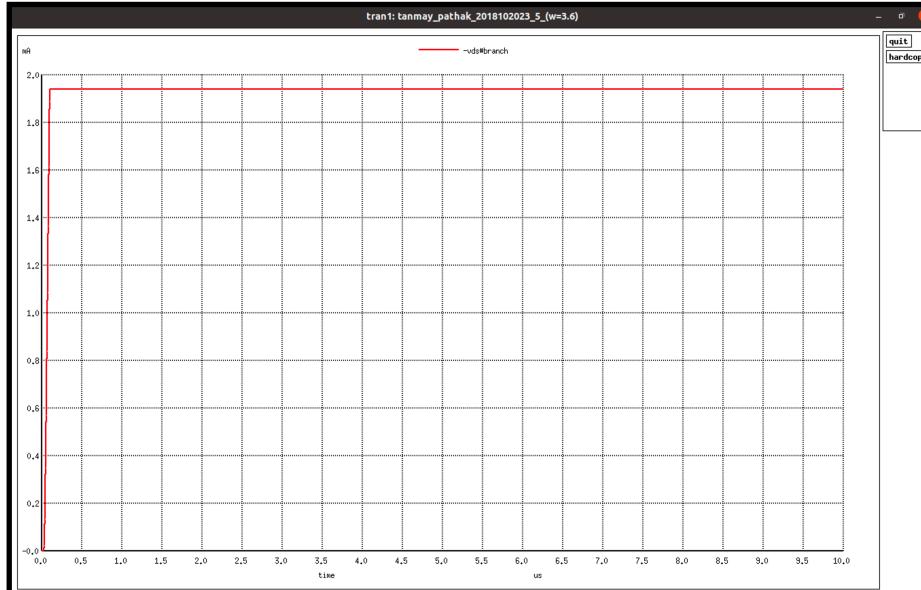


I_{ON}

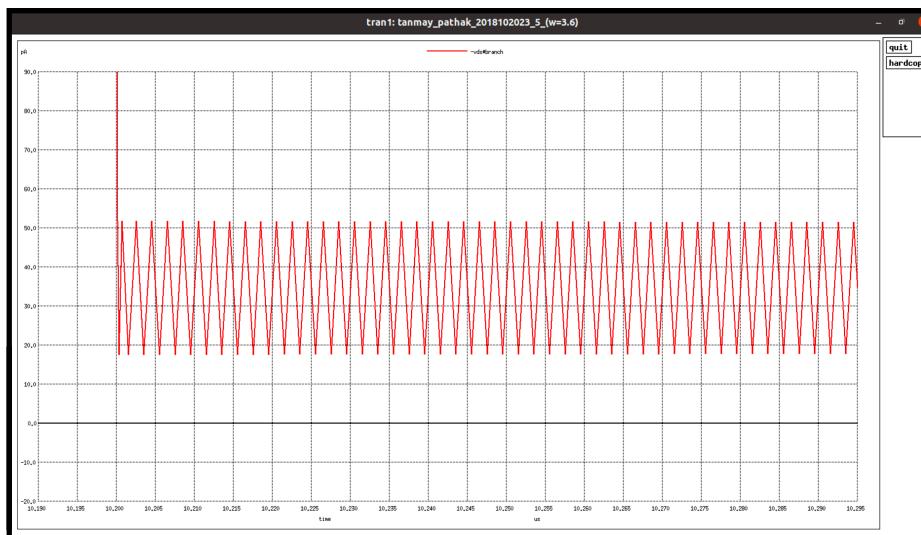


I_{OFF}

Output: $w=3.6\mu m$

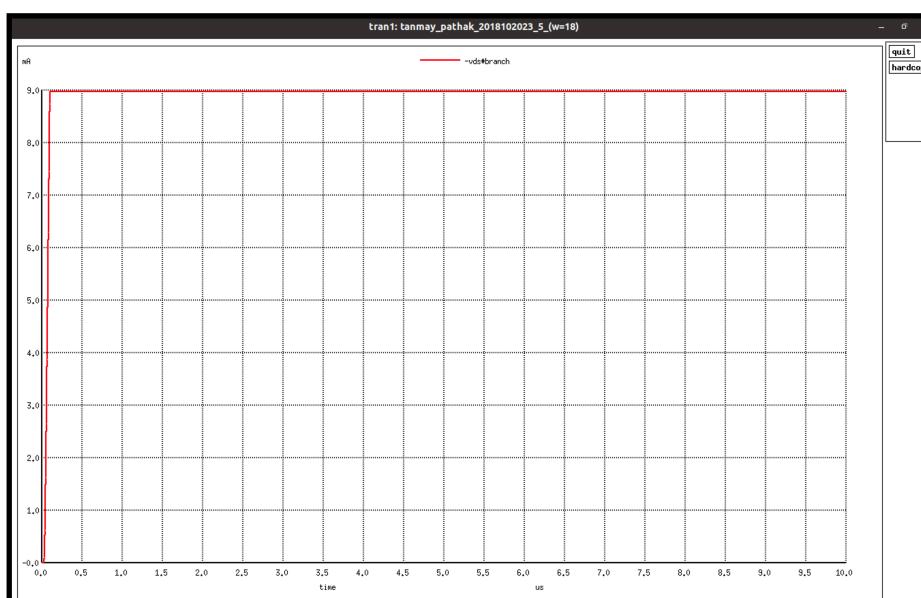


I_{ON}

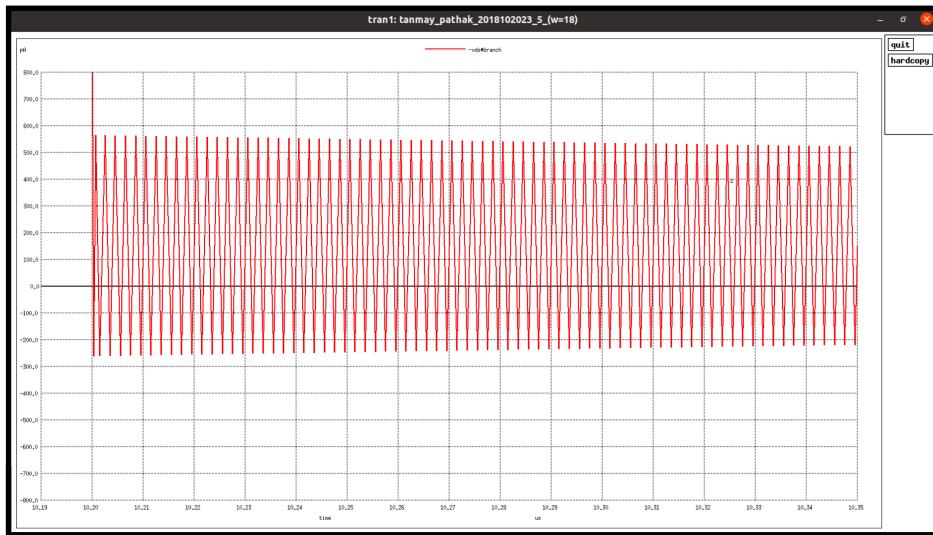


I_{OFF}

Output: $w=18\mu m$

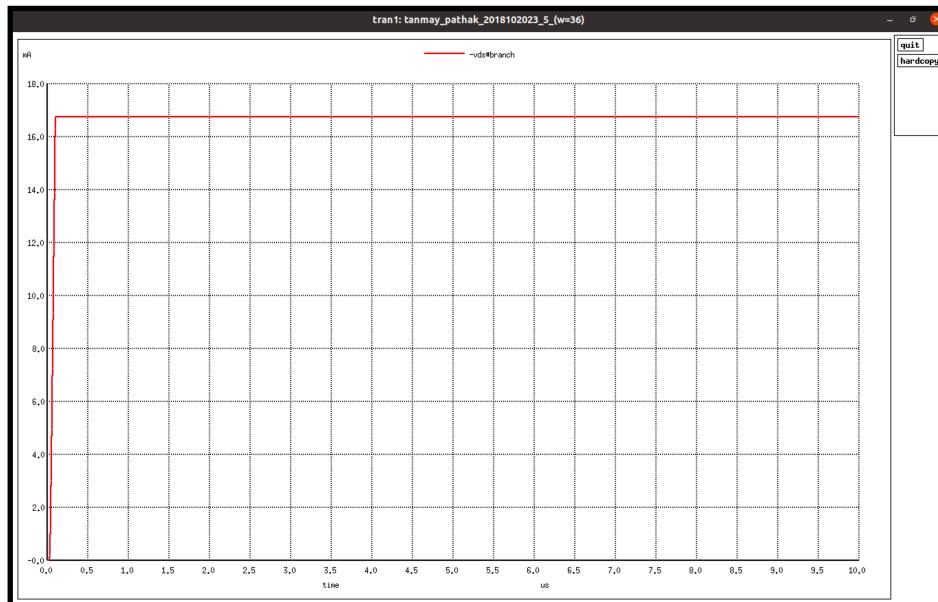


I_{ON}

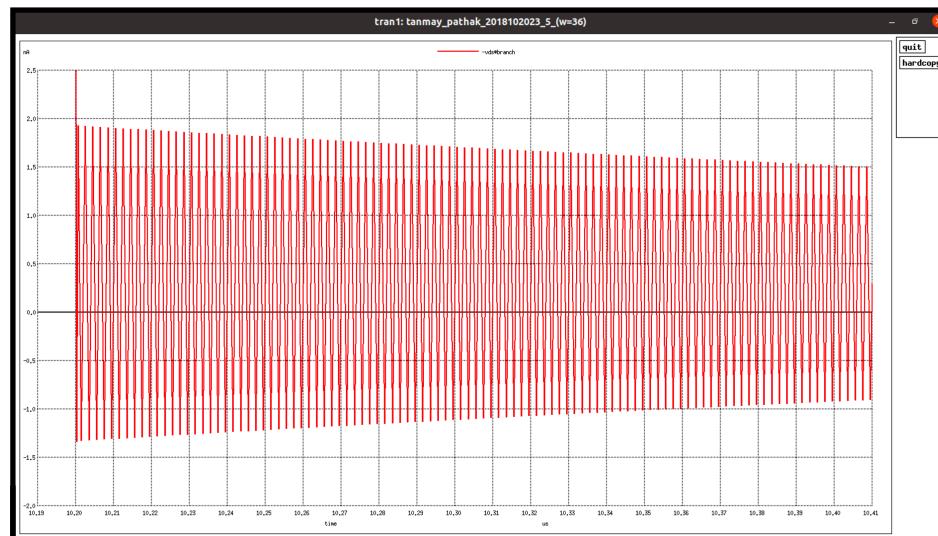


I_{OFF}

Output: $w=36\mu\text{m}$



I_{ON}



I_{OFF}

Tabulating the values of of I_{ON} peak and I_{OFF} average

Device width	I_{ON} peak	I_{OFF} average
1.8 μ m	1 mA	20.1 pA
3.6 μ m	1.93 mA	34.7 pA
18 μ m	8.96 mA	152 pA
36 μ m	16.7 mA	300 pA

Observations

- 1) Both I_{ON} and I_{OFF} scale with an increase in width
- 2) The approximate equation for I_d say that I_{ON} is supposed to be linearly increasing with W regardless of which region it resides. But the plot for I_{ON} is not exactly linear as the equations aren't entirely accurate.
- 3) I_{OFF} is the leakage current and it flows through the MOSFET in the cutoff region. I_{OFF} doesn't vary linearly with width W and the table concurs with that fact.

Question 6

The netlist used for the question is given below

```
Netlist for 6 - TANMAY PATHAK - 2018102023
.include TSMC_180nm.txt
.param SUPPLY=1.8
.param LAMBDA=0.09u
.global gnd vdd

VGS G gnd 'SUPPLY'
*VGS G gnd gnd

Vin D gnd 1.8
*Vin D gnd 0

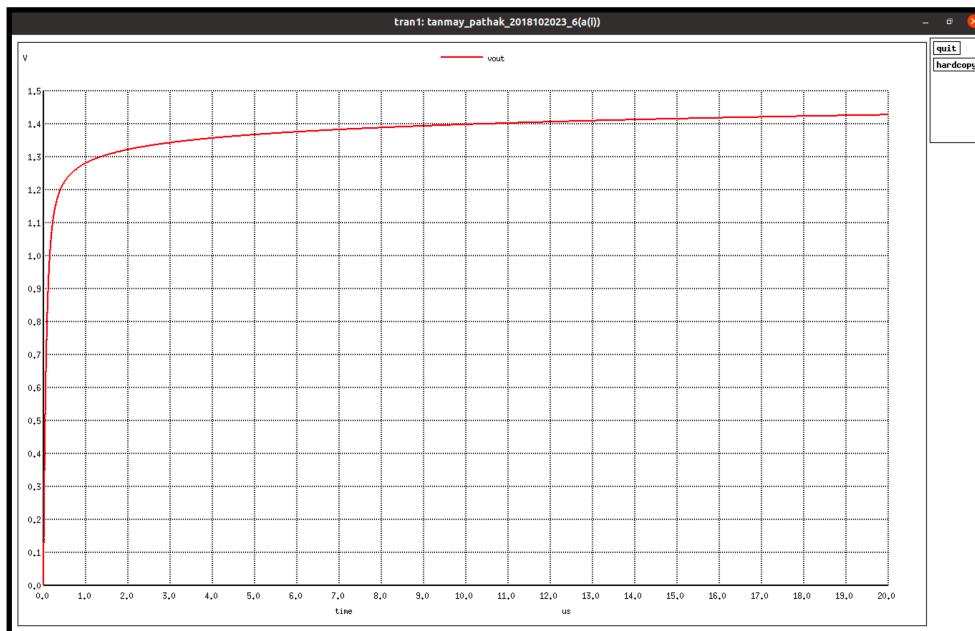
.param width_N={400*LAMBDA}
C1 vout gnd inf

*M1 D G vout vout CMOSN W={width_N} L={2*LAMBDA} + AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}
M1 vout G D vout CMOS P W={width_N} L={2*LAMBDA} + AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

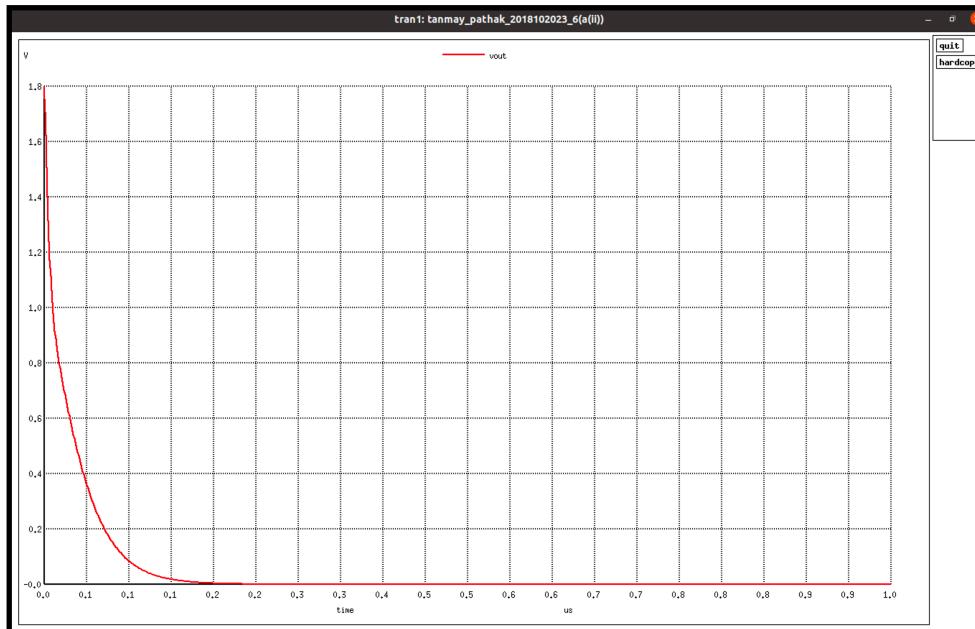
.ic v(vout) = 1.8
*.ic v(vout) = 0

.control
tran 1ns 20us
set hcopypscolor = 1 *White background for saving plots
set color0 = White
set color1 = black
run
set curplottitle="Tanmay_Pathak_2018102023_6(iv)"
plot vout
.endc
.end
```

Output (a(i)) : $V_c(0-) = 0V$ and $V(\text{in}) = 1.8V$



Output (a(ii)) : $V_c(0-) = 1.8V$ and $V(\text{in}) = 0V$

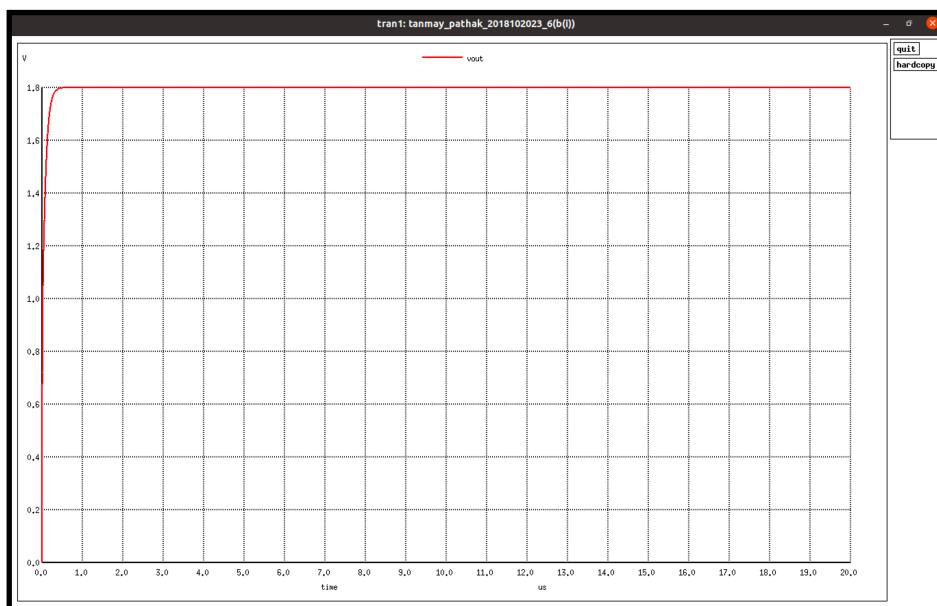


Observations

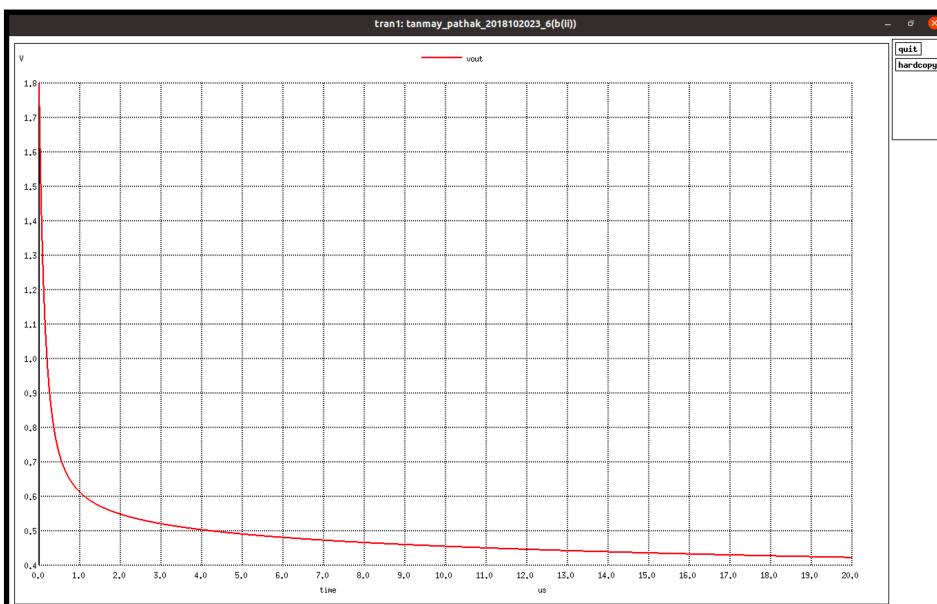
- 1) We expect that when $V_{\text{IN}}=1.8V$, the voltage across the capacitor should reach the same value as V_{IN} , but NMOS cannot pull up the V_{OUT} node to V_{IN} value completely. We see that the Peak value of V_{OUT} is about 1.42V, but when V_{IN} is grounded and $V_{\text{OUT}}(0^-) = 1.8 \text{ V}$, it gets discharged completely to 0V.

- 2) For a NMOS with drain at V_{IN} and gate connected to V_{DD} . The MOSFET is in saturation mode when V_{OUT} node gets pulled up to the point where V_{GS} is approximately equal to the V_T .
- 3) And now the NMOS is in a very weakly conducting state. Further as $V_{GS}=V_T$, the current flowing through the NMOS is small.
- 4) As V_{OUT} gradually increases, the NMOS is rapidly shutting off and the NMOS is no longer conductive and no longer pulls up the voltage at node V_{OUT} .
- 5) Pulling down to GND is not a problem with the NMOS, because then V_{OUT} would become the drain, the source would be at GND, and the gate at V_{DD} .

Output (b(i)) : $V_c(0-) = 0V$ and $V(in) = 1.8V$



Output (b(ii)) : $V_c(0-) = 1.8V$ and $V(in) = 0V$



Observations

- 1) We can expect when V_{IN} tends to 0, the voltages across the capacitor should discharge completely, but PMOS can't pull down V_{OUT} node completely to 0.
- 2) V_{OUT} is 0.42V even after considerable time. But when V_{IN} is 1.8V, and $V_{OUT}(0^-)$ is at 0, it gets charged completely to 1.8V
- 3) We're trying to pull the source of the PMOS "low" and here the drain is at V_{IN} and the gate is connected to GND. The node at the source of the NMOS is denoted as V_{OUT} . The V_{OUT} has initial potential as 1.8V and the drain is 0V. The MOSFET will be ON when $V_{GS} < V_T$ or when $0 - V_{OUT} < V_T$ or when $V_{OUT} > |V_T|$
- 4) As, the capacitor discharges, the V_{OUT} value decreases, but as V_{OUT} reaches values of $\text{abs}(V_T)$ the MOSFET goes into sub threshold region and this discharging becomes very slow. And thus V_{OUT} value saturates above the expected 0V value as we can see from the plots.
- 5) When V_{IN} is 1.8V and $V_{OUT}(0^-)$ is 0V, the source will be at V_{IN} node and drain at V_{OUT} node. $V_{GS} = -1.8V$. So, the condition $V_{GS} < V_T$ is always true and the MOSFET will always be on and V_{OUT} node could reach to the max value of 1.8 V.

Question 7

The netlist used for the question is given below

```
Netlist for 7 - TANMAY PATHAK - 2018102023

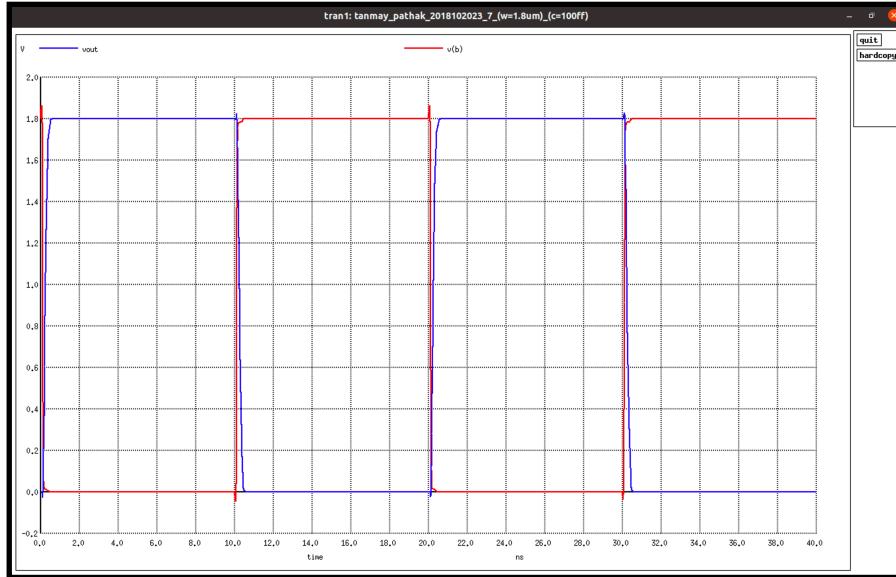
.include TSMC_180nm.txt
.param SUPPLY=1.8
.param LAMBDA=0.18u
.global gnd vdd
Vdd vdd gnd 'SUPPLY'
Vin a gnd 1.8
.subckt inv y x vdd gnd
.param width_N=[50*LAMBDA]
.param width_P=[2.5*width_N]
M1 y x gnd gnd CMOSN W=[width_N] L=[LAMBDA] + AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}
M2 y x vdd vdd CMOSP W=[width_P] L=[LAMBDA] + AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P} AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}
.ends inv
x1 b a vdd gnd inv
x2 vout b vdd gnd inv
C1 vout gnd 500fF
Vin a 0 pulse 0 1.8 0ns 100ps 100ps 9.9ns 20ns
.measure tran tperiod
+ TRIG v(b) VAL='SUPPLY/2' RISE=1
+ TARG v(b) VAL='SUPPLY/2' RISE=2
.measure tran tpdr
+ TRIG v(b) VAL='SUPPLY/2' FALL=1
+ TARG v(vout) VAL='SUPPLY/2' RISE=1
.measure tran tpdf
+ TRIG v(b) VAL='SUPPLY/2' RISE=1
+ TARG v(vout) VAL='SUPPLY/2' FALL=1
.measure tran tpd param='(tpdr+tpdf)/2' goal=0
.measure tran diff param='tpdr-tpdf' goal=0
.control
tran 1ns 40ns
set hcopypscolor = 1 *White background for saving plots
set color0 = White
set color1 = black
set color2 = blue
set color3 = red
run
set curplottitle="Tanmay_Pathak_2018102023_7_(w=1.8um)_(C=100fF)"
plot vout V(b)
.endc
.end
```

Output (a)

$C_L = 100\text{fF}$

$W_n = 1.8\mu\text{m}$

$W_p = 2.5 \times W_n$

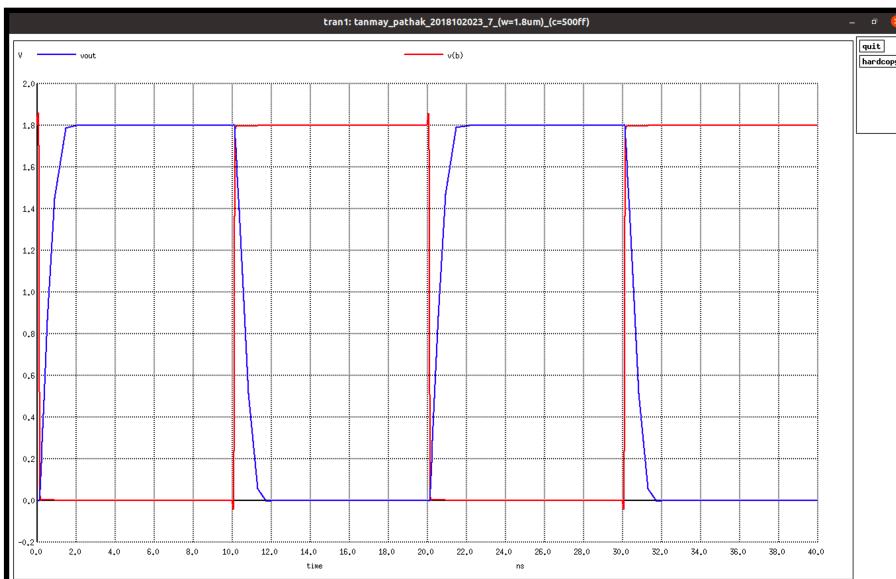


Output (b)

$C_L = 500\text{fF}$

$W_n = 1.8\mu\text{m}$

$W_p = 2.5 \times W_n$

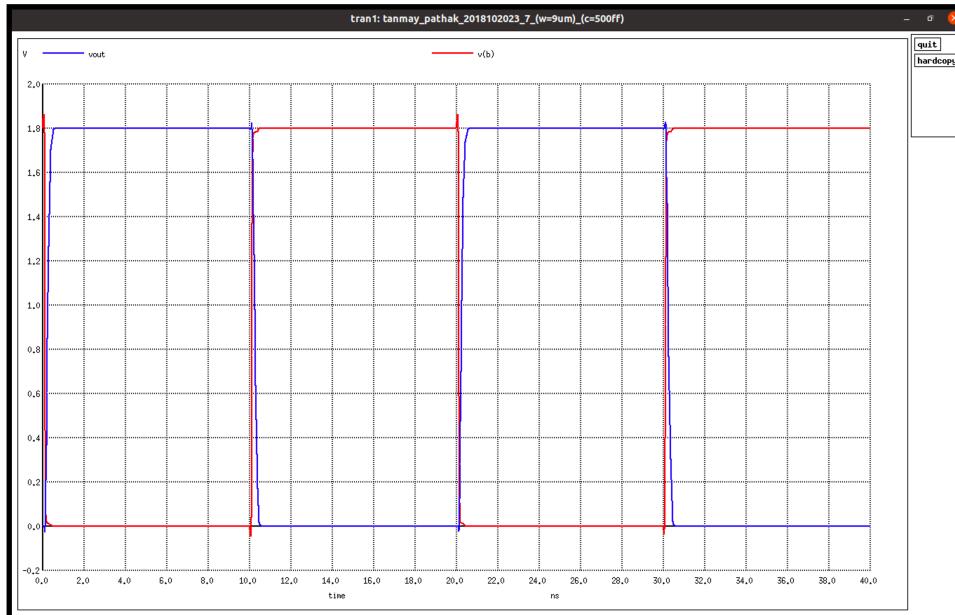


Output (c)

$C_L = 500\text{fF}$

$W_n = 9\mu\text{m}$

$W_p = 2.5 \times W_n$



Output - Measurements for transient analysis

Configuration	tpdr (ns)	tpdf (ns)	tpd (ns)
$C_L=100\text{fF}; W_n=1.8\mu\text{m}$	0.11406	0.12777	0.1209
$C_L=500\text{fF}; W_n=1.8\mu\text{m}$	0.44156	0.50283	0.4722
$C_L=500\text{fF}; W_n=9\mu\text{m}$	0.122486	0.13665	0.12957

(d)

We see an increase in time delay as we increase capacitance and keep the value of the width of the device the same. This is in line with the formula $\tau = RC$. According to the formula, an increase in capacitance will increase the time delay. As increasing the capacitance will increase the time constant and the capacitor will take more time to charge.

The time delay will decrease with an increase in the device width. As the device length increases, more current will flow through the MOSFET and the charging/discharging process of the capacitor will be faster.