

VLSI Assignment #2 - Tanmay Pathak

2018102023

3(a)

The Netlist used for this question is given below

```
Netlist for 3(a) - TANMAY PATHAK - 2018102023

.include TSMC_180nm.txt
.param SUPPLY=1.8
.param LAMBDA=0.09u
.param width_N={2*LAMBDA}
.param width_P={3*width_N}
.global gnd vdd
.subckt inv y x vdd gnd

M1 y x gnd gnd CMOSN W={width_N} L={2*LAMBDA} + AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA}
PD={10*LAMBDA+2*width_N}

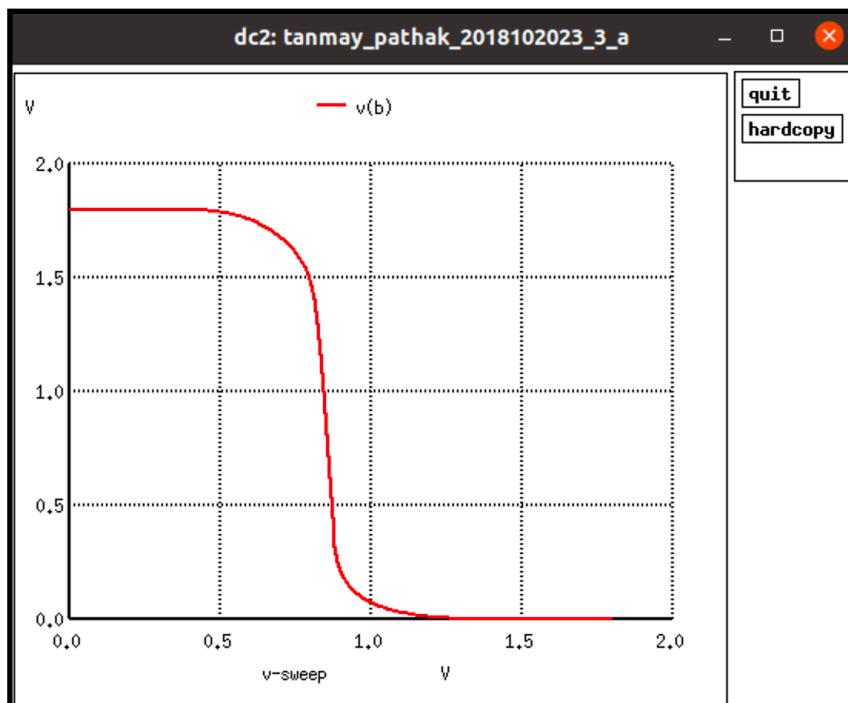
M2 y x vdd vdd CMOSP W={width_P} L={2*LAMBDA} + AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P} AD={5*width_P*LAMBDA}
PD={10*LAMBDA+2*width_P}

.ends inv

Vdd vdd gnd 'SUPPLY'
vin a gnd 0
x1 b a vdd gnd inv
x2 c b vdd gnd inv

.dc vin 0 'SUPPLY' 0.01
.control
set hcopypscolor = 1 *White background for saving plots
set color0=white ** color0 is used to set the background of the plot (manual sec:17.7)
set color1=black ** color1 is used to set the grid color of the plot (manual sec:17.7)
run
set curplottitle="Tanmay_Pathak_2018102023_3_a"
plot v(b)
.endc
```

Output - graph



Observations

- 1) We observe a sharp dip around the value $V_{dd}/2$.
- 2) This is in-line with the theory for the CMOS inverter.

3(b) - The theory paper will come here - Inverter wala

3(c)

The Netlist used for this question is given below

```
Netlist for 3(c) - TANMAY PATHAK 2018102023

.include TSMC_180nm.txt
.param SUPPLY=1.8
.param LAMBDA=0.09u
.param width_N={20*LAMBDA}
.param width_P={2.5*width_N}
.global gnd vdd
.subckt inv y x vdd gnd

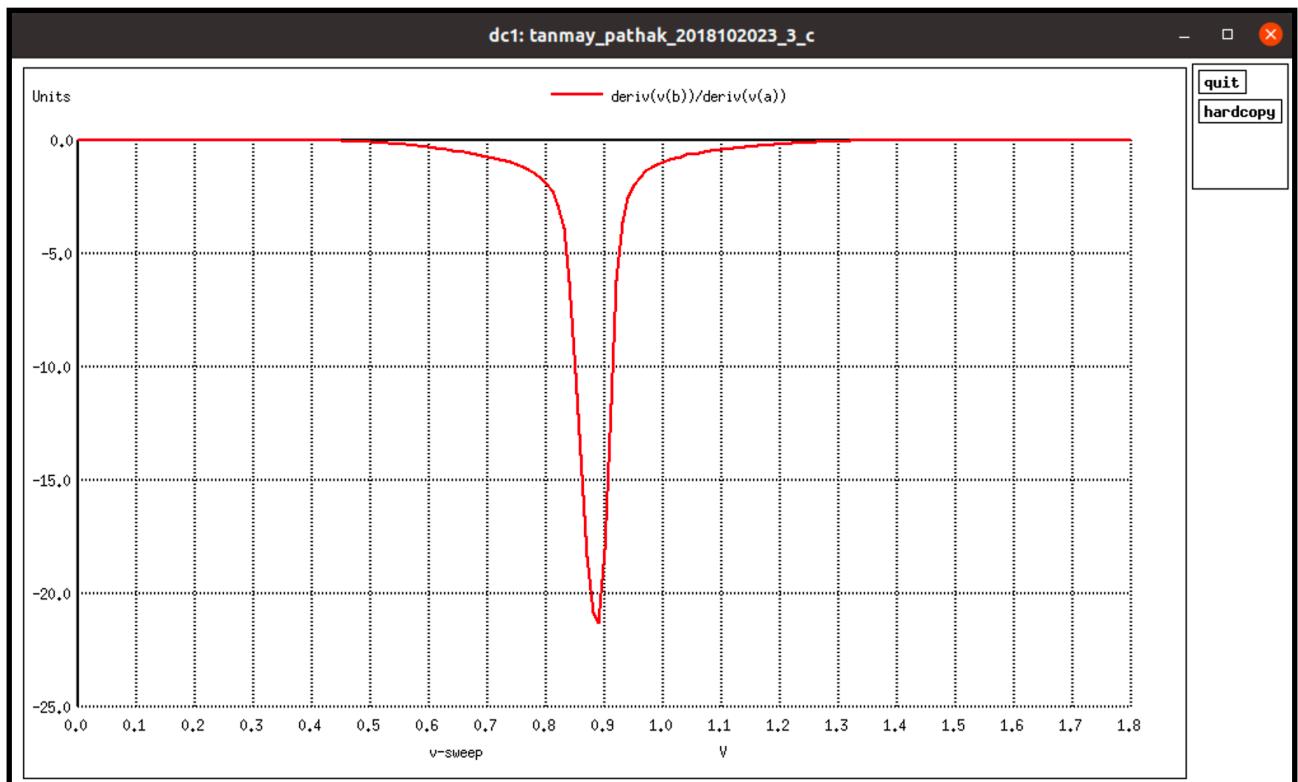
M1 y x gnd gnd CMOSN W={width_N} L={2*LAMBDA}+ AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA}
PD={10*LAMBDA+2*width_N}

M2 y x vdd vdd CMOSP W={width_P} L={2*LAMBDA} + AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P} AD={5*width_P*LAMBDA}
PD={10*LAMBDA+2*width_P}
.ends inv

Vdd vdd gnd 'SUPPLY'
vin a gnd 0
x1 b a vdd gnd inv
x2 c b vdd gnd inv
.dc vin 0 'SUPPLY' 0.01
.control

set hcopypscolor = 1 *White background for saving plots
set color0=white ** color0 is used to set the background of the plot (manual sec:17.7))
set color1=black ** color1 is used to set the grid color of the plot (manual sec:17.7))
run

set curplottitle="Tanmay_Pathak_2018102023_3_c"
plot deriv(v(b))/deriv(v(a))
.endc
```



Observations

- 1) At $V_i = 0.74$ and $V_i = 1.00$; we see that $(dV_o) / (dV_i) = -1$

- 2) From the graph in 3(a) we get $V_o = 1.687$ for $V_i = 0.74$ and $V_o = 0.0982$ for $V_i = 1.00$
- 3) From definitions in 3(b), $V_{OH} = 1.687$; $V_{IL} = 0.74$; $V_{OL} = 0.0982$ and $V_{IH} = 1.00$
- 4) Calculating noise margins, we get

$$NM_H = V_{OH} - V_{IH} = 0.69$$

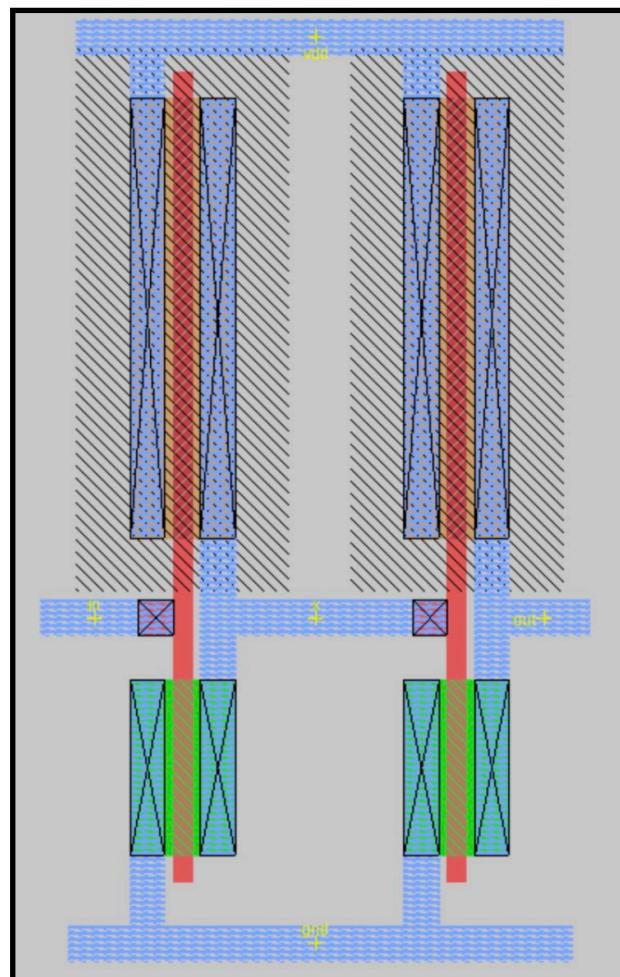
$$NM_L = V_{IL} - V_{OL} = 0.64$$

Tabulating the results

	Simulation	Theoretical
NM_H	0.69	0.69625
NM_L	0.64	0.68125

- 5) We observe that simulation noise margins are lesser than the theoretical for both NM_H and NM_L

3(d) - Layout



Post layout Netlist is given below

```
Post Layout Netlist for 3d - TANMAY PATHAK - 2018102023

.include TSMC_180nm.txt
.param SUPPLY=1.8
.param LAMBDA=0.09u
.param width_N={20*LAMBDA}
.param width_P={2.5*width_N}
.global gnd vdd
.option scale=0.09u

M1000 x in vdd w_n6_n6# CMOSP w=50 l=2 + ad=250 pd=110 as=500 ps=220
M1001 out x vdd w_25_n6# CMOSP w=50 l=2 + ad=250 pd=110 as=0 ps=0
M1002 x in gnd gnd CMOSN w=20 l=2 + ad=100 pd=50 as=200 ps=100
M1003 out x gnd gnd CMOSN w=20 l=2 + ad=100 pd=50 as=0 ps=0

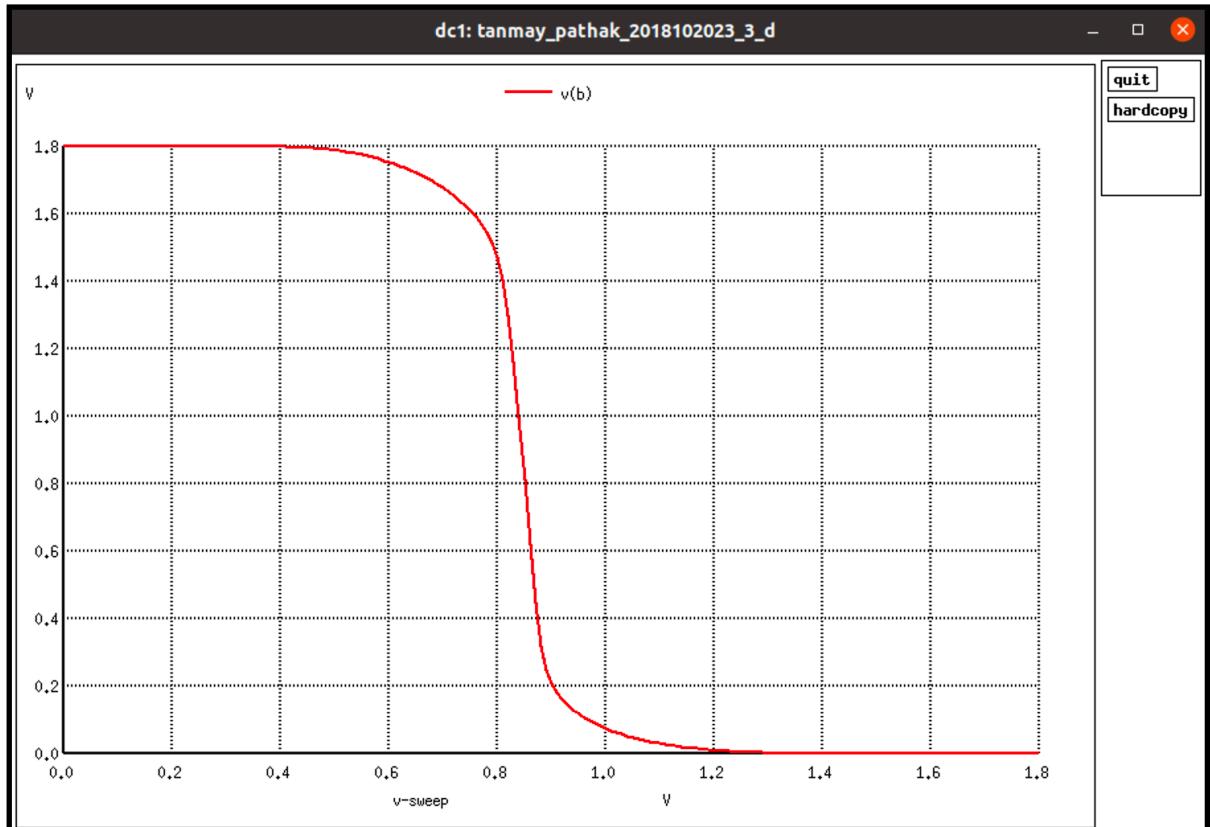
C0 w_25_n6# gnd 1.5fF
C1 w_n6_n6# gnd 1.5fF

Vdd vdd gnd 'SUPPLY'
vin in gnd 0

.dc vin 0 'SUPPLY' 0.01
.control

set hcopypscolor = 1 *White background for saving plots
set color0=white ** color0 is used to set the background of the plot (manual sec:17.7))
set color1=black ** color1 is used to set the grid color of the plot (manual sec:17.7))
run
set curplottitle="Tanmay_Pathak_2018102023_3d"
plot v(x)
* set curplottitle="Tanmay_Pathak_2018102023_3d"
* plot deriv(v(x))/deriv(v(in))
.endc
```

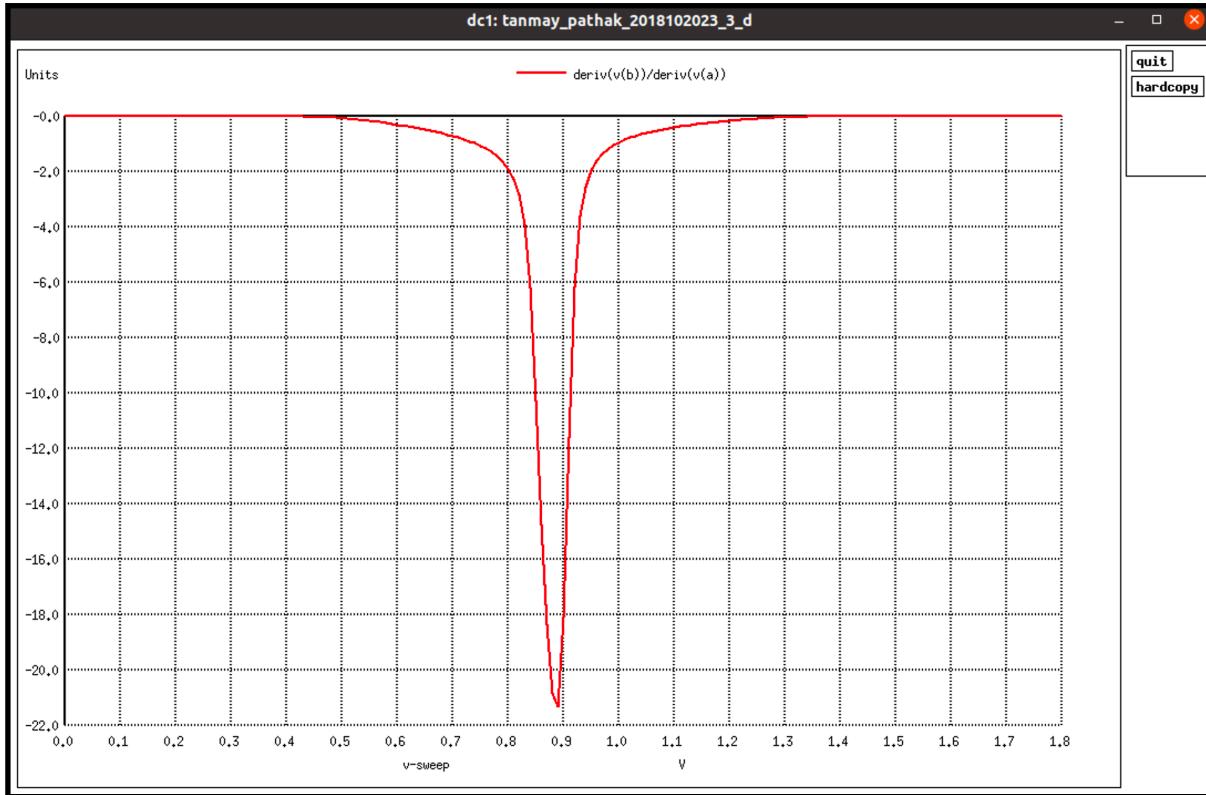
Output - graph



From the graph

$$(V_{IL}, V_{OH}) = (0.75, 1.687)$$

$$(V_{IH}, V_{OL}) = (1.04, 0.0941)$$



Observations

- 1) Again we observed that $(dV_o) / (dV_i) = -1$ at two points $V_i = 0.75$ and $V_i = 1.04$.
- 2) From the graph, we get $V_o = 1.687$ for $V_i = 0.75$ and $V_o = 0.0941$ for $V_i = 1.04$.
- 3) From definitions, $V_{OH} = 1.687$; $V_{IL} = 0.75$; $V_{OL} = 0.0941$ and $V_{IH} = 1.04$
- 4) Calculating noise margins, we get,

$$NM_H = V_{OH} - V_{IH} = 0.65$$

$$NM_L = V_{IL} - V_{OL} = 0.66$$

	NM_H	NM_L
Post-Layout	0.65	0.66
Pre-Layout	0.69	0.64
Theoretical	0.69625	0.68125

From the introduction of parasitic capacitors through the layout, we observe a difference between pre and post layout noise margin. We can see that noise margins depend on the threshold voltages of PMOS and NMOS which are controlled by the parasitic

capacitances in the circuit. Thus we observe a difference in the noise margins post-layout.

4(a) - Scan attached on next page

4(b)

The netlist used for the question is given below

```
Netlist for 4(b) - TANMAY PATHAK - 2018102023

.include TSMC_180nm.txt
.param SUPPLY=1.8
.param LAMBDA=0.09u
.param width_N={20*LAMBDA}
.param width_P={2.5*width_N}
.global gnd vdd

VIn a 0 pwl (0 0V 0.5ns 1.8V 1.1ns 1.8V 1.5ns 0V 10ns 0V)
Vdd vdd gnd 'SUPPLY'

M1 b a gnd gnd CMOSN W={width_N} L={2*LAMBDA} + AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}
M2 b a vdd vdd CMOSP W={width_P} L={2*LAMBDA} + AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P} AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}

.param width_N2={4*20*LAMBDA}
.param width_P2={2.5*width_N2}

M3 c b gnd gnd CMOSN W={width_N2} L={2*LAMBDA} + AS={5*width_N2*LAMBDA} PS={10*LAMBDA+2*width_N2} AD={5*width_N2*LAMBDA} PD={10*LAMBDA+2*width_N2}
M4 c b vdd vdd CMOSP W={width_P2} L={2*LAMBDA} + AS={5*width_P2*LAMBDA} PS={10*LAMBDA+2*width_P2} AD={5*width_P2*LAMBDA} PD={10*LAMBDA+2*width_P2}

.param width_N3={16*20*LAMBDA}
.param width_P3={2.5*width_N3}

M5 d c gnd gnd CMOSN W={width_N3} L={2*LAMBDA} + AS={5*width_N3*LAMBDA} PS={10*LAMBDA+2*width_N3} AD={5*width_N3*LAMBDA} PD={10*LAMBDA+2*width_N3}
M6 d c vdd vdd CMOSP W={width_P3} L={2*LAMBDA} + AS={5*width_P3*LAMBDA} PS={10*LAMBDA+2*width_P3} AD={5*width_P3*LAMBDA} PD={10*LAMBDA+2*width_P3}

.param width_N4={64*20*LAMBDA}
.param width_P4={2.5*width_N4}

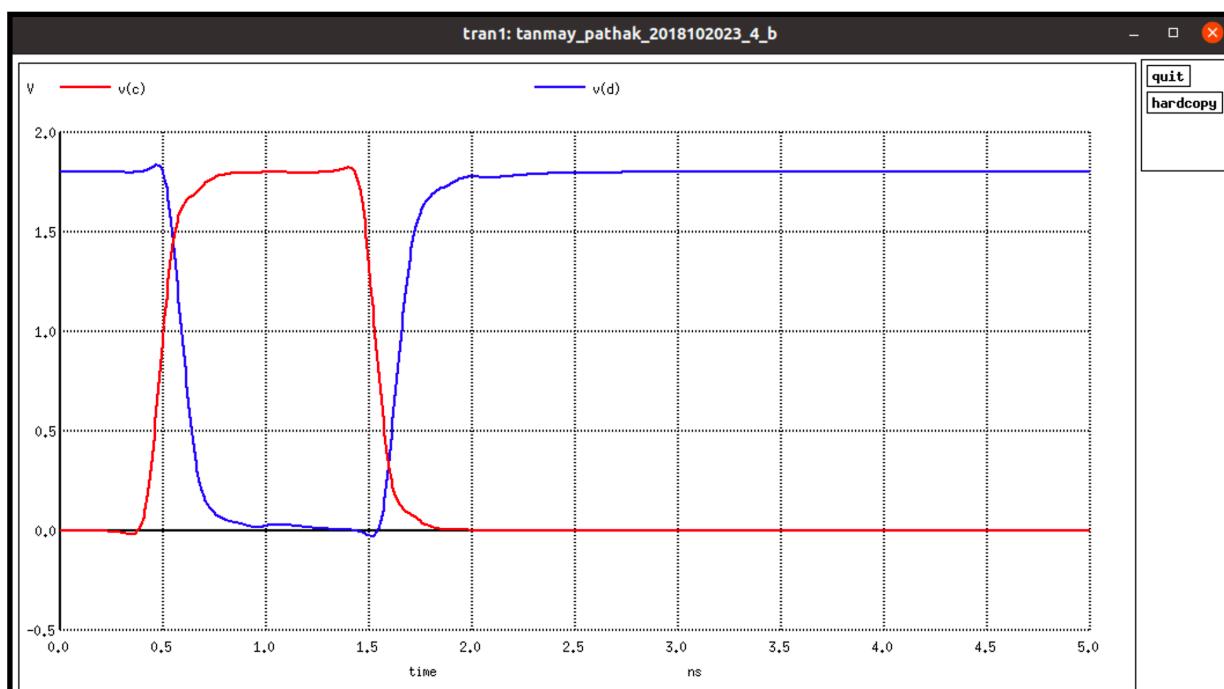
M7 e d gnd gnd CMOSN W={width_N4} L={2*LAMBDA} + AS={5*width_N4*LAMBDA} PS={10*LAMBDA+2*width_N4} AD={5*width_N4*LAMBDA} PD={10*LAMBDA+2*width_N4}
M8 e d vdd vdd CMOSP W={width_P4} L={2*LAMBDA} + AS={5*width_P4*LAMBDA} PS={10*LAMBDA+2*width_P4} AD={5*width_P4*LAMBDA} PD={10*LAMBDA+2*width_P4}
.param width_N5={376*20*LAMBDA}
.param width_P5={2.5*width_N5}

M9 f e gnd gnd CMOSN W={width_N5} L={2*LAMBDA} + AS={5*width_N5*LAMBDA} PS={10*LAMBDA+2*width_N5} AD={5*width_N5*LAMBDA} PD={10*LAMBDA+2*width_N5}
M10 f e vdd vdd CMOSP W={width_P5} L={2*LAMBDA} + AS={5*width_P5*LAMBDA} PS={10*LAMBDA+2*width_P5} AD={5*width_P5*LAMBDA} PD={10*LAMBDA+2*width_P5}

C1 f gnd 1pf

.tran 10p 5n
* inverter I3
.measure tran tpdc
+ TRIG v(c) VAL=0.18 RISE=1
+ TARG v(c) VAL=1.62 RISE=1
.measure tran tpfc
+ TRIG v(c) VAL=1.62 FALL=1
+ TARG v(c) VAL=0.18 FALL=1
* inverter I4
.measure tran tprd
+ TRIG v(d) VAL=0.18 RISE=1
+ TARG v(d) VAL=1.62 RISE=1
.measure tran tpfd
+ TRIG v(d) VAL=1.62 FALL=1
+ TARG v(d) VAL=0.18 FALL=1
.control
set hcopypscolor = 1 *White background for saving plots
set color0=white ** color0 is used to set the background of the plot (manual sec:17.7))
set color1=black ** color1 is used to set the grid color of the plot (manual sec:17.7))
run
set curplottitle="Tanmay_Pathak_2018102023_4_b"
plot v(c) v(d)
.endc
```

Output - Graph



Output - Measurements of Transient analysis

tprc	1.647159E-10	targ	5.882294E-10	trig	4.235134E-10
tpfc	1.562927E-10	targ	1.625180E-09	trig	1.468888E-09
tprd	1.801461E-10	targ	1.75624E-09	trig	1.576097E-09
tpfd	1.640229E-10	targ	6.935182E-10	trig	5.294954E-10

Observations - Rise and Fall times

	Rise time	Fall time
Node c	0.1647 ns	0.1563 ns
Node d	0.1801 ns	0.1640 ns

- 1) Since the output of Node c is connected to I3 and the output of Node d is connected to I4, we see that both rise time and fall time are higher at Node d compared to Node c.
- 2) Since I3 has width 16W and I4 has width 64W, the capacitive load seen by Node c due to I3 is lower than the capacitive load seen by Node d due to I4
- 3) We can consider rise time and fall time as the time taken for this capacitive load to charge and discharge. This difference in capacitive load is why the rise time and fall time are higher for Node d.

4(c)

```

Netlist for 4(c) - TANMAY PATHAK - 2018102023

.include TSMC_180nm.txt
.param SUPPLY=1.8
.param LAMBDA=0.09u
.param width_N={20*LAMBDA}
.param width_P={2.5*width_N}
.global gnd vdd

Vin a 0 pwl (0 0V 0.5ns 1.8V 1.1ns 1.8V 1.5ns 0V 10ns 0V)
Vdd vdd gnd 'SUPPLY'

M1 b a gnd gnd CMOS W={width_N} L={2*LAMBDA} + AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA}
PD={10*LAMBDA+2*width_N}
M2 b a vdd vdd CMOS W={width_P} L={2*LAMBDA} + AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P} AD={5*width_P*LAMBDA}
PD={10*LAMBDA+2*width_P}
.param width_N2={4*20*LAMBDA}
.param width_P2={2.5*width_N2}

M3 c b gnd gnd CMOS W={width_N2} L={2*LAMBDA} + AS={5*width_N2*LAMBDA} PS={10*LAMBDA+2*width_N2} AD={5*width_N2*LAMBDA}
PD={10*LAMBDA+2*width_N2}
M4 c b vdd vdd CMOS W={width_P2} L={2*LAMBDA} + AS={5*width_P2*LAMBDA} PS={10*LAMBDA+2*width_P2} AD={5*width_P2*LAMBDA}
PD={10*LAMBDA+2*width_P2}
.param width_N3={16*20*LAMBDA}
.param width_P3={2.5*width_N3}

M5 d c gnd gnd CMOS W={width_N3} L={2*LAMBDA} + AS={5*width_N3*LAMBDA} PS={10*LAMBDA+2*width_N3} AD={5*width_N3*LAMBDA}
PD={10*LAMBDA+2*width_N3}
M6 d c vdd vdd CMOS W={width_P3} L={2*LAMBDA} + AS={5*width_P3*LAMBDA} PS={10*LAMBDA+2*width_P3} AD={5*width_P3*LAMBDA}
PD={10*LAMBDA+2*width_P3}
.param width_N4={64*20*LAMBDA}
.param width_P4={2.5*width_N4}

M7 e d gnd gnd CMOS W={width_N4} L={2*LAMBDA} + AS={5*width_N4*LAMBDA} PS={10*LAMBDA+2*width_N4} AD={5*width_N4*LAMBDA}
PD={10*LAMBDA+2*width_N4}
M8 e d vdd vdd CMOS W={width_P4} L={2*LAMBDA} + AS={5*width_P4*LAMBDA} PS={10*LAMBDA+2*width_P4} AD={5*width_P4*LAMBDA}
PD={10*LAMBDA+2*width_P4}
.param width_N5={376*20*LAMBDA}
.param width_P5={2.5*width_N5}

M9 f e gnd gnd CMOS W={width_N5} L={2*LAMBDA} + AS={5*width_N5*LAMBDA} PS={10*LAMBDA+2*width_N5} AD={5*width_N5*LAMBDA}
PD={10*LAMBDA+2*width_N5}
M10 f e vdd vdd CMOS W={width_P5} L={2*LAMBDA} + AS={5*width_P5*LAMBDA} PS={10*LAMBDA+2*width_P5} AD={5*width_P5*LAMBDA}
PD={10*LAMBDA+2*width_P5}

C1 f gnd 1pf
.tran 10p 5n
* inverter I3
.measure tran trc
+ TRIG V(c) VAL='SUPPLY/2' FALL=1
+ TARG V(d) VAL='SUPPLY/2' RISE=1
.measure tran tfc
+ TRIG V(c) VAL='SUPPLY/2' RISE=1
+ TARG V(d) VAL='SUPPLY/2' FALL=1
.measure tran DelayC param='(trc+tfc)/2' goal=0
* inverter I4
.measure tran trd
+ TRIG V(d) VAL='SUPPLY/2' FALL=1
+ TARG V(e) VAL='SUPPLY/2' RISE=1
.measure tran tfd
+ TRIG V(d) VAL='SUPPLY/2' RISE=1
+ TARG V(e) VAL='SUPPLY/2' FALL=1
.measure tran DelayD param='(trd+tfdf)/2' goal=0
.control
run
.endc

```

Output - Measurements for Transient analysis

tprc	1.092809E-10	targ	1.644942E-09	trig	1.535661E-09
tpfc	1.068939E-10	targ	5.979655E-10	trig	4.910716E-10
delayc	1.08087E-10				
tprd	1.845302E-10	targ	7.824957E-10	trig	5.979655E-10
tpfd	1.649294E-10	targ	1.809871E-09	trig	1.644942E-09
delayc	1.74730E-10				

	Inverter I3	Inverter I4
Propagation Delay	0.108 ns	0.175 ns

The output of I4 is connected to an inverter of width 376W whereas I3 is connected to an inverter which has width 64W. The capacitive load seen at the output of I4 is much higher than that seen at output of I3 due to this difference in width; which leads to transient response being slower and hence the time taken for the output to reach a state of HIGH or LOW increases for I4 which is reflected in the propagation delay.

4(d)

The netlist used for the question is given below

```
Netlist for 4(d) - TANMAY PATHAK - 2018102023

.include TSMC_180nm.txt
.param SUPPLY=1.8
.param LAMBDA=0.09
.param width_N={20*LAMBDA}
.param width_P={2.5*width_N}
.global gnd vdd

Vin a 0 pw1 (0 0V 0.5ns 1.8V 1.1ns 1.8V 1.5ns 0V 10ns 0V)
Vdd vdd gnd 'SUPPLY'
V_temp_UP Vdd up 0
V_temp_DOWN down gnd 0

M1 b a gnd gnd CMOSN W={width_N} L={2*LAMBDA} + AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}
M2 b a vdd vdd CMOSP W={width_P} L={2*LAMBDA} + AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P} AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}
.param width_N2={4*20*LAMBDA}
.param width_P2={2.5*width_N2}

M3 c b gnd gnd CMOSN W={width_N2} L={2*LAMBDA} + AS={5*width_N2*LAMBDA} PS={10*LAMBDA+2*width_N2} AD={5*width_N2*LAMBDA} PD={10*LAMBDA+2*width_N2}
M4 c b vdd vdd CMOSP W={width_P2} L={2*LAMBDA} + AS={5*width_P2*LAMBDA} PS={10*LAMBDA+2*width_P2} AD={5*width_P2*LAMBDA} PD={10*LAMBDA+2*width_P2}
.param width_N3={16*20*LAMBDA}
.param width_P3={2.5*width_N3}

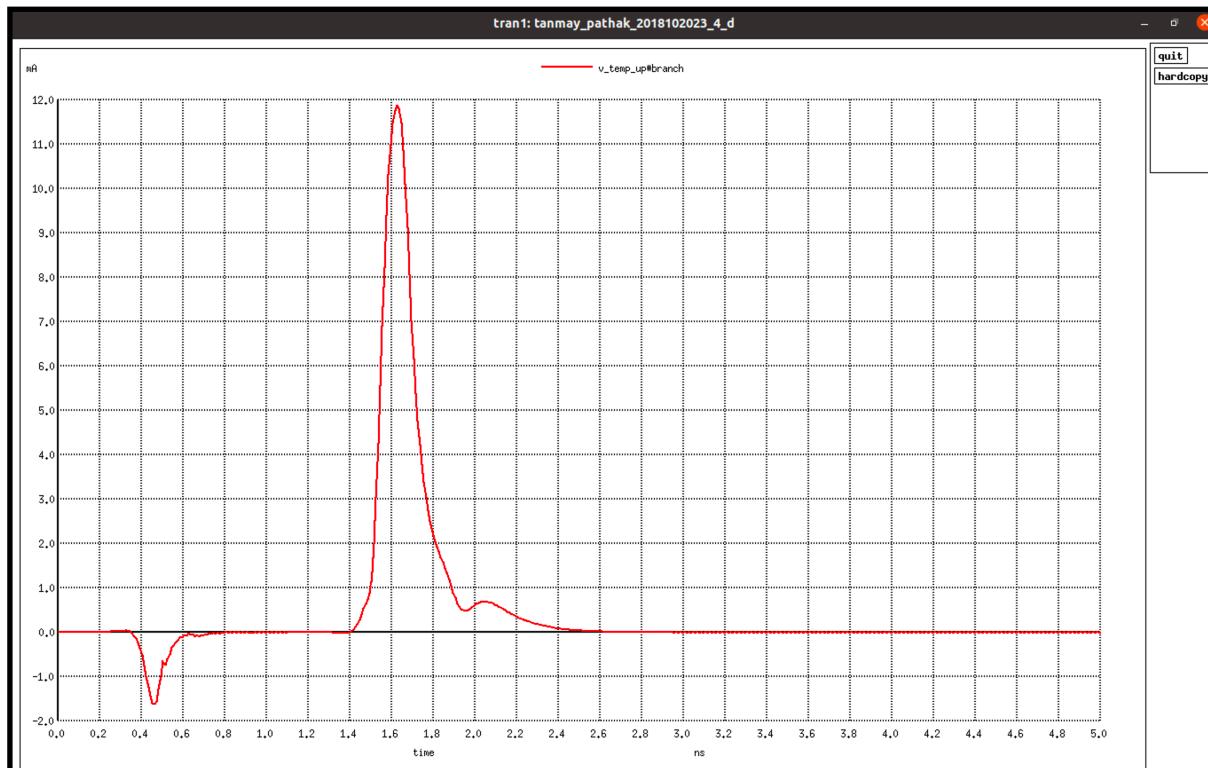
M5 d c down down CMOSN W={width_N3} L={2*LAMBDA} + AS={5*width_N3*LAMBDA} PS={10*LAMBDA+2*width_N3} AD={5*width_N3*LAMBDA} PD={10*LAMBDA+2*width_N3}
M6 d c up up CMOSP W={width_P3} L={2*LAMBDA} + AS={5*width_P3*LAMBDA} PS={10*LAMBDA+2*width_P3} AD={5*width_P3*LAMBDA} PD={10*LAMBDA+2*width_P3}
.param width_N4={64*20*LAMBDA}
.param width_P4={2.5*width_N4}

M7 e d gnd gnd CMOSN W={width_N4} L={2*LAMBDA} + AS={5*width_N4*LAMBDA} PS={10*LAMBDA+2*width_N4} AD={5*width_N4*LAMBDA} PD={10*LAMBDA+2*width_N4}
M8 e d vdd vdd CMOSP W={width_P4} L={2*LAMBDA} + AS={5*width_P4*LAMBDA} PS={10*LAMBDA+2*width_P4} AD={5*width_P4*LAMBDA} PD={10*LAMBDA+2*width_P4}
.param width_N5={376*20*LAMBDA}
.param width_P5={2.5*width_N5}

M9 f e gnd gnd CMOSN W={width_N5} L={2*LAMBDA} + AS={5*width_N5*LAMBDA} PS={10*LAMBDA+2*width_N5} AD={5*width_N5*LAMBDA} PD={10*LAMBDA+2*width_N5}
M10 f e vdd vdd CMOSP W={width_P5} L={2*LAMBDA} + AS={5*width_P5*LAMBDA} PS={10*LAMBDA+2*width_P5} AD={5*width_P5*LAMBDA} PD={10*LAMBDA+2*width_P5}

.tran 10p 5n
.control
set hcopypscolor = 1 *White background for saving plots
set color0=white ** color0 is used to set the background of the plot (manual sec:17.7)
set color1=black ** color1 is used to set the grid color of the plot (manual sec:17.7)
run
set curplottitle="Tanmay_Pathak_2018102023_4_d"
plot V_temp_UP#branch
.endc
```

Output - Graph



Observations

Comparing with previous outputs we see current I_{dd} spiked when node d is charging. PMOS is ON and the NMOS is OFF as the current flows through PMOS charging node d to 1.8v hence we can expect the spike. Further along I_{dd} is absent.

4(e)

The netlist used for the question is given below

```
Netlist for 4(e) - TANMAY PATHAK - 2018102023

.include TSMC_180nm.txt
.param SUPPLY=1.8
.param LAMBDA=0.09u
.param width_N={20*LAMBDA}
.param width_P={2.5*width_N}
.global gnd vdd

Vin a 0 pwl (0 0V 0.5ns 1.8V 1.1ns 1.8V 1.5ns 0V 10ns 0V)
Vdd vdd gnd 'SUPPLY'

Vdummyup Vdd up 0
Vdummydown down gnd 0

M1 b a gnd gnd CMOSN W={width_N} L={2*LAMBDA} + AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}
M2 b a vdd vdd CMOSP W={width_P} L={2*LAMBDA} + AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P} AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}
.param width_N2={4*20*LAMBDA}
.param width_P2={2.5*width_N2}

M3 c b gnd gnd CMOSN W={width_N2} L={2*LAMBDA} + AS={5*width_N2*LAMBDA} PS={10*LAMBDA+2*width_N2} AD={5*width_N2*LAMBDA} PD={10*LAMBDA+2*width_N2}
M4 c b vdd vdd CMOSP W={width_P2} L={2*LAMBDA} + AS={5*width_P2*LAMBDA} PS={10*LAMBDA+2*width_P2} AD={5*width_P2*LAMBDA} PD={10*LAMBDA+2*width_P2}
.param width_N3={16*20*LAMBDA}
.param width_P3={2.5*width_N3}

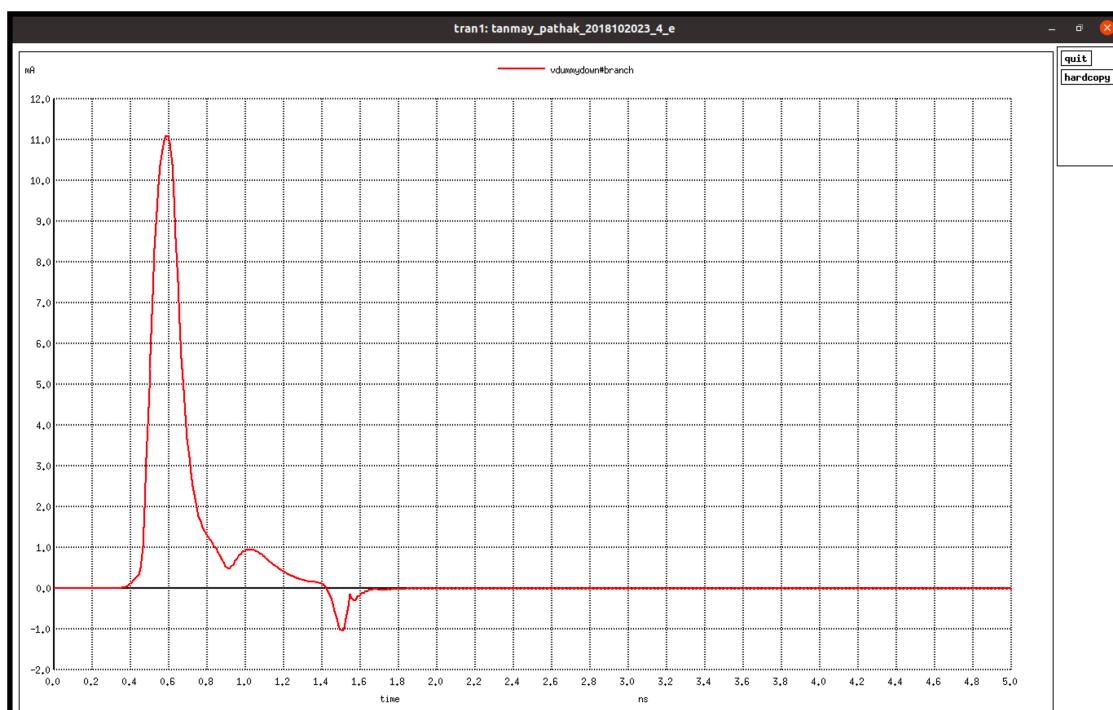
M5 d c down down CMOSN W={width_N3} L={2*LAMBDA} + AS={5*width_N3*LAMBDA} PS={10*LAMBDA+2*width_N3} AD={5*width_N3*LAMBDA} PD={10*LAMBDA+2*width_N3}
M6 d c up up CMOSP W={width_P3} L={2*LAMBDA} + AS={5*width_P3*LAMBDA} PS={10*LAMBDA+2*width_P3} AD={5*width_P3*LAMBDA} PD={10*LAMBDA+2*width_P3}
.param width_N4={64*20*LAMBDA}
.param width_P4={2.5*width_N4}

M7 e d gnd gnd CMOSN W={width_N4} L={2*LAMBDA} + AS={5*width_N4*LAMBDA} PS={10*LAMBDA+2*width_N4} AD={5*width_N4*LAMBDA} PD={10*LAMBDA+2*width_N4}
M8 e d vdd vdd CMOSP W={width_P4} L={2*LAMBDA} + AS={5*width_P4*LAMBDA} PS={10*LAMBDA+2*width_P4} AD={5*width_P4*LAMBDA} PD={10*LAMBDA+2*width_P4}
.param width_N5={376*20*LAMBDA}
.param width_P5={2.5*width_N5}

M9 f e gnd gnd CMOSN W={width_N5} L={2*LAMBDA} + AS={5*width_N5*LAMBDA} PS={10*LAMBDA+2*width_N5} AD={5*width_N5*LAMBDA} PD={10*LAMBDA+2*width_N5}
M10 f e vdd vdd CMOSP W={width_P5} L={2*LAMBDA} + AS={5*width_P5*LAMBDA} PS={10*LAMBDA+2*width_P5} AD={5*width_P5*LAMBDA} PD={10*LAMBDA+2*width_P5}

C1 f gnd 1pf
.tran 10p 5n
.control
set hcopyright= 1 *white background for saving plots
set color0=white ** color0 is used to set the background of the plot (manual sec:17.7)
set color1=black ** color1 is used to set the grid color of the plot (manual sec:17.7)
run
set curplottitle="Tanmay_Pathak_2018102023_4_e"
plot Vdummydown#branch
.endc
```

Output - Graph



Observations

Again comparing with previous outputs, we can see that I_{ss} spiked when Node d is discharging. NMOS is ON and the PMOS is OFF as the current flows through NMOS discharging Node d to 0v and hence we can expect this spike. Further along I_{ss} is absent.

5(a)

The netlist used for the question is given below

```
Netlist for 5(a) - TANMAY PATHAK - 2018102023

.include TSMC_180nm.txt
.param SUPPLY=1.8
.param LAMBDA=0.09u
.param width_N={10*LAMBDA}
.param width_P={2.5*width_N}
.global gnd vdd
.subckt inv y x vdd gnd
x1 1 in vdd gnd inv
x2 2 1 vdd gnd inv
x3 3 2 vdd gnd inv
x4 4 3 vdd gnd inv
x5 5 4 vdd gnd inv
x6 6 5 vdd gnd inv
x7 7 6 vdd gnd inv
x8 8 7 vdd gnd inv
x9 9 8 vdd gnd inv
x10 10 9 vdd gnd inv
x11 11 10 vdd gnd inv
x12 12 11 vdd gnd inv
x13 13 12 vdd gnd inv
x14 14 13 vdd gnd inv
x15 15 14 vdd gnd inv
x16 16 15 vdd gnd inv
x17 17 16 vdd gnd inv
x18 18 17 vdd gnd inv
x19 19 18 vdd gnd inv
x20 20 19 vdd gnd inv
x21 21 20 vdd gnd inv
x22 22 21 vdd gnd inv
x23 23 22 vdd gnd inv
x24 24 23 vdd gnd inv
x25 25 24 vdd gnd inv
x26 26 25 vdd gnd inv
x27 27 26 vdd gnd inv
x28 28 27 vdd gnd inv
x29 29 28 vdd gnd inv
x30 30 29 vdd gnd inv
x31 in 30 vdd gnd inv
Vdd vdd gnd 'SUPPLY'

.ic v(in) = 'SUPPLY'
.tran 0.001n 10n

.measure tran tperiod
+ TRIG v(in) VAL='SUPPLY/2' RISE=1
+ TARG v(in) VAL='SUPPLY/2' RISE=2

.measure tran tpdr
+ TRIG v(in) VAL='SUPPLY/2' FALL=2
+ TARG v(1) VAL='SUPPLY/2' RISE=2

.measure tran tpdf
+ TRIG v(in) VAL='SUPPLY/2' RISE=2
+ TARG v(1) VAL='SUPPLY/2' FALL=2
.measure tran tpd param='(tpdr+tpdf)/2' goal=0
.control
run
.endc
```

Output - Measurements of Transient analysis

tperiod	2.118229E-09	targ	3.193413E-09	trig	1.075183E-09
tpdr	3.364693E-11	targ	2.168462E-09	trig	2.134815E-09
tpdf	3.468330E-11	targ	3.228096E-09	trig	3.193413E-09
tpd	3.41651E-11				

Observations

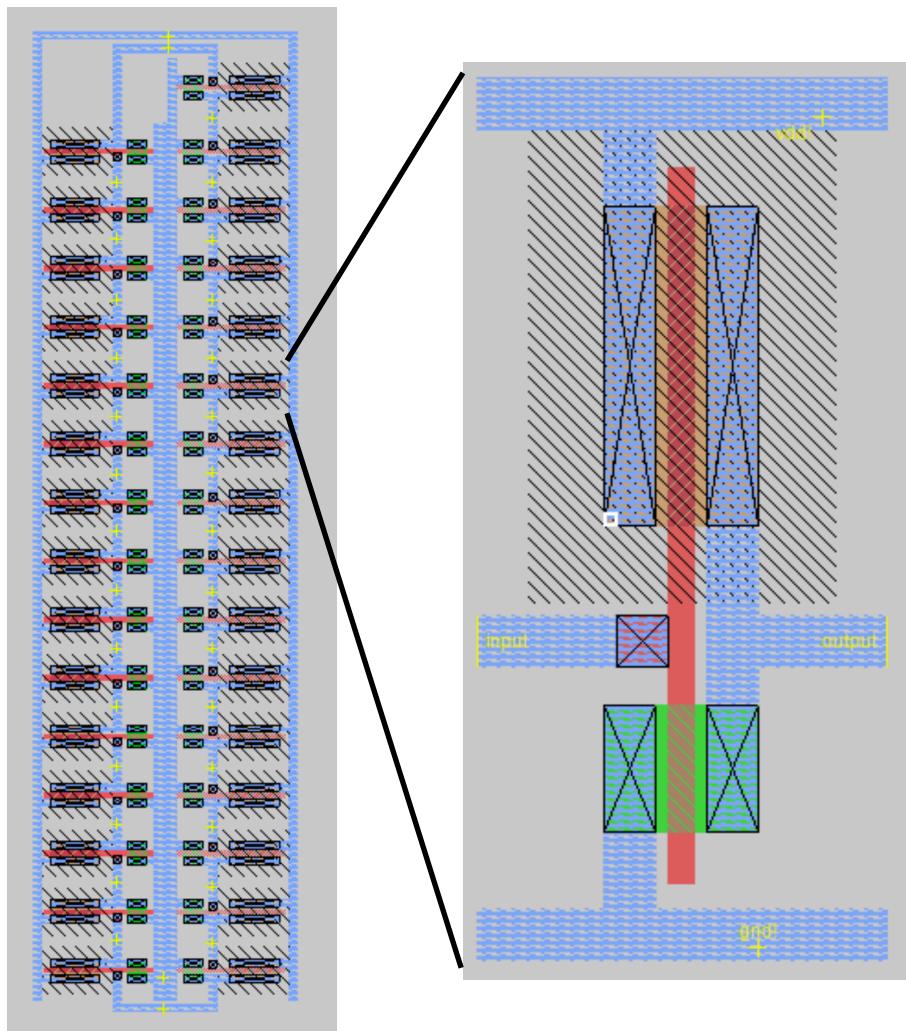
- 1) Time delay at single inverter $\tau_D = 3.4165E-11 = 34.165\text{ps}$
- 2) Time period for ring oscillator $T_o = 2.118229E-09 = 2.12\text{ns}$
- 3) Frequency of ring oscillator $f_{RO} = 1/T_o = 0.4717 \times 10^9$
- 4) Calculating the value of $1/(62\tau_D) = 0.472 \times 10^9$

Thus we can see that the value given by the simulation follows $f_{RO} = 1/(62\tau_D)$

Ring oscillators work on the principle of delay of CMOS inverter and when there are 31(which is an odd number) inverters in a ring oscillator, the input wire tips from HIGH to LOW. The signal at the input only shows effect when it has traveled across all 31 inverters, thus it has to pass through 31 delays before the input value can flip. Hence for the input to flip back to the original state it will have to travel through 62 delays. Thus time period is $62 \times (\text{single inverter time delay})$. Thus we get frequency as the inverse of time period i.e. $1/(62\tau_D)$.

5(b)

To minimise the area consumed so that the parasitic capacitances between layers is minimised, and thus we place the ring oscillator in a circular fashion with them sharing the ground node.



5(c)

The netlist for the question is given below

```
Netlist for 5(c) - TANMAY PATHAK - 2018102023
.include TSMC_180nm.txt
.param SUPPLY=1.8
.param LAMBDA=0.09u
.global gnd vdd

.option scale=0.09u

M1000 basicinv_0[1]/a_7_n5# 16 vdd basicinv_0[0]/w_0_0# CMOSP w=25 l=2 + ad=125 pd=60 as=3875 ps=1860
M1001 basicinv_0[1]/a_7_n5# 16 gnd gnd CMOSN w=10 l=2 + ad=50 pd=30 as=1550 ps=930
M1002 basicinv_0[1]/a_7_n5# basicinv_0[1]/a_7_n5# vdd basicinv_0[1]/w_0_0# CMOSP w=25 l=2 + ad=125 pd=60 as=125 ps=60
M1003 basicinv_0[2]/a_7_n5# basicinv_0[1]/a_7_n5# gnd gnd CMOSN w=10 l=2 + ad=50 pd=30 as=50 ps=30
M1004 basicinv_0[3]/a_7_n5# basicinv_0[2]/a_7_n5# vdd basicinv_0[2]/w_0_0# CMOSP w=25 l=2 + ad=125 pd=60 as=125 ps=60
M1005 basicinv_0[3]/a_7_n5# basicinv_0[2]/a_7_n5# gnd gnd CMOSN w=10 l=2 + ad=50 pd=30 as=50 ps=30
M1006 basicinv_0[4]/a_7_n5# basicinv_0[3]/a_7_n5# vdd basicinv_0[3]/w_0_0# CMOSP w=25 l=2 + ad=125 pd=60 as=125 ps=60
M1007 basicinv_0[4]/a_7_n5# basicinv_0[3]/a_7_n5# gnd gnd CMOSN w=10 l=2 + ad=50 pd=30 as=50 ps=30
M1008 basicinv_0[5]/a_7_n5# basicinv_0[4]/a_7_n5# vdd basicinv_0[4]/w_0_0# CMOSP w=25 l=2 + ad=125 pd=60 as=125 ps=60
M1009 basicinv_0[5]/a_7_n5# basicinv_0[4]/a_7_n5# gnd gnd CMOSN w=10 l=2 + ad=50 pd=30 as=50 ps=30
M1010 basicinv_0[6]/a_7_n5# basicinv_0[5]/a_7_n5# vdd basicinv_0[5]/w_0_0# CMOSP w=25 l=2 + ad=125 pd=60 as=125 ps=60
M1011 basicinv_0[6]/a_7_n5# basicinv_0[5]/a_7_n5# gnd gnd CMOSN w=10 l=2 + ad=50 pd=30 as=50 ps=30
M1012 basicinv_0[7]/a_7_n5# basicinv_0[6]/a_7_n5# vdd basicinv_0[6]/w_0_0# CMOSP w=25 l=2 + ad=125 pd=60 as=125 ps=60
M1013 basicinv_0[7]/a_7_n5# basicinv_0[6]/a_7_n5# gnd gnd CMOSN w=10 l=2 + ad=50 pd=30 as=50 ps=30
M1014 basicinv_0[8]/a_7_n5# basicinv_0[7]/a_7_n5# vdd basicinv_0[7]/w_0_0# CMOSP w=25 l=2 + ad=125 pd=60 as=125 ps=60
M1015 basicinv_0[8]/a_7_n5# basicinv_0[7]/a_7_n5# gnd gnd CMOSN w=10 l=2 + ad=50 pd=30 as=50 ps=30
M1016 basicinv_0[9]/a_7_n5# basicinv_0[8]/a_7_n5# vdd basicinv_0[8]/w_0_0# CMOSP w=25 l=2 + ad=125 pd=60 as=125 ps=60
M1017 basicinv_0[9]/a_7_n5# basicinv_0[8]/a_7_n5# gnd gnd CMOSN w=10 l=2 + ad=50 pd=30 as=50 ps=30
M1018 basicinv_0[10]/a_7_n5# basicinv_0[9]/a_7_n5# vdd basicinv_0[9]/w_0_0# CMOSP w=25 l=2 + ad=125 pd=60 as=125 ps=60
M1019 basicinv_0[10]/a_7_n5# basicinv_0[9]/a_7_n5# gnd gnd CMOSN w=10 l=2 + ad=50 pd=30 as=50 ps=30
M1020 basicinv_0[11]/a_7_n5# basicinv_0[10]/a_7_n5# vdd basicinv_0[10]/w_0_0# CMOSP w=25 l=2 + ad=125 pd=60 as=125 ps=60
M1021 basicinv_0[11]/a_7_n5# basicinv_0[10]/a_7_n5# gnd gnd CMOSN w=10 l=2 + ad=50 pd=30 as=50 ps=30
M1022 basicinv_0[12]/a_7_n5# basicinv_0[11]/a_7_n5# vdd basicinv_0[11]/w_0_0# CMOSP w=25 l=2 + ad=125 pd=60 as=125 ps=60
M1023 basicinv_0[12]/a_7_n5# basicinv_0[11]/a_7_n5# gnd gnd CMOSN w=10 l=2 + ad=50 pd=30 as=50 ps=30
M1024 basicinv_0[13]/a_7_n5# basicinv_0[12]/a_7_n5# vdd basicinv_0[12]/w_0_0# CMOSP w=25 l=2 + ad=125 pd=60 as=125 ps=60
M1025 basicinv_0[13]/a_7_n5# basicinv_0[12]/a_7_n5# gnd gnd CMOSN w=10 l=2 + ad=50 pd=30 as=50 ps=30
M1026 basicinv_0[14]/a_7_n5# basicinv_0[13]/a_7_n5# vdd basicinv_0[13]/w_0_0# CMOSP w=25 l=2 + ad=125 pd=60 as=125 ps=60
M1027 basicinv_0[14]/a_7_n5# basicinv_0[13]/a_7_n5# gnd gnd CMOSN w=10 l=2 + ad=50 pd=30 as=50 ps=30
M1028 in basicinv_0[14]/a_7_n5# vdd basicinv_0[14]/w_0_0# CMOSP w=25 l=2 + ad=125 pd=60 as=125 ps=60
M1029 in basicinv_0[14]/a_7_n5# gnd gnd CMOSN w=10 l=2 + ad=50 pd=30 as=50 ps=30
M1030 15 15 vdd basicinv_1/w_0_0# CMOSP w=25 l=2 + ad=125 pd=60 as=125 ps=60
M1031 15 15 gnd gnd CMOSN w=10 l=2 + ad=50 pd=30 as=50 ps=30
M1032 15 14 vdd w_2_423# CMOSP w=25 l=2 + ad=125 pd=60 as=125 ps=60
M1033 15 14 gnd gnd CMOSN w=10 l=2 + ad=50 pd=30 as=50 ps=30
M1034 14 13 vdd w_2_393# CMOSP w=25 l=2 + ad=125 pd=60 as=125 ps=60
M1035 14 13 gnd gnd CMOSN w=10 l=2 + ad=50 pd=30 as=50 ps=30
M1036 13 12 vdd w_2_363# CMOSP w=25 l=2 + ad=125 pd=60 as=125 ps=60
M1037 13 12 gnd gnd CMOSN w=10 l=2 + ad=50 pd=30 as=50 ps=30
M1038 12 11 vdd w_2_333# CMOSP w=25 l=2 + ad=125 pd=60 as=125 ps=60
M1039 12 11 gnd gnd CMOSN w=10 l=2 + ad=50 pd=30 as=50 ps=30
M1040 11 10 vdd w_2_303# CMOSP w=25 l=2 + ad=125 pd=60 as=125 ps=60
M1041 11 10 gnd gnd CMOSN w=10 l=2 + ad=50 pd=30 as=50 ps=30
M1042 10 9 vdd w_2_273# CMOSP w=25 l=2 + ad=125 pd=60 as=125 ps=60
M1043 10 9 gnd gnd CMOSN w=10 l=2 + ad=50 pd=30 as=50 ps=30
M1044 9 8 vdd w_2_243# CMOSP w=25 l=2 + ad=125 pd=60 as=125 ps=60
M1045 9 8 gnd gnd CMOSN w=10 l=2 + ad=50 pd=30 as=50 ps=30
M1046 8 7 vdd w_2_213# CMOSP w=25 l=2 + ad=125 pd=60 as=125 ps=60
M1047 8 7 gnd gnd CMOSN w=10 l=2 + ad=50 pd=30 as=50 ps=30
M1048 7 6 vdd w_2_183# CMOSP w=25 l=2 + ad=125 pd=60 as=125 ps=60
M1049 7 6 gnd gnd CMOSN w=10 l=2 + ad=50 pd=30 as=50 ps=30
M1050 6 5 vdd w_2_153# CMOSP w=25 l=2 + ad=125 pd=60 as=125 ps=60
M1051 6 5 gnd gnd CMOSN w=10 l=2 + ad=50 pd=30 as=50 ps=30
M1052 5 4 vdd w_2_123# CMOSP w=25 l=2 + ad=125 pd=60 as=125 ps=60
M1053 5 4 gnd gnd CMOSN w=10 l=2 + ad=50 pd=30 as=50 ps=30
M1054 4 3 vdd w_2_93# CMOSP w=25 l=2 + ad=125 pd=60 as=125 ps=60
M1055 4 3 gnd gnd CMOSN w=10 l=2 + ad=50 pd=30 as=50 ps=30
M1056 3 2 vdd w_2_63# CMOSP w=25 l=2 + ad=125 pd=60 as=125 ps=60
M1057 3 2 gnd gnd CMOSN w=10 l=2 + ad=50 pd=30 as=50 ps=30
M1058 2 1 vdd w_2_33# CMOSP w=25 l=2 + ad=125 pd=60 as=125 ps=60
M1059 2 1 gnd gnd CMOSN w=10 l=2 + ad=50 pd=30 as=50 ps=30
M1060 1 in vdd w_2_3# CMOSP w=25 l=2 + ad=125 pd=60 as=125 ps=60
M1061 1 in gnd gnd CMOSN w=10 l=2 + ad=50 pd=30 as=50 ps=30
C0 w_2_33# gnd 1.0FF
C1 w_2_63# gnd 1.0FF
C2 w_2_93# gnd 1.0FF
C3 w_2_123# gnd 1.0FF
C4 w_2_153# gnd 1.0FF
C5 w_2_183# gnd 1.0FF
C6 w_2_213# gnd 1.0FF
C7 w_2_243# gnd 1.0FF
C8 w_2_273# gnd 1.0FF
C9 w_2_303# gnd 1.0FF
C10 w_2_333# gnd 1.0FF
C11 w_2_363# gnd 1.0FF
C12 w_2_393# gnd 1.0FF
C13 w_2_423# gnd 1.0FF
C14 gnd gnd 6.4FF
C15 basicinv_1/w_0_0# gnd 13.0FF
C16 vdd gnd 8.4FF

Vdd vdd gnd 'SUPPLY'

.ic v(in) = 'SUPPLY'
.tran 0.1n 10n

.measure tran tperiod
+ TRIG v(in) VAL='SUPPLY/2' RISE=1
+ TARG v(in) VAL='SUPPLY/2' RISE=2
.measure tran tpd
+ TRIG v(in) VAL='SUPPLY/2' FALL=1
+ TARG v(1) VAL='SUPPLY/2' RISE=1
.measure tran tpd
+ TRIG v(in) VAL='SUPPLY/2' RISE=1
+ TARG v(1) VAL='SUPPLY/2' FALL=1
.measure tran tpd param='(tpdr+tpdf)/2' goal=0
.control
.tun
.endc
```

Output - Measurements for transient analysis

tperiod	2.135607E-09	targ	3.220441E-09	trig	1.084834E-09
tpdr	3.259784E-11	targ	4.964811E-11	trig	1.705027E-11
tpdf	3.574338E-11	targ	1.120577E-09	trig	1.084834E-09
tpd	3.41706E-11				

Observations

- 1) Time delay at single inverter $\tau_D = 3.4170E-11 = 34.17ps$
- 2) Time period for ring oscillator $T_o = 2.135607E-09 = 2.14ns$
- 3) Frequency of ring oscillator $f_{RO} = 1/T_o = 0.4682 \times 10^9$

5(d)

	f_{RO}	τ_D
Pre-layout	0.4717×10^9	34.16ps
Post layout	0.4682×10^9	34.17ps

Observations

- 1) The post layout frequency is lower
- 2) The post layout time delay is higher
- 3) These changes arise due to the effect of parasitic capacitances
- 4) After the parasitic capacitances were introduced, the time delay of single capacitor increases as the total self capacitance to be charged or discharged increases even though the driving current remains the same. Thus the time delay increases.
- 5) For the 31 ring oscillator, the extra delay adds up and hence frequency of ring oscillator reduces from pre-layout value.