B.Sc. EXAMINATION
School of Computing
2 Hours

May 2011

Computer Architecture and Operating Systems (AC32001)

This examination paper contains **SIX** questions.

Answer any **FOUR** questions.

Only calculators approved by the School of Computing for exam use may be used in this exam.

Answer any Four Questions

Question 1.

(a) Explain concisely

(i) what a **process** is, including the concept of process image and the characteristics associated with a process; **[5 Marks]**

(ii) the role of **scheduling** within an Operating System, distinguishing between short-term, medium-term and long-term scheduling. **[5 Marks]**

(b) Processes **P0, P2, P3 and P4** exist at **time 0**, each with a total run-time requirement of T time units, while Process **P1** arrives after **11 time units**, as indicated:

P0 (T=5 units)
P1 (T=7 units) arrives at time t = 11
P2 (T=4 units)
P3 (T=9 units)
P4 (T=14 units)

Draw a Gantt chart (timing chart) that illustrates the running of these processes when each of the following types of scheduling are used:

(i) Shortest Job First (Shortest Process Next);
(ii) Round Robin;
(iii) Highest Response Ratio Next (assuming P2 runs first).

Should time-slicing be required, assume that the quantum (time slice) = 1 time unit. Assume that no blocking events will occur. **[12 Marks]**

For each of these three types of scheduling, calculate how much time each process spends waiting and the average waiting time for all processes. **[3 Marks]**

Answer any Four Questions

Question 2.

(a) Give an overview of **security issues** that Operating Systems designers have to deal with. Your answer should cover at least the following aspects:

- Generic types of security threat
- Design principles for security measures
- User-oriented access control and data-oriented access control **[9 Marks]**

(b) Describe concisely how security measures operate in **Microsoft Windows™**. Marks will be awarded for a clear description of the means and structures used to impose control of process access to resources of all kinds in the system. **[8 Marks]**

(c) A residential estate for older and vulnerable people is being designed. The estate will be equipped throughout with "smart" technology to automate and oversee the domestic environment. The system will record domestic activity and build models of lifestyle patterns of residents in order to look for changes in their well-being. The estate will have a data centre to which all houses and flats will be connected for data processing and storage.

(i) Discuss ethical and legal issues that you think will arise here, and explain how Operating System security should be approached in the light of these issues. **[4 Marks]**

(ii) Describe arrangements that you would put in place for back-up storage of data, including how security of the back-up would be dealt with. **[4 Marks]**

Answer any Four Questions

Question 3.

(a) (i) Outline briefly the role of **middleware** in computing, and identify one well-known example of middleware associated with broking activity. **[4 Marks]**

(ii) Explain what a **Beowulf-type cluster** is in a computing context, and how middleware can contribute to the realisation and operation of such a cluster. Describe the philosophy taken regarding the hardware and software components that it uses. **[8 Marks]**

(b) Explain the need for **Direct Memory Access** controllers within the architecture of a modern PC, describing their operation and typical uses. **[8 Marks]**

(c) A microcomputer, functioning as a traffic lights controller, will use a series of sensors around a junction to count how many cars cross each entrance to the junction; each sensor normally outputs a "0" which becomes "1" while a vehicle is passing over. State which type of I/O scheme you would select for the implementation of this system, describing your reasons. **[5 Marks]**

Question 4.

(a) Explain the operation of **memory management** within a modern PC workstation. Your answer should include brief descriptions of **paging** and **two other** memory partitioning schemes. **[10 Marks]**

(b) A particular 32-bit computer has **1GB** of main memory, split into **1MB** pages. A paged, byte addressable virtual memory is in use. The processor is executing a program of size 5 MB, split into five pages.

(i) How many bits are required to store the frame number in the page translation table? **[2 Marks]**

(ii) Pages 1 and 4 of the program are in virtual memory, and pages 2, 3 and 5 are loaded into main memory frames 12, 6 and 27 respectively. Draw the relevant part of the page translation table to reflect the current state of this program. **[5 Marks]**

(iii) Explain why **multi-level** page translation tables are often used. **[2 Marks]**

(c) The Pentium series of processors contained two integer **pipelines**, but are now being superseded by processors with multiple **cores**. Explain why this shift in hardware design has occurred, and suggest any implications it has for future **software** design. **[6 Marks]**

Answer any Four Questions

Question 5.

(a) Describe the **von Neumann bottleneck** in microcomputer architecture, and explain how a **cache** can be used to reduce its effects. **[5 Marks]**

(b) A certain microprocessor (with a 32-bit address bus and 32-bit data bus) incorporates a set-associative cache which is shown in Figure 1, including the contents of parts of the cache (all numbers within the cache are in hexadecimal).

		Way 0		Way 1		
		Tag	**Data**	**Tag**	**Data**	**LRU**
	0	FF808F	45645334	FF0050	45645334	1
	1	78FF00	01234567	FF00A0	0000FFEE	1
64	**2**	78FF00	00000000	56ABC5	11223344	0
sets	**3**	00344F	56789A23	45AAA0	12345678	1
	4	782345	48AABB00	003456	34560011	0
	5	45FFAA	0011FFFF	453452	00FFFF11	1
	63	00FAB1	1A191A19	FF9900	ABCD0000	0

Figure 1

(i) How many bits are required in the **byte** field of the cache mapping calculation?

[2 Marks]

(ii) Hence (or otherwise) derive the **{tag, set, byte}** mapping figures for this cache.

[2 Marks]

(iii) The microprocessor then issues the following sequence of (hexadecimal) addresses, all of which are *fetches*:

```
00344F0C
78FF0008
45FFAA00
FF808F01
45FFAA03
45FFAA14
```

For each address, state whether it results in a cache **hit** or **miss**, and give the byte of data which is fetched; assume that any data fetched from main memory is all-zero.

[12 Marks]

(c) Name and briefly describe the function of **two other types** of cache found in modern microprocessors (excluding main memory caches). **[4 Marks]**

Answer any Four Questions

Question 6.

(a) Explain what **deadlock** is, and identify and explain the four conditions that need to exist for deadlock to occur. Cite a practical example of deadlock that might occur in a computer system. **[8 Marks]**

(b) (i) Briefly explain the nature of the problem known as the **"Dining Philosophers Problem"**, and its relevance to the subject of deadlock. **[3 Marks]**

(ii) Develop a solution to the Dining Philosophers Problem using semaphores, justifying any restrictions that the semaphores impose on the behaviour of the philosophers. Produce your answer in pseudo-code. (You may assume that appropriate semaphore primitives exist for use in your pseudo-code.) **[6 Marks]**

(c) Discuss the extent to which each of the following conditions would change the situation for the Dining Philosophers and show any modifications that you would make to your pseudo-code in the light of the possibility of these conditions. (Consider each condition individually and separately, i.e. the different conditions will not occur simultaneously.)

(i) **three** extra philosophers join the group, but no extra dining equipment is available; **[4 Marks]**

(ii) **one** philosopher becomes paralysed as a result of an accident, and needs to be fed by (any) one of the other philosophers. **[4 Marks]**

[End of Examination Paper]