

Quick reference guide for Instructors

32-bit Inline Assembly Programming in Visual Studio 2019

Introduction to 32-bit programming

Intel 8386 was the first 32-bit processor of the Intel family of microprocessors. It has 32-bit address and data buses. The protected mode was also introduced in this processor that limits the operation of user programs. It doesn't allow user programs to go beyond their memory limits assign to them and directly access IO devices. The size of existing registers, except the segment registers, were extended to 32-bit as shown below.

General-Purpose Registers					
31	16	15	8	7	0
	AH	AL			
	BH	BL			
	CH	CL			
	DH	DL			
	BP				
	SI				
	DI				
	IP				
				16-bit	32-bit
				AX	EAX
				BX	EBX
				CX	ECX
				DX	EDX
					EBP
					ESI
					EDI
					ESP

Addressing Modes

The addressing modes are the same.

In the 80386 and above, any register from EAX, EBX, ECX, EDX, EBP, EDI, ESI may be used in register indirect addressing mode. (Example: The MOV [EDX], CL instruction copies the byte sized contents of register CL into the data segment memory location addressed by EDX)

In the 80386 and above, any two registers from EAX, EBX, ECX, EDX, EBP, EDI, or ESI may be combined to generate the memory address. (Example: The MOV [EAX+EBX], CL instruction copies the byte sized contents of register CL into the data segment memory location addressed by EAX plus EBX.)

The 80386 and above use any 32-bit register except ESP to address memory. (Example: MOV AX, [ECX] or MOV AX, ARRAY[EBX]. The first instruction loads AX from the data segment address formed by ECX plus 4. The second instruction loads AX from the data segment memory location ARRAY plus the contents of EBX.

Inline Assembler (*Microsoft Specific*)

Assembly language serves many purposes, such as improving program speed, reducing memory needs, and controlling hardware when writing kernel modules. You can use the inline assembler to embed assembly-language instructions directly in your C and C++ source programs without extra assembly and link steps. The inline assembler is built into the compiler, so you don't need a separate assembler such as the Microsoft Macro Assembler (MASM). Because the inline assembler doesn't require separate assembly and link steps, it is more convenient than a separate assembler. Inline assembly code can use any C or C++ variable or function name that is in scope, so it is easy to integrate it with your program's C and C++ code.

And because the assembly code can be mixed with C and C++ statements, it can do tasks that are cumbersome in C or C++ alone.

The `__asm` keyword invokes the inline assembler and can appear wherever a C or C++ statement is legal. It cannot appear by itself. It must be followed by an assembly instruction, a group of instructions enclosed in braces, or, at the very least, an empty pair of braces.

Example

```
__asm mov eax,ebx
```

or

```
__asm
```

```
{
```

```
    Mov eax,ebx
```

```
}
```

Using and Preserving Registers in Inline Assembly (*Microsoft Specific*)

In general, you should not assume that a register will have a given value when an `__asm` block begins. Register values are not guaranteed to be preserved across separate `__asm` blocks. If you end a block of inline code and begin another, you cannot rely on the registers in the second block to retain their values from the first block. An `__asm` block inherits whatever register values result from the normal flow of control.

When using `__asm` to write assembly language in C/C++ functions, you don't need to preserve the EAX, EBX, ECX, EDX, ESI, or EDI registers. You should preserve other registers you use (such as DS, SS, ESP, EBP, and flags registers) for the scope of the `__asm` block.

Example#1: Program to add two integer numbers using the inline assembly.

```
#include<iostream>
using namespace std;

int main(void)
{
    int a = 10, b = 20, c = 0;
    __asm
    {
        mov ebx,a
        add ebx,b
        mov c,ebx
    }
    cout << "Sum of " << a << " and " << b << " is " << c << endl;
}
```

Example#2: Program to access array using inline 32-bit assembly. Both codes are incrementing every element of the array.

```
#include<iostream>
using namespace std;

int array1[] = {1,2,3,4,5};

int main(void)
{
    __asm
    {
        push ebp
        mov ebp, offset array1
        mov esi, 0
        mov ecx, 5

    l1:
        inc dword ptr[ebp + esi]
        add esi, 4
        loop l1
        pop ebp
    }
    for (int i = 0; i < 5; i++)
        cout << array1[i];
}
```

```
#include<iostream>
using namespace std;

int array1[] = {1,2,3,4,5};

int main(void)
{
    for (int i = 0; i < 20; i=i+4)
    {
        __asm
        {
            mov esi,i
            inc dword ptr [array1+esi]
        }
    }
    for (int i = 0; i < 5; i++)
        cout << array1[i];
}
```

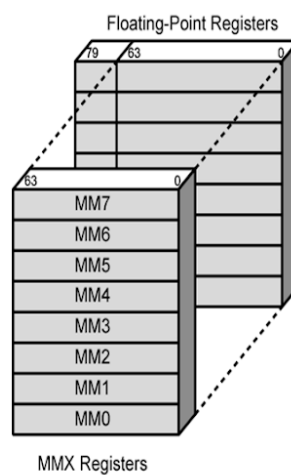
Example#3: Program to rotate right each element of the array using 1) C++ and 2) inline assembly.

Rotate left in C++	Rotate left using inline assembly
<pre> #include<iostream> using namespace std; int main() { int array1[] = { 1,2,3,4,5 }; int DROPPED_MSB; for (int i = 0; i < 5; i++) { DROPPED_MSB = (array1[i] << 1); array1[i] = (array1[i] << 1) DROPPED_MSB; } for (int i = 0; i < 5; i++) { cout << array1[i] << endl; } return 0; } </pre>	<pre> #include<iostream> using namespace std; int main(void) { int array1[] = { 1,2,3,4,5 }; for (int i = 0; i < 20; i=i+4) { __asm { mov eax,i rol dword ptr [array1+eax],1 } for (int i = 0; i < 5; i++) { cout << array1[i] << endl; } } } </pre>

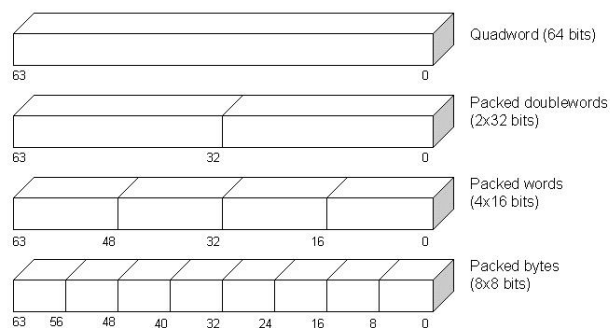
Multimedia Extension (MMX)

MMX refers to a feature that exist in the Intel processors, which can boost up multimedia software, by executing integer instructions on several data parallelly. It allows **single instruction** to work on **multiple data** (SIMD). Though the processor supports the acceleration, it does not mean your application can make use of it automatically. Hence, your application must be manually written in order to take advantage of it.

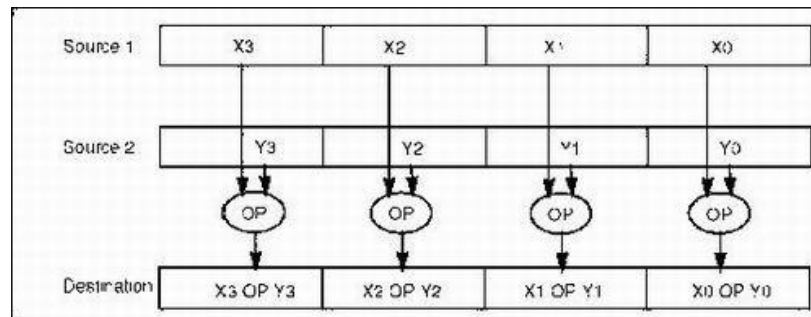
So far, we have seen general purpose registers. Besides that, we also have another 8 80-bit registers located in the FPU (Floating Point Unit) named as **mm0**, **mm1**, **mm2**, **mm3**, **mm4**, **mm5**, **mm6** and **mm7** as shown below. We can make use of these 8 registers in FPU if we have MMX feature in our processor. Only least 64 bits of these registers are accessible for mmx operations.



The MMX registers can store 8 bytes, 4 words, 2 double words and 1 quad word as shown in the image below.



MMX instructions performs operations on the corresponding bytes, words or doublewords store in registers as shown below.



MMX™ Instruction Set Summary

The instructions and corresponding mnemonics in the table below are grouped by function categories. If an instruction supports multiple data types—byte (B), word (W), doubleword (DW), or quadword (QW), the datatypes are listed in brackets. Only one data type may be chosen for a given instruction. For example, the base mnemonic PADD (packed add) has the following variations: PADDB, PADDW, and PADDD. The number of opcodes associated with each base mnemonic is listed.

Category	Mnemonic	Number of Different Opcodes	Description
Arithmetic	PADD[B,W,D]	3	Add with wrap-around on [byte, word, doubleword]
	PADD[S,B,W]	2	Add signed with saturation on [byte, word]
	PADDUS[B,W]	2	Add unsigned with saturation on [byte, word]
	PSUB[B,W,D]	3	Subtraction with wrap-around on [byte, word, doubleword]
	PSUB[S,B,W]	2	Subtract signed with saturation on [byte, word]
	PSUBUS[B,W]	2	Subtract unsigned with saturation on [byte, word]
	PMULHW	1	Packed multiply high on words
	PMULLW	1	Packed multiply low on words
	PMADDWD	1	Packed multiply on words and add resulting pairs
Comparison	PCMPEQ[B,W,D]	3	Packed compare for equality [byte, word, doubleword]
	PCMPGT[B,W,D]	3	Packed compare greater than [byte, word, doubleword]
Conversion	PACKUSWB	1	Pack words into bytes (unsigned with saturation)
	PACKSS[WB,DW]	2	Pack [words into bytes, doublewords into words] (signed with saturation)
	PUNPCKH [BW,WD,DQ]	3	Unpack (interleave) high-order [bytes, words, doublewords] from MMX™ register
	PUNPCKL [BW,WD,DQ]	3	Unpack (interleave) low-order [bytes, words, doublewords] from MMX register
Logical	PAND	1	Bitwise AND
	PANDN	1	Bitwise AND NOT
	POR	1	Bitwise OR
	PXOR	1	Bitwise XOR

Shift	PSLL[W,D,Q]	6	Packed shift left logical [word, doubleword, quadword] by amount specified in MMX register or by immediate value
	PSRL[W,D,Q]	6	Packed shift right logical [word, doubleword, quadword] by amount specified in MMX register or by immediate value
	PSRA[W,D]	4	Packed shift right arithmetic [word, doubleword] by amount specified in MMX register or by immediate value
Data Transfer	MOV[D,Q]	4	Move [doubleword, quadword] to MMX register or from MMX register
FP & MMX State Mgmt	EMMS	1	Empty MMX state

Instruction Examples

The following section will briefly describe five examples of MMX instructions. For illustration, the data type shown in this section will be the 16-bit word data type; most of these operations also exist for 8-bit or 32-bit packed data types. The following example shows a packed add word with wrap around. It performs four additions of the eight, 16-bit elements, with each addition independent of the others and in parallel. In this case, the right-most result exceeds the maximum value representable in 16-bits—thus it wraps around. This is the way regular IA arithmetic behaves. FFFFh + 8000h would be a 17-bit result. The 17th bit is lost because of wrap around, so the result is 7FFFh.

a3	a2	a1	FFFFh
+	+	+	+
b3	b2	b1	8000h
<hr/>			
a3+b3	a2+b2	a1+b1	7FFFh

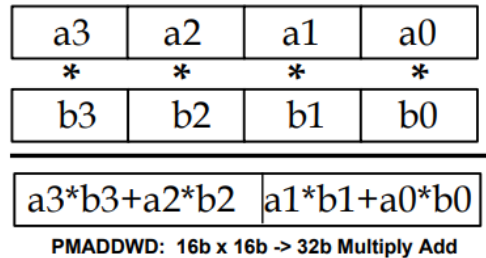
PADD[W]: Wrap-around Add

The following example is for a packed add word with unsigned saturation. This example uses the same data values from before. The right-most add generates a result that does not fit into 16 bits; consequently, in this case saturation occurs. Saturation means that if addition results in overflow or subtraction results in underflow, the result is clamped to the largest or the smallest value representable. For an unsigned, 16-bit word, the largest and the smallest representable values are FFFFh and 0x0000; for a signed word the largest and the smallest representable values are 7FFFh and 0x8000.

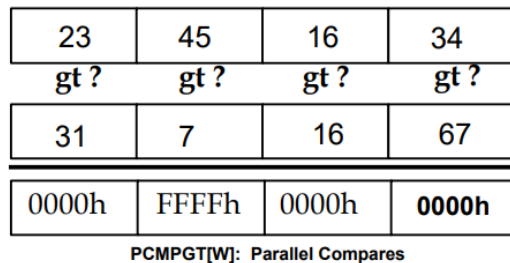
a3	a2	a1	FFFFh
+	+	+	+
b3	b2	b1	8000h
<hr/>			
a3+b3	a2+b2	a1+b1	FFFFh

PADDUS[W]: Saturating Arithmetic

The PMADD instruction starts from a 16-bit, packed data type and generates a 32-bit packed, data type result. It multiplies all the corresponding elements generating four 32-bit results and adds the two products on the left together for one result and the two products on the right together for the other result. To complete a multiply-accumulate operation, the results would then be added to another register which is used as the accumulator.



The following example is a packed parallel compare. This example compares four pairs of 16-bit words. It creates a result of true (FFFFh), or false (0000h). This result is a packed mask of ones for each true condition, or zeros for each false condition. The following example shows an example of a compare “greater than” on packed word data. There are no new condition code flags, nor are any existing IA condition code flags affected by this instruction.



Example#4: Program to add two byte arrays using MMX instructions.

```
#include<iostream>
using namespace std;
int main()
{
    char array1[8] = { 1,2,3,4,5,6,7,8 };
    char array2[8] = { 6,7,8,9,10,11,12,13 };
    char array3[8];

    __asm
    {
        movq mm0,[array1]
        movq mm1,[array2]
        paddb mm0,mm1
        movq [array3],mm0
    }
    for (int i = 0; i < 8; i++)
    {
        cout <<"Sum of "<<(uint8)array1[i] <<" and "<< (int)array2[i]<<" is "<<
(int)array3[i]<< endl;
    }
    return 0;
}
```

Example#5: Program to shift left all elements of int array using MMX instructions.

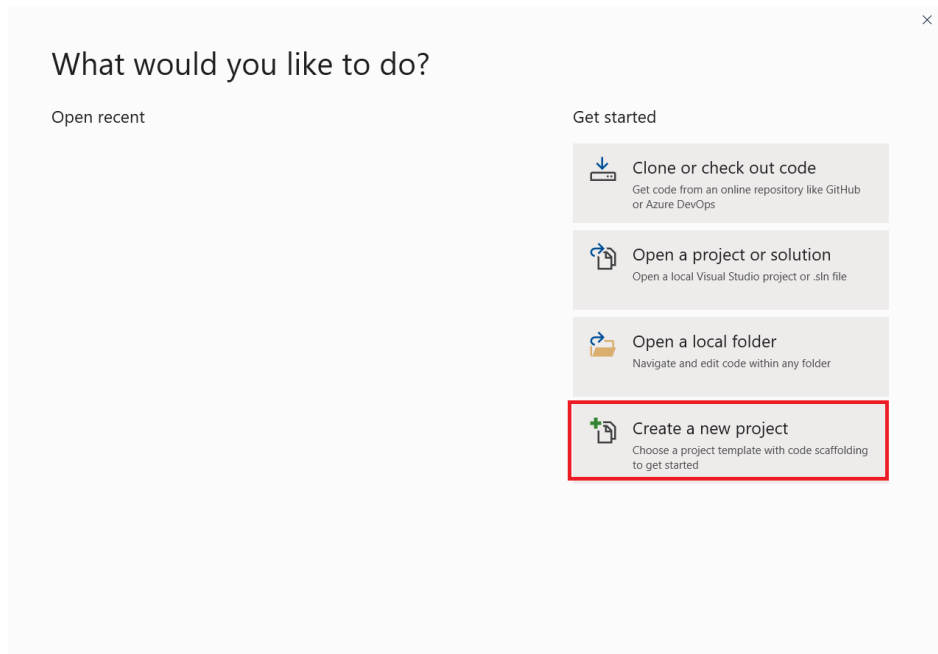
```
#include<iostream>
using namespace std;
int main()
{
    int array1[6] = { 1,2,3,4,5,6 };
    int array2[6];
    for(int i=0;i<24;i=i+8)
        __asm
        {
            mov esi,i
            movq mm0,[array1+esi]
            psllq mm0,1
            movq [array2+esi],mm0
        }
    for (int i = 0; i < 6; i++)
    {
        cout << "Sum of " << (int)array2[i] << endl;
    }
    return 0;
}
```

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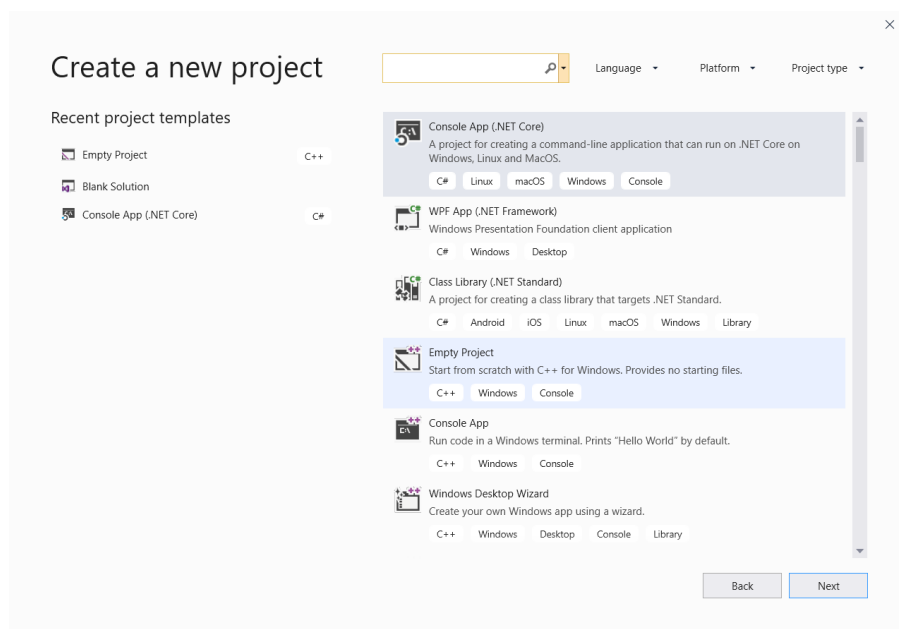
Step#1:

Open Visual Studio 2019

Step#2: Click on “Create a new project”



Step#3: Click on C++ under “Empty Project” and press Next



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Step#4: Write your project name (e.g., Myproject) and click on Create

Configure your new project

Empty Project C++ Windows Console

Project name

Myproject

Location

C:\Users\Adnan\source\repos

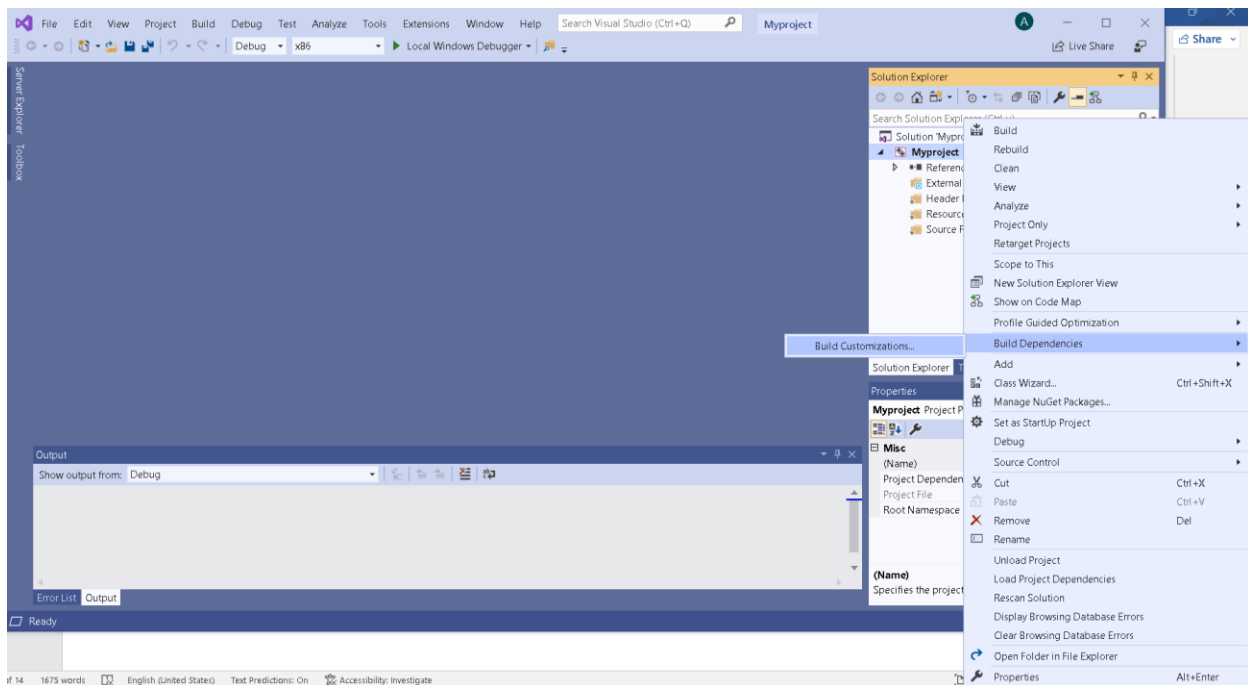
Solution name ⓘ

Myproject

☒ Place solution and project in the same directory

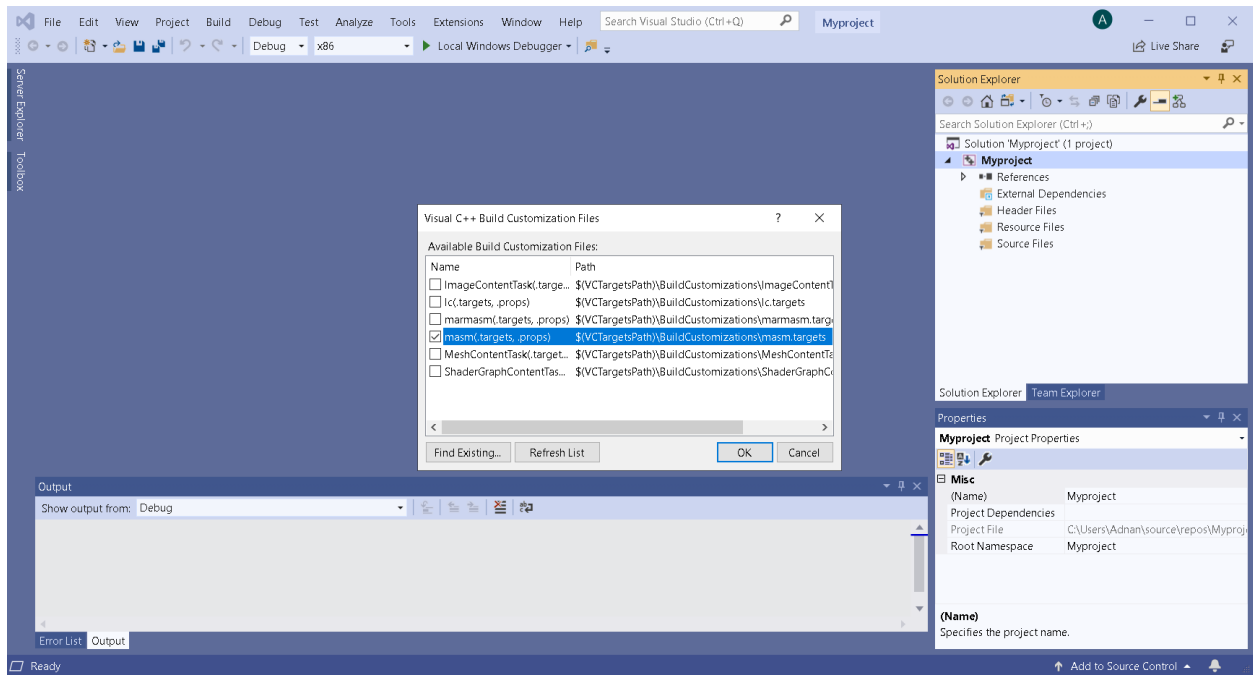
Back Create

Step#5: Right click on project name (i.e., Myproject) → Build Dependencies → Build Customizations

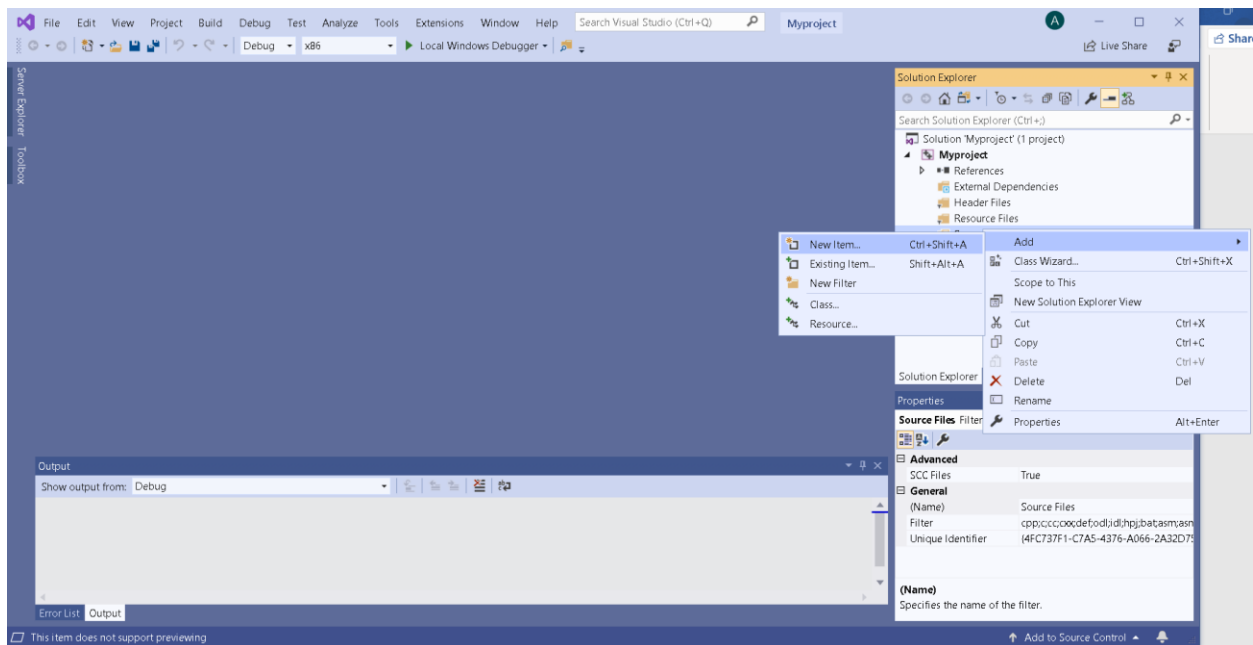


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Step#5: Select “masm” and press OK

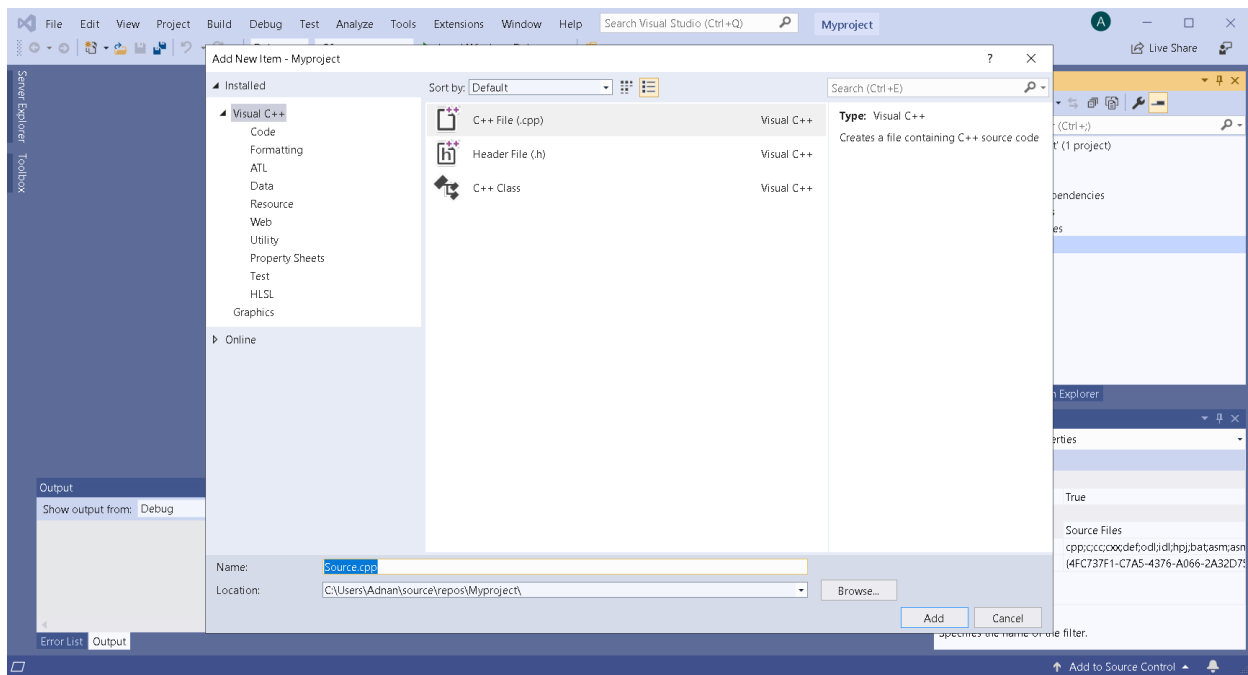


Step#6: Right click on “Source Files” → Add → New Item

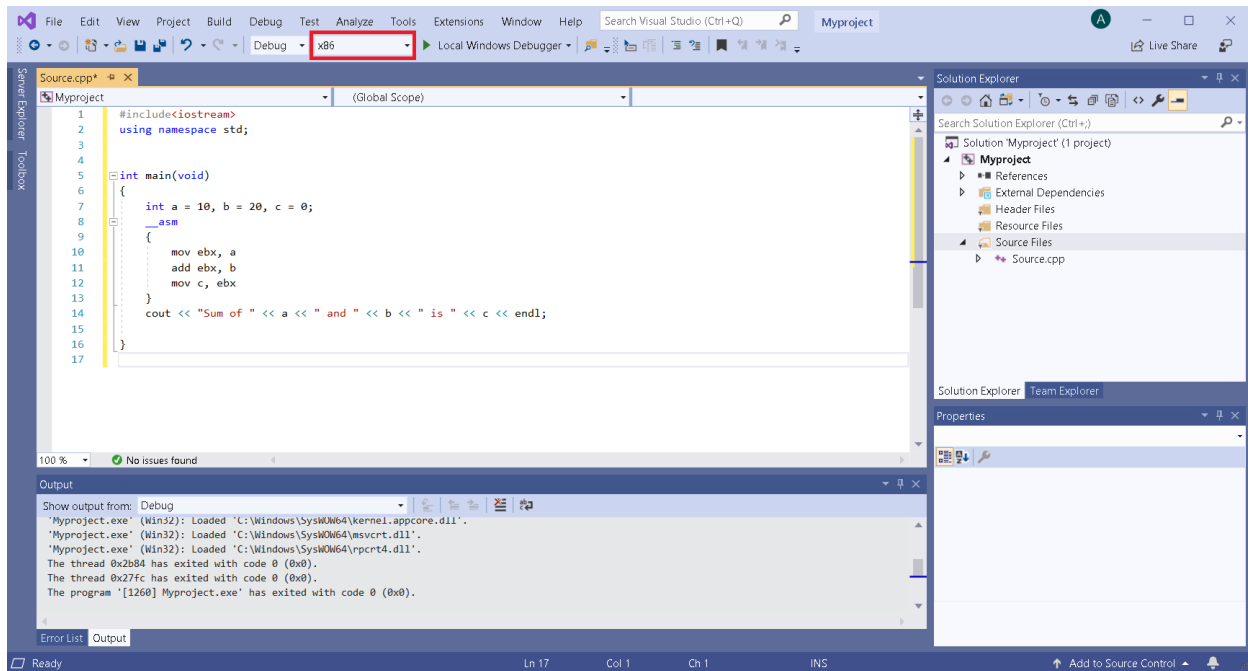


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Step#7: Click in “C++ File (.cpp)”, write a file name and click on Add.



Step#8: Paste code in Example#1 in the text window. Make sure that the environment is set to x86.



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Step#8: Click on “Local Windows Debugger” to run the code.

