



University of Central Punjab

(Incorporated by Ordinance No. XXIV of 2002 promulgated by Government of the Punjab)

Faculty of Information Technology & Computer Science

Mid-term Theory Exam, F22

NAME _____ REG# _____

Computer Organization and Assembly Language

BS(CS), PADP(CS)

Instructions

- All questions are mandatory.
- A scientific calculator is allowed.
- Correction, cutting, or overwriting is not allowed. If you do so, that part of the question will not be counted.
- There is no mistake in the question paper. If you find any, make a sensible guess and solve the question.
- Understanding the problem is part of the problem.
- Solve the first two questions on the question paper and the third question on the answer booklet.

Question#1 (6 + 10 points)

a) The values of various registers before executing each of the following instructions are as follows:

DS:0x1AB0 SI:0x0014 DI:0x0002 AX:0xACBD BX:0x012C CX:0xFEDC DX:0x3120

SS:0x08C0 BP:0x0100

Execute the following instructions and update the registers and memory accordingly. Also, calculate the physical addresses in the hexadecimal number system.

Instructions	Physical Address	Register's contents
MOV [BX], CX	0x1AC2C	
MOV [BP+SI], DX	0X08D14	
MOV AX, [BX+DI]	0x1AC2E	AX: 0xEA3F

Memory

		0x0	0x1	0x2	0x3	0x4	0x5	0x6	0x7	0x8	0x9	0xA	0xB	0xC	0xD	0xE	0xF
0x1AB0	: 0x0100																
0x1AB0	: 0x0110																
0x1AB0	: 0x0120													DC	FE	3F	EA
0x08C0	: 0x0100																
0x08C0	: 0x0110					20	31										
0x08C0	: 0x0120															DA	BF



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- b) Which of the following instructions is invalid? In the case of invalid, give reasons; otherwise, write "valid."

Instructions	Reasons
MOV AX, BH	Invalid: Both operands should be the same size.
MOV BL, 256	Invalid: 256 is a 9-bit number.
MOV ES, CS	Invalid: Both operands cannot be segment registers.
MOV ES, 0xFFCD	Invalid: Immediate addressing is not allowed for sreg.
MOV [DX], BX	Invalid: DX cannot be used in register indirect addressing
MOV [BL], AX	Invalid: BL cannot be used in register indirect addressing
MOV [SI + DI], AX	Invalid: Both registers can't be index registers.
MOV CS, AX	Invalid: Can't modify CS register using mov instruction.
PUSH IP	Invalid: Cannot push IP register
POP CS	Invalid: Cannot pop to CS register

Question#2: (5+ 5 points)

- a) For the given program, write the value of destination operand after execution of each instruction.

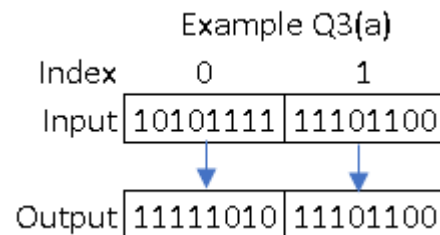
Instructions	AX (Hexadecimal)
XOR AX, AX	0x0000
XOR AX, 0x6450	0x6450
SHL AX, 2	0x9140
ROR AX, 1	0x48A0
AND AX, 0xFEFA	0x48A0

- b) Write the status of various flags after the execution of the ADD instruction.

MOV AX, 128	OF	ZF	SF	PF	AF	CF
ADD AX, AX	0	0	0	1	0	0

Question#3: (20 + 4 points)

- a) Create a procedure that receives a byte array and its size via the stack. The procedure swaps the nibbles of array elements having an even number of ones. Also, call this procedure from the main procedure.
- b) Write a code to write 0xDEAD at physical address 0x3FAE3.





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<pre>;Q3_a .model small .data array db 0x1,0x2,0x3,0x4,0x5 .code main proc mov ax,@data mov ds,ax mov bx,offset array mov si,0 mov cx,5 mov bx,offset array push bx push cx call swap_nibbles pop ax pop ax .exit main endp swap_nibbles proc push bp push cx push bx push si mov bp,sp</pre>	<pre>;Q3_b .model small .data .code Mov ax,0x3FAE Mov es,ax Mov word ptr es:[0x3],0xDEAD .exit</pre>
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```
mov bx,[bp+12]
mov cx,[bp+10]
mov si,0
```

11:

```
mov al,[bx+si]
add al,0
jp l2
inc si
loop l1
```

12:

```
ror al,4
mov [bx+si],al
inc si
loop l1
```

```
pop si
pop bx
pop cx
pop bp
```

ret

swap_nibbles endp