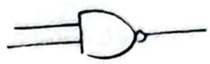
DIGITAL LOGIC DESIGN

x = any possible combination

		0	Y_0	Y_1	Y_2	Y_3
		x	0	0	0	0
1	0	0	1	0	0	0
1	0	1	0	1	0	0
1	1	0	0	0	1	0
1	1	1	0	0	0	1

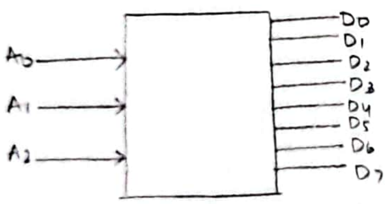
ACTIVE LOW

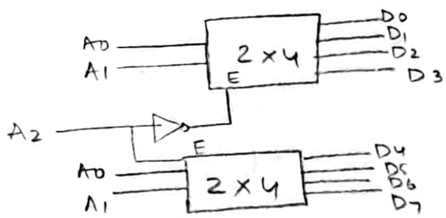
Enable	X_1	X_0	Y_0	Y_1	Y_2	Y_3
1	x	x	1	1	1	1
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0



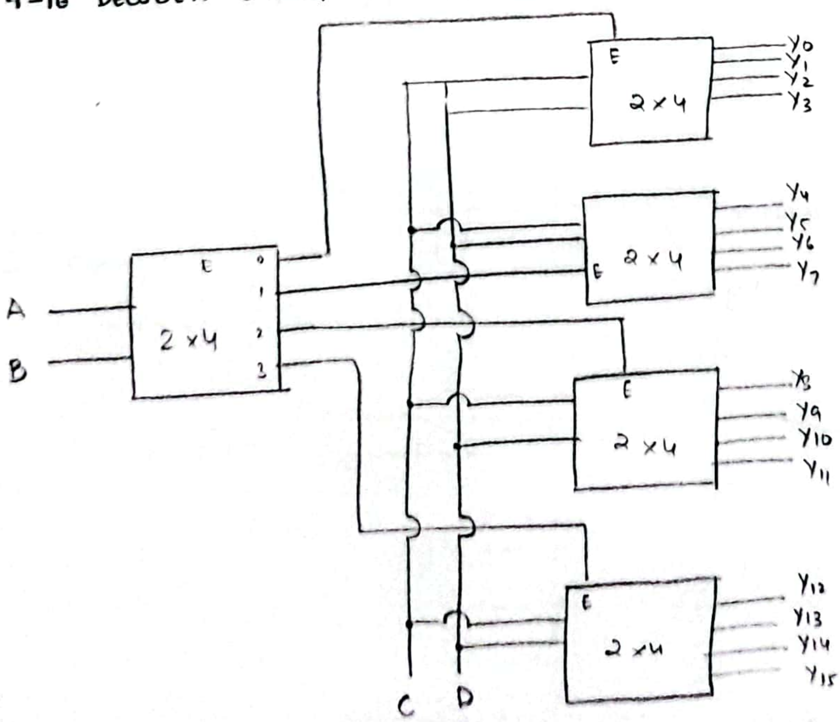
$$Y_0 = E + X_1 + X_0$$

3-8 DECODER USING 2-4 DECODER

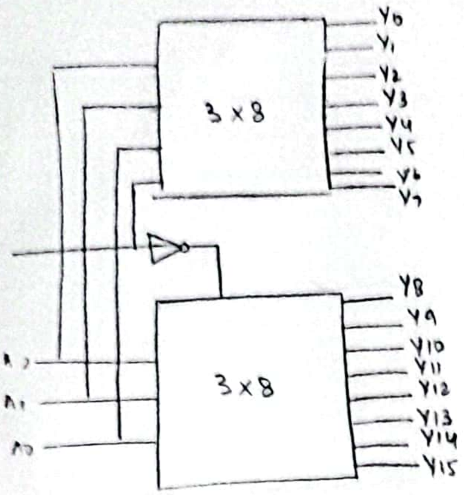




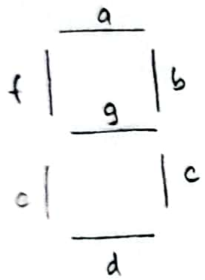
4-16 DECODER USING 2-4 DECODER



4-16 DECODER USING 3-8 DECODER



SEVEN SEGMENT CONVERTER

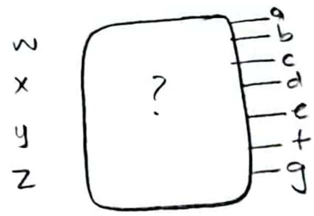


a = ______

b = ______

c = ______

d = ______

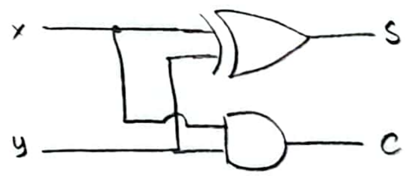


BINARY ADDER - HALF ADDER

x	y	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

$S = x'y + x'y$

$C = xy$



FULL ADDER

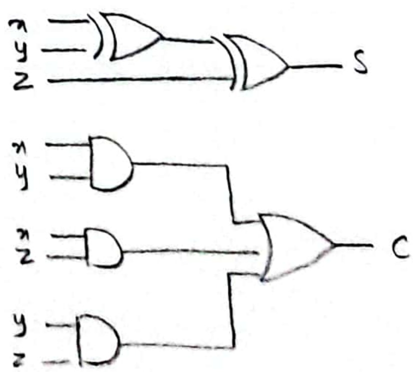
x	y	z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

$S = x \oplus y \oplus z$

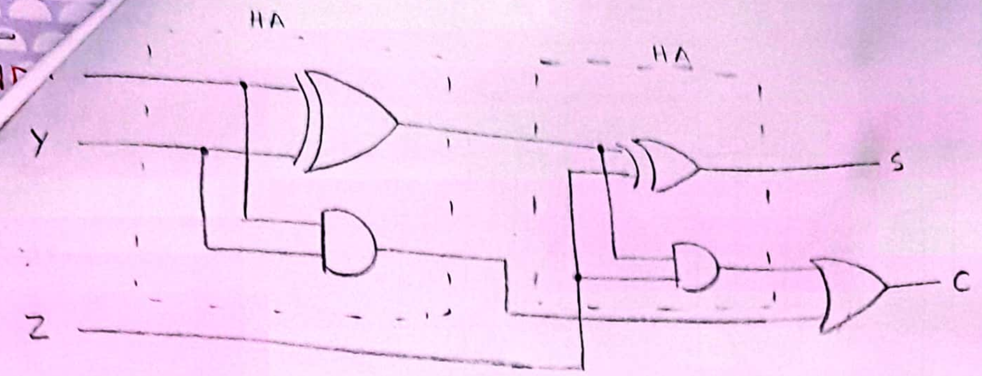
$C = xy + xz + yz$

$x\bar{y}\bar{z} + \bar{x}y\bar{z} + \bar{x}\bar{y}z + xyz$

$\bar{z}(x\bar{y} + \bar{x}y) + z(\bar{x}\bar{y} + xy)$



R = 2 HALF ADDER



$S = (x \oplus y) \oplus z$

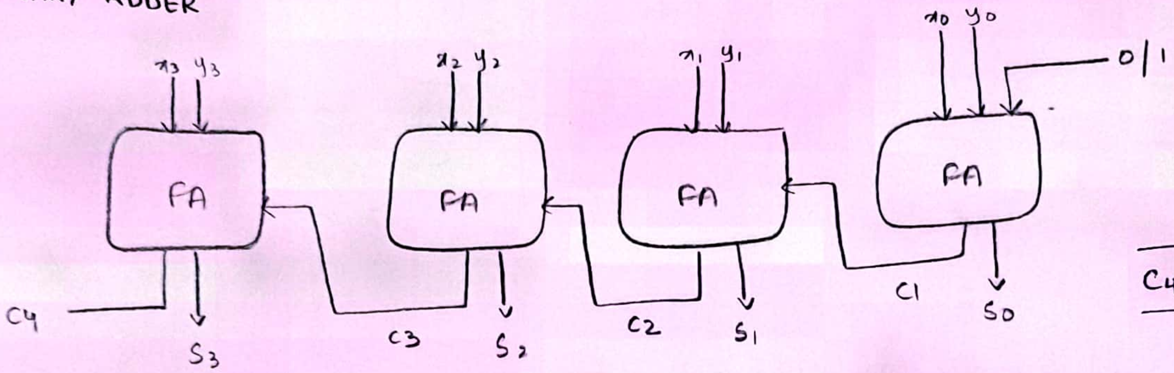
$C = xy + xz + yz$

$= xy + xyz + x\bar{y}z + \bar{x}yz + xyz$

$= xy(1+z) + z(x\bar{y} + \bar{x}y)$

$= xy + z(x \oplus y)$

BINARY ADDER



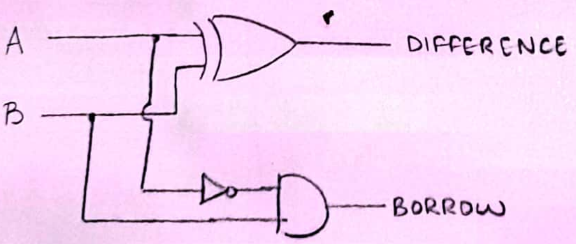
Add = 0

Subtract = 1

$C_4 S_3 S_2 S_1 S_0$

BINARY SUBTRACTOR

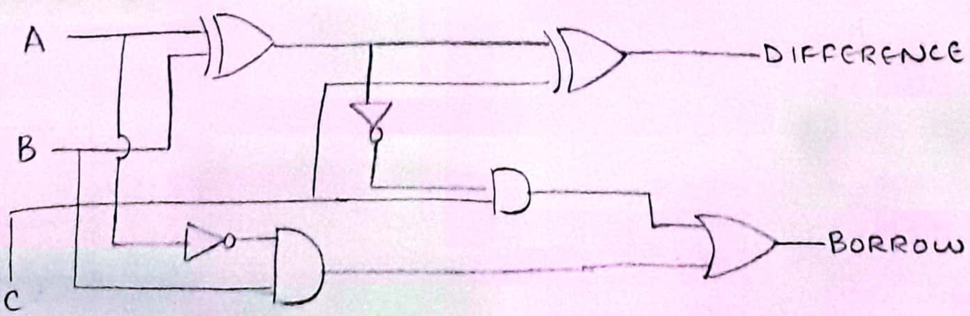
- Half Subtractor
- Full subtractor



HALF

$D = \bar{A}B + A\bar{B} = A \oplus B$

$B = \bar{A}B$

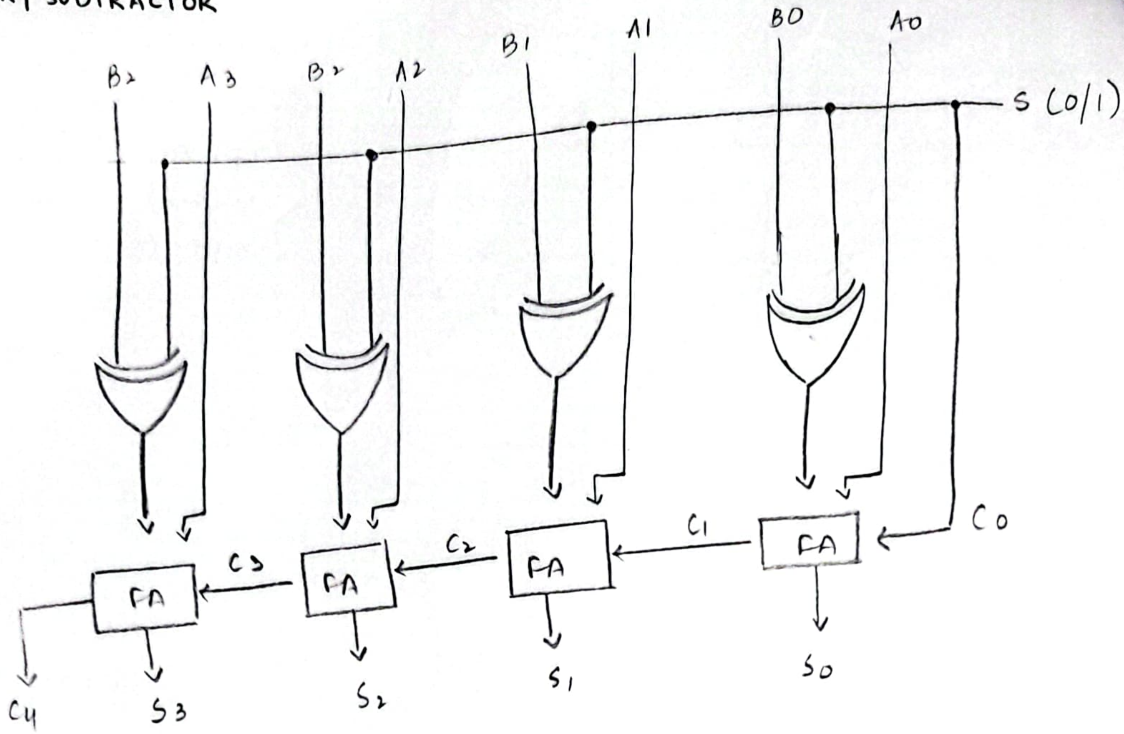


FULL

$D = A \oplus B \oplus C$

$B = \bar{A}B + BC + \bar{A}C$

ADDER / SUBTRACTOR



BCD ADDER

- output sum cannot be greater than 9+9+1 = 19
- add binary of 6 (0110) from binary sum 10 onwards

```
 0 1 0 1 0
   0 1 1 0
 ---------
 1 0 0 0 0
```

IDS

positive, two negative overflow is generated

- overflow generated when XOR of C3 and C4 is 1

COMPARATOR

$A > B$

$A = B$

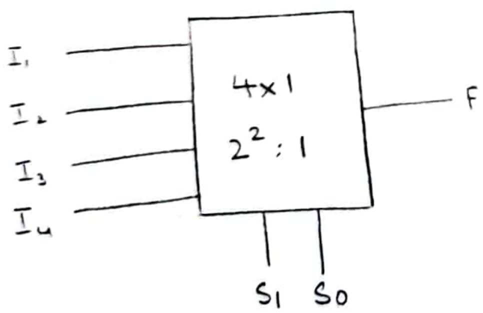
$A < B$

A_1A_0 / B_1B_0	00	01	11	10
00	0	0	0	0
01	1	0	0	0
11	1	1	0	1
10	1	1	0	0

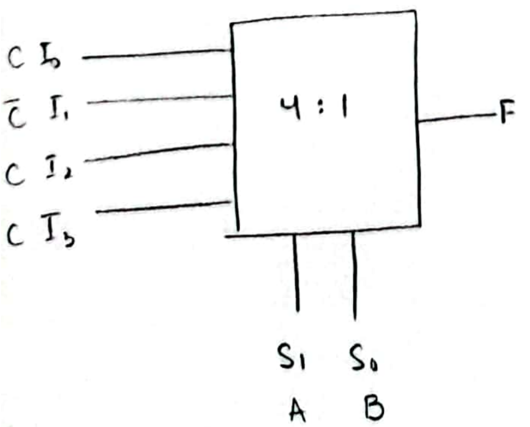
$A_1\bar{B} + A_1A_0\bar{B_0} + A_0\bar{B_1}\bar{B_0}$

MULTIPLEXER

- 2^n input lines, single output, n select lines

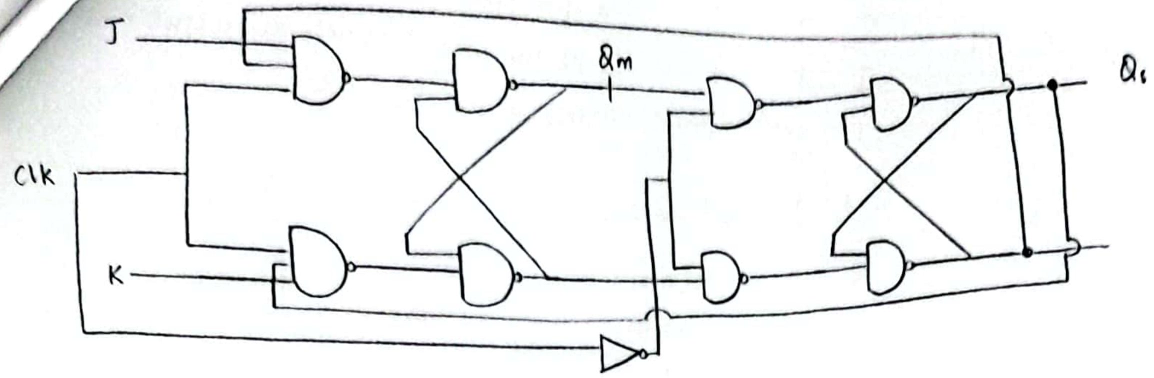


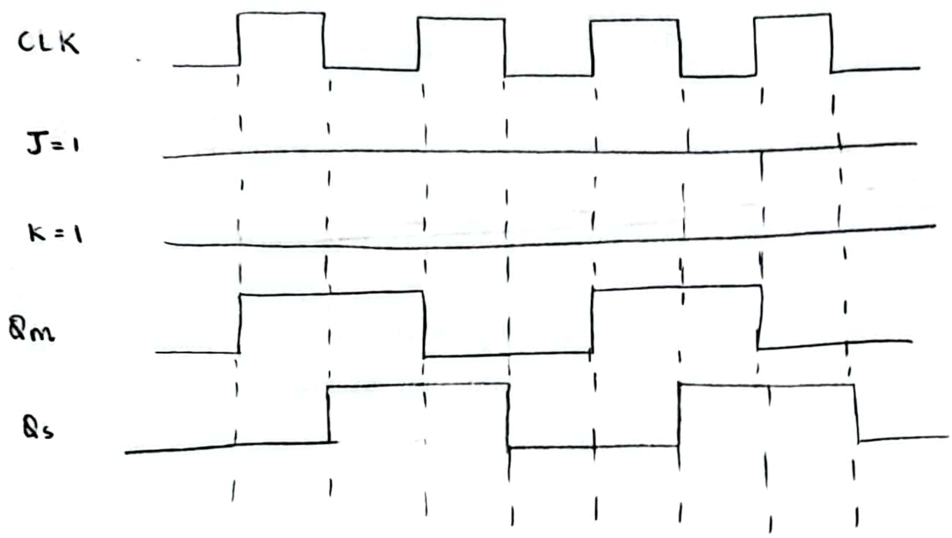
$f(A,B,C) = \Sigma(2,5,7,1)$



A	B	C	F	
0	0	0	0	F = C
0	0	1	1	
0	1	0	1	$F = \bar{C}$
0	1	1	0	
1	0	0	0	F = C
1	0	1	1	
1	1	0	0	F = C
1	1	1	1	

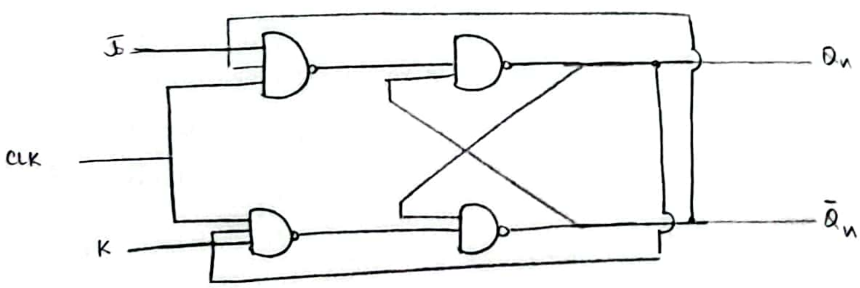
SLAVE JK - FLIPFLOP





* for Qm, state is stored at low so remains same
* for Qs, state is stored at high so remains same.
* if value of Qm is 0 in start the clock will trigger Qm and it will go up until the next up is triggered.
* Qs will then work on negative

JK - FLIPFLOP

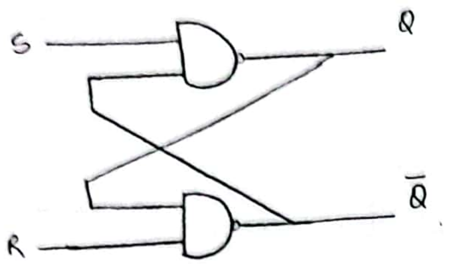


J	K	Q_{n+1}
0	0	Hold
0	1	0
1	0	1
1	1	invalid

* case 1 → $Q_n = 1$ $Q_{n+1} = 0$;
* case 2 → $Q_n = 0$ $Q_{n+1} = 1$;

J	K	Q_{n+1}	
0	0	Q_T	no change
0	1	0	reset
1	0	1	set
1	1	$\overline{Q_T}$	toggle

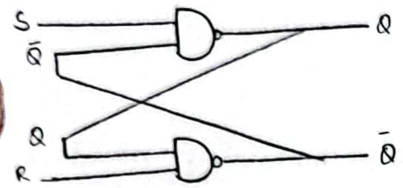
SR LATCH - NAND GATE



x	y	F
0	0	1
0	1	1
1	0	1
1	1	0

* if any one of the input is 0, ... at the second input, as output w... always be 1.

~ S=1 R=1 ~



S	R	Q(n+1)
0	0	invalid
0	1	1
1	0	0
1	1	Q_T

* For S=1 → $\overline{1 \cdot \bar{Q}}$

$\bar{1} + \bar{\bar{Q}}$

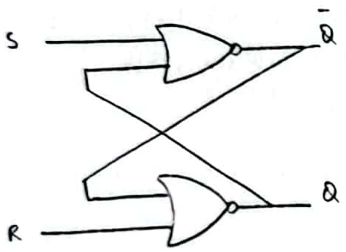
$0 + Q = Q$

* For R=1 → $\overline{1 \cdot Q}$

$\bar{1} + \bar{Q}$

$0 + \bar{Q} = \bar{Q}$

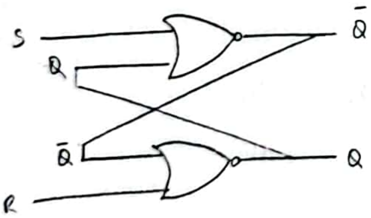
SR LATCH - NOR GATE



x	y	F
0	0	1
0	1	0
1	0	0
1	1	0

* if any one of input is 1, output will always be 0

~ S=0 R=0



S	R	Q(n+1)
0	0	Q_T
0	1	0
1	0	1
1	1	invalid

* For S=0 → $\overline{0 + Q}$

$\bar{0} \cdot \bar{Q}$

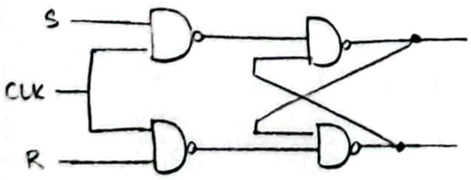
$1 \cdot \bar{Q} = \bar{Q}$

* For R=0 → $\overline{0 + \bar{Q}}$

$\bar{0} \cdot \bar{\bar{Q}}$

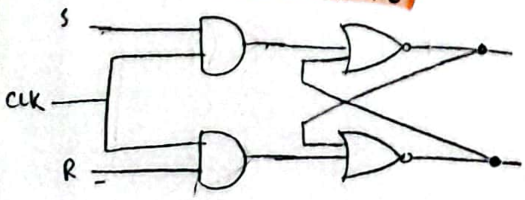
$1 \cdot Q = Q$

SR FLIP FLOP - NAND GATE



CLK	S	R	Q_{n+1}	
0	x	x	Q_n	
1	0	0	Q_n	hold
1	0	1	0	reset
1	1	0	1	set
1	1	1	invalid	

SR FLIP FLOP - NOR GATE



CLK	S	R	Q_{n+1}	
0	x	x	Q_n	
1	0	0	Q_n	hold
1	0	1	0	
1	1	0	1	
1	1	1	invalid	

IDS

CHARACTERISTIC TABLE

S	R	Q(n)	Q(n+1)
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	x
1	1	1	x

} present state holds.

} next state is always 0

} next state is always 1

} invalid.

SR FLIP FLOP EQUATION

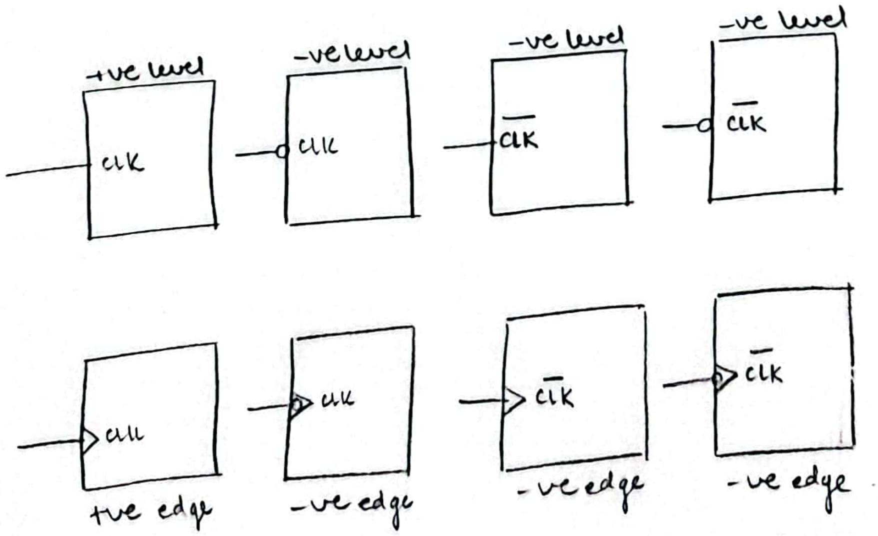
S\R$Q_n$	00	01	11	10
0	0	1	0	0
1	1	1	X	X

$F = \bar{R}Q_n + S$

SR FLIP FLOP EXCITATION TABLE

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

* compare with characteristics table if values are changing then use don't care.



JK FLIP FLOP CHARACTERISTIC TABLE

J	K	Q(n)	Q(n+1)
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

JK FLIP FLOP EQUATION

J\KQn	00	01	11	10
0	0	1	0	0
1	1	1	0	1

$F = \quad + \bar{K}Q_n + J\bar{Q}_n$

JK FLIP FLOP EXCITATION TABLE

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

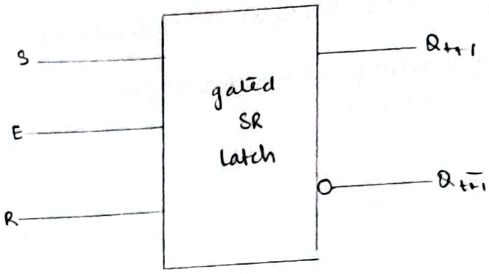
* compare with characteristics table.

IDS

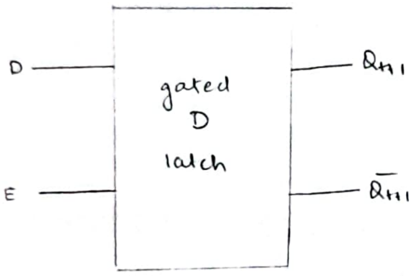
LATCH

E	S	R	Q_{t+1}	$\overline{Q_{t+1}}$
0	x	x	Q_t	$\overline{Q_t}$
1	0	0	Q_t	$\overline{Q_t}$
1	0	1	0	1
1	1	0	1	0
1	1	1	invalid	

- additional gates beside SR latch - NAND
- NAND beside SR-latch



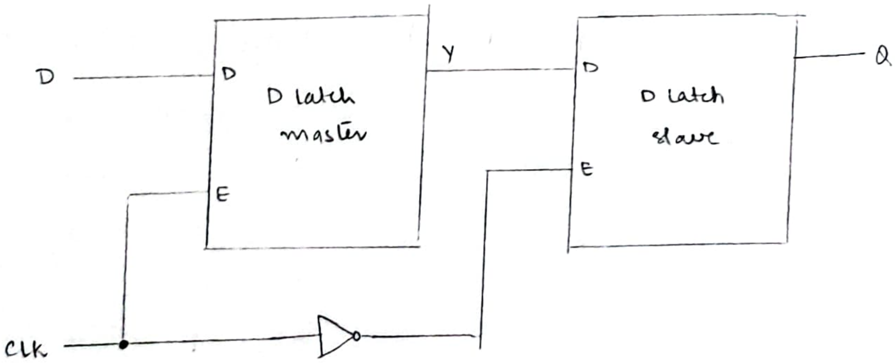
GATED D LATCH



E	D	Q_{t+1}	$\overline{Q_{t+1}}$
0	x	Q_t	$\overline{Q_t}$
1	0	0	1
1	1	1	0

- D is passed as inverter
- D value is reflected in output Q_{t+1}

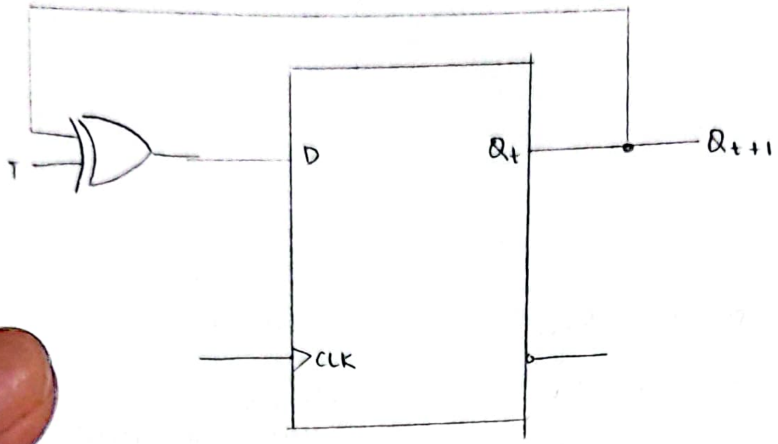
MASTER SLAVE D FLIP FLOP



- if 0 previous state in D, then it will be reflected in Y when clock is 1, but will not be reflected in Q.
- check for falling edge ($1 \to 0$), the output D will be reflected in Q.
- negative edge in clock.

D FLIP FLOP TO T FLIP FLOP

- characteristic table of required flip flop (T)
- excitation table of given flip flop (D)
- insert a column to the right of characteristic table of required FF(T) and name it D
- write a function of D based on input T and present state (Q_T)
- circuit diagram by starting from given FF(D)
- replace D with its equation.



D FLIP FLOP TO JK - FLIP FLOP

1.

J	K	Q_t	Q_{t+1}	D
0	0	0	0	0
0	0	1	1	1
0	1	0	0	0
0	1	1	0	0
1	0	0	1	1
1	0	1	1	1
1	1	0	1	1
1	1	1	0	0

2.

Q_t	Q_{t+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

equation $\rightarrow$ $D = J\bar{Q} + \bar{K}Q$

$Q_{t+1} = J\bar{Q} + \bar{K}Q$

...lop

• ...acteristic table.

D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

★ input is reflected in output.

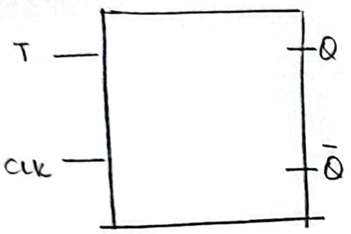
state equation:

$$Q_{t+1} = D$$

• excitation table.

Q_t	Q_{t+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

T FLIP FLOP



• characteristic table.

T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

★ toggle if T=1

T	Q_{t+1}
0	Q_T
1	$\overline{Q_T}$

CHARACTERISTIC EQUATION

$$= T \oplus Q_n$$

$$= T\overline{Q}_T + \overline{T}Q_T$$

EXCITATION TABLE

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

IDS

.and B are two flipflops, input x

$J_A = x \quad K_A = B$

$J_B = x \quad K_B = A'$

state equations $A(t+1)$, $B(t+1)$

$Q_{t+1} = J\bar{Q}_t + \bar{K}Q_T$

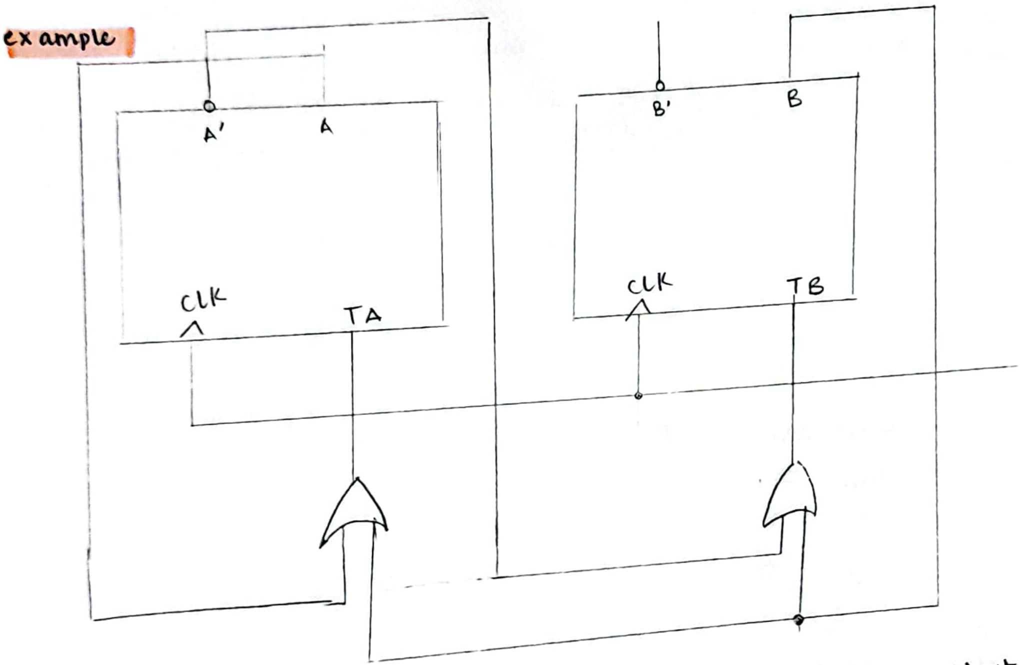
$A_{t+1} = x\bar{Q}_t + \bar{B}Q_T \rightarrow x\bar{A} + \bar{B}A$

$B_{t+1} = x\bar{Q}_t + AQ_T \rightarrow x\bar{B} + AB$

- x, A, B will be input and A(t+1), B(t+1) is the output
- plug in values
- on what value of x will present state move to next state.

x	A	B	A(t+1)	B(t+1)

example



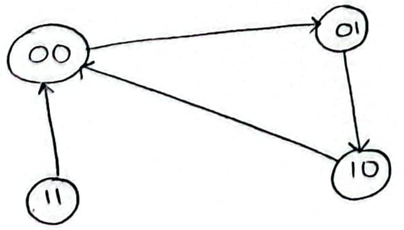
T-flip flop

T	Q_{T+1}
0	Q_t
1	$\bar{Q}_t$

$T_A = B + A$

$T_B = B + \bar{A}$

Present state		Next state		Input	
A	B	A_{t+1}	B_{t+1}	T_A	T_B
0	0	0	1	0	1
0	1	1	0	1	1
1	0	0	0	1	0
1	1	0	0	1	1

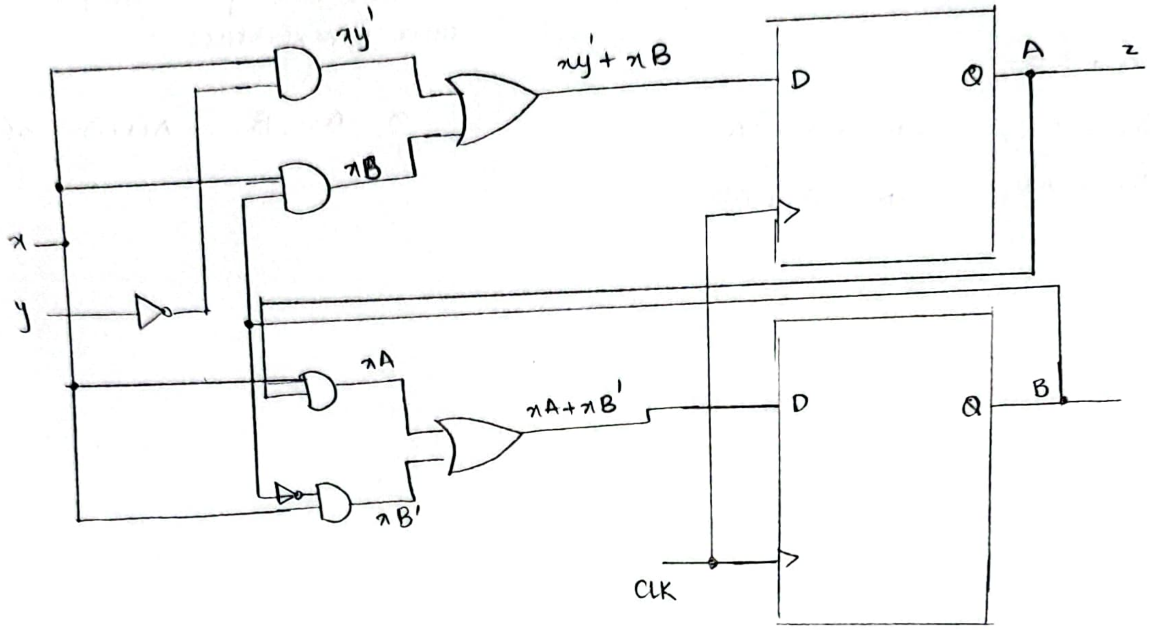


example

$A(t+1) = xy' + xB$

$B(t+1) = xA + xB'$

$z = A$



State Table

Present State		Input		Next State		Output
A	B	X	Y	A_{t+1}	B_{t+1}	Z
0	0	0	0	0	0	0
0	0	0	1	0	0	0
0	0	1	0			
0	0	1	1			
0	1	0	0	0	0	
0	1	0	1	0	0	
0	1	1	0			
0	1	1	1			
1	0	0	0	0	0	
1	0	0	1	0	0	
1	0	1	0			
1	0	1	1			
1	1	0	0	0	0	
1	1	0	1	0	0	
1	1	1	0			
1	1	1	1			

Poin complement, if an end carry is generated, discard it

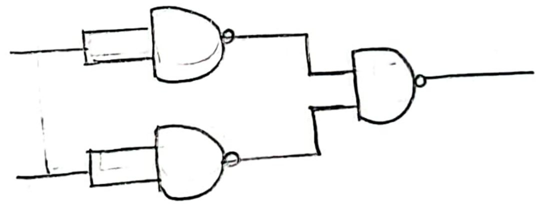
no end cary is generated, then answer is negative and equal to r's complement of the answer.

in (R-1)'s complement, end carry is added to the least significant digit

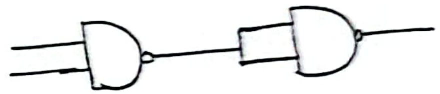
. if no end carry is generated, then answer is negative and equal to (r-1)'s complement.

NAND → NOT

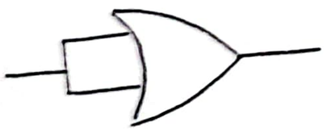
NAND → OR



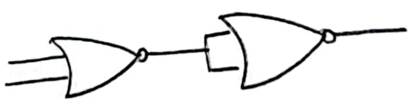
NAND → AND



NOR → NOT



NOR → OR



NOR → AND