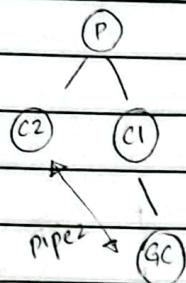


## Dated:

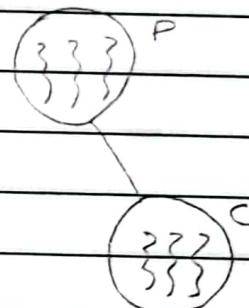


- two fork, first pipe then second pipe
- create pipe before fork.
- parent is the common.

- there cannot be multiple readers because it is a buffered area so data is lost for second reader.
- when buffer is full you'll be block on write's end.

## Threads

- problem 1: if at a time, we have to make multiple processes work it can be done through child process.  
additional cost is to be paid.
- problem 2: CPU times is wasted because of context switching.  
IPC increases.
- problem 3: data sharing. multiple processes and we need to utilize each process for work
- thread is a lightweight process.
- threads exist inside the processes and address space.
- a process can create multiple threads.
- 



PCB		
unit of computation	address	unit of resources
P_id		
T_id		open file resources
Status		
TR		
PC		

- in multiple core, each core has a thread to be executed, means a process can execute multiple threads concurrently.
- different processes can not execute threads.
- context switching between threads of the same process is faster. PCB is not loaded as they're shared. but for different processes it takes the same time.
- IPC exists by default. make global variables. as one data is shared with others in PCB.
- if one file closes, it closes for other

## Dated:

- multicore is hardware component.
- multithread is software component
- thread is always assigned a function.
- pthread-create → this function is used to create
- container → thread id and return.
- attribute → to make joinable or not.
- function ptr → generic, any type of function
- argument to function ptr → arguments in function and then typecast.
- threads which are interested in synchronization are called joinable threads. to send and receive signals.
- those which cannot send or receive signals is called detach.
- joinable threads can be converted into detach. but not vice versa.
- by default, attribute is joinable.
- void\* is a data type in which any type of data type can be stored.
- directly void\* data cannot be used and should be typecasted at first. go back to original
- if a thread has to wait from another thread, then join is called and join tells which thread it is waiting for. typecast - a problem
- same process so thread id will be told by user or the process - data sharing {} {} {} {}
- multiple threads cannot call join for one thread.
- if a thread is terminated then signals won't reach to every thread.

- State process model.
- scheduling rule with queue
- on which basis can scheduling objective.

## Dated:

• ready state means other than CPU, it has everything.

• running state To blocked or exit.

• blocked state To ready.

• running To ready.

• degree of multiprogramming is controlled by the job scheduler.

• since blocked in hard disk, access will be long term  
easier. time taken will be less.

• short term schedule / CPU schedule.

• preemptive scheduling, non pre-emptive

↳ cannot come from ready to running.

• non-preemptive -

• context switching takes place in both preemptive and non-preemptive.

• more in preemptive because of time sharing.

• whichever uses CPU is useful, not keeping it idle.

- increased

• number of processes completed in a unit amount of time. is throughput

- increased.

• turnaround time: adding up all the time from new to exit

- decreased.

• waiting time, wait for CPU so ready queue takes time.

• response time: the first time we tell to start work, user engagement

## SCHEDULING

	1	4	11	16			
	A	B	C		A=0	B=3	C=9
	2				1-1	4-1	11-2
	B						3
PID	Arrived	CPU					
A	3	1	3				
B	1	1	7				
C	2	2	5				

Dated:

Name	PID	Arrival Time	CPU Burst
A	3	0	3
B	1	2	7
C	2	3	5

0 3 10 15



A B C  
0 2 3

A B C

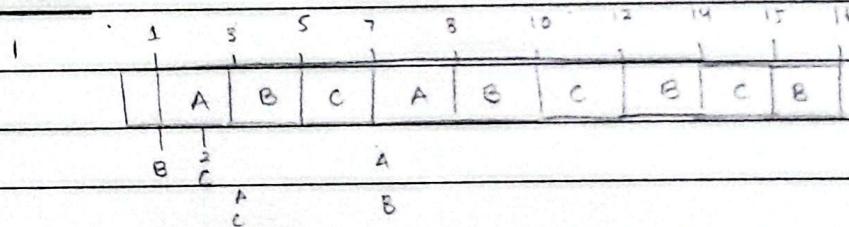
$$0 - 0 + 0 \quad 3 - 2 = 1 \quad 10 - 3 = 7$$

$$= 0 + 1 + 7 = 2.87 \text{ turnaround time}$$

3

- FCFS is non-preemptive in nature
- cannot go from ready to running
- FCFS has an issue known as "starvation effect"

Round Robin

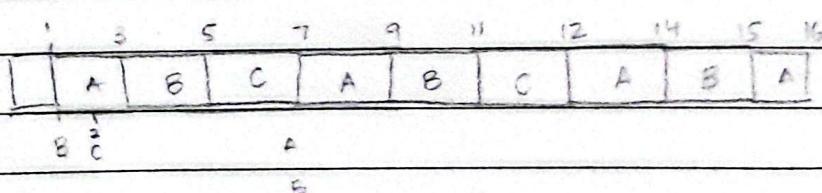


$$A = 2 + 4 = 6$$

$$B = 2 + 2 + 1 = 5$$

$$C = 3 + 3 + 2 = 8$$

CPU Burst	Name	Arrival Time	quantum = 2
7	A	1	
5	B	1	
3	C	2	



$$A = 2 + 4 + 3 + 1 = 10$$

$$B = 2 + 4 + 1 + 2 = 9$$

$$C = 3 + 4 = 7$$

## Dated:

- Race condition where the code has no issue when 2 queue are used and inserted.
- a code which is accessed by shared memory is called critical section.
- in critical section, solution designed has 4 requirements:
  1. mutual exclusion : when 1 process enters CS, a second process cannot enter its shared memory.
  2. no assumptions.
  3. bounded wait : wait has upper bound, no process should be left undefined.  
whichever process enters CS, shouldn't be taken out.
  4. progress : it shouldn't stop
- solution: strict alternation.  
to decide turns between processes.
- 2nd solution: turns and interest both are seen. - in between A can show interest
- semaphores can never be a negative number.
  - the operations are atomic - check and update, OS doesn't disturb
- counting and binary
  - ↳ min = 0, max = 1
  - they are mutex ; lock and unlock.
- deadlock: a state where 2 or more than 2 processes enter into an indefinite wait because of shared resources.
  - if either one gives off resources, then every
- 4 things to create deadlock
  - mutual exclusion:
  - non-preemptive in nature (some resources) - printer
  - hold and wait : those allocated then it is holding and not received is waiting
  - circular wait can be created by above 3 causes.
- ↳ between 2 or more processes, waiting for itself and others to create a circle.

ted:

Deadlock Prevention. → deadlock aashi nihata.

→ remove any one of the 4 causes.

① X

cannot remove because of race conditions.

② X

③ .

give all resources or do nothing. → throughput

④ ✓

strict alternation,

Avoiding Deadlocks. → asata hai, mgh rokein kese?

→ Bankers Algorithm.

↳ available resource, maximum resource for each process, all resources.

↳ check whether the system goes into unsafe state.

↳ extra calculations so throughput is destroyed

Deadlock Detection

• processes are divided into partitions.

page = frame

• in PM and VM, partition size are same.

PM ≠ VM

• virtual memory is greater than PM

• pages and frame calculated, divided by frame/page.

$$mtz = x + y$$

↑ ↑ ↑

\* if one frame doesn't exist, it first needs to upload page in

P7 P5 P10

frame in PM.

F? F? F?

\* after updating z, reflect change in VM.

• Page Faults →

• Demand Paging → through page fault request is seen.

• Page Table → organized way to search a specific page, and then find in PM.

IMPORTANT

• page table in physical memory and interleaved address space, is protected.

• it is required before every operation.

• make convenience or cost, using preset/absent bit

use as flag → 0 means no need to see page table, just load

1 means that in physical memory

inverted page table  
and page table advantages  
and disadvantages?

## Dated:

1. Page size and frame size to be identified.
2. determine size of PM and VM
3. calculate total number of pages in virtual memory and total frames in physical memory.
4. convert these numbers | determine the number of bits required to calculate store these numbers
5. calculate offset bits.
6. determine frame number identify page number.
7. check page table for frame number
8. go to offset in frame.

offset: ik page ke andar kisi bits se save ki ja sakti hain.

page size = offset

- \* offset phle alegi from LSB
- \* offset ki bagis bits, padding keke zero krdein. (page number)
- \* page ki offset bits all frame ki same hongi.

Dated:

fragmentation, wastage of memory.

$$m=16, n=12$$

$$\text{page number} = 16-12 = 4 = m-n \quad (\text{leftmost})$$

$$\text{page offset} = n = 12 \quad (\text{rightmost})$$

$$\text{logical address } 8196 = \underline{\underline{001000000000100}}$$

page number is 2

page offset is 4

- check in page table index 2 and then look into frames.
- append the offset in physical address.

$$\text{address} = \underline{\underline{0100\ 000011000000}}$$

$$m = 16, n = 12$$

$$\text{page number} = 4$$

$$\text{page offset} = 12$$

$$\text{answer} \rightarrow 100000011000000$$

offset is attached as it is.

Translation look aside buffer  $\rightarrow$  special fast lookup hardware cache.

hit ratio

$$2^n = 4$$

virtual memory: when data exceeds RAM limit

$$n = \log_2(m) = 2$$

$$m = 12$$

$$2^m = 6$$

$$n = 4$$

$$2^n$$

$$m-n = 12-4 = 8$$

$$2^m = 6 \times 2^4$$

$$\underline{\underline{00\ 000}} \quad \underline{\underline{11,00}}$$

$$m = 2^4$$

$$m-n = 2^4 - 4 = 2^3$$

## BANKER'S ALGORITHM

Instances  $\rightarrow A=10, B=5, C=7$

PROCESS	ALLOCATION			MAX			AVAILABLE			NEED		
	A	B	C	A	B	C	A	B	C	A	B	C
P1	0	1	0	7	5	3	3	3	2	7	4	3
P2	2	0	0	3	2	2				1	2	2
P3	3	0	2	9	0	2				6	0	0
P4	2	1	1	4	2	2				2	1	1
P5	0	0	2	5	3	3				5	3	1

1. Available : Initial Existing Instance - Allocation

$$A = 0+2+3+2 = 7 \rightarrow 10-7 = 3$$

$$B = 1+0+1+0 = 2 \rightarrow 5-2 = 3$$

$$C = 0+0+2+1+2 = 5 \rightarrow 7-5 = 2$$

2. Need : Max - Allocation

$$P1 \rightarrow 7-0, 5-1, 3-0 \rightarrow 7, 4, 3$$

$$P2 \rightarrow 3-2, 2-0, 2-0 \rightarrow 1, 2, 2$$

$$P3 \rightarrow 9-3, 0-0, 2-2 \rightarrow 6, 0, 0$$

$$P4 \rightarrow 4-2, 2-1, 2-1 \rightarrow 2, 1, 1$$

$$P5 \rightarrow 5-0, 3-0, 3-2 \rightarrow 5, 3, 1$$

3. Safe Sequence.

P1, P3, P4, P5, P2  
P2, P4, P5, P1, P3

Check if Need  $\leq$  Available.

$$P1 \rightarrow [7, 4, 3] \leq [3, 3, 2]$$

$$P2 \rightarrow [1, 2, 2] \leq [3, 3, 2] \rightarrow P2 \text{ will now release allocated resources. } [3, 3, 2] + [2, 0, 0]$$

$$P3 \rightarrow [5, 3, 1] \leq [6, 0, 0] \rightarrow [6, 0, 0] \leq [5, 3, 2]$$

$$P4 \rightarrow [2, 1, 1] \leq [5, 3, 2] \rightarrow P4 \text{ will now release resources. } [5, 3, 2] + [2, 1, 1]$$

$$P5 \rightarrow [5, 3, 1] \leq [7, 4, 3] \rightarrow P5 \text{ will now release resource } [7, 4, 3] + [0, 0, 2]$$

$$P1 \rightarrow [7, 4, 3] \leq [7, 4, 5] \rightarrow P1 \text{ will now release resource } [7, 4, 5] + [0, 1, 0]$$

$$P3 \rightarrow [6, 0, 0] \leq [7, 5, 5] \rightarrow P3 \text{ will now release resource } [7, 5, 5] + [3, 0, 2]$$

$$= [10, 5, 7]$$

Example: P2 requests (1,0,1)

$$\text{Available } [3,3,2] \rightarrow [3,3,2] - [1,0,1] = [2,3,1]$$

$$P2\text{-Need } [1,2,1] \rightarrow [1,2,1] - [1,0,1] = [0,2,0]$$

$$P2\text{-Allocation } [2,0,0] \rightarrow [2,0,0] + [1,0,1] = [3,0,1]$$

new state is safe.

Example: P4 requests (3,3,0)

since P1 had requested (1,0,1), we now have available resources

(2,3,0) which is not sufficient for P4, hence P4 has to wait.

Example: P1 requests (0,1,2)

$$\text{Available } [2,3,0] \rightarrow [2,3,0] - [0,1,2] = [2,1,0]$$

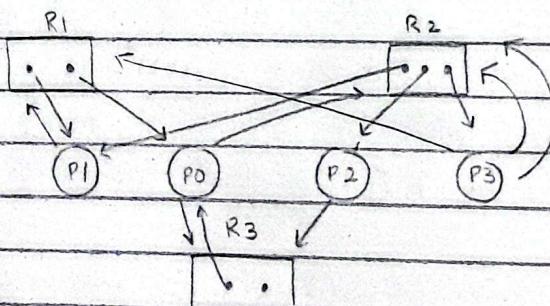
$$P1\text{-Need } [7,4,3] \rightarrow [7,4,3] - [0,1,2] = [7,2,1]$$

$$P1\text{-Allocation } [0,1,0] \rightarrow [0,1,0] + [0,1,2] = [0,3,0]$$

no row in the table has need < available, hence unsafe state.

P0 should wait.

#### MULTIPLE INSTANCE RESOURCE ALLOCATION GRAPH



PROCESS	ALLOCATE			REQUEST		
	R1	R2	R3	R1	R2	R3
P0	1	0	1	0	1	1
P1	1	1	0	1	0	0
P2	0	1	0	0	0	1
P3	0	1	0	1	2	0

Current Availability  $\rightarrow$  
$$\begin{bmatrix} R_1 & R_2 & R_3 \\ 0 & 0 & 1 \end{bmatrix}$$
  
check resources

2. safe sequence

$$P_0 [0, 1, 1] \leq [0, 0, 1] \times$$

$$P_1 [1, 0, 0] \leq [0, 0, 1] \times$$

$$P_2 [0, 0, 1] \leq [0, 0, 1] \checkmark$$

$$[0, 0, 1] + [0, 1, 0] = [0, 1, 1] \rightarrow P_2$$

$$P_3 [1, 2, 0] \leq [0, 1, 1] \times$$

$$[0, 1, 1] + [0, 1, 0] = [0, 2, 1] \rightarrow P_2 P_3$$

$$P_0 [0, 1, 1] \leq [0, 1, 1] \checkmark$$

$$[0, 1, 1] + [1, 0, 1] = [1, 1, 2] \rightarrow P_2 \dots P_0$$

$$P_1 [1, 0, 0] \leq [1, 1, 2] \checkmark$$

$$[1, 1, 2] + [1, 1, 0] = [2, 2, 2] \rightarrow P_2 \dots P_0 P_1$$

$$P_3 [1, 2, 0] \leq [2, 2, 2] \checkmark$$

$$[2, 2, 2] + [0, 1, 0] = [2, 3, 2] \rightarrow P_2 P_0 P_1 P_3$$

### LEAST RECENTLY USED

Reference string: 7, 0, 1, 1, 2, 0, 3, 0, 4, 2, 3, 0, 3, 2, 1, 1, 2, 0, 1, 1, 7, 0, 1

Frames = 4

F4	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2
F3	1	1	1	1	1	4	4	4	4	4	4	1	1	1	1	1	1	1	1
F2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
F1	7	7	7	7	7	3	3	3	3	3	3	3	3	3	3	3	7	7	7
	PF	PF	PF	PF	H	PF	H	H	H	H	H	PF	H	H	H	PF	H	H	.

• least recently used page in past



• page fault : 8

• page hit : 12

### CLOCK POLICY

Reference string: 2, 1, 3, 1, 2, 1, 1, 5, 2, 1, 4, 1, 5, 1, 3, 2, 1, 5, 2

Frames = 3

F3	→	→	1*	1	→	1	4*	4*	4	4	4	5*	5*					
F2	→	3*	3*	3*	→	3	2*	2*	2*	→	2	→	2*	2*	2*			
F1	2*	2*	2*	2*	→	2*	5*	5*	5*	→	5*	3*	3*	3*	3*	3*		
	PF	.																



if all bits are set to 1, then

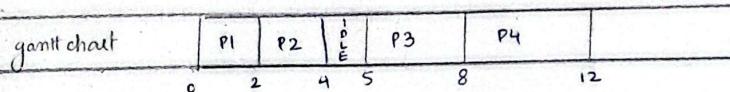
change it to .



## SCHEDULING POLICIES

### 1. FIRST COME FIRST SERVED - NON PREEMPTIVE

PROCESS	ARRIVAL	BURST	COMPLETION	TURN AROUND	WAITING TIME	RESPONSE TIME
P1	0	2	2	2	0	0
P2	1	2	4	3	1	1
P3	5	3	8	3	0	0
P4	6	4	12	6	2	2



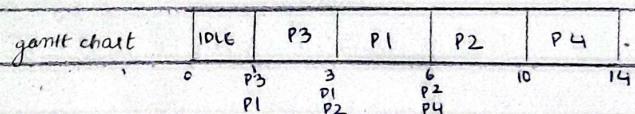
$$\text{turnaround time} = \text{completion} - \text{arrival}$$

$$\text{waiting time} = \text{turnaround} - \text{burst}$$

$$\text{response time} = \text{CPU allotted} - \text{arrival time}$$

### 2. SHORTEST JOB FIRST - NON PREEMPTIVE

PROCESS	ARRIVAL	BURST	COMPLETION	TURN AROUND	WAITING TIME
P1	1	3	6	5	2
P2	2	4	10	8	4
P3	1	2	3	2	0
P4	4	4	14	10	6



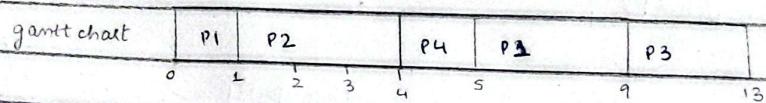
- criteria is burst time

- check for arrival time = 0, if not keep it idle

- shortest burst time

3. SHORTEST REMAINING TIME FIRST - PREMPTIVE

PROCESS	ARRIVAL	BURST	COMPLETION	TURN AROUND	WAITING TIME	RESPONSE TIME	
P1	0	5	4	9	4	0	
P2	1	3	4	3	0	0	
P3	2	4	19	11	7	7	
P4	4	1	5	1	0	0	



$$P1 \rightarrow 5-1=4-4=0$$

$$P2 \rightarrow 3-1=2-1=1-1=0 \text{ DONE}$$

$$P3 \rightarrow 4-4=0$$

$$P4 \rightarrow 1-1=0$$

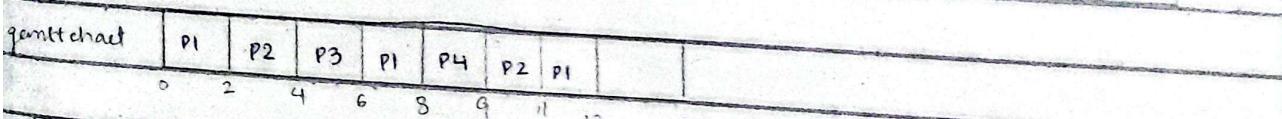
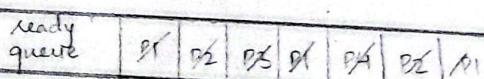
\* criteria is burst time.

4. ROUND ROBIN

PROCESS	ARRIVAL	BURST	COMPLETION	TURN AROUND	WAITING TIME	RESPONSE TIME	
P1	0	5	12	12	7	0	
P2	1	4	11	10	6	1	
P3	2	2	6	4	2	2	
P4	4	1	9	5	4	4	

$$TQ = 2$$

\* criteria is time quantum



$$P1 \rightarrow 5-2=3-2=1-1=0$$

$$P2 \rightarrow 4-2=2-2=0$$

$$P3 \rightarrow 2-2=0$$

$$P4 \rightarrow 1-1=0$$

## PAGING

logical address space of 256 pages with a 4KB pagesize  
physical memory of 64 frames.

$$\text{page size} = 4 \times 1024 = 4096 \text{ bytes}$$

$$\text{frame size} = \text{page size}$$

a) bits for logical address

$$\text{size of logical address space} = 2^m$$

$$\# \text{ of pages} (2^{m-n}) \times \text{page size} (2^n)$$

$$2^n = 4096 \rightarrow \log_2(4096) = m \rightarrow 12 = m \text{ (offset) [bits]}$$

$$2^m / 2^n = 256$$

$$2^m = 256 \times 4096$$

$$4096$$

$$m = \log_2 \left( \frac{256}{4096} \right)$$

$$m = 8$$

$$m - n = 12 - 8 = 4 \text{ (pagenumber) [bits]}$$

b) bits for physical address

$$\text{offset} = n = 12 \text{ [bits]}$$

$$2^m = 64$$

$$2^n$$

$$2^m = 64 \times 4096$$

$$m = 18$$

$$m - n = 18 - 12 = 6 \text{ (frames) [bits]}$$