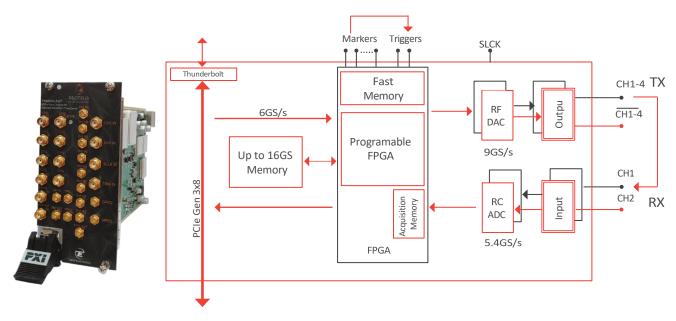


Arbitrary Waveform Generator/Transceiver

The Proteus Arbitrary Waveform Generator (AWG) is ideal for applications in Quantum Computing, Electronic Warfare, Radar, and next generation communications such as 5G, 6G, Ultrawide Bandwidth (UWB), Wi-Fi 6, 7, and more. Built on the latest RF DAC and RF ADC technology, this versatile product platform has sample rates up to 9GS/s that allows for multiple Nyquist zone operation providing frequency ranges in excess of 10GHz. It has an innovative hardware based (FPGA) task oriented programming and signal processing environment. When used in combination with its optional RF Digitizer it becomes an Arbitrary Waveform Transceiver (AWT) giving you the ability to change waveforms in real-time; making it ideal for improving the coherence time of a Qubit, characterizing an RF amplifier, or responding to an EW (Electronic Warfare) threat.

Modular Scalable Architecture

Proteus is a modular design based on the industry standard PXIe format. Each module can be configured to have up to four RF/ μ W differential outputs and two digitizer inputs. Hardware based user programming is facilitated by the easy to use FPGA based DSP programming system, large waveforms and acquisitions can use the its large 16GS onboard memory and fast data transceiver is facilitated through its PCIe Gen 3 x 8 interface.





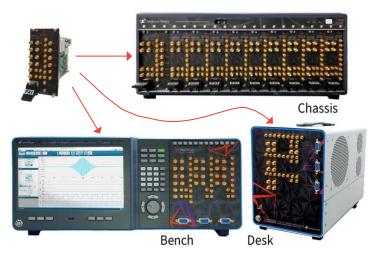


Multiple Formfactors

Infinite possibilities

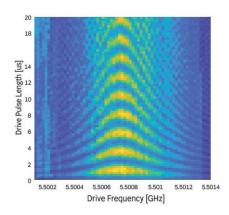
For high density applications such as a high Qubit count Quantum Computers, Massive MIMO or phased array Radar and Electronic Warfare Systems the PXIe Chassis system allows you to scale. It is compatible with the industry standard PXIe modular architecture, providing custom systems capability alongside other PXIe compatible instrumentation such as the Tabor A10200 20GHz Amplifier.

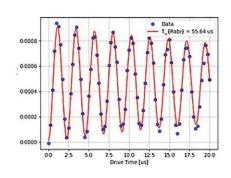
The benchtop version of the Proteus series offers up to 12 channels in a 4U, 19" box. With a 9" touch display and on-board PC that can run Tabor, Python and MATLAB applications. The desktop is identical to the bench, but has the screen and keyboard omitted.

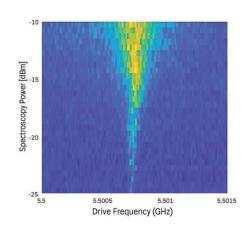


Applications

Quantum Physics - Proteus plays a part in many Quantum Physics Experiments. Its unique AWT architecture allows for the generation and analysis of pulses in real time, with fast measurement response and feedback provided with its FPGA based decision block architecture. Applications include NMR/EPR, Device Characterization, Computing, Communications and Sensing. With direct to RF/ μ W capability it eliminates the need of cumbersome up/down converting units and requires no IQ alignments. It can be scaled to 1000s of coherent channels, and its advanced signal processing engine has the capability of analyzing up to 10 frequency multiplexed readout lines.



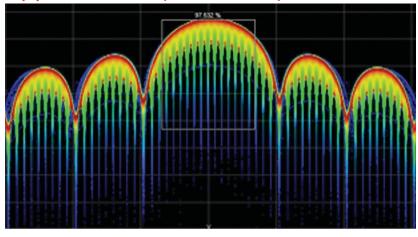






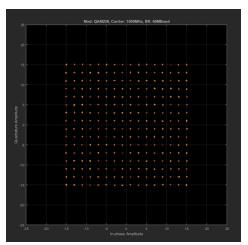


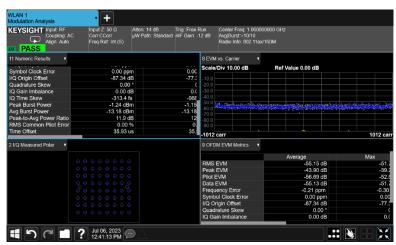
Applications - (continued)



Radar and Electronic Warfare - Proteus is an ideal tool for real time waveform generation and analysis up to and including X-Band. The transceiver allows for real-time closed loop analysis for fast feedback systems such as Radar Target Generation and Adaptive Electronic Warfare Systems. The scalable multi-channel, coherent, deterministic waveform playout capability, allows for the generation of multiple active emitters, while its 2GHz of Bandwidth allows for easy creation of background electromagnetic emissions.

Next Generation Wireless Communications Systems – When designing, developing and manufacturing new wireless systems based on technologies such as Multiple In and Multiple Out (MIMO) antenna matrices and Orthogonal Frequency Division Multiplex (OFDM) modulation, Proteus is built on a scalable wide bandwidth (2GHz) architecture, high performance RF DAC/ADC (EVM better than -50dBc) that is compatible with MATLAB. Allowing you to create, model, then transfer waveforms or sequencies of waveforms to Proteus for real world test.





Generate any Imaginable Scenario - Proteus has an innovative hardware-based task-oriented programming system for complex waveform sequences. You can generate and download waveforms simultaneously, stream data directly to the FPGA (by-passing the memory) at speeds of up to 4GS/s, a full and easy to program digital subsystem of digital up and down converters, finite impulse response filters, FFT and multiple real time averaging blocks. This makes the Proteus AWT the most comprehensive measurement solutions available.





Proteus Series Specifications

CHANNEL CHARACTERISTICS	P908xy ¹	P258xy ¹	P128xy ¹	P948xy ¹
FORM FACTOR ¹	M/B/D	M/B/D	M/B/D	M/B/D
NUMBER OF CHANNELS	M=2, B=2/4/6, D=2/4/6	M=2/4, B=2/4/8/12, D=2/4/8/12	M=2/4, B=2/4/8/12, D=2/4/8/12	M=2/4, B=2/4/8/12, D=2/4/8/12
INITIAL SKEW				
BETWEEN CHANNELS		<50ps typ., 1 SCLK max.		
BETWEEN MODULES	<100ps typ., 1 SCLK or 300ps max.			
FINE DELAY				
RANGE	0 to 3ns			
RESOLUTION	5ps			
ACCURACY	±5ps			
COARSE DELAY				
RANGE	0 to wavelength			
RESOLUTION	1 sample point			

ARBITRARY MODE	P908xy	P258xy	P128xy	P948xy
MAX. SAMPLE RATE	9GS/s	2.5GS/s	1.25GS/s	9GS/s
RESOLUTION	8-bit	16-bit		
MAX. MEMORY SIZE	Up to 16GS	Up to 8GS		
NUMBER OF SEGMENTS	64k			
MINIMUM SEGMENT LENGTH				
NORMAL	2048 points	1024 points		
FAST SEGMENT	224 points	64 points		
WAVEFORM GRANULARITY				
STANDARD	64 points	32 points	32 points	32 points
OPTIONAL	32 points	16 points	16 points	16 points

TASK MODE	
TASK TABLE LENGTH	64K tasks per channel
TASK LOOPS	1M
SEQUENCE	A sequence is defined as a continuous and looped series of tasks
MAX. NUMBER OF SEQUENCES	32k sequences
SEQUENCE LOOPS	1M
SCENARIO	A scenario is defined as a continuous series of tasks/sequences
MAX. NUMBER OF SCENARIOS	1k scenarios

STREAMING (STM OPTION)	
MAX. STREAM RATE	Up to 6GS/s
MINIMUM PC REQUIREMENTS	
CPU	i7
MEMORY	32GB
OPERATING SYSTEM	Windows 10
SOURCE	PXI Express Bus

SIGNAL PURITY	DC OUTPUT	DIRECT OUTPUT
HARMONIC DISTORTION (2)		
fout = 10 MHz - 200 MHz, Measured @ DC to 2 GHz	<-70 dBc (typ.)	<-70 dBc (typ.)
fout = 200 MHz - 1.5 GHz, Measured @ DC to 4.5 GHz	<-60 dBc (typ.)	<-60 dBc (typ.)
fout = 1.5 GHz - 4.5 GHz, Measured @ DC to 4.5 GHz	<-50 dBc (typ.)	<-50 dBc (typ.)
SFDR (3)		
fout = 10 MHz500 MHz, Measured @ DC to 1.5 GHz	-80 dBc (typ.)	<-85 dBc (typ.)
fout = 500 MHz4.5 GHz , Measured @ DC to 4.5 GHz	-70 dBc (typ.)	<-75 dBc (typ.)
PHASE NOISE (@10kHz offset)		
fout = 140.625MHz	-134 dBc/Hz	
fout = 280.25MHz	-128 dBc/Hz	
fout = 562.5MHz	-122 dBc/Hz	
fout = 1.125GHz	-116 dBc/Hz	
fout = 2.25GHz	-110 dBc/Hz	
fout = 4.5GHz	-104 dBc/Hz	

² SCLK=Max sample rate, amplitude = 400mVpp, direct mode, measured using balun.

³ SCLK=Max sample rate, amplitude = 400mVpp, excluding SCLK/2-fout, measured using balun.



 $^{^{1}}$ x = Number of channels, y=M/B/D=Module/Benchtop/Desktop.



DC OUTPUT	
OUTPUT TYPE	Single-ended or differential, DC-coupled
IMPEDANCE	50Ω (nom)
AMPLITUDE	50 mVp-p to 1.3 Vp-p
AMPLITUDE RESOLUTION	1mV
DC AMPLITUDE ACCURACY	±(3% of amplitude ±2 mV)
VOLTAGE WINDOW	±1.15V
DC OFFSET	±0.5V
OFFSET RESOLUTION	10mV
DC OFFSET ACCURACY	±(3% of setting ±15 mV)
SKEW BETWEEN NORMAL AND COM- PLEMENT OUTPUTS	0ps
RISE/FALL TIME (20% TO 80%)	< 130ps (typ.)
INSTANTANEOUS BANDWIDTH	
P128xy P258xy P908xy P948xy	625MHz 1.25GHz 4.5GHz 4.5GHz
MAX. USABLE FREQUENCY	1 st /2 nd Nyquist
P128xy P258xy P908xy P948xy	1.25GHz 2.5GHz 4.5GHz 4.5GHz
JITTER (PEAK-PEAK)	<1ps (typ.)
OVERSHOOT	<5% (typ.)
CONNECTOR	SMA (female)

DIRECT OUTPUT (OPTIONAL, STAND	AR for P9482xy)
OUTPUT TYPE	Single-ended or differential, AC coupled
IMPEDANCE	50Ω (nom)
AMPLITUDE	
SINGLE-ENDED	1mVpp to 550mVpp, single-ended into 50Ω
DIFFERENTIAL	1mV to 1.1Vpp
AMPLITUDE RESOLUTION	1mV
AMPLITUDE ACCURACY	±(3% of amplitude ±2 mV)
RISE/FALL TIME (20% TO 80%)	< 60ps (typ.)
INSTANTANEOUS BANDWIDTH	
P128xy P258xy P908xy P948xy	625MHz 1.25GHz 4.5GHz
MAX. USABLE FREQUENCY	3 rd Nyquist
P128xy P258xy P908xy P948xy	1.25GHz 2.5GHz 10GHz 10GHz
SKEW BETWEEN NORMAL AND	0 ps
COMPLEMENT OUTPUTS	
JITTER (PEAK-PEAK)	<1ps (typ.)
CONNECTOR	SMA (female)

SYNC CLOCK OUTPUT	
AMPLITUDE	500mVpp, typ.
FREQUENCY	
P908xy	SCLK/32
P128xy, P258xy	SCLK/8
P948xy	SCLK/8 (standard), SCLK/32 (x1 mode)
WAVEFORM	Square
RISE/FALL TIME (20% TO 80%)	<150ps
IMPEDANCE	LVCMOS
CONNECTOR	SMP (male)

MARKER OUTPUTS	
NUMBER OF MARKERS	Refer to ordering information
OUTPUT TYPE	Single ended
OUTPUT IMPEDANCE	50Ω (nom.)
AMPLITUDE	
VOLTAGE WINDOW	±1.15V
LEVEL	32mVpp to 1.2Vpp (32 discrete levels)
RESOLUTION	10mVpp
ACCURACY	±7%
OFFSET	
RANGE	±0.5V
RESOLUTION	10mV
ACCURACY	±(3% of setting ±15 mV)
RISE/FALL TIME (20% TO 80%)	<200ps
MARKER LENGTH	0 - waveform length
RESOLUTION	
P128xy, P258xy P9082y	2 pts
P948xy	8 pts 2 pts (standard) 8 pts (x1 mode)
MARKER DELAY	2 pts (standard) 6 pts (x1 mode)
COARSE DELAY	
RANGE	0 to 2048 points
RESOLUTION	
P128xy, P258xy P9082y	8 points
P948xy	32 points
	8 pts (standard), 32 pts (x1 mode)
FINE DELAY	
RANGE	0 to 1.2ns
RESOLUTION	1ps
ACCURACY	15ps
CONNECTOR	SMP (male)

TTL MARKER OUTPUTS (OPTION)	
NUMBER OF MARKERS	8
OUTPUT TYPE	Single ended
OUTPUT IMPEDANCE	50Ω or $10k\Omega$ factory configured
OUTPUT HIGH LEVEL	3.3V typ., 2.4V min.
OUTPUT LOW LEVEL	0.1V typ., 0.25V max.
RISE/FALL TIME (20% TO 80%)	<1ns
RESOLUTION	2ns
MIN PULSE WIDTH	2ns
CONNECTOR	SMP (male)





REFERENCE CLOCK OUTPUT		
SOURCE	Internal TCXO	
WAVEFORM	Square	
FREQUENCY	100MHz or REF IN	
STABILITY	+/- 2.5 PPM	
AGING	+/- 1 PPM @ +25°C (per year)	
CONNECTOR	SMP (male)	

REFERENCE CLOCK INPUT	
INPUT FREQUENCIES	10MHz / 100MHz selectable
LOCK RANGE	± 1MHz
INPUT LEVEL	0.6 Vp-p to 1.7 Vp-p
IMPEDANCE	50Ω, AC coupled (nom.)
CONNECTOR	SMP (male)

SAMPLE CLOCK OUTPUT	
SOURCE	Selectable, internal synthesizer or sample clock input
FREQUENCY RANGE	SCLK range
OUTPUT AMPLITUDE	0.5V to 1V depending on SCLK
IMPEDANCE	50Ω (nom.), AC coupled
CONNECTOR	SMA (female)

SAMPLE CLOCK INPUT	
FREQUENCY RANGE	SCLK Range
INPUT LEVEL RANGE	0.4Vpp to 1.2Vpp
DAMAGE LEVEL	<-0.5V or >1.5V
INPUT IMPEDANCE	50Ω nom., AC coupled
CONNECTOR	SMA (female)

TRIGGER INPUTS	
RANGE	−5V to +5V
THRESHOLD	±5V
RANGE	−5V to +5V
RESOLUTION	100mV
SENSITIVITY	200mV
JITTER	
STANDARD	8 SCLK periods
P128xy, P258xy,P908xy	32 SCLK periods
P948xy	8 SCLK periods (standard), 32 SCLK periods
	(x1 mode)
LOW TRIGGER JITTER OPT.	SQRT(SCLK period^2 + 150e-12^2)
LATENCY / SYSTEM DELAY	
P128xy, P258xy, P948xy STANDARD	<900 SCLK periods
P908xy, P948xy x1 MODE	<2700 SCLK periods
POLARITY	Positive or negative
SOURCE	Selectable between channels
INPUT IMPEDANCE	10 k Ω or 50Ω (nom.), DC coupled, factory
	configured
MAX TOGGLE FREQUENCY	10MHz (50MHz optional)
MINIMUM PULSE WIDTH	50ns (5ns optional)
CONNECTOR	SMP (male)

FAST SEGMENT DYNAMIC CONTROL INPUT (OPTIONAL)		
INPUT SIGNALS	Data 10bit, channel select 2 bit, valid 1 bit	
SEGMENTS / SEQUENCES	1024 (128 fast)	
DATA RATE	35MHz	
MINIMUM LATENCY (Dynamic control input to direct out)		
FAST SEGMENT	<250ns	
NORMAL SEGMENT	<1µs	
INPUT LEVEL	LVTTL	
CONNECTOR	MDR (Benchtop D-Sub)	

DIGITIZER (AWT OPTION)	
NUMBER OF CHANNELS	1 or 2
INPUT VOLTAGE RANGE	500 mVpp (full scale)
INPUT VOLTAGE OFFSET	-2V to +2V
INPUT FREQUENCY RANGE	9GHz
RESOLUTION	12 bits
ACQUISITION MEMORY	Up to max. arbitrary memory
SAMPLE CLOCK SOURCES	Internal or external
INTERNAL CLOCK SOURCE	Internal, external reference
MAX SAMPLING RATE	5.4GS/s in single channel mode 2.7Gs/s in dual channel mode
MIN SAMPLING RATE	800Ms/s
CLOCK ACCURACY	<2 ppm
IMPEDANCE	50Ω
COUPLING	DC or AC (factory configured)
TRIGGER SYSTEM	
TRIGGER MODES	Positive, negative edge
TRIGGER SOURCES	External, software, channel
COUPLING	DC
IMPEDANCE	50Ω (nominal)
LEVEL RANGE	>± 2.5 V (nominal)
FREQUENCY RANGE	DC to 65MHz
CONNECTOR	SMA (female)

FPGA PROGRAMMING	
FPGA TYPE	Xilinx Kintex UltraScale XCKU060 upgradeable to XCKU115
MODES	
STANDARD	Tabor standard built-In functionality
DECISION BLOCKS	Built-in library of mathematical functions, modulation & digital filters
SHELL	Open core providing all interfaces and configuration path to the user





DIGITAL UPCONVERTER			
MODES			
P258xy, P948xy	NCO / interpolation / IQ modulation		nodulation
ALL OTHERS MODELS		NCO only	
SAMPLING RATE	1GS/	1GS/s to max. sample rate	
CARRIER FREQUENCY			
RANGE	0 to 4	40% of sampling	g rate
RESOLUTION	48 bit		
PHASE RANGE	0 to 360°		
PHASE RESOLUTION	16 bit		
INTERPOLATION FACTORS	x2, x4, x8		
IQ FORMAT P258xy	x2 mode		
IQ PAIR PER CHANNEL	1		
MAX INPUT RATE	1,250MS/s		
NUMBER OF CHANNELS	2		
IQ FORMAT P948xy	x2 mode	x4 mode	x8 mode
IQ PAIR PER CHANNEL	1	1	1 or 2
MAX INPUT RATE	2,500MS/s	2,500MS/s	1,125MS/s
NUMBER OF CHANNELS	2	2	4
SFDR AND HARMONICS	Same as Arbitrary		У
MEMORY	Same as Arbitrary		

GENERAL BENCHTOP	
INPUT VOLTAGE RANGE	100VAC to 264VAC
INPUT FREQUENCY RANGE	47Hz to 63Hz
POWER CONSUMPTION:	550W max.
EMBEDDED PC	
CPU	Intel Pentium 3MB cache, 2.20GHz
MEMORY	8GB (Upgradeable)
STORAGE	120GB (Upgradeable)
OPERATING SYSTEM	Windows 10 IoT
DISPLAY	9" TFT touch LCD 1024x600
INTERFACES	
USB	Front panel 1 x USB 3 host (type A)
	Rear panel 2 x USB 3 host, (type A)
	Rear panel 1 x USB 3 device, (type C)
LAN (1000BASE-T)	Rear panel 1 x RJ45 1000/100/10
HDMI	HDMI type A
STORAGE	120GB removable
DIMENSIONS	
WITH FEET	440 X 175 x 330 mm (W x H x D)
WITHOUT FEET	440 X 190 x 330 mm (W x H x D)
WEIGHT	
WITHOUT PACKAGE	7.5 kg
SHIPPING WEIGHT	9 kg

GENERAL DESKTOP	
INPUT VOLTAGE RANGE	100VAC to 264VAC
INPUT FREQUENCY RANGE	47Hz to 63Hz
POWER CONSUMPTION:	550W max.
BUILT-IN PC	
CPU	Intel Pentium 3M Cache, 2.20GHz
MEMORY	8GB (Upgradeable)
STORAGE	120GB (Upgradeable)
OPERATING SYSTEM	Windows 10
INTERFACES	
USB	Front panel 1 x USB 3 host (type A) Rear panel 2 x USB 3 host, (type A) Rear panel 1 x USB 3 device, (type C)
THUNDERBOLT (OPTIONAL)	Rear panel 1 x Thunderbolt 3
LAN (1000BASE-T)	Rear panel 1 x RJ45 1000/100/10
SFP+ (OPTIONAL, REPLACES RJ45)	Rear panel 1 x SFP+ 10G optical
GPIB (OPTIONAL)	IEEE 488.2 – GPIB
HDMI	HDMI type A
STORAGE	120GB removable
DIMENSIONS	
WITH FEET	175 X 221 x 316 mm (W x H x D)
WITHOUT FEET	175 X 235 x 316 mm (W x H x D)
WEIGHT	
WITHOUT PACKAGE	7.5 kg
SHIPPING WEIGHT	9 kg

GENERAL MODULE	
INTERFACE	PXIe Gen3 x8 lanes
POWER CONSUMPTION	50W max. per slot
CURRENT CONSUMPTION	+3.3V 4A max., +12V 4A max.
DIMENSIONS	3U, 8HP PXIe (2 slots) Add 4HP (1 slot) for each AWT/MRK option

GENERAL	
TEMPERATURE	
OPERATING	0°C to +40°C
STORAGE	-40°C to +70°C
WARM UP TIME:	15 minutes
HUMIDITY:	85% RH, non-condensing
SAFETY:	CE Marked, EC61010-1:2010
EMC:	IEC 61326-1:2013
CALIBRATION:	2 years
WARRANTY	3 years





Proteus Series Ordering Information

ORDERING	INFORMATION BENCHTOP
MODEL	DESCRIPTION
P1282B	1.25 GS/s, 16 bit, 1 GS memory, 2 channels, 4 markers, benchtop RF AWG
P1284B	1.25 GS/s, 16 bit, 1 GS memory, 4 channels, 4 markers, benchtop RF AWG
P1288B	1.25 GS/s, 16 bit, 2 GS memory, 8 channels 8 markers, benchtop RF AWG
P12812B	1.25 GS/s, 16 bit, 2 GS memory, 12 channels 12 markers, benchtop RF AWG
P2582B	2.5 GS/s, 16 bit, 2 GS memory, 2 channels, 8 markers, benchtop RF AWG
P2584B	2.5 GS/s, 16 bit, 2 GS memory, 4 channels, 8 markers, benchtop RF AWG
P2588B	2.5 GS/s, 16 bit, 2 GS memory, 8 channels 16 markers, benchtop RF AWG
P25812B	2.5 GS/s, 16 bit, 2 GS memory, 12 channels, 24 markers, benchtop RF AWG
P9082B	9 GS/s, 16 bit, 4 GS memory, 2 channels, 8 markers, benchtop RF AWG
P9084B	9 GS/s, 16 bit, 4 GS memory, 4 channels, 16 markers, benchtop RF AWG
P9086B	9 GS/s, 16 bit, 4 GS memory, 6 channels, 24 markers, benchtop RF AWG
P9482B	9 GS/s, 16 bit, 8 GS memory, 2 channels, 8 markers, benchtop RF AWG
P9484B	9 GS/s, 16 bit, 8 GS memory, 4 channels, 8 markers, benchtop RF AWG
P9488B	9 GS/s, 16 bit, 8 GS memory, 8 channels, 16 markers, benchtop RF AWG
P94812B	9 GS/s, 16 bit, 8 GS memory, 12 channels, 24 markers, benchtop RF AWG

ORDERING	INFORMATION DESKTOP
MODEL	DESCRIPTION
P1282D	1.25 GS/s, 16 bit, 1 GS memory, 2 channels, 4 markers, desktop RF AWG
P1284D	1.25 GS/s, 16 bit, 1 GS memory, 4 channels, 4 markers, desktop RF AWG
P1288D	1.25 GS/s, 16 bit, 2 GS memory, 8 channels, 8 markers, desktop RF AWG
P12812D	1.25 GS/s, 16 bit, 2 GS memory, 12 channels, 12 markers, desktop RF AWG
P2582D	2.5 GS/s, 16 bit, 2 GS memory, 2 channels, 8 markers, desktop RF AWG
P2584D	2.5 GS/s, 16 bit, 2 GS memory, 4 channels, 8 markers, desktop RF AWG
P2588D	2.5 GS/s, 16 bit, 2 GS memory, 8 channels 16 markers, desktop RF AWG
P25812D	2.5 GS/s, 16 bit, 2 GS memory, 12 channels, 24 markers, desktop RF AWG
P9082D	9 GS/s, 16 bit, 4 GS memory, 2 channels, 8 markers, desktop RF AWG
P9084D	9 GS/s, 16 bit, 4 GS memory, 4 channels, 16 markers, desktop RF AWG
P9086D	9 GS/s, 16 bit, 4 GS memory, 6 channels, 24 markers, desktop RF AWG
P9482D	9 GS/s 16 bit, 8 GS memory, 2 channels, 8 markers, desktop RF AWG
P9484D	9 GS/s 16 bit, 8 GS memory, 4 channels, 8 markers, desktop RF AWG
P9488D	9GS/s 16 bit, 8 GS memory, 8 channels, 16 markers, desktop RF AWG
P94812D	9 GS/s 16 bit, 8 GS memory, 12 channels, 24 markers, desktop RF AWG

ORDERING INFORMATION MODULE			
MODEL	DESCRIPTION		
P1282M	1.25 GS/s, 16 bit, 1 GS memory, 2 channels, 4 markers, module RF AWG		
P1284M	1.25 GS/s, 16 bit, 1 GS memory, 4 channels, 4 markers, module RF AWG		
P2582M	2.5 GS/s, 16 bit, 2 GS memory, 2 channels, 8 markers, module RF AWG		
P2584M	2.5 GS/s, 16 bit, 2 GS memory, 4 channels, 8 markers, module RF AWG		
P9082M	9 GS/s, 8 bit, 4 GS memory, 2 channels, 8 markers, module RF AWG		
P9482M	9 GS/s, 16 bit, 8 GS memory, 2 channels, 8 markers, module RF AWG		
P9484M	9 GS/s, 16 bit, 8 GS memory, 4 channels, 8 markers, module RF AWG		





Options

ORDERING IN	FORMATION OPTIONS ¹	
OPTION	DESCRIPTION	MODEL
4M1	4 GS memory	P1282y, P2582y
4M2	4 GS memory	P1284y, P2584y
4M3 ²	4 GS memory option	P1288y, P2588y, P9084y
4M4 ²	4 GS memory	P12812y, P25812y, P9086y
8M1	8 GS memory	P1282y, P2582y
8M2	8 GS memory	P1284y, P2584y, P9082y
8M3 ²	8 GS memory	P1288y, P2588y, P9084y
8M4 ²	8 GS memory	P12812y, P25812y, P9086y
16M1	16 GS memory	P9082y
16M2	16 GS memory	P9084y
16M3 ²	16 GS memory	P9086y
DO1	9 GHz BW direct output	P1282y, P2582y
DO2	9 GHz BW direct output	P1284y, P2584y, P9082y
DO3 ²	9 GHz BW direct output	P1288y, P2588y, P9084y
DO4 ²	9 GHz BW direct output	P12812y, P25812y,P9086y
DC1	DC output for IQ baseband applications	P9482y
DC2	DC output for IQ baseband applications	P9484y
DC3 ²	DC output for IQ baseband applications	P9488y
DC4 ²	DC output for IQ baseband applications	P94812y
DJ1	Dynamic jump input, occupies an additional slot	P1282y, P2582y, P9482y
DJ2	Dynamic jump input, occupies an additional slot	P1284y, P2584y, P9082y, P9484y
DJ3 ²	Dynamic jump input, occupies an additional slot	P1288y, P2588y, P9084y, P9488y
TTL1	TTL 8 markers output (replaces the 1.3 Vpp default markers). Specify at order if $50\Omega/10k\Omega$	All models
MRK1	4 extra markers	P1282y
MRK2 ²	8 extra markers	P1288y
MRK3 ²	12 extra markers	P12812y
LTJ1	Ultra-low trigger jitter (200 ps typ.)	P1282y, P2582y, P9482y
LTJ2	Ultra-low trigger jitter (200 ps typ.)	P1284y, P2584y, P9082y, P9484y
LTJ3 ²	Ultra-low trigger jitter (200 ps typ.)	P1288y, P2588y, P9084y, P9488y
LTJ4 ²	Ultra-low trigger jitter (200 ps typ.)	P12812y, P25812y, P9086y, P94812y

ORDERING IN	FORMATION OPTIONS CONTINUATION	1
OPTION	DESCRIPTION	MODEL
G1	Low waveform granularity	P1282y, P2582y, P9482y
G2	Low waveform granularity	P1284y, P2584y, P9082y, P9484y
G3 ²	Low waveform granularity	P1288y, P2588y, P9084y, P9488y
G4 ²	Low waveform granularity	P12812y, P25812y, P9086y, P94812y
DUC	Digital up-converter	P258xy
SEC ²	Removable SSD	All models
SSD ²	Extra factory duplicated SSD disk for SEC	All models
TRG	Fast trigger input (50 MHz instead of 10 MHz)	All models
AWT	5.4 GS/s single, 2.7 GS/s dual channel 12 bit digitizer, occupies an additional slot	All models
STM	Up to 6 GS/s streaming varies depending model	All models
WE	1 year warranty extension	All models
PROG	FPGA programming capability with built- in demodulation and digital filters	All models
SHELL	Integration to allow simple FPGA control and programming IP (includes 50 hours support pack)	All models
PXE21100	21 slot PXIe chassis	All modules
PXE6410	6 slot PXIe chassis with an embedded PC	All modules
COM1	Upgrade of the PXE6410/Desktop/Benchtop to an Intel Xeon 4 core, 6 MB cache, 2.2 GHz processor	
COM2	Upgrade of the PXE6410/Desktop/Benchtop to an Intel Xeon 8 core, 12 MB cache, 2 GHz processor	
COM3	Upgrade of the PXE6410/Desktop/Benchtop to an Intel Xeon 12 core, 18 MB cache, 1.5 GHz processor	
RAM32	Upgrade to 32 GB on-board memory for the COM	
RAM64	Upgrade to 64 GB on-board memory for the COM	
RAM128	Upgrade to 128 GB on-board memory for the COM	

All rights reserved to Tabor Electronics Itd. Tabor makes no representations nor warranties with respect to the accuracy or completeness of the contents and reserves the right to make changes at any time without notice. Ver.3.32, revised May 26, 2024.



 $^{^{1}}x = Number of channels, y=M/B/D=Module/Benchtop/Desktop$

² Only for Benchtop/Desktop