XUPP3R

Xilinx UltraScale+ 3/4-Length PCIe Board with Quad QSFP and 512 GBytes DDR4

- Xilinx Virtex UltraScale+ VU7P/VU9P/VU11P
- Up to two PCIe x16 interfaces supporting Gen1, Gen2, or Gen3
- Up to two PCIe x8 interfaces supporting Gen4
- Four QSFP28 cages for 1x 400GbE, 4x 100GbE, 4x 40GbE, 16x 25GbE, or 16x 10GbE
- Memory options:
  - up to 512 GBytes of DDR4 SDRAM with ECC
  - Up to 2.3 Gbits QDR-II+
- Board Management Controller for Intelligent Platform Management
- Timestamping support
- Utility I/O: USB 2.0, SATA, serial expansion port

XILINX ALLIANCE PROGRAM

BittWare's XUPP3R is a 3/4-length PCIe x16 card based on the Xilinx Virtex UltraScale+ FPGA. The UltraScale+ devices deliver high-performance, high-bandwidth, and reduced latency for systems demanding massive data flow and packet processing. The board offers extensive memory configurations supporting up to 512 GBytes of memory, sophisticated clocking and timing options, and four front panel QSFP cages, each supporting up to 100 Gbps (4x25) - including 100GbE. The XUPP3R also incorporates a Board Management Controller (BMC) for advanced system monitoring, which greatly simplifies platform integration and management. All of these features combine to make the XUPP3R ideal for a wide range of data center applications, including network processing and security, acceleration, storage, broadcast, and SigInt.

Xilinx Virtex UltraScale+ FPGA

The Xilinx UltraScale+ FPGAs are built on 16 nm process technology using 16FF+ FinFET 3D transistors to offer higher performance per watt than previous generations. Virtex UltraScale+ devices feature 32.75 Gbit/s transceivers, which enable 400GbE, 100GbE, and 25GbE. The UltraScale+ FPGAs offer programmable system integration with over 300 Mb of on-chip memory, integrated 100G Ethernet MAC with RS-FEC and 150G Interlaken cores, and IP blocks for PCIe Gen3 x16 and Gen4 x8. Up to 8,928 DSP slices provide high-level DSP compute performance.

I/O Interfaces

The XUPP3R provides a variety of interfaces for high-speed serial I/O as well as debug support. Four QSFP28 cages are available on the front panel, each supporting 100GbE, 40GbE, four 25GbE, or four 10GbE channels, for a total of up to 400 Gbps of bandwidth. The four QSFPs can also be combined for 400GbE. The QSFP channels are connected directly to the UltraScale+ FPGA via 16 transceivers. The QSFP cages can optionally be adapted for SFP+.

A Gen3 x16 or Gen4 x8 PCIe interface connects to the FPGA via 16 transceivers. An optional serial expansion port provides a 20x transceiver port connection to the FPGA and can be used to add serial memory, such as Hybrid Memory Cube (HMC) or an additional PCIe interface. The expansion interface also provides 14 GPIO signals.

A USB 2.0 interface provides debug and programming support, and a SATA connector is available to connect external storage devices or provide direct board-to-board communication. The board also supports timestamping with provision for a 1 PPS and reference clock input.

Memory

The XUPP3R features four DIMM sites that support standard DDR4 DIMMs and proprietary QDR-II+ RDIMMs. Each DIMM site supports up to 128 GBytes of DDR4 with optional ECC or up to 576 Mbits QDR-II+ (2x 288Mbit banks x18). Additional on-board memory includes Flash with factory default and support for multiple FPGA images.

Board Management Controller

The XUPP3R features an advanced system monitoring subsystem, similar to those typically found on today's server platforms. At the heart of the board's monitoring system lies a Board Management Controller (BMC), which accepts Intelligent Platform Management Interface (IPMI) messaging protocol commands. The BMC provides a wealth of features, including control of power and resets, monitoring of board sensors, FPGA boot loader, voltage overrides, configuration of programmable clocks, access to I²C bus components, field upgrades, and IPMI messaging. Access to the BMC is via PCIe or USB. BittWare's BittWorks II Toolkit also provides utilities and libraries for communicating with the BMC components at a higher, more abstract level, allowing developers to remotely monitor the health of the board.

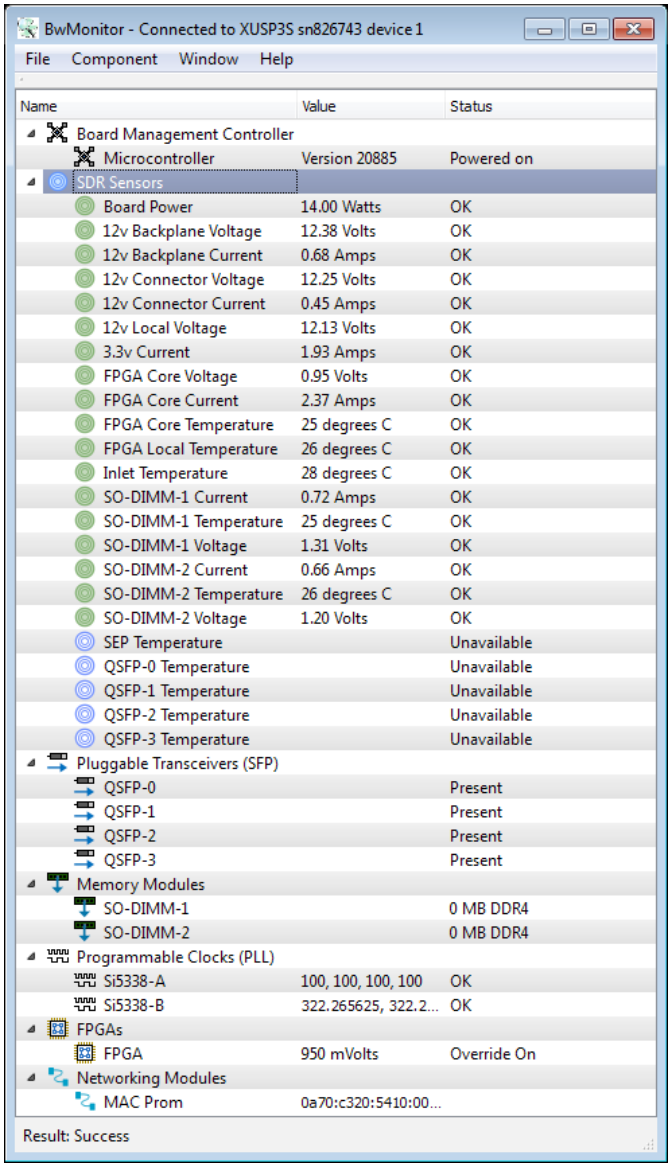
Development Tools

BittWorks II Toolkit

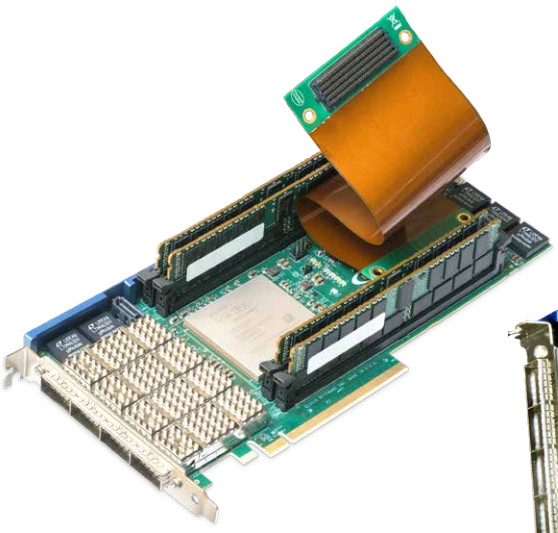
BittWare offers complete software support for the XUPP3R with its BittWorks II software tools. Designed to make developing and debugging applications for BittWare's boards easy and efficient, the Toolkit is a collection of libraries and applications that provides the glue between the host application and the hardware. A variety of features allow developers to take full advantage of the Xilinx UltraScale+ FPGA capabilities on the BittWare board, including FPGA control via PCIe, Flash programming, custom ISR scripts, and convenient control of FPGA loads. The Toolkit supports 64-bit Windows and Linux platforms and can connect to the board via PCIe or USB, providing a common API no matter the connection method.

FPGA Example Projects

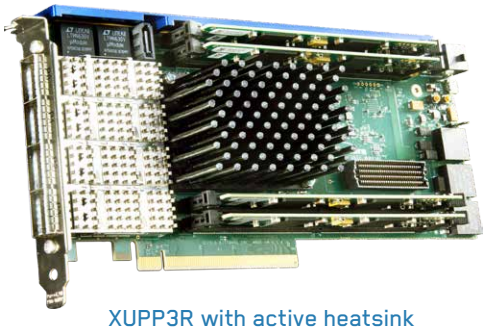
BittWare offers FPGA example projects to provide board support IP and integration for its Xilinx FPGA-based boards. The example projects easily integrate into existing FPGA development environments and illustrate how to move data between the board's different interfaces. Available example projects include the following: PCIe Gen3x16 Base Project, PCIe DMA, DDR4, QDR II/II+, and SerDes (iBERT). All examples are available for download on BittWare's developer website.



BwMonitor in the BittWorks II Toolkit provides a view into the board management capabilities of your BittWare hardware.



XUPP3R with SEP cable



XUPP3R with active heatsink

XUPP3R with high-performance heatsink

XUPP3R

Specifications

Board Specifications

FPGA

- Virtex UltraScale+ VU7P/VU9P/VU11P
- 52x GTY transceivers at 32.75 Gbps
- Up to 2.8 million logic elements
- Up to 341 Mb of embedded memory
- Up to 6 integrated PCIe cores
- Up to 8,928 DSP slices with 27x18 multipliers

On-Board Memory

- Flash memory for booting FPGA

Optional DIMM Memory

- 4 DIMM sites, each supporting*:
  - Up to 128 GBytes DDR4 x72 with ECC
  - Up to 576 Mbits dual QDR-II+ x18 (2 independent 288 Mbit banks)

PCIe Interface

- x16 Gen1, Gen2, Gen3 interface direct to FPGA
- x8 Gen4 to FPGA
- Serial Expansion Port supports an additional x16 or x8 PCIe interface (requires second slot)

USB Header

- Micro USB port (USB 2.0) for debug and programming FPGA and Flash

QSFP Cages

- 4 QSFP28 (zQSFP) cages on front panel connected directly to FPGA via 16 transceivers
- Each supports 100GbE, 40GbE, 4x 25GbE, or 4x 10GbE and can be combined for 400GbE
- Backward compatible with QSFP and can be optionally adapted for use as SFP+

Serial Expansion Port

- Expansion interface to FPGA via 20x GTY transceivers (optional; requires second slot)
- 14x GPIO signals to the FPGA

Serial ATA

- SATA connector, connected to FPGA

Timestamping

- 1 PPS input
- Reference clock input

Board Management Controller

- Voltage, current, temperature monitoring
- Power sequencing and reset
- Field upgrades
- FPGA configuration and control
- Clock configuration
- I²C bus access
- USB 2.0 and JTAG access
- Voltage overrides

Size

- 3/4-length, standard-height PCIe dual slot card
- 241mm x 111.15mm
- Max. component height: 34.79mm dual slot

Development Tools

System Development

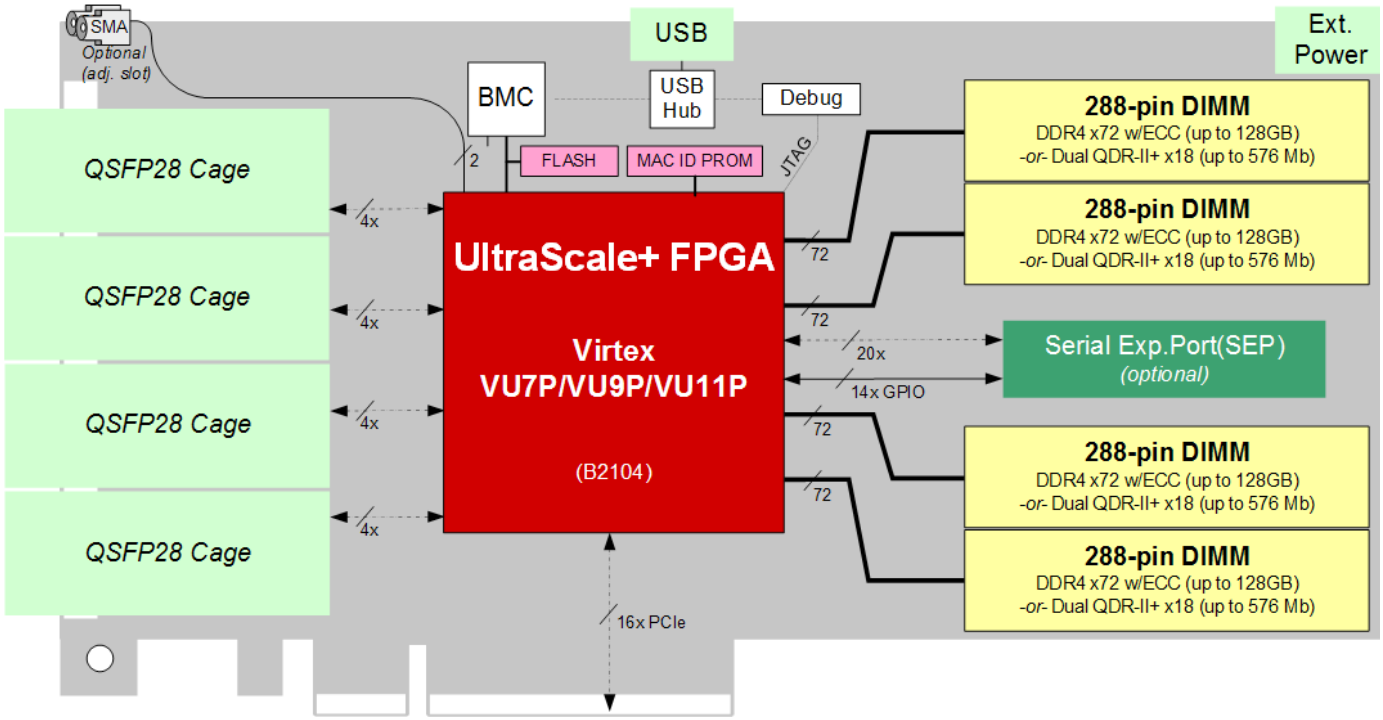
- BittWorks II Toolkit - host, command, and debug tools for BittWare hardware; Matlab API; source code porting kit also available

FPGA Development

- FPGA Example Projects
  - PCIe Gen3x16 Base Project
  - PCIe DMA
  - DDR4
  - QDR II/II+
  - SerDes (iBERT)
- Xilinx Tools
  - Vivado® Design Suite
  - Embedded USB to JTAG converter

*DIMM sites 1 & 2 and DIMM sites 3 &4 must have the same memory types, since they share voltage settings. For example, if DIMM 1 is DDR4, then DIMM 2 must be as well (or be empty).

XUPP3R System Block Diagram



XUPP3R Ordering Options

XUPP3R - RW-ABBBBCD-EEFFGGHH-IJKLMNOP-QR-S-T

RW	**Ruggedization** 0U = Commercial (0°C to 50°C)
A	**UltraScale Printed Wiring Board** F = VU9P*
BBBB	**FPGA Type and Size** 09VP = Virtex VU9P*
C	**FPGA Core Speed Grade** 1 = Slower 2 = Standard* 3 = Faster
D	**FPGA Temperature Range** E = Extended (Tj = 0 to +100C)*
EE	**DIMM 1‡** 00 = None* R4 = DDR4 16GB RDIMM R5 = DDR4 32GB RDIMM R7 = DDR4 128GB RDIMM L5 = DDR4 32GB LRDIMM L6 = DDR4 64GB LRDIMM Q4 = QDRII+ x18 288Mb (dual 144Mb) Q5 = QDRII+ x18 576 Mb (dual 288Mb)
FF	**DIMM 2‡** 00 = None* R4 = DDR4 16GB RDIMM R5 = DDR4 32GB RDIMM R7 = DDR4 128GB RDIMM L5 = DDR4 32GB LRDIMM L6 = DDR4 64GB LRDIMM Q4 = QDRII+ x18 288Mb (dual 144Mb) Q5 = QDRII+ x18 576 Mb (dual 288Mb)
GG	**DIMM 3‡** 00 = None* R4 = DDR4 16GB RDIMM R5 = DDR4 32GB RDIMM R7 = DDR4 128GB RDIMM L5 = DDR4 32GB LRDIMM L6 = DDR4 64GB LRDIMM Q4 = QDRII+ x18 288Mb (dual 144Mb) Q5 = QDRII+ x18 576 Mb (dual 288Mb)
HH	**DIMM 4‡** 00 = None* R4 = DDR4 16GB RDIMM R5 = DDR4 32GB RDIMM R7 = DDR4 128GB RDIMM L5 = DDR4 32GB LRDIMM L6 = DDR4 64GB LRDIMM Q4 = QDRII+ x18 288Mb (dual 144Mb) Q5 = QDRII+ x18 576 Mb (dual 288Mb)
I	**Oscillator** S = Standard*
J	**Auxilliary Oscillator** 0 = 322.265625 MHz*
K	**Timing** S = Front panel SMAs (in adj. slot) X = On-board circuits only*
L	**QSFP Configuration** 4 = 4 QSFP cages
M	**Serial Expansion Port** 0 = Not Installed 1 = Installed*
N	**Factory JTAG Header** 0 = Not Installed* 1 = Installed
O	**USB-to-JTAG** 1 = Installed*
P	**Heatsink** 3 = Active 2-slot* 4 = Passive 2-slot † 5 = Passive 1.5-slot † 6 = High-performance passive †
Q	**Misc. Configuration** 0 = Default
R	**Power Supply** R = Right angle connector* V = Vertical connector
S	**Mechanical Options** 0 = No stiffener S = Standard stiffeners*
T	**Assembly** 6 = RoHS 6/6

* Default
† Contact BittWare for availability
‡ DIMM sites 1/2 and sites 3/4 must have the same memory type, or be empty.

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BittWare FPGA PLATFORMS