



Roll No:

--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--

MCA
(SEM I) THEORY EXAMINATION 2024-25
COMPUTER ORGANIZATION & ARCHITECTURE

TIME: 3 HRS**M.MARKS: 70****Note:** Attempt all Sections. In case of any missing data; choose suitably.**SECTION A****1. Attempt all questions in brief.****2 x 07 = 14**

Q no.	Question	CO	Level
a.	Explain functional units of a digital computer and their interconnections in brief.	1	K2
b.	Differentiate Computer architecture and Computer organization.	1	K3
c.	Look ahead carry adders are faster than Ripple Carry adders. Why?	2	K3
d.	When Bus arbitration is required?	2	K3
e.	Why is wait-for-memory-function-completed (WMFC) steps needed when reading from or writing to memory.	3	K2
f.	Write $(-8)_{10}$ and $(+8)_{10}$ in twos complement form in 5-bit system.	4	K2
g.	Define interrupt. How is it handled?	5	K2

SECTION B**2. Attempt any three of the following:****07 x 3 = 21**

Q no.	Question	CO	Level
a.	Illustrate different addressing modes with suitable examples.	1	K3
b.	Explain the Booth's multiplication method and apply this method to multiply decimal numbers $(-9)_{10}$ and $(-13)_{10}$. Also sketch hardware diagram and flowchart for Booth's multiplication method.	2	K4
c.	Represent $(128.25)_{10}$ in IEEE 754 Standard with Single precision.	3	K2
d.	How the execution of a complete instruction takes place in Single-bus organization explain in detail.	4	K3
e.	Discuss the modes of transfer & explain the following (i) Programmed I/O (ii) Interrupt initiated I/O	5	K3

SECTION C**3. Attempt any one part of the following:****07 x 1 = 07**

Q no.	Question	CO	Level
a.	Illustrate various methods of Bus arbitration with their advantages and disadvantages.	1	K3
b.	Produce a program to evaluate the arithmetic statement $X = (A-B) / [C + (D * E)]$ i. Using general register computer with 3-address instruction ii. Using general register computer with 2-address instruction Using general register computer with 1-address instruction	1	K4



Roll No:

--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--

MCA
(SEM I) THEORY EXAMINATION 2024-25
COMPUTER ORGANIZATION & ARCHITECTURE

TIME: 3 HRS**M.MARKS: 70**

4. Attempt any one part of the following: 07 x 1 = 07

Q no.	Question	CO	Level
a.	Divide 8/3 by Restoring division method.	2	K3
b.	Draw and explain the flow chart for floating point multiplication.	3	K3

5. Attempt any one part of the following: 07 x 1 = 07

Q no.	Question	CO	Level
a.	Explain arithmetic pipeline and instruction pipeline with suitable diagram.	3	K3
b.	Write down the differences between RISC and CISC processor.	3	K3

6. Attempt any one part of the following: 07 x 1 = 07

Q no.	Question	CO	Level
a.	A virtual memory system has an address space of 8k words, a memory space of 4k words and page and block/frame sizes of 1k words. The following page reference changes occur during time interval. 4 2 0 1 2 6 1 4 0 1 0 2 3 5 7 Determine the four pages that are resident in main memory after each page reference change if the replacement algorithm used is (a) FIFO (b) LRU	4	K3
b.	Differentiate 2D and 2.5 D memory organization along with neat diagram.	4	K3

7. Attempt any one part of the following: 07 x 1 = 07

Q no.	Question	CO	Level
a.	Describe asynchronous data transfer. What are the methods through which it can be achieved? Explain strobe control and Handshaking.	5	K3
b.	Outline the block diagram of DMA controller. Illustrate, why are the read and write control lines in a DMA controller bidirectional?	5	K3