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Experiment no. 1

Aim: Implementation of half adder and full adder using logic gates

Apparatus Required:

1. IC 7486, IC 7432, IC 7408, IC 7400
2. Digital trainer kit.

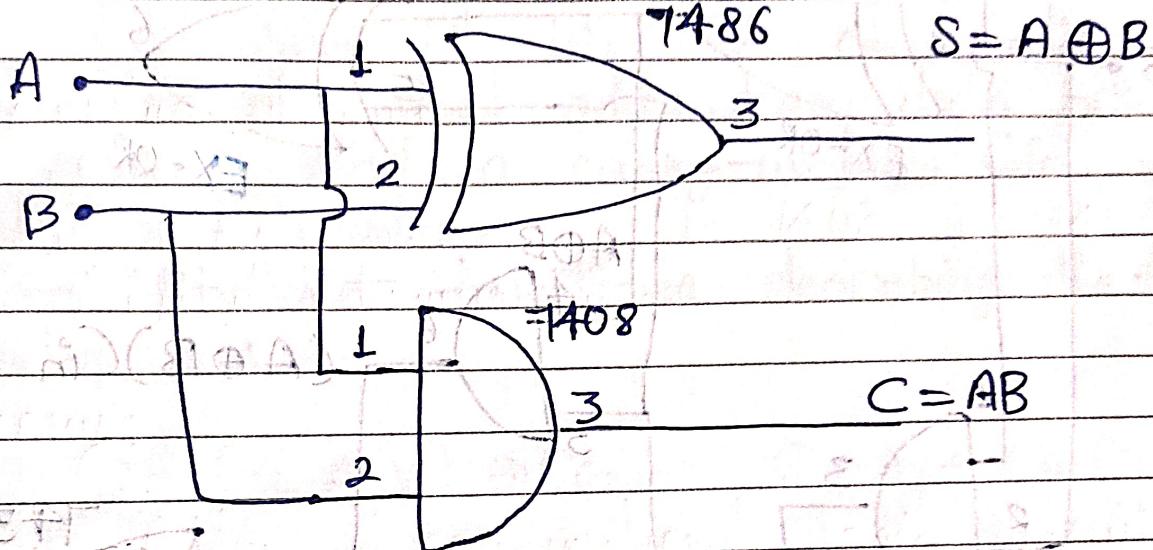
Theory:

Half-Adder: A combinational logic circuit that performs the addition of two data bits, A and B is called a half-adder. Addition will return in two output bits; one of which is the sum bit, S, and the other carry bit, C. The Boolean functions describing the half-adder are:

$$S = A \oplus B \quad C = A \cdot B$$

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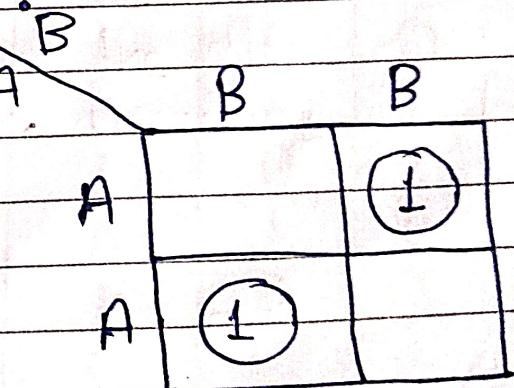
Half Adder using basic gates:



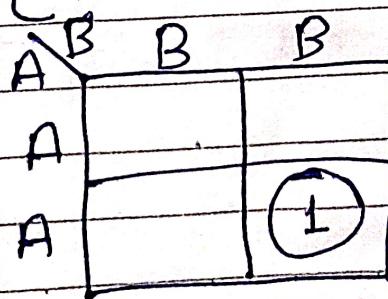
K-map for half adder

Half adder			
A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

for S:



for C:

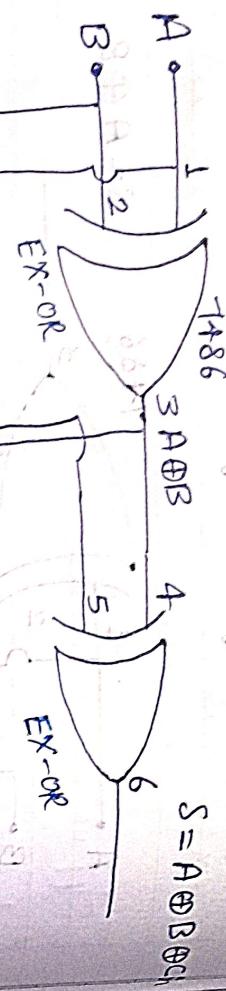


$$S = A \oplus B$$

$$C = A \cdot B$$

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Full Adder using basic gates.



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 Full Adder: The half-adder does not take the carry bit from its previous stage into account. This carry bit from its previous stage is called carry-in bit. A combinational logic circuit that adds two data bits, A and B and a carry-in bit, C_{in} , is called a full-adder.
 The Boolean functions describing the full-adder are:

$$S = (x \oplus y) \oplus C_{in} \quad C = xy + C_{in}(x \oplus y)$$

Truth Table:

		Full Adder		
A	B	C_{in}	S	C
0	0	0	0	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

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K-map for full adder:

For S:

A	\bar{A}	$\bar{B}Cin$	$B\bar{C}in$	$\bar{B}Cin$	$BCin$	$\bar{B}Cin$
A	\bar{A}	1		1		1
\bar{A}	A		1		1	
A	\bar{A}				1	

$$S = A \oplus B \oplus Cin$$

For Cin:

A	\bar{A}	$\bar{B}Cin$	$B\bar{C}in$	$\bar{B}Cin$	$BCin$	$\bar{B}Cin$
A	\bar{A}				1	
\bar{A}	A		1		1	
A	\bar{A}			1	1	1

$$Cout = AB + BCin + CinA$$

Procedure:

1. Verify the gates.
2. Make the connections as per the circuit diagram.
3. Switch on V_{cc} and apply various combinations of input according to the truth table.
4. Note down the output readings for half and full adder sum and the carry bit for different combinations of inputs.

Conclusion:

Half adder and full adder are constructed and their truth table are verified.

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Experiment - 2

Aim: To design and verify four bit binary to gray, gray to binary Number converter circuit.

Apparatus Required:

S.No.	Component	Specification	QTY
1.	X-OR GATE	IC 7486	1
2.	IC TRAINER KIT	-	1
3.	PATCH CORDS	-	10

Theory: The availability of large variety of codes for the same discrete elements of information results in the use of different codes by different systems. A conversion circuit must be inserted between the two systems if each uses different codes for same information. Thus, code converter is a circuit that makes the two systems compatible even though each uses different binary code.

The bit combination assigned to binary code to gray code. Since each code uses four bits to represent a decimal digit. There are four inputs and four outputs. Gray code is a non-weighted code.

The input variables are designated as B₃, B₂, B₁, B₀ and the out variables are designated as C₃, C₂, C₁, C₀. From the truth table, combinational circuit is designed. The Boolean functions are obtained from K-map for each output.

A code converter is a circuit that makes the two systems compatible even though each used a different binary code. To convert from binary code to Excess-3 code, the input lines must supply the bit combination of elements as specified by code of and the output lines generate the corresponding bit combination of code. Each one of four maps represents one of the four outputs of the circuit as a function of the four input variables.

Logic diagram:



Binary to Gray Code Converter:

Truth Table:

Binary input Gray code output

B ₃	B ₂	B ₁	B ₀	G ₃	G ₂	G ₁	G ₀
0	0	0	0	0	0	0	0
0	0	0	1	0	0	1	1
0	0	1	0	0	0	0	1
0	0	1	1	0	0	1	0
0	1	0	0	1	0	1	0
0	1	0	1	1	0	1	1
0	1	1	0	0	1	1	1
1	0	0	0	1	1	0	1

Logic Diagram:

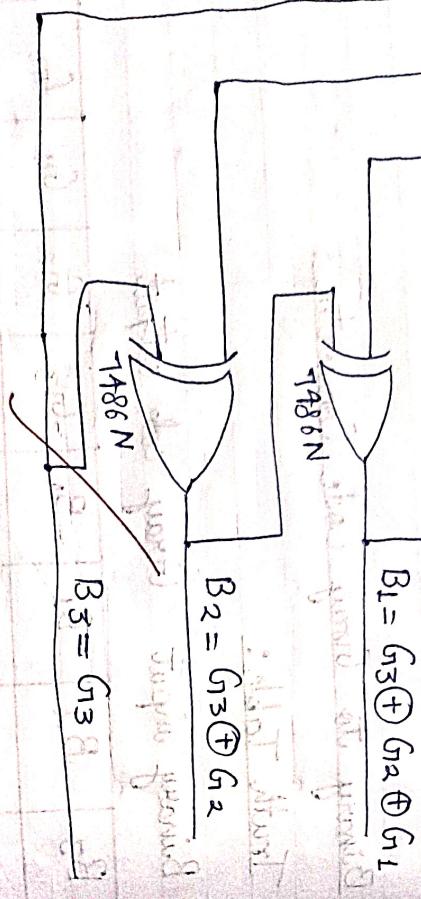


$$B_0 = G_3 \oplus G_2 \oplus G_1 \oplus G_0$$

$$B_1 = G_3 \oplus G_2 \oplus G_1$$

$$B_2 = G_3 \oplus G_2$$

$$B_3 = G_3$$



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Gray Code to Binary Converter:
 Truth Table

Gray Code	Binary Code
G ₃	B ₄
G ₂	B ₃
G ₁	B ₂
G ₀	B ₁
	B ₀

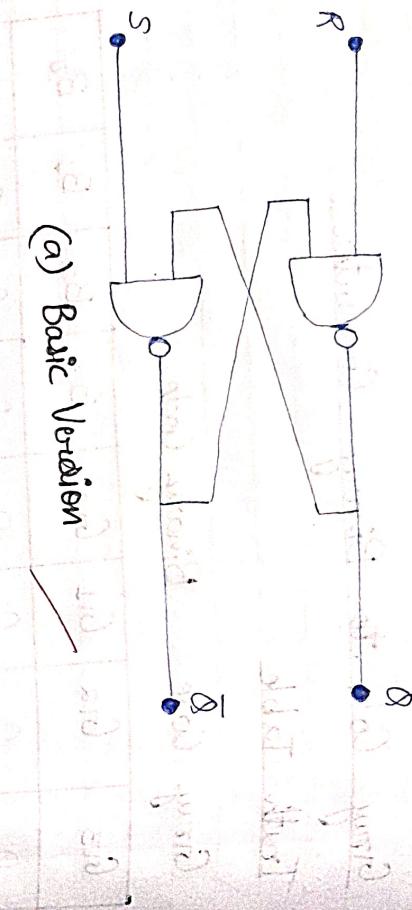
G ₃	G ₂	G ₁	G ₀	B ₃	B ₂	B ₁	B ₀
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	1	0	0	1	1
0	0	1	0	0	0	1	0
0	1	0	0	0	1	0	0
0	1	0	1	0	1	0	1
0	1	1	0	0	0	1	0
1	0	0	0	1	0	1	0

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Experiment-3 (Flip-Flop)

Objective: To construct different types of Flip-Flops and verify their truth tables.



Theory: The Flip-Flop is one of the most versatile blocks of digital computer systems. The output of a Flip-Flop changes its state when driven by a trigger pulse. The Flip-Flop can be used as a memory cell since it holds the information until the arrival of the next trigger pulse at the input. The Flip-Flop's applications are:

1. RS Flip-Flop
2. JK Flip-Flop

1. RS Flip-Flop:

The basic flip-flop may be realized using coupling two inverting gates (either NAND or NOR) as shown in Figure 3.1. The Truth Table for this is given in Table 3.1.

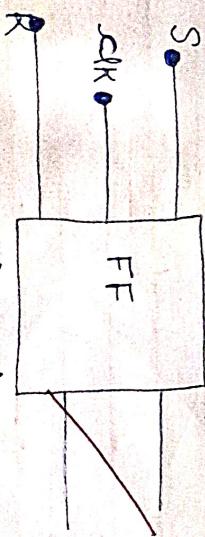
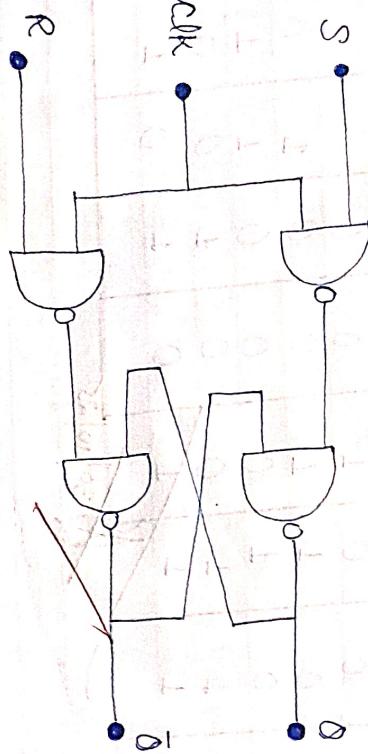


figure: 3.1 RS Flip-Flop

The output of RS Flip-Flop is not affected by multiple pulses at the signal input. This property can be utilized to eliminate contact bouncing of keyboard switches and to eliminate glitches in digital data which otherwise cause malfunctions of digital circuitry.

When it is necessary to set or reset the RS Flip-Flop in synchronism with the clock pulses, a modified version of RS flip-flop is used in (Figure - 3.1 b). This is known as clocked RS Flip-Flop. The truth table for this is given in Table 3.2 .

Input R S	Output Q	Input R S	clk	Output Q
0 0	Intermediate	0 0	1	0
0 1	1	0 1	1	1
1 0	0	1 0	1	0
1 1	0	1 1	Intermediate	Intermediate

Table 3.1 Truth table of RS Flip-Flop

Table 3.2 Truth Table of RS flip-flop modified version.

The above table Q is the state before the occurrence of clock pulse and \bar{Q} is the state after the practice of clock pulse.

2. JK FLIP - FLOP:

The JK Flip - Flop shown in Figure - eliminates the indeterminate state which occurs when $S = R = 1$. clocked RS gives the truth table for JK Flip - Flop.

Inputs	Output	Q_{t+1}	\bar{Q}_{t+1}
J 0 K 0	Q_t	0	1
1 0	1	1	0
0 1	0	0	1
1 1	\bar{Q}_t	1	0

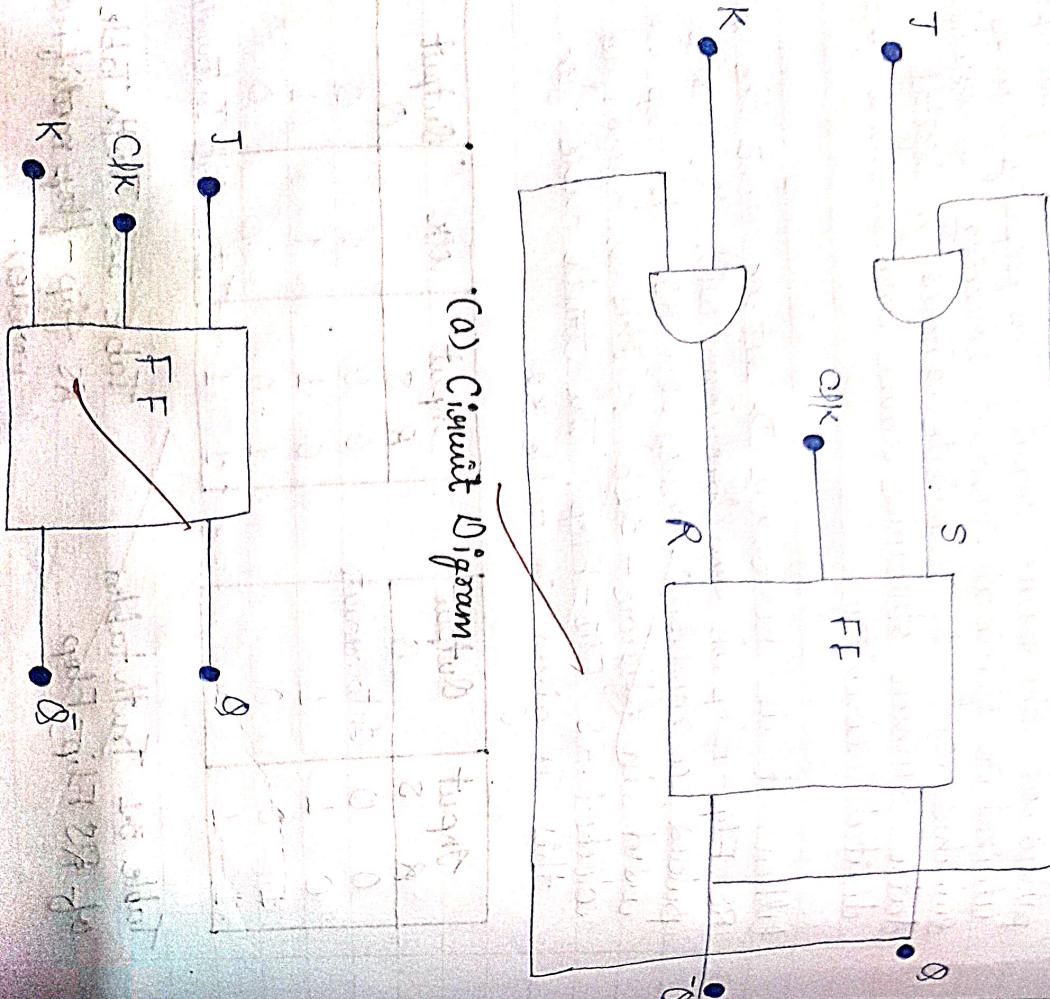
Table 3.3 Truth table for JK flip-flop

The basic JK Flip - Flop is subjected to a called race around condition, which occurs whenever two inputs make simultaneous transitions. Such a situation leads to the change of output more

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Figure 3.2 JK Flip - Flop

(b) Symbol



than once for a single input and eventually lead to an indefinite output state. To eliminate this problem, one has to use master-slave configurations (figure) is essentially a cascade of two RS Flip-Flop with feedback from the output of the second Flip-Flop to input of the first Flip-Flop. The first Flip-Flop is inverted before being applied to the ~~set~~ slave.

The Operation Clock pulses applied to the Master are inverted before being applied to the Slave.

The Operation of this JK Flip-Flop is evident from the circuit diagram itself.

An edge-triggered Master-Slave JK Flip-Flop is available in IC form in Duplicate as IC 7476 (Figure).

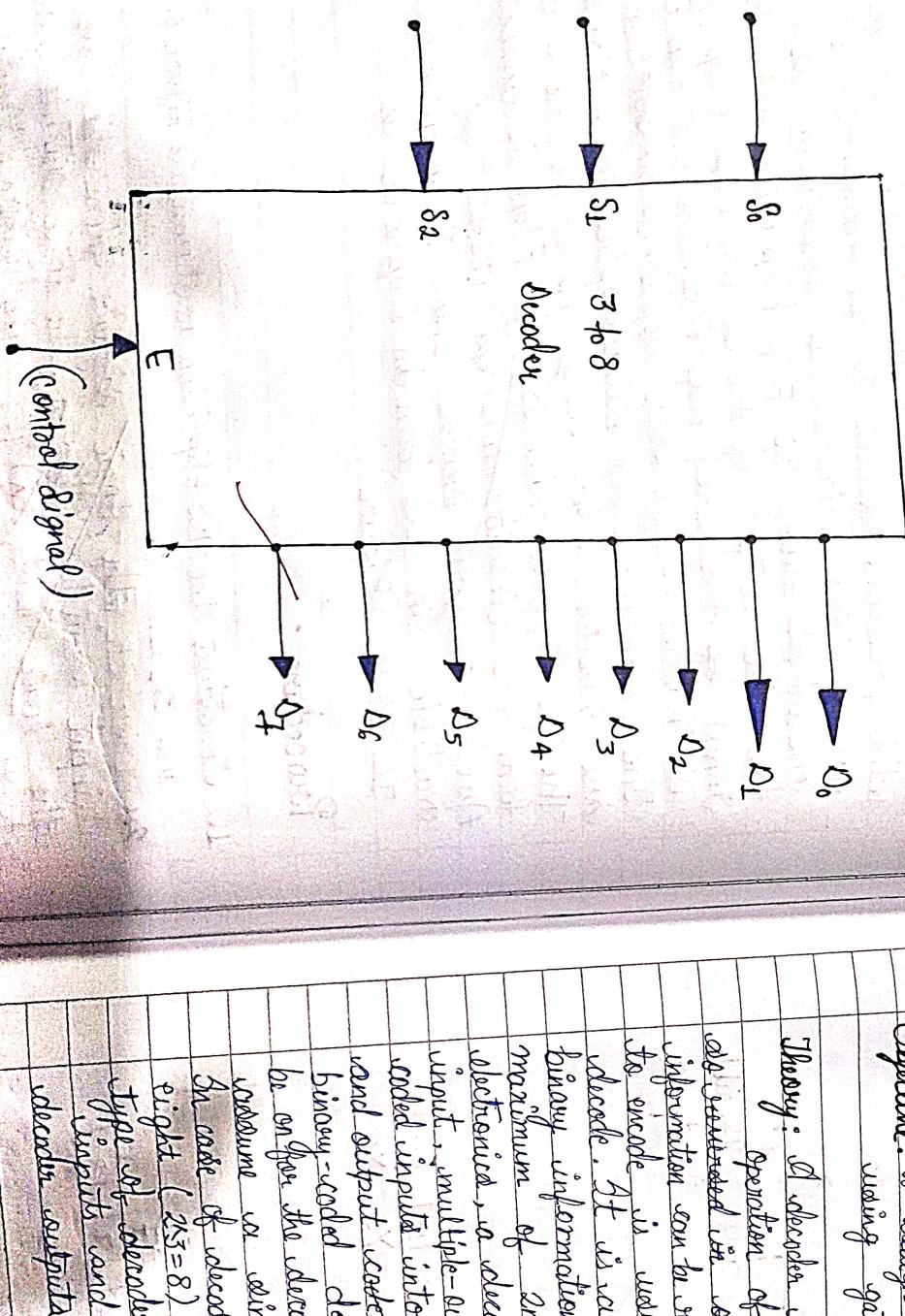
Procedure :

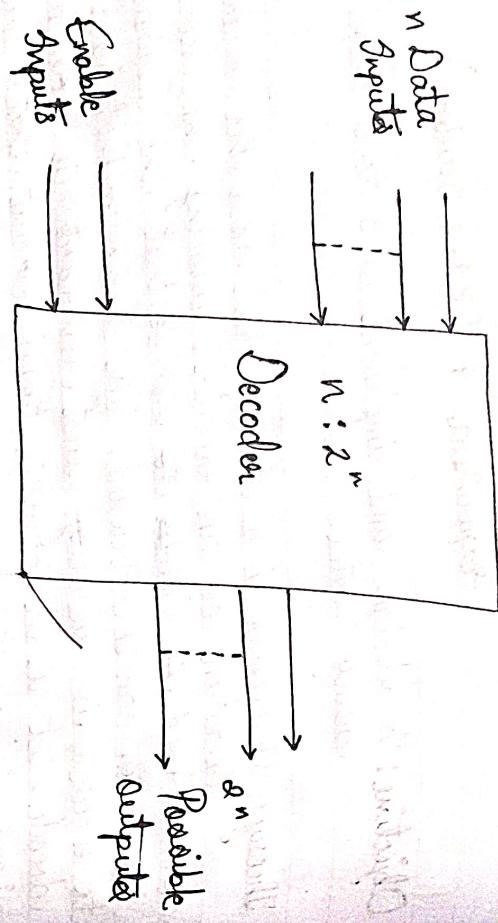
1. Construct the RS Flip-Flop as shown in Figure 3.1 b and 3.1 c.
2. ~~Observe the logic signals from the logic input switches. Verify the logic outputs on the logic level indicators. Verify the truth table of basic and clocked RS Flip-Flops.~~ 6/11/25
3. Construct Master Slave JK Flip-Flop (Figure) and repeat step 2.

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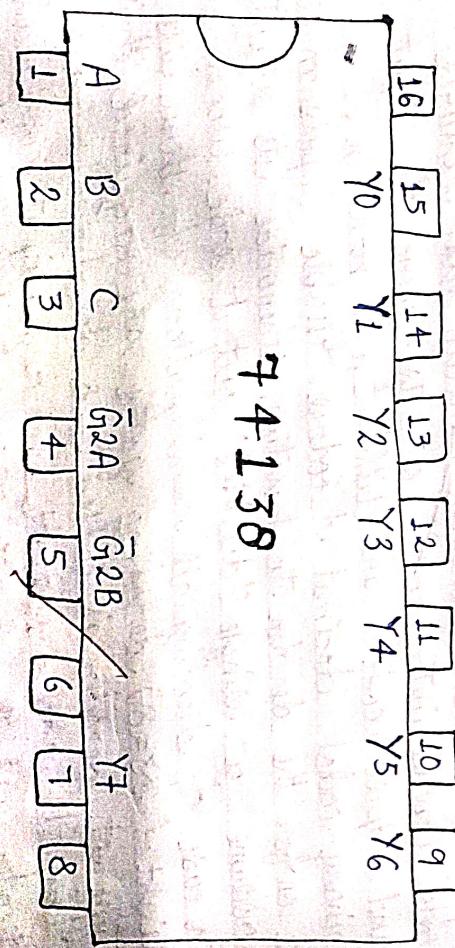
3 Line to 8 Line Decoder:

Objective: To design and implement a 3-to-8 decoder using gates.





Pain Diagram of 74138 IC



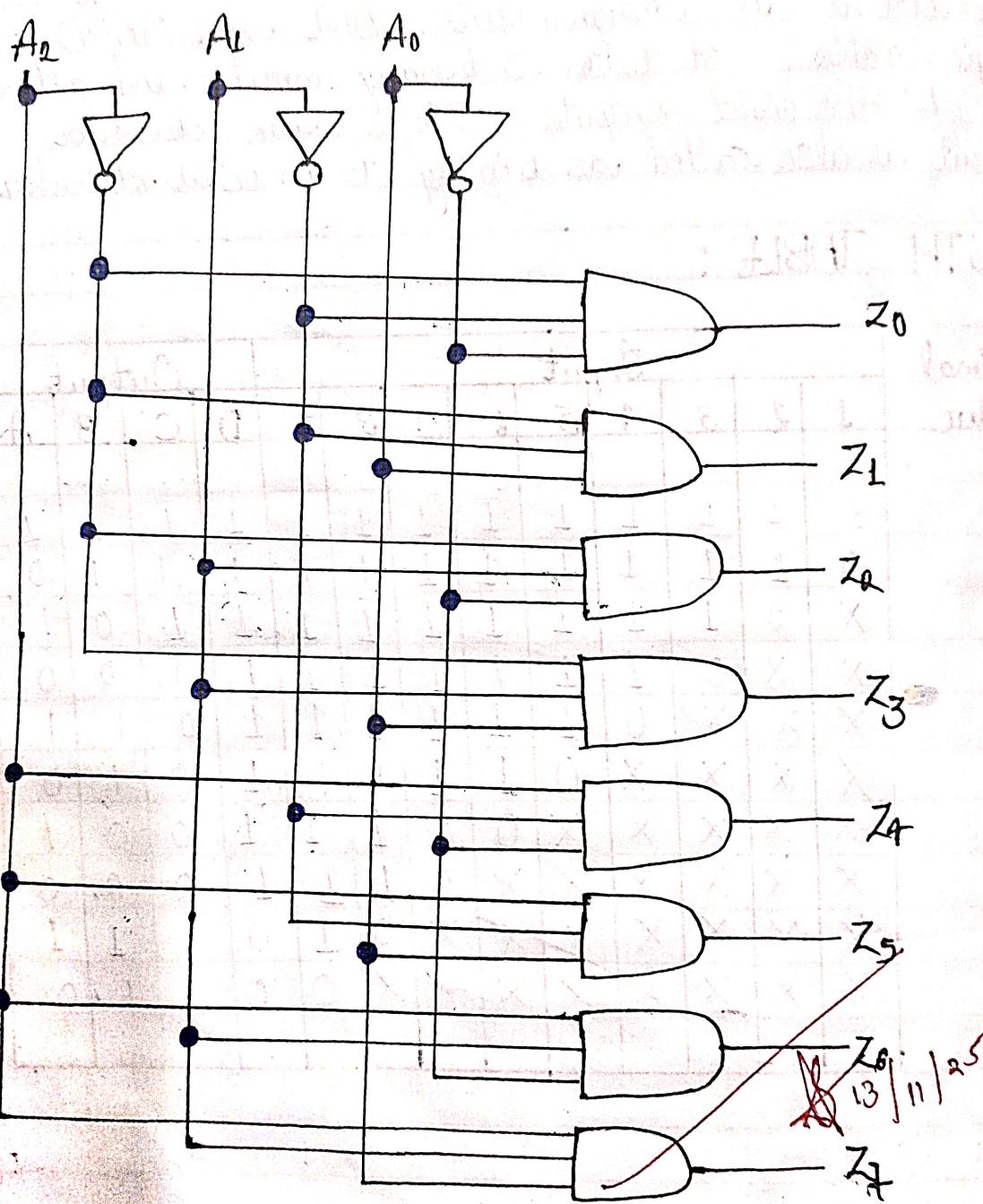
74138

Decimal Value	1	2	3	4	5	6	7	8	9	0	C.	B	A	Output
	1	1	1	1	1	1	1	1	1	1	1	1	1	Input
0	1	1	1	1	1	1	1	1	1	1	1	1	1	L
1	0	1	1	1	1	1	1	1	1	1	1	1	1	L
2	X	0	1	1	1	1	1	1	1	1	1	1	0	1.
3	X	X	0	1	1	1	1	1	1	1	1	1	0	0
4	X	X	X	0	1	1	1	1	1	1	1	1	0	1
5	X	X	X	X	0	1	1	1	1	1	1	1	0	1
6	X	X	X	X	X	0	1	1	1	1	0	0	1	0
7	X	X	X	X	X	X	0	1	1	1	0	0	0	0
8	X	X	X	X	X	X	X	0	1	0	1	1	1	1
9	X	X	X	X	X	X	X	X	0	0	1	1	0	0

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8 logic outputs for 3 inputs and had an enable pin
the circuit is designed with AND and NAND
logic gates. It takes 3 binary inputs and activates
one of the eight outputs. 3 to 8 line decoder
circuit is also called as binary to an octal decoder.

Logic Diagram:



Experiment - 5

Objective : To implement ALU

Apparatus required :

- (I) IC
- (II) Bread Board
- (III) Connecting Wire
- (IV) Power Supply

Theory : Arithmetic logic unit is multipurpose device capable of providing several different arithmetic and logic operation to be performed is selected by placing a specific binary code on the mode selected input. ALU are available in large scale integrated circuit package.

~~Functional block diagram for 74181 ALU known is shown in figure (a).~~ It is a bit (1) ALU which provides 16 arithmetic plus 16 logic operations. The unit accepts two 1 bit words ($A_0 A_1 A_2 A_3$ and $B_0 B_1 B_2 B_3$) and a carry input C_n as inputs. The operation to be performed on these inputs are determined by logic levels on inputs $S_0 S_1 S_2 S_3$ and (mode). When $M=1$, the operation are logical, while a combination of

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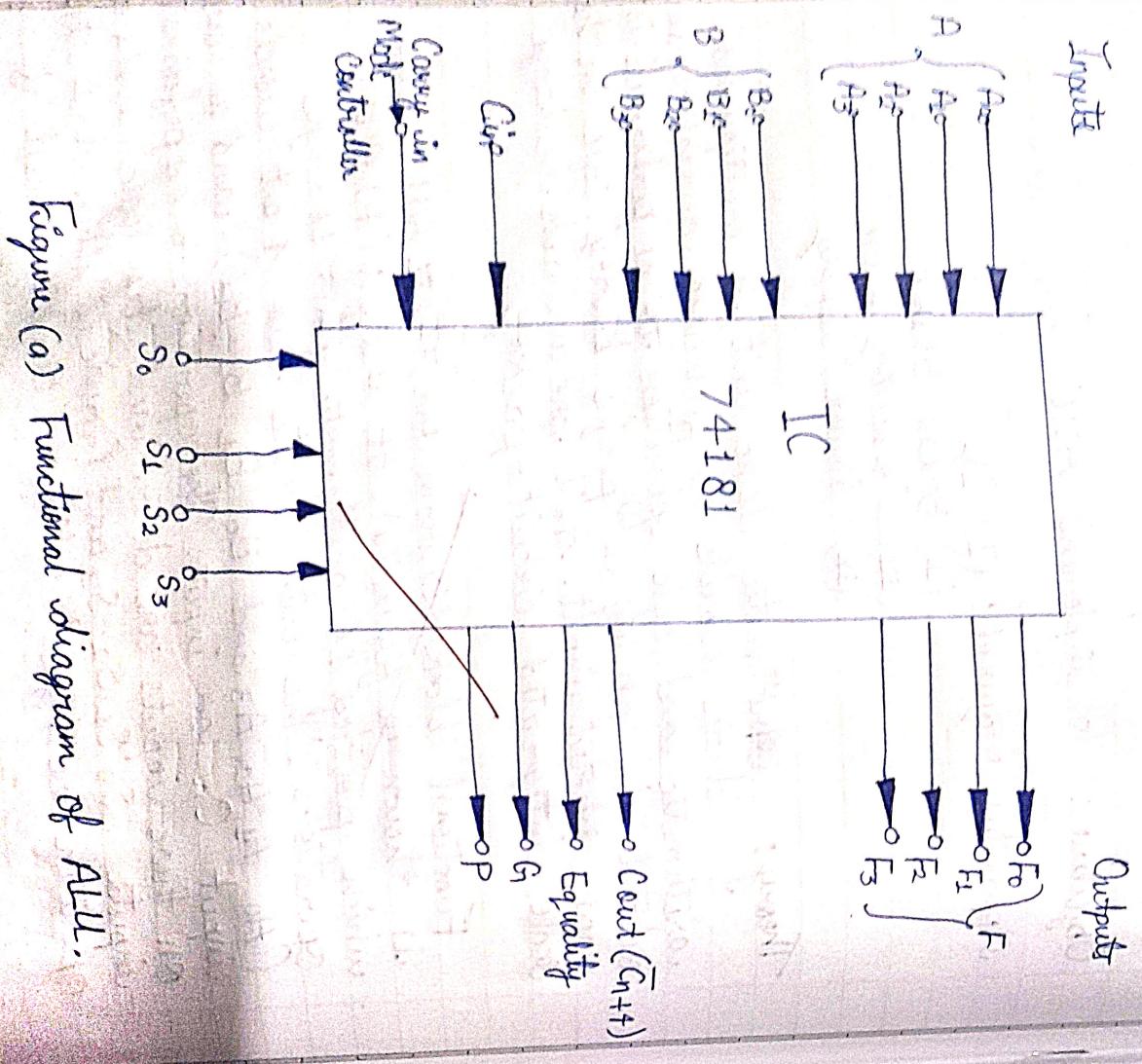


Figure (a) Functional diagram of ALU.

Input
Output
when $M=0$, the output are available at F_0 , F_1 , F_2 , F_3 and the carry output at C_{n+1} . In a typical case when $M=0$ and $S=0110$, then the output E is arithmetic difference of A and B .

~~Outputs~~

logical and arithmetic operation are selected when $M=0$, the output are available at F_0 , F_1 , F_2 , F_3 and the carry output at C_{n+1} . In a typical case when $M=0$ and $S=0110$, then the output E is arithmetic difference of A and B .

The Pin diagram of IC 74181 is shown in Figure (b)

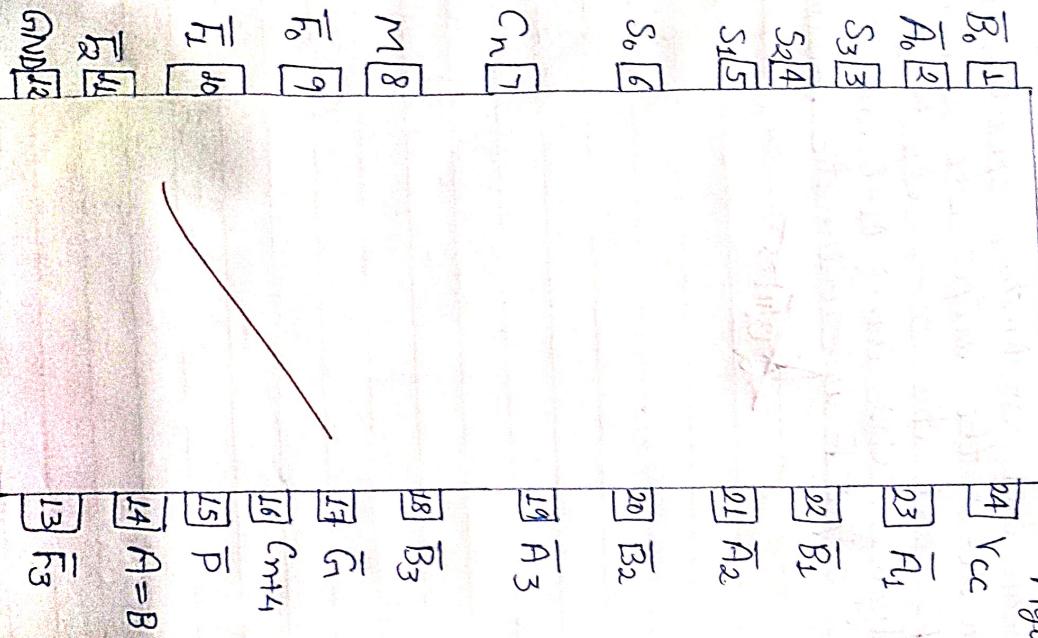


Figure (b). Pinout Diagram of IC 74181.

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Selection				M.L. logic function	No. Arithmetic operation $\bar{C} = \bar{A} + \bar{B}$ (no carry)
S_3	S_2	S_1	S_0		
0	0	0	0	$F = \bar{A}$	$F = A$
0	0	0	1	$F = A + B$	$F = A + B$
0	0	1	0	$F = \bar{A}B$	$F = A + \bar{B}$
0	0	1	1	$F = 0$	$F = \text{minus 1}$
0	1	0	0	$F = \bar{A}\bar{B}$	$F = A \text{ plus } \bar{B}$
0	1	0	1	$F = \bar{B}$	$F = (A + B) \text{ plus } \bar{A}$
0	1	1	0	$F = A \oplus B$	$F = A \text{ minus } B \text{ minus 1}$
0	1	1	1	$F = A\bar{B}$	$F = A\bar{B} \text{ minus 1}$
1	0	0	0	$F = \bar{A} + B$	$F = A \text{ plus } AB$
1	0	0	1	$F = \bar{A} \oplus B$	$F = A \text{ plus } B$
1	0	1	0	$F = B$	$F = (A + \bar{B}) \text{ plus } AB$
1	0	1	1	$F = AB$	$F = AB \text{ minus 1}$
1	0	1	1	$F = 1$	$F = A + A$
1	1	0	0	$F = A + \bar{B}$	$F = (A + B) \text{ plus } A$
1	1	0	1	$F = A + B$	$F = (A + \bar{B}) \text{ plus } A$
1	1	1	0	$F = A$	$F = A \text{ minus 1}$
1	1	1	1		

* Each bit is shifted to the next more significant position.

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Fast look ahead carry is provided at G and P, for high speed arithmetic operation. C_n and C_{n+1} are active low.

The ALU is the heart of every micro-processor unit. In microprocessor ALU is combined with other devices (shift registers, ROMs and RAMs), so that a complex sequence of arithmetic and logical operation can be performed.

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Experiment - 6

Objective: 8-Line to 1-Line Multiplexer & Demultiplexer.

Theory: Multiplexer - Multiplexer means many into one. A multiplexer is a circuit with many inputs but only one output. By applying control signals, we can steer any input to the output.

Fig-1. Illustrated the general idea. The circuit has n inputs and 1 output signals. One of the popular multiplexer is the 8-to-1 multiplexer which has 8 input bits, 3 control bits, and 1 output bit.

Figure-2 shows an 8-to-1 multiplexer, which is also called a data selector because the output bit depends on the input data bit that is selected. The input bits are labeled D₀ to D₇. Only one of these is transmitted to the input. Which one depends on the value of ABC, the control input. For instance, when

$$ABC = 000$$

DATA SELECT (BINARY)

DATA INPUTS

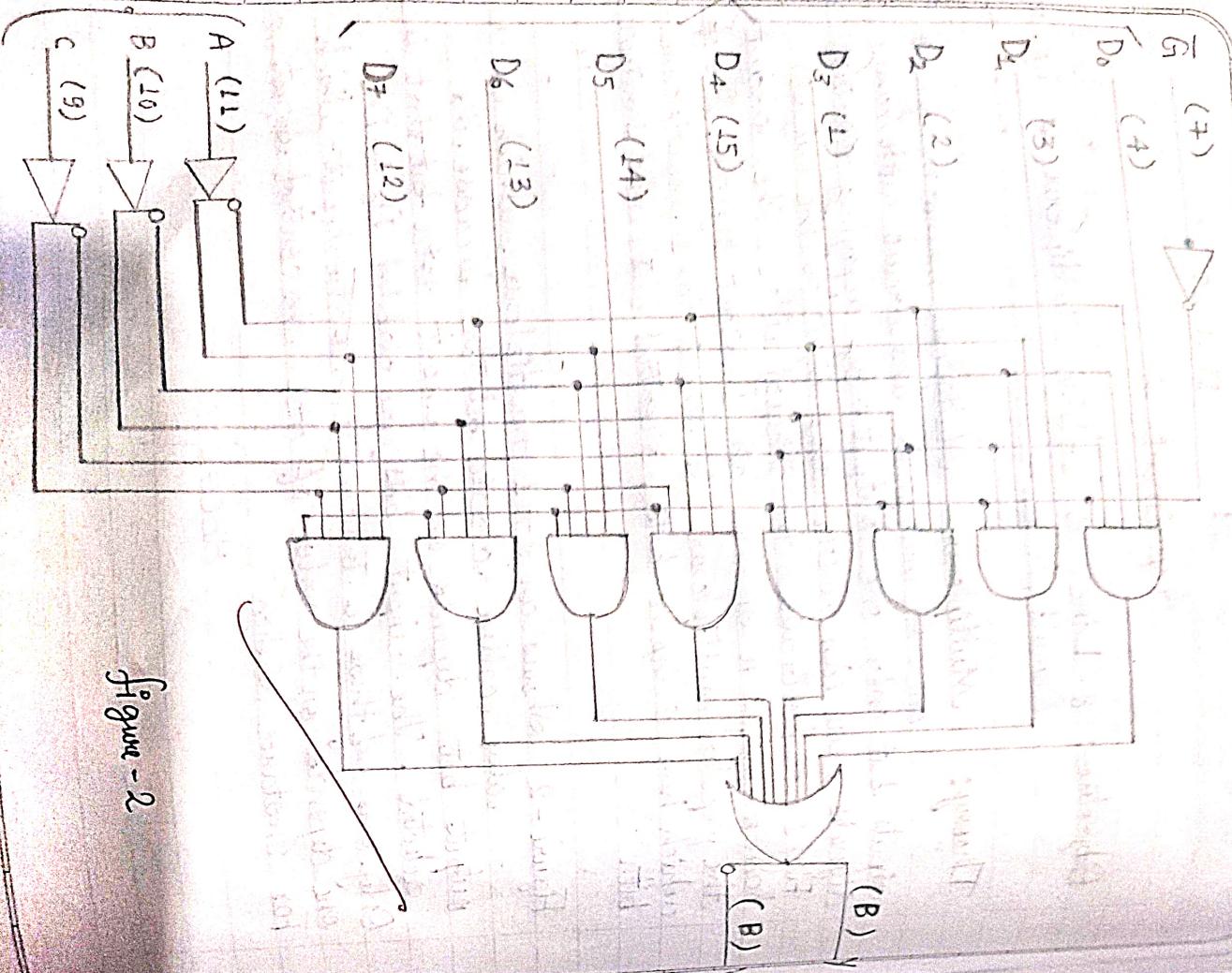


figure - 2

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If D_0 is low, Y is low, if D_0 is high, Y is high. The point is that Y depends only on the value of D_0 .

$$Y = D_0$$

If control was changed to: $ABC = 111$
All gates are disabled except the bottom AND gate. In this case, D_7 is the only bit transmitted to the output ..and

As you can see, the control word determines which of the input data bits is transmitted to output.

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Circuit Description:

In the Trinity experimental kit, 74151 IC is used as 8 to 1 multiplexer and 74138 IC is used as 1 to 8 line demultiplexer. Basically, one monostable is constructed with 7400 IC. In this the circuit is a bistable multivibrator constructed with two NAND gates to get bouncless pulse output. This pulse output is its the input of the 74163 / 74161 synchronous binary counter. In this only 3 output bits are used as the address inputs to the 74151 and 74138 ICs. When we are pressing the push button, at each time, one pulse is generated and counter increments by one step. The counter output changes from 000 to 111 and repeat the same cycle. The counter output is used as the address to the multiplexer and demultiplexer, so the which input of the multiplexer is selected is depends on the address input. Suppose address bit is 111, 1st input is activated. The LED at the multiplexer output indicates this.

During demultiplexing the output of the multiplexer is connected to the input of the demultiplexer. Address bits also we have to connect to the demultiplexer. So same channel can select at both multiplexer and demultiplexer.

Objective: To study 4 to 1 Multiplexer.

Apparatus Required: Kit, Connecting Lead.

	Address	Input Selected
	0 0 0	1
	0 0 1	2
	0 1 0	3
	0 1 1	4
	1 0 0	5
	1 0 1	6
	1 1 0	7
	1 1 1	8

Table - 1

Experimental Procedure :

1. Switch ON the experimental kit.
2. Observe the output LEDs of 74153 are changing from 000 to 111 by pressing the push button switch provided at monopulse generator.
3. Now set the output of the 74153 as 000, that means input 1 should be activated. Change the position of the switch at input 1 between L (low) and H (high) and corresponding the multiplexer output changed.
4. Verify Table 1.
5. Now also verify the Table - 1 and in addition to the multiplexer output.

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Experiment - 7

Object : To study different logic gate and verify their truth table.

Apparatus Required:

1. Digital Trainer
2. Connecting leads.

Theory: In logic gate there may be many input but only one output.

There are different logic gate:

1. AND Gate: (7408)
2. OR Gate: (7432)
3. NOT Gate: (7404)
4. NAND Gate: (7400)
5. NOR Gate: (7402)
6. X-OR Gate: (7486)
7. X-NOR Gate: (7499)

1. AND Gate: The AND gate is a logic circuit that has two or more than two inputs and same outputs. If any of the input signal is 0 (or low) then the output will be 0 (or low) and if both the input are high, the output will also be high (or 1).

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2. OR Gate: The OR Gate has two or more input but only one output, If any of the input is 1 (or high), the output is 1 and if both the input are 0 then output will 0 (zero).

Truth Table:

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

3. NOT Gate: The simplest form of a digital circuit is the NOT Gate. Another name of the NOT gate is inverter because the output is inverse of the input. Sometimes the output is called the complement or opposite of the input. The term inverter can be defined as "a gate with only one input signal and one output signal; the output state is always the opposite of the input i.e. if input is zero, the output is one if input is one then output is zero.

4. NAND Gate: A NAND gate is in fact a NOT-AND gate. It can be obtain by connecting a NOT gate in the output of an AND gate. The fig (d) shows the basic diagram of NAND gate.

If this both the input is high then the output should be low. For high output, it is necessary that either one input is low or both the input is low. If A & B are two input then the Boolean expression for NAND gate is - $Y = \overline{A \cdot B}$.

We can say that the output of (NAND gate) is done the complement of the output of AND gate

Truth Table:

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

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5. NOR Gate: A NOR gate is in fact a NOT-OR gate. It can be obtained by connecting a NOT gate in the output of OR gate. The basic diagram of NOR gate is shown in figure (e).

It is similar the OR-symbol, but a circle has been added at the output to represent the inversion that take place. If A & B are two inputs then the Boolean expression for

$$\text{NOR gate is } Y = \overline{A+B}$$

Truth Table:

	A	B	Y
1	0	0	1
2	0	1	0
3	1	0	0
4	1	1	0

6. X-OR Gate: X-OR gate obeys the give statement
 "Two input circuit provides an output when one input or the other is present but not when both inputs are present".

In other words we can say that the output is true i.e. $Y=1$, when $A=1$ or $B=1$ i.e., true but not both. It is known as X-OR gate. The standard symbol for an X-OR gate is shown in fig. (f).

Truth Table:

	A	B	Y
	0	0	0
	0	1	1
	1	0	1
	1	1	0

7 X-NOR Gate: X-NOR gate is the opposite function of X-NOR gate.

Truth Table:

	A	B	Y
	0	0	1
	0	1	0
	1	0	0
	1	1	1

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NOTE: NAND & NOR gate are called universal gate.

Result: We studied different logic gate & also verified their truth table.

Precaution:

1. Reading should be taken carefully.
2. Connection should be right & tight.
3. After taking the reading we switch off the kit.

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