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SCS16000/SCS16000J
Stressed Clock Synthesizer

User's Guide

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1. Setting Up the SCS16000/SCS16000J

The SCS16000/SCS16000J Stressed Clock Synthesizer is shipped in a protective box with all the accessories required for operation. The case includes:

- SCS16000 or SCS16000J Stressed Clock Synthesizer
- AC power cord
- SMA male to SMA male cable (2)
- SCS16000/SCS16000J Quick Start Guide
- CD, which includes:
  - Users Guide
  - USB Drivers

1.1. Unpacking

Carefully remove the instrument from the case in an ESD-safe environment.

1.2. Important Notes

- Use ESD protection at all times when using the instrument
- Review min/max specifications before applying input signals
- Use high quality SMA-connectors on the SMA ports
- Leave dust jackets on unused back panel connectors
- Situate the instrument away from heat sources, do not block the fans, and do not block the exhaust vents (minimum of 3 inches clearance)

1.3. Measurement Best Practices

- When using differential-mode connections, ensure the cables are phase balanced for best performance
- Use high quality cables and connector savers (or adaptors)
- Keep cable lengths short and minimize the number of cable bends
- Use a 8 in-lbs (90 N-cm) torque wrench when attaching connectors

1.4. General Specifications

Before installing the SCS16000/SCS16000J, review the specifications in Table 1.

Table 1. Specification considerations before installation

Parameter	Specification
Connector Type All signals except 10 MHz Ref In/Out – 10 MHz Ref In/Out –	 SMA BNC
Remote Control Interface	USB2.0 and IEEE-488 (GPIB)
Operating Temperature	+10 °C to +40 °C
Storage Temperature	-40 °C to +70 °C
Operating Humidity	95% relative humidity, non-condensing
Voltage	100 – 240 VAC 10% autoranging
Frequency	50/60 Hz
Power	145 Watts MAX
Current	1.8 A RMS MAX
Fuse	250 V 2 A 5x20 mm Always replace instrument fuse with one of the same type and rating.
Weight	3.2 kg (7.0 lbs)
Height	100 mm (3.9 in)
Width	214 mm (16.7 in)
Depth	425 mm (16.7 in)

1.5. Safety and Regulatory

Warning: Do not remove instrument covers. There are no user serviceable parts within. Operation of the instrument in a manner not specified by Centellax may result in personal injury or loss of life.

Warning: To prevent electrical shock, disconnect instrument from mains before cleaning. Use a dry cloth or one slightly dampened with water to clean the external case parts. Do not attempt to clean internally.

1.5.1. Warnings, Cautions, and Notes

Before operating the SCS16000/SCS16000J Stressed Clock Synthesizer, familiarize yourself with the following safety notations.

Warning: A *Warning* indicates a hazard. It calls attention to a procedure which, if not performed correctly, could result in personal injury or loss of life. Do not proceed beyond a warning note until the indicated conditions are fully understood and met.

Caution: A *Caution* indicates a hazard. It calls attention to a procedure that, if not performed correctly, could result in damage to, or destruction of, the instrument. Do not proceed beyond a caution note until the indicated conditions are fully understood and met.

Note: A *Note* provides important or special information.

1.5.2. Instrument Markings

The SCS16000/SCS16000J Stressed Clock Synthesizer has the following markings on the front and/or rear panel. Familiarize yourself with these markings before operating the instrument.

	The instruction manual symbol. The product is marked with this symbol when it is necessary for you to refer to instructions in the manual.
	This symbol indicates that internal circuits can be damaged by electrostatic discharge (ESD), therefore, avoid applying static discharges to the panel input connectors
~	This symbol indicates that the instrument requires alternating current (AC) input.
	This symbol indicates separate collection for electrical and electronic equipment, mandated under EU law as of August 13, 2005. All electrical and electronic equipment are required to be separated from normal waste for disposal. (Reference WEEE Directive, 2002/96/EC.)
|	This symbol indicates that the power line switch is in the ON position.
O	This symbol indicates that the power line switch is in the OFF position.
CE	The CE mark indicates compliance with the applicable European Community regulations.
TUV C US	The TUV mark indicates compliance with USA/Canada safety regulations.
ICES/NMB-001	This mark indicates compliance with the Canadian EMC regulations.
ISM 1-A	This text denotes the instrument is and Industrial Scientific and Medical Group 1 Class A product

The C-tick mark indicates compliance with Australian/New Zealand EMC regulations.

This mark indicates compliance with China RoHS regulations.
China RoHS environmental protection use period – 25 Years

1.6. Installation

The following procedure describes how to install the SCS16000/SCS16000J.

1 Install on a flat surface with unobstructed airflow to the back panel and side vents.

Note: For rack mount installation, refer to Appendix B.

2 Plug the AC power cord into a suitable wall socket (100-240 V AC, 50/60 Hz).

Warning: To prevent electrical shock, do not remove instrument covers.

3 Plug the AC power cord into the SCS16000/SCS16000J.

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2. Operation Overview

The SCS16000/SCS16000J Stressed Clock Synthesizer is a 0.5 to 16 Gb/s stressed clock source with multi-jitter capability. Its primary application is to generate a clock for a Bit Error Rate tester. It can also be used as a general purpose clock source in a variety of serial data characterization applications

2.1. Features

All features can be controlled through the Control Panel, or remotely through the GPIB or USB interface using the remote commands.

- Operation from 0.5 to 16.0 GHz
- Two independent sinusoidal jitter injection sources (one for SCS16000)
- True Gaussian random jitter stress (SCS16000J only)
- Spread spectrum clock (SCS16000J only)
- Fully programmable clock output parameters
- Low intrinsic jitter
- Jittered, non-jittered, and divided outputs
- GPIB or USB control
- User interface along with SCPI command set for easy automation and test system integration

2.2. Control

System configuration settings are all available from the local control panel interface, the remote GPIB (IEEE 488.2) interface, or the USB interface. Instrument status is conveyed on the front panel by the display.

The SCS16000/SCS16000J is supported by the Signal Integrity Studio software, which provides a complete user control interface.

2.3. Options

2.3.1. Rack Mount Kit and Power Cords

OPT101	European Power Cord
OPT102	UK Power Cord
OPT103	Domestic Power Cord
OPT109	China Power Cord
OPTRCK	Single Rack Mount Kit
OPTRCKD	Double Rack Mount Kit

2.3.2. Warranty, Calibration, and Services

OPT300 SCS16000	+ 1 Year Warranty Extended to 3 Years
OPT301 SCS16000	+ 1 Year Warranty Extended to 5 Years
OPT320 SCS16000	+ Centellax Calibration – Per Incident
OPT321 SCS16000	+ Annual Centellax Calibration for 3 Years

2.4. Introduction to Stress

The SCS16000 and SCS16000J are stressed clock synthesizers. The term "Stress" refers to the ability to modulate the output signal with a calibrated level of timing jitter. Timing jitter is the short term variation of a signal with respect to its ideal position in time. Timing jitter can be seen and measured at the signal logic state transitions.

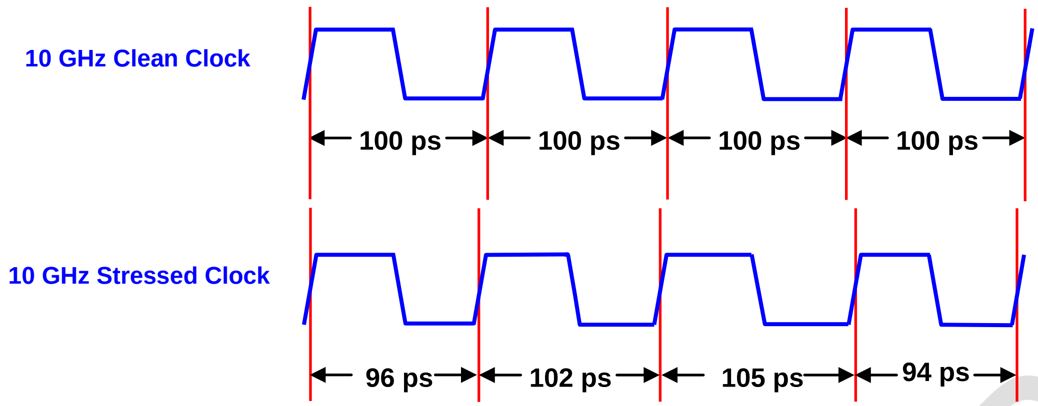


Figure 1. Timing jitter

Amplitude jitter, also known as "interference" or simply noise, will act on the finite rise and fall times of transitions to produce effective timing jitter. The SCS16000 series does not generate interference (amplitude jitter). From this point forward, the term timing jitter will be reduced to simply jitter.

In serial data systems, excessive jitter acts to "close the eye" which will eventually result in bit errors, as the bit transition moves closer to the receiver's decision point time window.

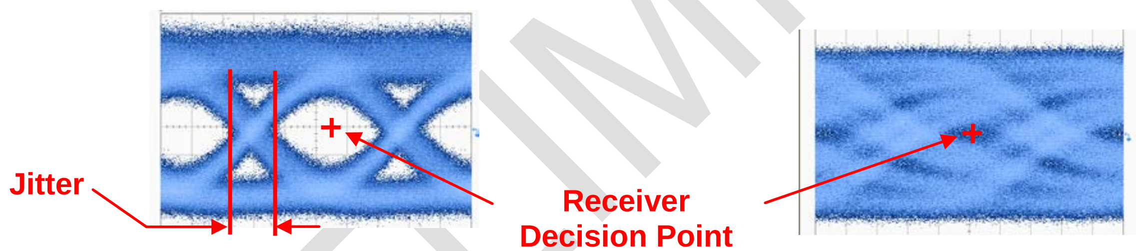


Figure 2. Eye closure with low (left) and high level of jitter (right)

A common test for a serial data receiver is its susceptibility to jitter. The test is performed by driving a known data pattern into the receiver which is stressed with a known amount of jitter. The received data is compared with a reference replica of the input pattern, and the number of incorrect detected bits is counted. A bit error rate tester (BERT) is commonly used for this purpose. By varying the characteristics of the jitter used to modulate the test data generator, the receiver's performance can be characterized.

2.4.1. Quantifying Jitter

The level or “amplitude” of jitter refers to the instantaneous displacement in time of the measure point (transition) from its ideal location. When applied to a stress generator, the amplitude refers to a level of reoccurring jitter, rather than a single instantaneous edge displacement. The jitter amplitude will be stated as a peak to peak displacement, or a Root Means Squared (rms) value, depending on the nature of the jitter distribution.

2.4.2. Types of Jitter / Stress

The jitter that a serial data receiver is exposed to in an operating environment is a composite of several elemental types. These types correspond to mechanisms in the environment which create the jitter, and are duplicated in the data pattern generator clock used to test a receiver.

The “type” of jitter represents its distribution when looking at a continuous measurement of edge displacement over time. The representation of this is a Time Interval Error (TIE) plot. The TIE plot is a graph of the absolute displacement of each transition edge in the jittered waveform with respect to its ideal location versus time (or bit location).

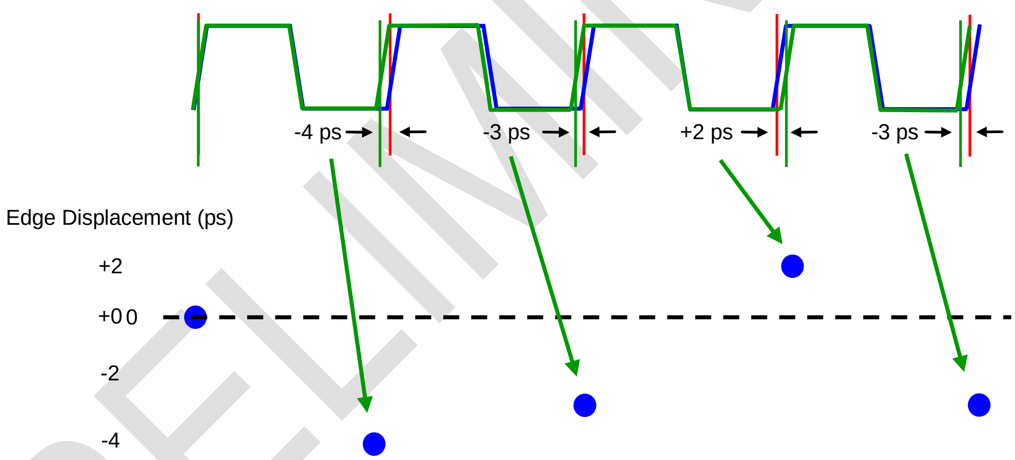


Figure 3. Time Interval Error plot of edge displacement

The resulting TIE plot shows the modulation of the jitter. The wave shape of the modulation envelop (TIE plot), relates to the type of jitter in the signal.

Jitter can be qualified as being one of a combination of several types, which again refer to the wave shape of the deviation versus time. The most basic distinction is deterministic versus non-deterministic. As its name implies, deterministic jitter forms a pattern which can be recognized. Deterministic jitter can be further broken down into data dependent, which is synchronous to the data pattern, and periodic, which has frequency components that are asynchronous to the data. While periodic jitter can have any wave shape, sinusoidal (SJ) is the most common.

The jitter amplitude (deviation in time from ideal location) of deterministic jitter is bounded. Once enough transition edges have been sampled to determine the peaks of the TIE envelop, additional sampling will not show an increase in the peak instantaneous jitter. A common graphical representation of jitter is referred to as a TIE histogram, or simply a jitter histogram. The histogram shows peak deviation versus number of samples. Figure 4 shows a typical TIE histogram plot of sinusoidal jitter.

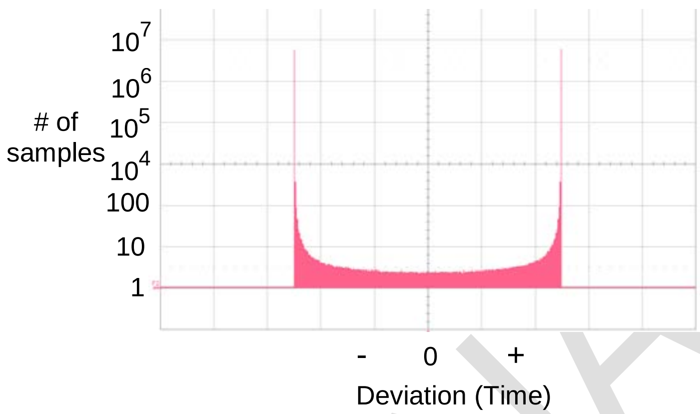


Figure 4. TIE histogram of pure sinusoidal jitter

The horizontal axis is jitter magnitude – deviation in time of the actual edge location relative to its ideal location. The axis has polarity, with 0 deviation occurring in the center. Points to the right of center are from transitions which occur after the ideal location (lag), while those to the left of center occur before the ideal location (lead).

The vertical axis shows the number of occurrences, plotted on a log scale. The characteristic shape reflects what is expected from a sine wave. The amplitude is near the positive and negative peak for most of the time, and in the zero crossing point for the least amount of time.

Generating a jitter histogram of pure deterministic jitter with a measurement instrument which updates the plot as additional samples are taken would quickly show fill out the envelop, with no change in shape or peaks as additional samples are taken.

Because deterministic jitter is bounded, its magnitude is usually expressed as a peak to peak value. The units are either absolute time, e.g. picoseconds (ps), or relative to bit time, in Unit Intervals (UI).

Non-deterministic jitter is composed primarily of random jitter components. As the name implies, the envelope of random jitter will have no recognizable pattern. Random jitter results from noise artifacts in the system. Non-deterministic jitter is un-bounded. As more samples are measured, the TIE histogram will show ever increasing peak jitter, occurring at small number of samples, with the process unending. The TIE histogram of pure random jitter (RJ) will have a true Gaussian deviation, as shown in Figure 5.

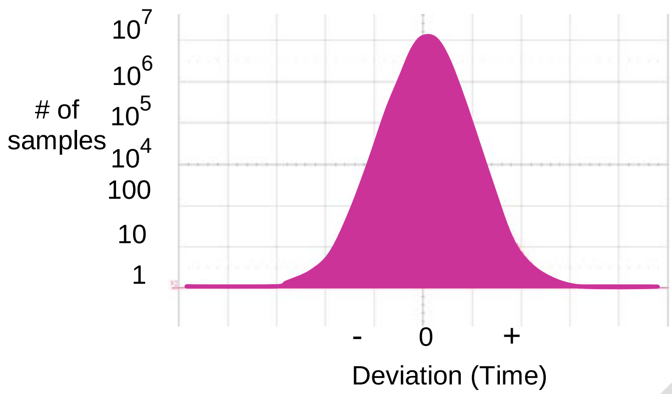


Figure 5. Typical TIE histogram of Random Jitter

When only random jitter is present in the signal, the majority of transitions will occur at the ideal location in time (zero deviation), with decreasing numbers of transitions occurring at increasing levels of deviation in time. Due to the distribution, the magnitude of random jitter is usually expressed as a root means squared (rms) value. The RJ magnitude can also be expressed as a peak to peak value, at a given confidence level. The confidence level can be computed from the number of samples. As with deterministic jitter, the units are either absolute time, e.g. picoseconds (ps), or relative to bit time, in Unit Intervals (UI).

Data and clock signals in real life operating systems will usually contain jitter which has both deterministic and non-deterministic components within it.

2.4.3. Stress for Jitter Tolerance Testing

Stressed clock synthesizers such as the SCS16000 are used to clock a data pattern generator, which in turn is used to test a serial data receiver's susceptibility to jitter. The jitter tolerance test is the basic method generally used to characterize a receiver. The test is performed with a BERT, used to monitor the receiver detected output and determine when it does and when it does not operate error free. The test is started by operating the receiver and initializing the test setup to achieve error free operation. Then stress is added, usually as a single tone of SJ at a specific frequency with low amplitude. The SJ amplitude is increased until bit errors start to occur. The stress amplitude at this point is recorded, the SJ amplitude reduced and the frequency changed. The process then repeats at the new SJ frequency. The resulting jitter tolerance plot shows the limits of error free operation as jitter amplitude versus jitter frequency.

Some communication standards include a base line mixture of RJ and SJ to be constant throughout the test, with the larger SJ used for the measurement summed into the baseline. The addition of the baseline represents the intended operating environment.

3. Operation

The following section provides detailed information regarding the use of the SCS16000/SCS16000J Stressed Clock Synthesizer.

3.1. General Information

The SCS16000/SCS16000J Stressed Clock Synthesizer should be used in accordance with the following:

- Read and follow operating instructions of all system equipment and do not exceed min/max specifications.
- Use ESD protection at all times, but especially when handling RF input/outputs.
- Situate the instrument away from heat sources.
- Do not block airflow to the fans or exhaust vents and do not allow foreign material into enclosure.
- Do not modify the power plug or wall outlet to remove the third (ground) pin.
- Do not drop or shake the instrument, minimize vibration, and handle with care.

Note: There are no user-serviceable parts within. Return damaged instruments for factory-authorized repair. Refer to instrument warranty for more information.

3.1.1. Performance Recommendations

The following recommendations ensure best performance:

- When using differential mode connection for outputs, ensure the cables are phase balanced. If the electrical length of one cable is a significant fraction of a unit interval longer than the other, the quality of the differential signal will be degraded.
- Keep cable lengths short and minimize number of cable bends.

It is not necessary to terminate unused outputs of a differential pair when a single ended signal is used.

3.1.2. Connector Care

The SCS16000/SCS16000J features high-quality SMA connectors for the front and rear panel input and output connections. Connector damage will degrade signal fidelity.

Use high quality SMA-connectors on the SMA ports. Always leave dust jackets on unused ports.

Inspect the connectors for the following:

- Worn or damaged threads
- Scratches to mating surface
- Burrs and loose metal particles
- Ensure that female contacts are straight and aligned

Clean the connectors as follows:

1 Remove any loose particles using a low-pressure air source.

2 Moisten a lint-free swab with isopropyl alcohol. Do not saturate the swab.

3 Minimize the wicking of the alcohol into the connector structure.

4 Clean the mating plane surfaces and threads.

5 Allow alcohol to evaporate, and then use a low-pressure air source to blow surfaces clean.

6 Make sure no particles or residue remains.

7 Inspect connector for damage.

3.2. Power on Settings

On power on, the instrument always returns to the factory preset settings, listed in Appendix A, Table 24. Users who wish to quickly return to last used settings may save them in one of the 5 saved settings locations, and recall them on power on.

3.3. Front Panel

The SCS16000/SCS16000J Stressed Clock Synthesizer front panel indicates the system status and contains a control panel for local operation of the instrument.

Figure 6 shows the front panel.

Figure 6. Front panel

Table 2 describes the front panel functions.

Table 2. Front panel

Item	Description
Display	The display is part of the Control Panel and is used to view the menu structure.
Softkey Buttons	The four softkey buttons to the right of the display are part of the Control Panel and are used to switch between menu items, move the highlight up or down, and edit or select parameters.
Rotary Knob	The rotary knob is part of the Control Panel and is used to increase or decrease a numeric value and move the highlight to the next digit, character, or item in a list.
Keypad	The Keypad is part of the Control Panel and is used to enter numeric values for parameters. The PRST hardkey button is used to perform an instrument preset.

Item	Description
Clock Outputs	
Jitter	The Jitter output is the main stressed clock output. The clock phase can be modulated in time with one or more calibrated jitter sources. The output amplitude, offset, and termination voltage are user settable. The jitter sources are: • Sinusoidal jitter 1 (SJ1) • Sinusoidal jitter 2 (SJ2) (SCS16000J only) • Sinusoidal periodic jitter (PJ) • Externally supplied jitter • Random jitter (RJ) is internally sourced (SCS16000J only) Sinusoidal jitter 1, Sinusoidal jitter 2, random jitter, and external jitter (high band) can be enabled simultaneously. However, the sum of these paths cannot exceed 1.0 UI. In addition, the periodic jitter path or external low band (high deviation) jitter path cannot be enabled if any of the other jitter paths are enabled. By disabling the stress sources, this output can be used to provide a clean (non-jittered) clock.
Delay	The Delay differential output connectors provide a non-stressed clock output phase offset (in UI) with amplitude, offset, and termination voltage adjustment. By setting the delay value to 0, this output can be used as a non-delayed clean (non-jittered) clock.
Divided	The divided differential clock output connectors produce a non-stressed signal that is related to the clock frequency by a divider factor. The Divided clock output signal also has amplitude, offset, and termination voltage adjustment. By setting the divide ratio to 1, this output can be used as a non-divided clean (non-jittered) clock.
Ext Clock In	Accepts an external clock to be substituted for the internal synthesizer. Note: The instrument calibration requires knowledge of the clock frequency. To facilitate externally sourced clock input, it contains a frequency counter with sufficient resolution and accuracy to support this calibration. The counter and instrument systems require a finite time to respond to large frequency changes. Thus, in order to maintain calibration, the external clock must be either a stable CW (Continuous Wave) signal, or modulated over relatively low frequency (< 100 MHz) at low rates of change.
Ext Jitter In	Accepts an external jitter source for either the low or high frequency band modulation paths. Low band input must be sinusoidal waveshape, with frequency in the range of 1 Hz to 4 MHz.
Status LEDs	
Outputs On	The Outputs On LED indicator is lit when any of the clock outputs are turned on.
Jitter On	The Jitter On LED indicator is lit when a stress source is enabled.
SSC	The SSC LED indicator is lit when the spread spectrum clock function is enabled.
Attention	The Attention LED indicator is lit when an error has occurred. The indicator will not turn off until the error message has been cleared in the Error Log in the System menu.

3.4. Rear Panel

Figure 7 shows the rear panel.

Figure 7. Rear panel

Table 3 describes the rear panel functions.

Table 3. Rear panel

Item	Description
USB Connector	The USB connector is a Type B USB port that connects the SCS16000/SCS16000J to an external PC for remote operation.
GPIB Connector	The GPIB connector is a General Purpose Interface Bus (GPIB, IEEE 488.1) connection that can be used for remote operation.
RJ Out and RJ In Connectors	The RJ loop through path is used for inserting modulation frequency contour filters in the random jitter path. The signal impedance is 50 Ω.
10MHz In Connector	The 10 MHz In connector accepts a 10 MHz reference signal from an external source.
10MHz Out Connector	The 10 MHz Out connector is a 10 MHz reference output used to lock the frequency reference of other equipment to the SCS16000/SCS16000J.
S/N	SCS16000/SCS16000J serial number.

Item	Description
Fuse Drawer	Contains the primary power mains fuse. To replace, remove the fuse by depressing the snap in tab and withdrawing the fuse drawer. A blown primary fuse generally indicates a significant component failure. The instrument should be returned to Centellax for service in the event the fuse blows.
Power Switch	SCS16000/SCS16000J main power switch (1=On; 0=Off).
Power Input Connector	Connect to power mains using approved power cable.

3.5. Block Diagram

Figure 8 is a simplified block diagram that emphasizes all inputs and outputs.

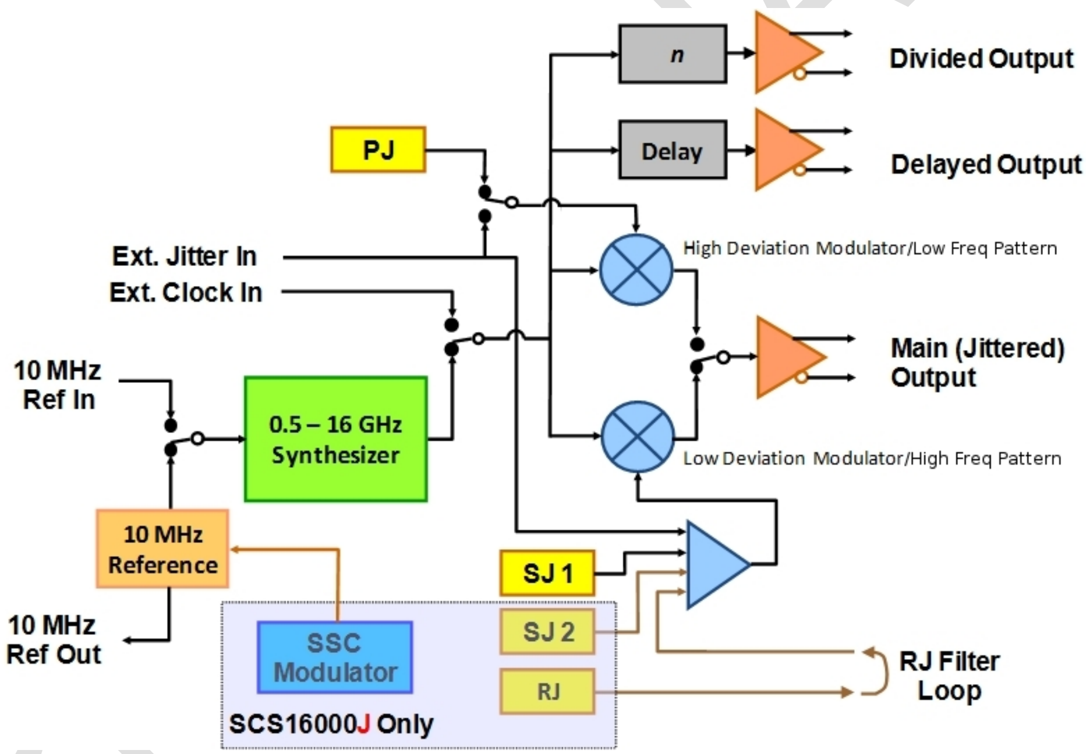


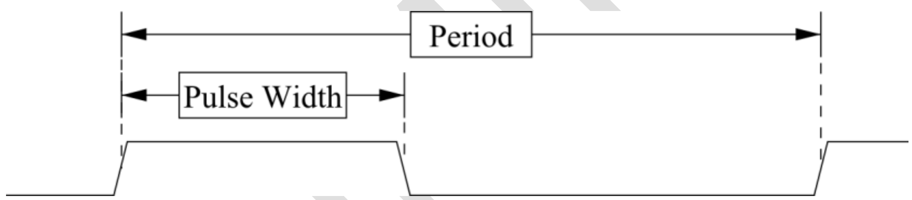
Figure 8. SCS16000/SCS16000J simplified block diagram

3.6. Divided Clock Output

The SCS16000/SCS16000J controller has the capability to divide the clock frequency over a broad range of divide ratios and return the divided signal as fully differential non-stressed outputs with adjustable amplitude and offset. This provides the user a convenient method for generating a trigger signal to use with a scope, or other applications requiring a sub rate clock.

The divide ratios are 1 to 99,999,999 with no missing integers. The divided clock settings can be controlled programmatically or through the front panel.

The divided clock output duty cycle varies between 33% and 66% as a function of the divide ratio, N. When N is a power of two, the duty cycle is exactly 50%. As N deviates from a power of two, the duty cycle deviates from 50%. For example, N=64 has 50% duty cycle, N=60 has 47% duty cycle, and N=56 has 43% duty cycle. Figure 9 shows the formulas for calculating pulse width and duty cycle as a function of N, for any integer N from 2 to 99,999,999. The duty cycle of the divided clock is 50% ± 10% when the divide ratio is set to 1.



$$\text{Pulse Width (input cycles)} = N - 2^{\text{floor}\,[\log2(N/3) + 1]}$$

$$\text{Duty Cycle (\%)} = (\text{Pulse Width}/N)*100$$

Figure 9. Calculating pulse width and duty cycle

Figure 10 is a plot of the duty cycle versus the divide ratio for N = 2 to 1024.

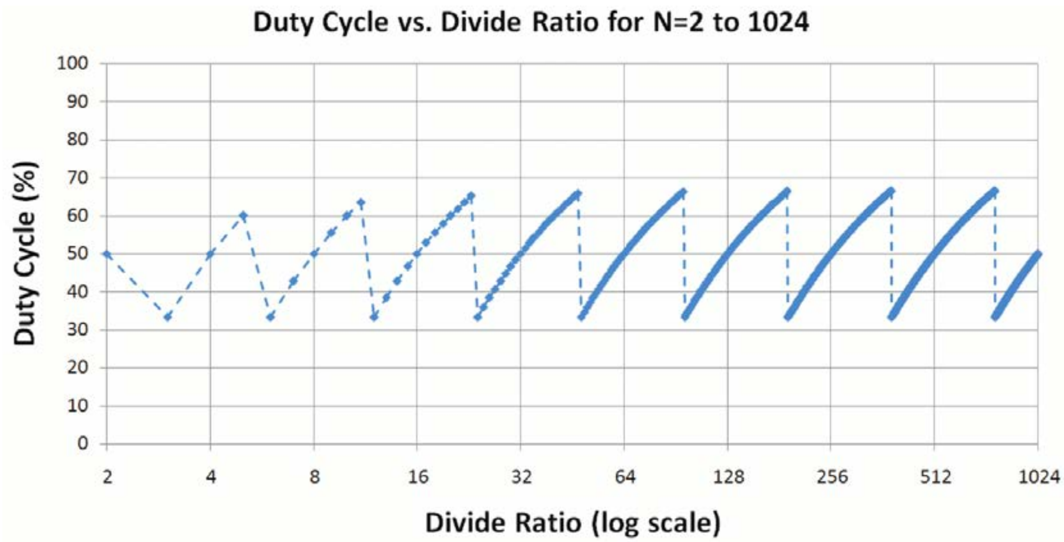


Figure 10. Duty cycle versus divide ratio

3.7. Delayed Clock Output

The delayed clock output is a non-stressed clean output that can be set from -1000 UI to 1000 UI in 0.001 UI increments. When used as a clock source for a BERT, the Delayed Clock would generally be used to clock the error detector.

The delayed clock settings can be controlled programmatically or through the front panel.

3.8. Jittered Clock Output

The Jittered Clock is the main stressed output signal. When used with a BERT, it would normally provide the clock for the pattern generator. The Jittered Clock output parameters can be controlled programmatically or through the front panel.

Refer to section 2.4, Introduction to Stress, for a full description of the stress implementation in the SCS16000/SCS16000J.

The total stress appearing in the output is a summation of the individual active stress components available in the instrument model.

For the SCS16000, the stress can be either high frequency band sinusoidal jitter (SJ1) plus externally applied high band jitter, or low frequency periodic jitter, or low frequency (high deviation) externally applied jitter.

For the SCS16000J, the stress source choices are one or two tones of high frequency sinusoidal (SJ1 + SJ2), summed with Random Jitter and any externally applied high band jitter, or low frequency periodic jitter, or low frequency (high deviation) externally applied jitter.

3.8.1. Sinusoidal, Random, and External High Band Paths

The SJ1, SJ2, random jitter, and the external high frequency band (low deviation) jitter input paths can be enabled simultaneously. However, the sum of these paths has a modulation limit of 1.0 UI.

The frequency range of SJ1 and SJ2 is 1 Hz to 200 MHz with a modulation range of 0.001 UI to 1.0 UI (or off). The external low deviation frequency range is 1 Hz to 350 MHz, with a modulation range of 0.001 UI to 1.0 UI.

Note: Applying an external jitter signal with amplitude which results in more than 1.0 UI of phase deviation from itself or as a sum with SJ1, SJ2 and/or RJ may overdrive the high frequency band modulator. Overdriving the modulator may result in distorted or intermittent clock output (clock slips). The SCS16000 cannot detect conditions which overdrive the modulator.

The RJ source provides true Gaussian random jitter with a crest factor of at least 14. The unfiltered spectral content is flat from DC to the contour of the high frequency band modulator, which has -3 dB BW of approximately 350 MHz. For applications which require a specified RJ frequency contour, an external filter can be placed the RJ modulation signal path. Both a low pass and a high pass filter can be used in series when both ends of the spectrum require filtering. The RJ signal is available on the rear panel (SCS16000J only) between the RJ Out and RJ In connectors. The impedance of the signal is 50 Ω.

The RJ modulation range is 0 to 0.107 UI-rms (1.5 UI peak-peak). However, if a filter is inserted in the RJ path, then the modulation amplitude may be attenuated. For this reason, the user can program the RJ modulation amplitude to a maximum of 0.150 UI-rms. However, setting RJ amplitude to >0.107 UI-rms will result in an "uncalibrated" error.

Note: The RJ is settable to as low as 0 UI-rms. However, each SCS16000J will have its own intrinsic RJ minimum, below which, the system cannot achieve the desired value. Typically, this lower limit is between 5 to 12 mUI-rms. It is suggested that the intrinsic RJ be checked for operation in the intended application.

The SJ1, SJ2, random jitter, and external low deviation settings can be controlled programmatically or through the front panel.

3.8.2. Low Frequency Band Periodic or External Jitter Path

A second modulation path is available for low frequency (high deviation) stress injection. It can only be operated when all of the high frequency band (low deviation) stress sources (SJ1, SJ2, RJ, and external low deviation) are disabled. The low band path operates over lower modulation frequencies, up to 17 MHz (using internal PJ), or up to 4 MHz (external). The modulation source can be either an internally generated sinusoid (Periodic Jitter, or PJ), or externally supplied through the Ext Jitter In connector. Externally applied low band jitter must have a sinusoidal wave shape. Both internal and external jitter modulation amplitude decreases as a function of modulation frequency.

The internal PJ source can be programmed to the modulation ranges shown in Table 4. Note that the modulation range is a function of modulation frequency.

Table 4. PJ modulation range

PJ Frequency	PJ Amplitude Range
1 Hz to 62.5 kHz	0.01 UI to 100 UI
62.5 kHz to 17 MHz	0.01 UI to (6.25E6/PJ Frequency)

The externally supplied sinusoidal jitter in the low frequency band (high deviation) should be supplied within the limits shown in Table 5. Note that the modulation range is a function of modulation frequency.

Note: Applying excessive amplitude to the external jitter input will overdrive the modulation driver, resulting in non-linear operation or intermittent output (clock slips). The instrument does not detect an external modulation overdrive condition.

Table 5. Low Band External Jitter modulation range

Low Band External Jitter Frequency	Low Band External Jitter Amplitude Range
≤68.4 kHz	0.01 UI to 50 UI
≥68.4 kHz to 4 MHz	0.01 UI to (3.42E6/PJ Frequency)

3.9. Spread Spectrum Clock Modulation (SCS16000J Only)

The main synthesizer in the SCS16000J can be modulated to enable Spread Spectrum Clocking (SSC). Spread Spectrum Clocking is not generally considered to be a stress, but rather a method of controlling Electromagnetic Magnetic Interference (EMI), by spreading the peak energy of the system clock over a broad portion of the spectrum. In practice, SSC modulates the system clock in the device with a large phase deviation at a relatively low frequency, generally 30 or 33 kHz. The modulation wave shape is usually triangle, to keep the power spectrum even over the modulation band. SSC is included in clock synthesizers used in BERTs to emulate a transmitter from a device which employs SSC. To assure proper tracking of the BERT or sampling scope testing a device with SSC, all three clock outputs of the SCS16000J (Jittered, Delayed and Divided) are modulated with the same SSC signal. The SSC deviation range is 0 – 1% (1% = 10,000 ppm). The modulation envelope is a triangle waveform. The modulation frequency can be set from 1 Hz to 50 kHz. In addition, there are three settings for deviation direction: down, center and up (relative to the clock frequency setting).

The spread spectrum clock modulation settings can be controlled programmatically or through the front panel.

3.10. External Clock Input

The external clock input accepts an external clock to be substituted for the internal synthesizer. The supplied signal is a full rate (X1) clock. Spread spectrum clock modulation is not available when using the external clock input.

The external clock input can be enabled or disabled programmatically or through the front panel.

Note: Setting the clock source to External with no signal applied to the External Clock input connector will result in unstable operation.

3.11. Control Panel Operation

This section describes how to use the Control Panel to operate the SCS16000/SCS16000J. Refer to Figure 11.

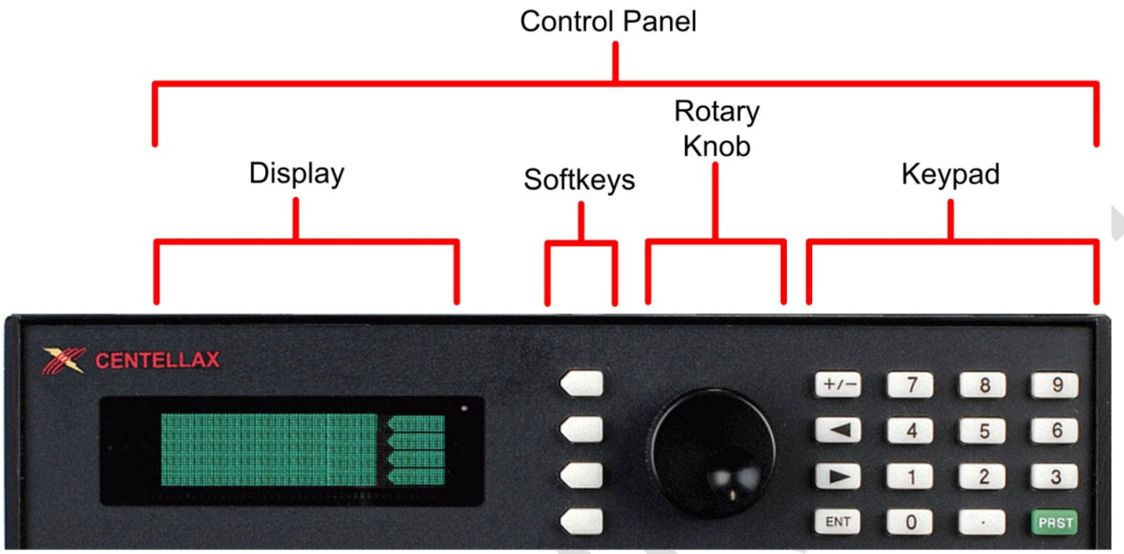


Figure 11. Control panel

3.11.1. Menu Navigation

Navigation through the menus is accomplished with the four softkeys to the right of the display and the rotary knob. Refer to Figure 12.

Figure 12. Softkey navigation buttons and rotary knob

Scroll through menu items using either the softkeys corresponding to the up and down arrow labels, or using the rotary knob. Refer to Figure 13.

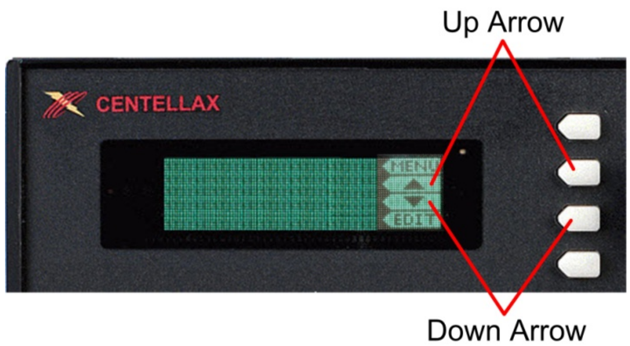


Figure 13. Scrolling through menu items

If a menu item has a lower-level menu that can be accessed, the **SEL** softkey appears. Press it to access the corresponding lower-level menu. Refer to Figure 14.

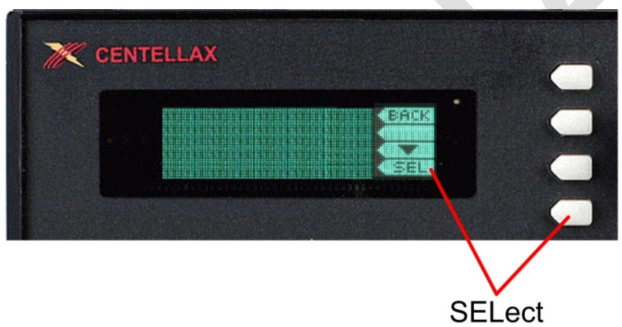


Figure 14. Accessing lower-level menus

3.11.2. Changing Parameters

The **EDIT** label appears if a menu item has a numeric value that can be changed or has multiple selections (for example, on and off). Refer to Figure 15.

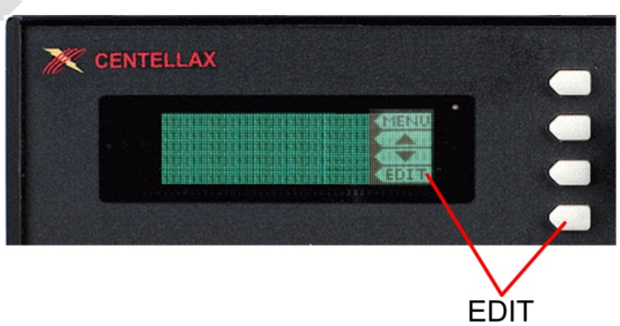


Figure 15. EDIT label

When the softkey corresponding to the **EDIT** label is pressed, the function’s parameter can be changed using the rotary knob or the keypad.

Note: The keypad is used if a parameter is a numeric value only.

Figure 16 is an example of changing parameters using the rotary knob.

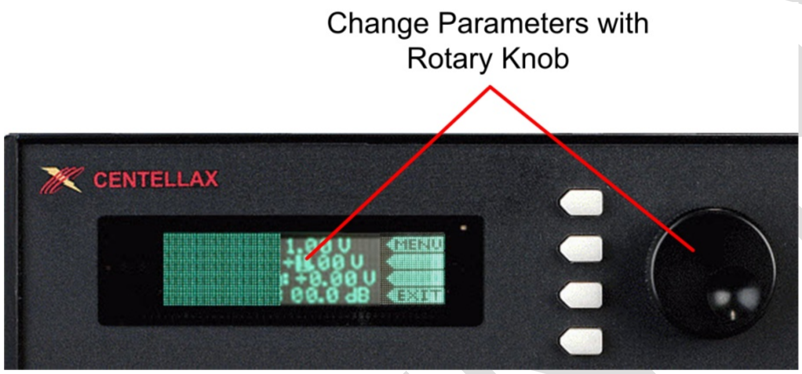


Figure 16. Changing parameters using the rotary knob

If you are using the rotary knob to change numeric values, use the right/left arrows on the keypad to highlight the digit you wish to change. The right arrow highlights the digit to the right. The left arrow highlights the digit to the left. When finished, press the softkey corresponding to the **EXIT** label to accept the changes. Refer to Figure 17.

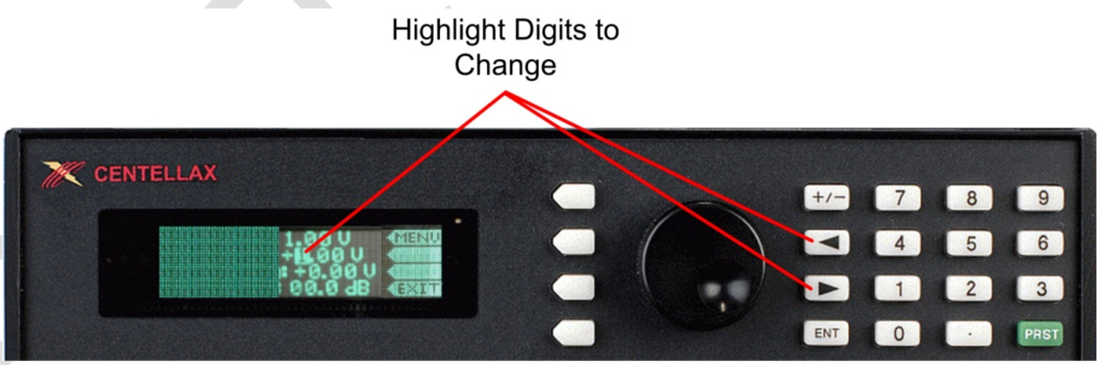


Figure 17. Highlighting digits to change

In addition to the rotary knob, the numeric keypad can be used to change numeric values. Once the softkey corresponding to the **EDIT** label is pressed, simply enter the value using the numeric keypad. When finished, either press the **ENT** hardkey on the keypad, or press the softkey corresponding to the associated units label to accept the entry. Refer to Figure 18.

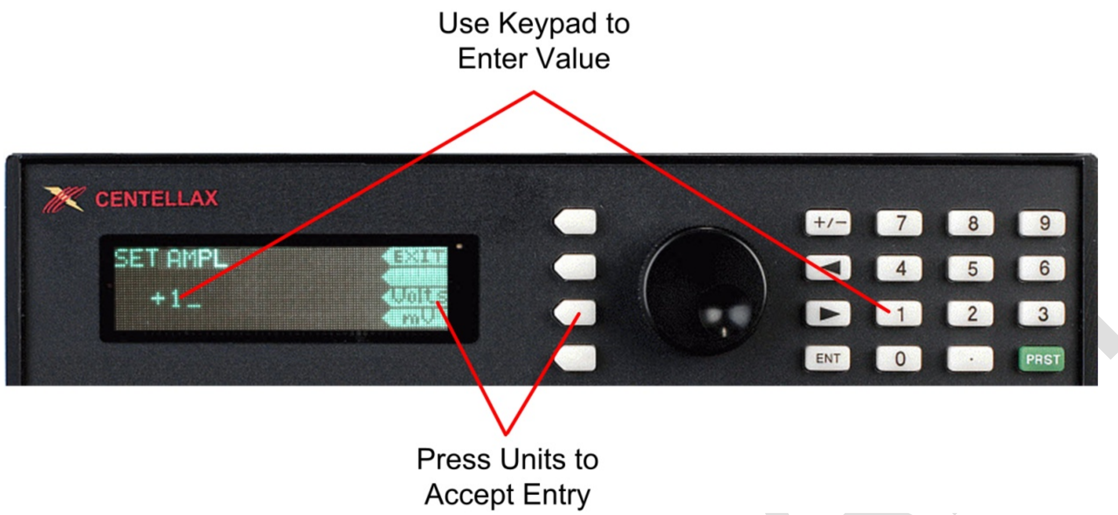


Figure 18. Using the numeric keypad

> **Note: When changing values using the rotary knob or numeric keys, the change is not accepted until the** EXIT **softkey, the** ENT **hardkey, or the units softkeys are pressed.**

3.11.3. Power-on Menu

When the SCS16000/SCS16000J is powered on, the **MAIN MENU** appears in the display window of the Control Panel. Refer to Figure 19.

```
MAIN MENU
  Synthesizer Menu
  Jit Clk Out Menu
  Dly Clk Out Menu
  Div Clk Out Menu
  System Menu
```

Figure 19. Main menu

3.11.4. Menu Structure

Figure 20 shows the hierarchical structure of the menus.

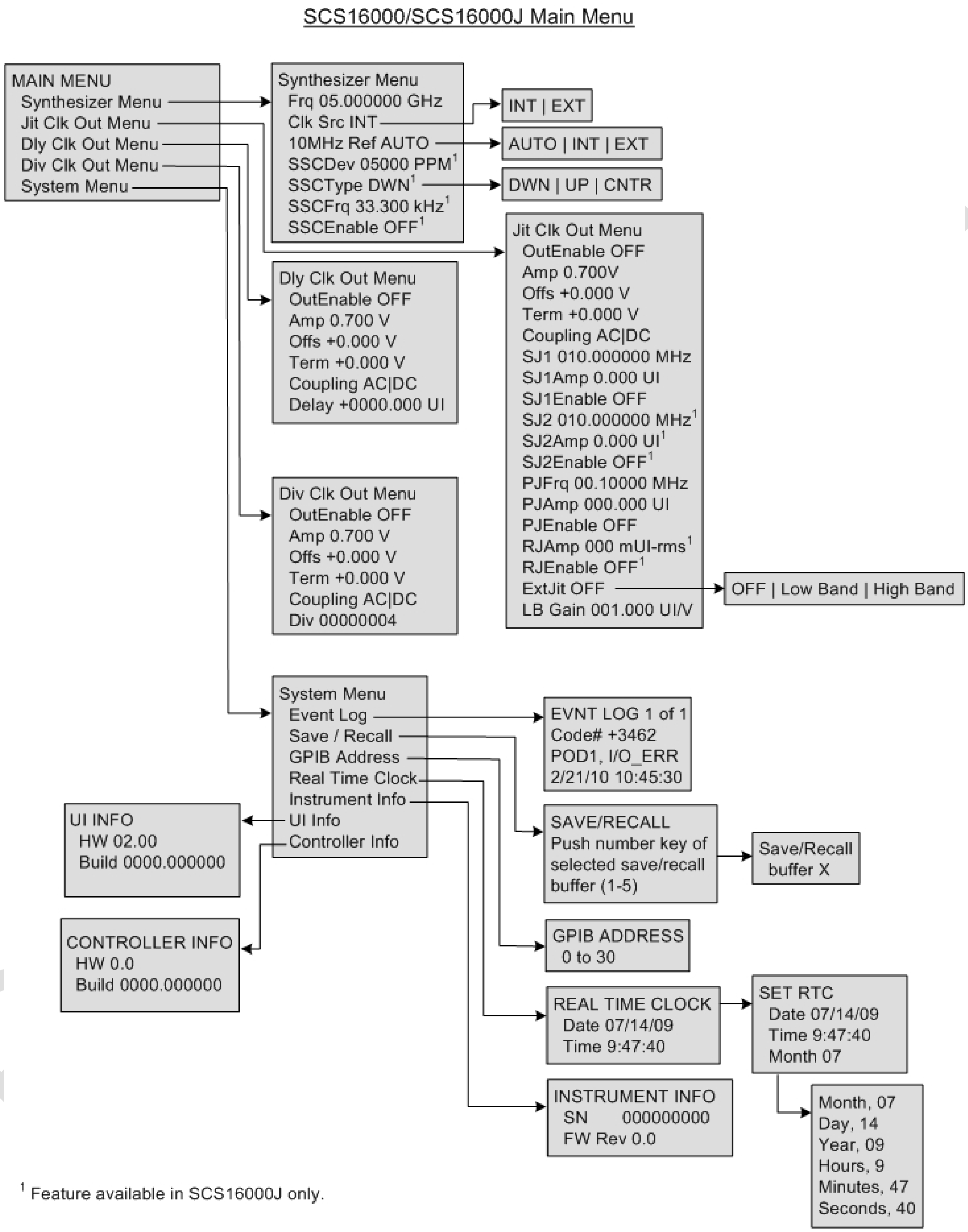


Figure 20. SCS16000/SCS16000J menu structure

3.11.5. Menu Label Descriptions

Refer to Table 6 for the Synthesizer Menu descriptions.

Table 6. Synthesizer Menu descriptions

Label Name	Description
Frq	Sets the clock source frequency. The optional units are kHz, MHz, and GHz. The resolution is 1 kHz. Displays EXTERNAL when External clock source is selected.
ClkSrc	Sets the clock source to INT for using the internal clock source or EXT for using an external clock source. *SSC cannot be enabled if the clock source is external. If the SSC enabled state conflicts with the clock source, a message indicating a conflict appears in the SCS16000/SCS16000J display. Selecting Yes to resolve the conflict will set the SSC enabled state to an appropriate value.*
10MHzRef	Sets the 10 MHz reference to INT for using the internal 10 MHz reference, EXT for using an external 10 MHz reference, or AUTO for detecting and connecting to an external reference automatically.
SSCDev[1]	Sets the spread spectrum clock deviation. The units are PPM (parts per million). The resolution is 1 PPM.
SSCType[1]	Sets the spread spectrum clock deviation direction from down (DWN) spread, up (UP) spread, or center (CNTR) spread.
SSCFrq[1]	Sets the spread spectrum clock frequency. The optional units are Hz and kHz. The resolution is 1 Hz.
SSCEnable[1]	Enables/disables the spread spectrum clock function. *SSC cannot be enabled if the clock source is external. If the clock source conflicts with the SSC enabled state, a message indicating a conflict appears in the SCS16000/SCS16000J display. Selecting Yes to resolve the conflict will set the clock source to an appropriate value.*

[1] Feature available in SCS16000J only.

Note: If the clock source is set to External without a valid clock signal connected, then the results from the :SOUR:FREQ? query may fluctuate or return "0000 Hz". In addition, a "FREQ/OOR" (frequency out of range) error may be generated. If either of these conditions is detected, check the external clock source.

Note: If the 10MHz Reference is set to Auto mode, whenever it switches between Internal and External, a message indicating the switch is generated ("REF,INTERNAL" and "REF,EXTERNAL") respectively. If the 10MHz Reference is using an External source and there is a loss of signal, a loss of signal error will be generated ("REF,LOS").

Refer to Table 7 for the Jittered Clk Out Menu descriptions.

Table 7. Jit Clk Out Menu descriptions

Label Name	Description
OutEnable	Enables/disables the jittered clock output.
Amp	Sets the amplitude of the jittered clock. The optional units are mV and V. The resolution is 0.001 V.
Offs	Sets the offset of the jittered clock. The maximum range is a function of the termination voltage setting. The optional units are mV and V. The resolution is 0.001 V. *The offset may be limited by the current termination voltage. If the desired offset value conflicts with the current termination value, a message indicating a conflict appears in the SCS16000/SCS16000J display. Selecting Yes to resolve the conflict will set the termination to an appropriate value.*
Term	Sets the termination voltage of the jittered clock. The maximum range is a function of the offset setting. The optional units are mV and V. The resolution is 0.001 V. *The termination may be limited by the current offset voltage. If the termination value conflicts with the offset value, a message indicating a conflict appears in the SCS16000/SCS16000J display. Selecting Yes to resolve the conflict will set the offset to an appropriate value.*
Coupling	Selects AC or DC output coupling. *Coupling must be set to DC before offset or termination can be set to a non-zero value. If an attempt to change the offset or termination to a non-zero value conflicts with the AC coupling setting, a message indicating a conflict appears in the SCS16000/SCS16000J display. Selecting Yes to resolve the conflict will set the coupling to DC.*
SJ1	Sets the sinusoidal jitter 1 frequency. The optional units are Hz and MHz. The resolution is 1 Hz.
SJ1Amp[2]	Sets the sinusoidal jitter 1 amplitude. The optional units are mUI and UI pk-pk. The resolution is 0.001 UI. *During the setting of SJ1 amplitude, if SJ1 and SJ2 are enabled simultaneously and their amplitude sum is greater than 1.0 UI, a message indicating a conflict appears in the SCS16000/SCS16000J display. Selecting Yes to resolve the conflict will set the SJ2 amplitude to an appropriate value.*

Label Name	Description
SJ1Enable	Enables/disables the sinusoidal jitter 1. *SJ1 cannot be enabled if PJ or external jitter (low band) is enabled. If the SJ1 enabled state conflicts with these other jitter sources, a message indicating a conflict appears in the SCS16000/SCS16000J display. Selecting Yes to resolve the conflict will disable all conflicting jitter sources.*
SJ2[1]	Sets the sinusoidal jitter 2 frequency. The optional units are Hz and MHz. The resolution is 1 Hz.
SJ2Amp[1,2]	Sets the sinusoidal jitter 2 amplitude. The optional units are mUI and UI pk-pk. The resolution is 0.001 UI. *During the setting of SJ2 amplitude, if SJ1 and SJ2 are enabled simultaneously and their amplitude sum is greater than 1.0 UI, a message indicating a conflict appears in the SCS16000/SCS16000J display. Selecting Yes to resolve the conflict will set the SJ1 amplitude to an appropriate value.*
SJ2Enable[1]	Enables/disables the sinusoidal jitter 2. *SJ2 cannot be enabled if PJ or external jitter (low band) is enabled. If the SJ2 enabled state conflicts with these other jitter sources, a message indicating a conflict appears in the SCS16000/SCS16000J display. Selecting Yes to resolve the conflict will disable all conflicting jitter sources.*
PJFrq	Sets the periodic jitter frequency. The optional units are Hz and MHz. The resolution is 1 Hz. *The maximum PJ amplitude is a function of PJ frequency. If the PJ frequency conflicts with the current PJ amplitude, a message indicating a conflict appears in the SCS16000/SCS16000J display. Selecting Yes to resolve the conflict will set PJ amplitude to an appropriate value.*
PJAmp	Sets the periodic jitter amplitude. The optional units are mUI and UI pk-pk. The resolution is 0.001 UI. The maximum PJ amplitude is a function of PJ frequency.
PJEnable	Enables/disables the periodic jitter. *Periodic Jitter cannot be enabled if any other internal or external jitter source is enabled. If the PJ enabled state conflicts with other jitter sources, a message indicating a conflict appears in the SCS16000/SCS16000J display. Selecting Yes to resolve the conflict will disable all other jitter sources.*
RJAmp[1]	Sets the random jitter amplitude in RMS. The optional units are mUI-rms and UI-rms. The resolution is 1 mUI-rms. The maximum RJ amplitude is 107 mUI-rms, but the system allows values up to 150 mUI-rms to offset any amplitude loss caused by use of a filter on the RJ input. When used in combination with other high frequency band stresses (SJ1, SJ2, and external high band jitter), the sum of all jitter source amplitudes should not exceed 1.0 UI.
RJEnable[1]	Enables/disables the random jitter output. *RJ cannot be enabled if PJ or external jitter (low band) is enabled. If the RJ enabled state conflicts with these other jitter sources, a message indicating a conflict appears in the SCS16000/SCS16000J display. Selecting Yes to resolve the conflict will disable all conflicting jitter sources.*

Label Name	Description
ExtJit	Selects the external jitter input path. *High band external jitter can be enabled in combination with SJ1, SJ2, and RJ. Low band external jitter cannot be enabled if any other jitter source is enabled. If the low band external jitter enabled state conflicts with other jitter sources, a message indicating a conflict appears in the SCS16000/SCS16000J display. Selecting Yes to resolve the conflict will disable all other jitter sources.*
LB Gain	Sets the gain of the external low band gain. The optional units are mUI/V or UI/V.

[1] Feature available in SCS16000J only.

[2] Note that the sum of SJ1, SJ2, RJ, and external jitter low deviation amplitude cannot exceed 1.0 UI. However, the system only checks SJ1 and SJ2.

Note: Sinusoidal 1 jitter, Sinusoidal 2 jitter, random jitter, and external jitter high frequency band (low deviation) can be enabled simultaneously. However, when used in combination, the sum of these paths cannot exceed 1.0 UI. In addition, periodic jitter or external low band jitter cannot be enabled if any of the other jitter paths are enabled.

Refer to Table 8 for the Dly Clk Out Menu descriptions.

Table 8. Dly Clk Out Menu descriptions

Label Name	Description
OutEnable	Enables/disables the delayed clock output.
Amp	Sets the amplitude of the delayed clock. The optional units are mV and V. The resolution is 0.001 V.
Offs	Sets the offset of the delayed clock. The maximum range is a function of the termination voltage setting. The optional units are mV and V. The resolution is 0.001 V. *The offset may be limited by the current termination voltage. If the desired offset value conflicts with the current termination value, a message indicating a conflict appears in the SCS16000/SCS16000J display. Selecting Yes to resolve the conflict will set the termination to an appropriate value.*
Term	Sets the termination voltage of the delayed clock. The maximum range is a function of the offset setting. The optional units are mV and V. The resolution is 0.001 V. *The termination may be limited by the current offset voltage. If the termination value conflicts with the offset value, a message indicating a conflict appears in the SCS16000/SCS16000J display. Selecting Yes to resolve the conflict will set the offset to an appropriate value.*

Label Name	Description
Coupling	Selects AC or DC output coupling. *Coupling must be set to DC before offset or termination can be set to a non-zero value. If an attempt to change the offset or termination to a non-zero value conflicts with the AC coupling setting, a message indicating a conflict appears in the SCS16000/SCS16000J display. Selecting Yes to resolve the conflict will set the coupling to DC.*
Dly	Sets the delay of the delayed clock. The optional units are mUI and UI. The resolution is 0.001 UI.

Refer to Table 9 for the Div Clk Out Menu descriptions.

Table 9. Div Clk Out Menu descriptions

Label Name	Description
OutEnable	Enables/disables the divided clock output.
Amp	Sets the amplitude of the divided clock. The optional units are mV and V. The resolution is 0.001 V.
Offs	Sets the offset of the divided clock. The maximum range is a function of the termination voltage setting. The optional units are mV and V. The resolution is 0.001 V. *The offset may be limited by the current termination voltage. If the desired offset value conflicts with the current termination value, a message indicating a conflict appears in the SCS16000/SCS16000J display. Selecting Yes to resolve the conflict will set the termination to an appropriate value.*
Term	Sets the termination voltage of the divided clock. The maximum range is a function of the offset setting. The optional units are mV and V. The resolution is 0.001 V. *The termination may be limited by the current offset voltage. If the termination value conflicts with the offset value, a message indicating a conflict appears in the SCS16000/SCS16000J display. Selecting Yes to resolve the conflict will set the offset to an appropriate value.*
Coupling	Selects AC or DC output coupling. *Coupling must be set to DC before offset or termination can be set to a non-zero value. If an attempt to change the offset or termination to a non-zero value conflicts with the AC coupling setting, a message indicating a conflict appears in the SCS16000/SCS16000J display. Selecting Yes to resolve the conflict will set the coupling to DC.*
Div	Sets the divided clock divide ratio.

Refer to Table 10 for the System Menu descriptions.

Table 10. System Menu descriptions

Label Name	Description
Error Log	Accesses the list of error messages. The Attention LED indicator on the front panel is lit when an error occurs and added to the Error Log.
Save / Recall	Stores the current instrument state into a buffer (1-5), which can then be recalled.
GPIB Address	Sets the GPIB Address from 0 to 30.
Real Time Clock	Sets the instrument time and date.
Instrument Info	Accesses the firmware version information and hardware version information.

3.11.6. Working With Settings Dependencies

The SCS16000/SCS16000J has a number of settings which have a dependency on another setting, noted in the tables above in *italic text*. For example, the sum of SJ1 and SJ2 Amplitudes cannot exceed 1.0 UI when they are both enabled. In other words, the range of one setting is restricted by the value of another.

Table 11 contains a summary of all dependent settings. When a conflict between multiple settings is detected, the SCS16000/SCS16000J front panel gives the user the opportunity to clear the conflicts in order to proceed with the desired setting.

Table 11. Summary of dependent settings

Settings	Dependency
Clock Source and SSC Enable	SSC cannot be enabled if the clock source is set to external and vice versa.
Offset, Termination (all clock outputs)	On all clock outputs, the range of the offset voltage is defined by the current termination voltage and vice versa. See Figure 21.
Offset, Termination, and Coupling (all clock outputs)	On all clock outputs, the coupling must be set to DC in order for the offset and termination voltage to be set to a non-zero value.
PJ vs. all other jitter sources	PJ cannot be enabled if any other jitter source is enabled and vice versa.
PJ amplitude vs. PJ frequency	The PJ amplitude range is a function of PJ frequency. The system will resolve conflicts in the PJ amplitude when the PJ frequency is adjusted. However it will simply limit the PJ amplitude range according to the current PJ frequency.

Settings	Dependency
External jitter low band vs. all other jitter sources	External jitter low band cannot be enabled if any other jitter source is enabled and vice versa.
SJ1, SJ2, RJ, external jitter high band	These high frequency band jitters can all be enabled at the same time, however, the sum of their amplitudes must be kept to below 1.0 UI. However, the SCS16000/SCS16000J only provides a check for the sum of SJ1 and SJ2 amplitudes.

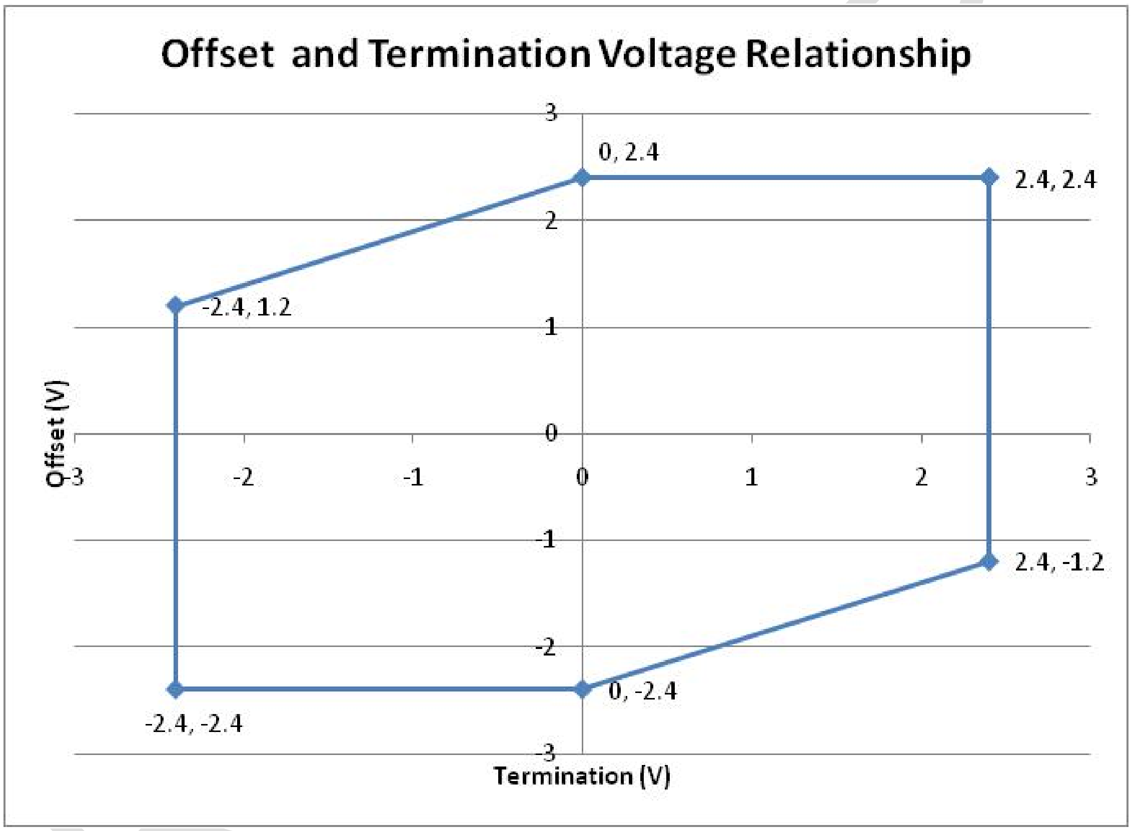


Figure 21. Relationship between Offset and Termination Voltage

3.12. Verifying Operation

The following procedures will familiarize you with the features of the SCS16000/SCS16000J and provide a quick check of system operation. The procedures all assume starting from a power up preset state. In all cases where the preset value of the setting parameter can be used, no steps are included to set the value.

3.12.1. Initial Hardware Setup

1 Connect the equipment as shown in Figure 22.

2 Tighten cables to 8 lbf-in (90 N-cm).

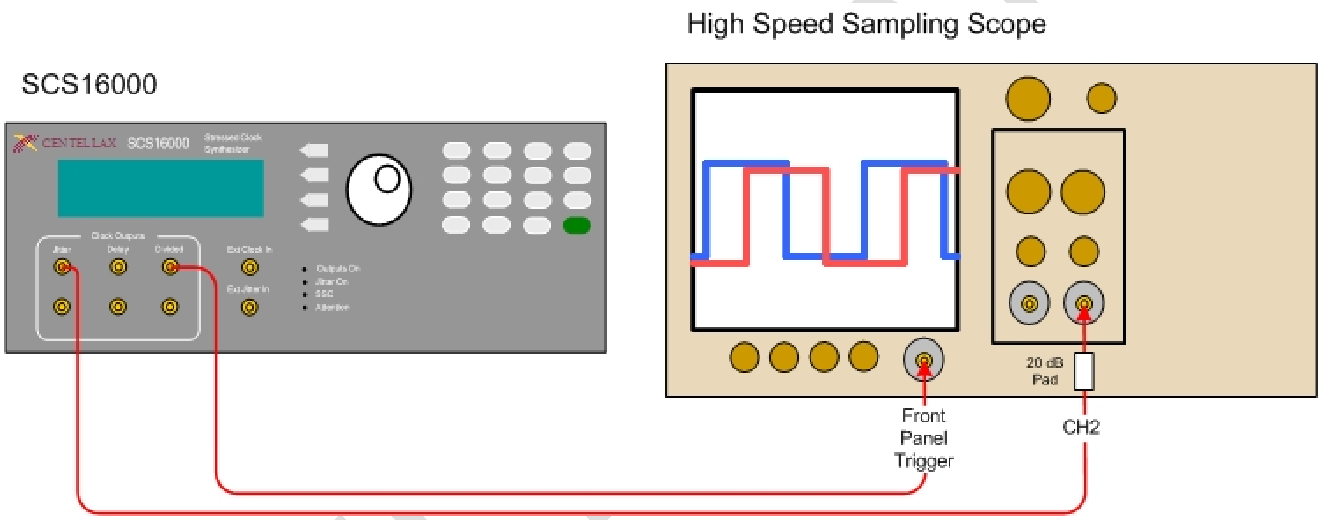


Figure 22. Setup for checking jitter

3.12.2. Initial Settings

1 Set up the high speed sampling scope as follows:

Note: For purposes of this example setup, an Agilent 86100J Infiniium DCA-J was used. High-speed sampling scope setup option names may differ between models. Signal path delays will be affected by cable lengths. It may be necessary to adjust the scope delay values to center the waveform for proper viewing.

Set the high speed sampling scope to Oscilloscope mode

Trigger Setup

Trigger Level:	20 mV
Source:	Front Panel
Trigger Bandwidth:	Standard (DC-3.2 GHz)

Timebase Setup

Scale:	16.3 ps/div
Delay From Trigger:	24.00 ns
Reference:	left

Channel 2 Setup (data)

Attenuation:	20 dB (20 dB attenuator placed at the input)
Bandwidth:	18.0 GHz
Display:	On
Scale:	100 mV/Div
Offset:	0.0 V
Units:	Volt

2 Turn the SCS16000/SCS16000J on and wait until the **MAIN MENU** appears on the display.

3 In the **MAIN MENU** position the arrow next to the **Synthesizer Menu** label then press the softkey corresponding to the **SEL** label.

4 In the **Synthesizer Menu** position the arrow next to the **Frq** label then press the softkey corresponding to the **EDIT** label.

5 Adjust the synthesizer frequency to **12 GHz**.

Note: Refer to 3.11.2 Changing Parameters for instructions on how to use the rotary knob or numeric keypad to make changes.

6 Press the softkey corresponding to the **BACK** label until the **MAIN MENU** appears.

7 In the **MAIN MENU** position the arrow next to the **Div Clk Out Menu** label then press the softkey corresponding to the **SEL** label.

8 In the **Div Clk Out Menu** position the arrow next to the **OutEnabl** label then press the softkey corresponding to the **EDIT** label.

9 Use the rotary knob to set **OutEnabl** to **ON** then press the softkey corresponding to the **EXIT** label to accept the entry and return to the **Div Clk Out Menu**.

10 Position the arrow next to the **Div** label then press the softkey corresponding to the **EDIT** label.

11 Adjust the divide ratio to **8** using the rotary knob.

12 Press the softkey corresponding to the **EXIT** label to accept the entry and return to the **MAIN MENU**.

A suitable trigger signal is now provided to the oscilloscope.

3.12.3. EnablingJitter

1 In the **MAIN MENU** position the arrow next to the **Jit Clk Out Menu** then press the softkey corresponding to the **SEL** label.

2 In the **Jit Clk Out Menu** position the arrow next to the **OutEnabl** label then press the softkey corresponding to the **EDIT** label.

3 Set **OutEnabl** to **ON** using the rotary knob. Press the softkey corresponding to **EXIT** to accept the entry. A "clean" waveform should now be displayed on the high speed sampling scope similar to the one shown in Figure 23.

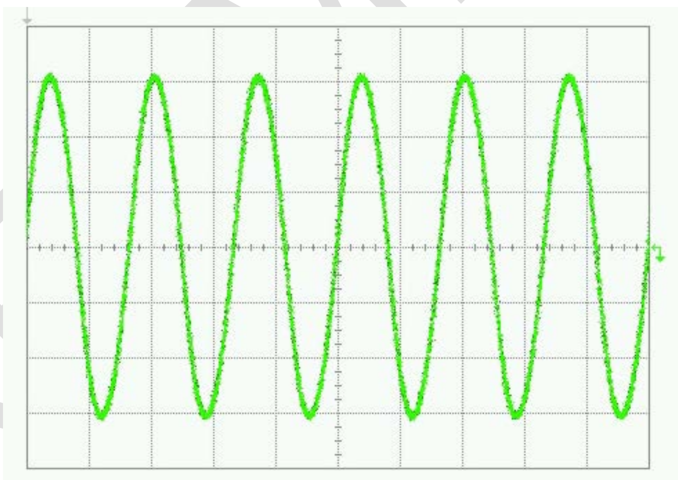


Figure 23. "Clean" waveform example

4 In the **Jit Clk Out Menu** position the arrow next to the **SJ1** label then press the softkey corresponding to the **EDIT** label.

5 Adjust the SJ1 frequency to **200.000** using the rotary knob or the numeric keypad then press the softkey corresponding to the **MHz** label to enter 200 MHz.

6 In the **Jit Clk Out Menu** position the arrow next to the **SJ1Amp** label then press the softkey corresponding to the **EDIT** label.

7 Adjust the SJ1 modulation to **1.000** using the numeric keypad then press the softkey corresponding to the **UI** label to enter 1.0 UI.

8 In the **Jit Clk Out Menu** position the arrow next to the **SJ1Enabl** label then press the softkey corresponding to the **EDIT** label.

9 Use the rotary knob to set **SJ1Enabl** to **ON**.

10 Press the softkey corresponding to the **EXIT** label to accept the entry and return to the **Jit Clk Out Menu**. A jittered waveform should now be displayed on the high speed sampling scope similar to the one shown in Figure 24.

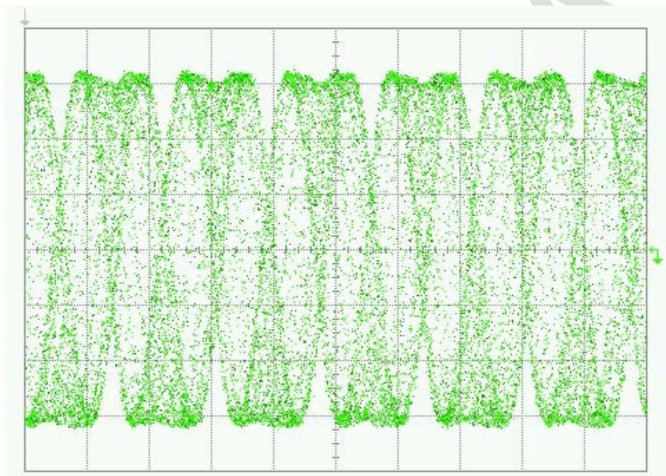


Figure 24. Jittered waveform example

11 In the **Jit Clk Out Menu** position the arrow next to the **SJ1Enabl** label then press the softkey corresponding to the **EDIT** label.

12 Use the rotary knob to set **SJ1Enabl** to **OFF**.

13 Press the softkey corresponding to the **EXIT** label to accept the entry and return to the **Jit Clk Out Menu**.

3.12.4. Enabling Random Jitter (SCS16000J Only)

1 In the **Jit Clk Out Menu** position the arrow next to the **RJAmp** label then press the softkey corresponding to the **EDIT** label.

2 Adjust the RJAmp modulation to **050** using the rotary knob or the numeric keypad then press the softkey corresponding to the **mUI-rms** label to enter 50 mUI-rms.

3 In the **Jit Clk Out Menu** position the arrow next to the **RJEnabl** label then press the softkey corresponding to the **EDIT** label.

4 Use the rotary knob to set **RJEnabl** to **ON**.

5 Press the softkey corresponding to the **EXIT** label to accept the entry and return to the **Jit Clk Out Menu**. A random jittered waveform should now be displayed on the high speed sampling scope similar to the one shown in Figure 25.

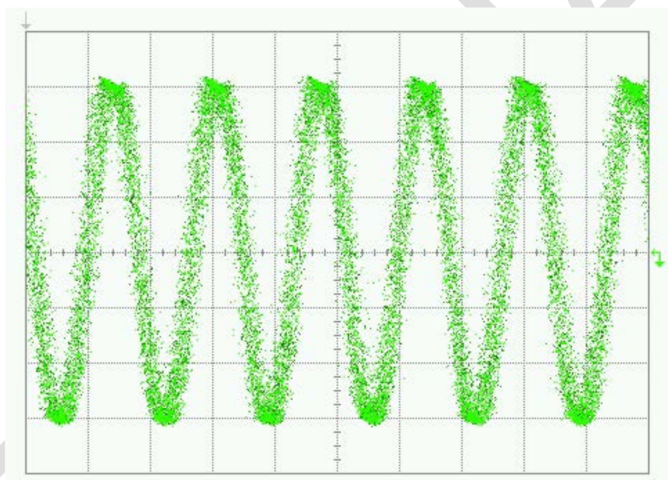


Figure 25. Random jittered waveform example

6 In the **Jit Clk Out Menu** position the arrow next to the **RJEnabl** label then press the softkey corresponding to the **EDIT** label.

7 Use the rotary knob to set **RJEnabl** to **OFF**.

8 Press the softkey corresponding to the **EXIT** label to accept the entry and return to the **Jit Clk Out Menu**.

9 Press the softkey corresponding to the **BACK** label to return to the **MAIN MENU**.

3.12.5. Viewing Delay

1 Connect the equipment as shown in Figure 26.

2 Tighten cables to 8 lbf-in (90 N-cm).

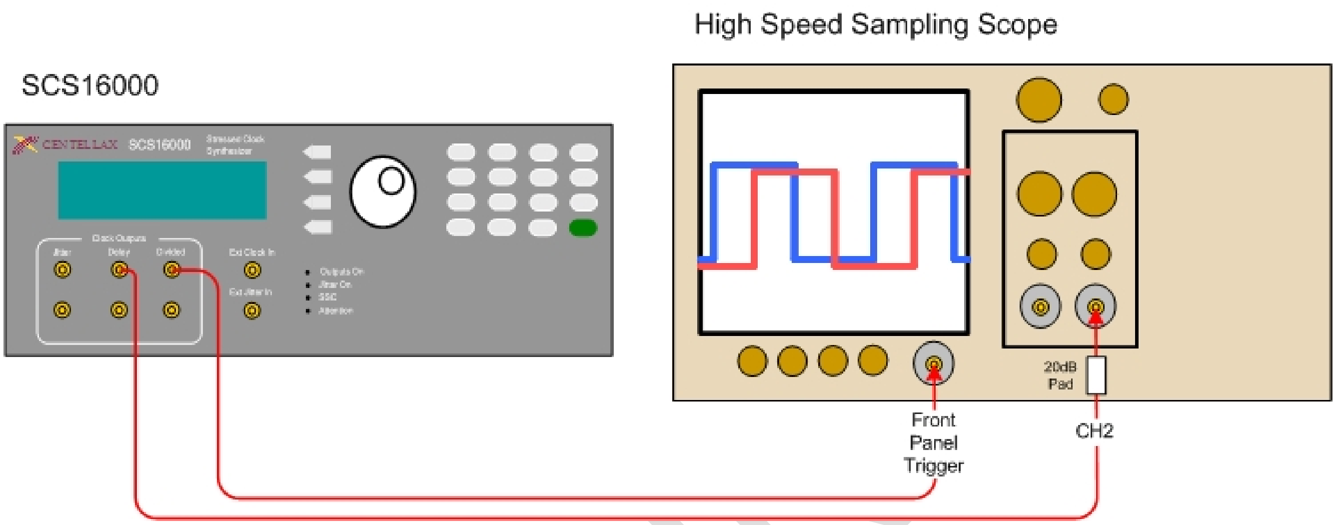


Figure 26. Setup for checking delay

3 In the **MAIN MENU** position the arrow next to the **Dly Clk Out Menu** label then press the softkey corresponding to the **SEL** label.

4 In the **Dly Clk Out Menu** position the arrow next to the **OutEnabl** label then press the softkey corresponding to the **EDIT** label.

5 Use the rotary knob to set **OutEnabl** to **ON** then press the softkey corresponding to the **EXIT** label to accept the entry.

6 Position the arrow next to the **Dly** label then press the softkey corresponding to the **EDIT** label.

7 Note the time location of a transition edge on the sampling oscilloscope. Adjust the delay using the rotary knob and ensure that the signal on the high speed sampling scope moves to the right as the delay is increased.

8 Press the softkey corresponding to the **EXIT** label to return to the **Dly Clk Out Menu**.

9 Position the arrow next to the **Dly** label then press the softkey corresponding to the **EDIT** label.

10 Adjust the delay to **00.000** using the rotary knob then press the softkey corresponding to the **EXIT** label to enter 0.0 UI (no delay).

11 Press the softkey corresponding to the **BACK** label to accept the entry and return to the **MAIN MENU**.

3.12.6. Enabling Spread Spectrum Clock (SCS16000J Only)

1 In the **MAIN MENU** position the arrow next to the **Synthesizer Menu** label then press the softkey corresponding to the **SEL** label.

2 In the **Synthesizer Menu** position the arrow next to the **SSCDev** label then press the softkey corresponding to the **EDIT** label.

3 Adjust the deviation to **04500** using the rotary knob or the numeric keypad then press the softkey corresponding to the **PPM** label to enter 4500 ppm.

Note: Refer to 3.11.2 Changing Parameters for instructions on how to use the rotary knob or numeric keypad to make changes.

4 In the **Synthesizer Menu** position the arrow next to the **SSCEnabl** label then press the softkey corresponding to the **EDIT** label.

5 Use the rotary knob to set **SSCEnabl** to **ON**.

6 Press the softkey corresponding to the **EXIT** label to accept the entry and return to the **Synthesizer Menu**. A waveform similar to the one shown in Figure 27 should now be displayed on the high speed sampling scope.

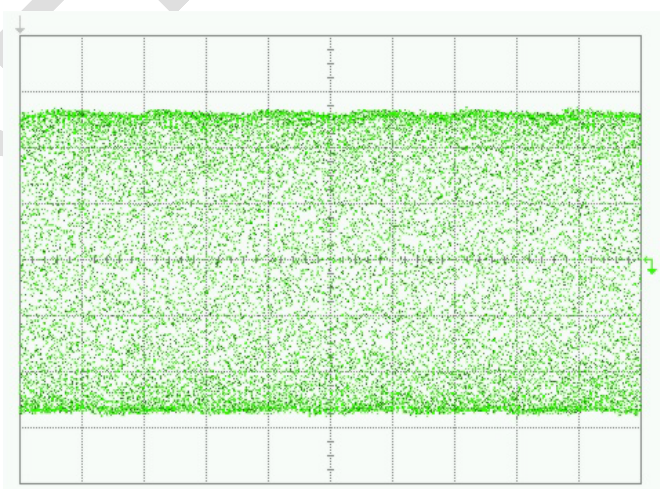


Figure 27. Spread spectrum clock waveform example

7 In the **Synthesizer Menu** position the arrow next to the **SSCEnabl** label then press the softkey corresponding to the **EDIT** label.

8 Use the rotary knob to set **SSCEnabl** to **OFF**.

9 Press the softkey corresponding to the **EXIT** label to accept the entry and return to the **MAIN MENU**. Note the waveform displayed on the oscilloscope again shows a clean clock.

3.13. Setting Frequency and Output Amplitude

The following procedure shows how to set the frequency and output amplitude of the SCS16000/SCS16000J. The output can be taken from either the Jitter or Delay clock output connector on the front panel of the SCS16000/SCS16000J.

1 In the **MAIN MENU** position the arrow next to the **Synthesizer Menu** label then press the softkey corresponding to the **SEL** label.

2 In the **Synthesizer Menu** position the arrow next to the **Frq** label then press the softkey corresponding to the **EDIT** label.

3 Adjust the synthesizer frequency using the rotary knob or the numeric keypad.

Note: Refer to 3.11.2 Changing Parameters for instructions on how to use the rotary knob or numeric keypad to make changes.

4 Press the softkey corresponding to the **EXIT** label to accept the entry and return to the **MAIN MENU**.

5 Determine which clock output will be used. Either the Jitter or Delay output can be used as a "clean" (non-jittered or non-delayed) output provided that the corresponding **OutEnabl** function is set to **OFF**.

6 In the **MAIN MENU** position the arrow next to the **Jit Clk Out Menu** (if using the Jitter clock output) or the **Dly Clk Out Menu** label (if using the Delay clock output) then press the softkey corresponding to the **SEL** label.

7 In the **Jit Clk Out Menu** or the **Dly Clk Out Menu** position the arrow next to the **Amp** label then press the softkey corresponding to the **EDIT** label.

8 Adjust the jittered clock output amplitude using the rotary knob or the numeric keypad.

9 Press the softkey corresponding to the **EXIT** label to accept the entry.

3.14. Setting Random Jitter Injection (SCS16000J Only)

The following procedure shows how to enable and set the random jitter modulation. The output is taken from the Jitter clock output connector on the front panel of the SCS16000/SCS16000J.

1 In the **MAIN MENU** position the arrow next to the **Jit Clk Out Menu** label then press the softkey corresponding to the **SEL** label.

2 In the **Jit Clk Out Menu** position the arrow next to the **Amp** label then press the softkey corresponding to the **EDIT** label.

3 Adjust the jittered clock output amplitude using the rotary knob or the numeric keypad.

Note: Refer to 3.11.2 Changing Parameters for instructions on how to use the rotary knob or numeric keypad to make changes.

4 Press the softkey corresponding to the **EXIT** label to accept the entry.

5 Adjust the random jitter modulation using the rotary knob or the numeric keypad.

6 Position the arrow next to the **RJEnabl** label then press the softkey corresponding to the **EDIT** label.

7 Use the rotary knob to set **RJEnabl** to **ON**.

8 Press the softkey corresponding to the **EXIT** label to accept the entry and return to the **MAIN MENU**.

3.15. Setting Sinusoidal Jitter Injection

The following procedure shows how to set up a single sinusoidal jitter path. The output is taken from the Jitter clock output connector on the front panel of the SCS16000/SCS16000J.

1 In the **Jit Clk Out Menu** position the arrow next to the **SJ1** label then press the softkey corresponding to the **EDIT** label.

2 Adjust the SJ1 frequency using the numeric keypad.

3 Position the arrow next to the **SJ1Amp** label then press the softkey corresponding to the **EDIT** label.

4 Adjust the SJ1 modulation using the rotary knob or the numeric keypad.

5 Position the arrow next to the **SJ1Enabl** label then press the softkey corresponding to the **EDIT** label.

6 Use the rotary knob to set **SJ1Enabl** to **ON**.

7 Press the softkey corresponding to the **EXIT** label to accept the entry and return to the **MAIN MENU**.

3.16. Setting External Jitter High Frequency Injection

The following procedure shows how to set up the external high frequency (low deviation) jitter path. This procedure requires an external jitter source be connected to the Ext Jitter In connector on the front panel of the SCS16000/SCS16000J

1 In the **MAIN MENU** position the arrow next to the **Jit Clk Out Menu** label then press the softkey corresponding to the **SEL** label.

2 In the **Jit Clk Out Menu** position the arrow next to the **ExtJit** label then press the softkey corresponding to the **EDIT** label.

3 Use the rotary knob to set **ExtJit** to **High Band**.

4 Press the softkey corresponding to the **BACK** label to accept the entry and return to the **MAIN MENU**.

3.17. Setting Delay Clock Output

The following procedure shows how to set up the delay clock output. The output is taken from the Delay clock output connector on the front panel of the SCS16000/SCS16000J.

1 In the **MAIN MENU** position the arrow next to the **Dly Clk Out Menu** label then press the softkey corresponding to the **SEL** label.

2 In the **Dly Clk Out Menu** position the arrow next to the **OutEnabl** label then press the softkey corresponding to the **EDIT** label.

3 Use the rotary knob to set **OutEnabl** to **ON** then press the softkey corresponding to the **BACK** label to accept the entry.

4 In the **Dly Clk Out Menu** position the arrow next to the **Amp** label then press the softkey corresponding to the **EDIT** label.

5 Adjust the delayed clock output amplitude using the rotary knob or the numeric keypad.

Note: Refer to 3.11.2 Changing Parameters for instructions on how to use the rotary knob or numeric keypad to make changes.

6 Press the softkey corresponding to the **EXIT** label to accept the entry.

3.18. Setting Divided Clock Output

The following procedure shows how to set up the divided clock output. The output is taken from the Divided clock output connector on the front panel of the SCS16000/SCS16000J.

1 In the **MAIN MENU** position the arrow next to the **Div Clk Out Menu** label then press the softkey corresponding to the **SEL** label.

2 In the **Div Clk Out Menu** position the arrow next to the **OutEnabl** label then press the softkey corresponding to the **EDIT** label.

3 Use the rotary knob to set **OutEnabl** to **ON** then press the softkey corresponding to the **BACK** label to accept the entry.

4 In the **Div Clk Out Menu** position the arrow next to the **Amp** label then press the softkey corresponding to the **EDIT** label.

5 Adjust the divided clock output amplitude using the rotary knob or the numeric keypad.

Note: Refer to 3.11.2 Changing Parameters for instructions on how to use the rotary knob or numeric keypad to make changes.

6 Press the softkey corresponding to the **EXIT** label to accept the entry.

3.19. Event/Error Log

Refer to Table 12 and Table 13 for the list of message origins and values found in the event/error Log.

Note: When an event/error is received, the Attention LED will illuminate.

Each event log entry contains the following information:

- Log Number: 1 to n, with 1 being the most recent error and 'n' being the oldest error.
- Message Value: The error.
- Message Origin: Identifies the sub-system which produced the error.
- Datestamp: Date of error receipt (mm/dd/yy).
- Timestamp: Time of error receipt (hh/mm/ss).

Table 12. Message origin

Message Origin	Description
IPC	IPC protocol related codes
FREQ	Frequency control
PHASE	Phase control
REF	10MHz reference clock

Table 13. Message values

Message Values	Description
OK	Status good, no errors
UNK	Status unknown
ERR	Misc. error
LOS	Loss of signal/phase slip
OOR	Value out of range
TIMEOUT	Command or operation took too long. See Section 6.13.3.
AMPL_LIMIT_WARN	Amplitude limited, non-fatal (warning), used for PJ amplitude adjustment during SCPI PJ frequency setting. See section 6.9.1.
INTERNAL	Used to indicate the 10MHz reference clock is set to Internal
EXTERNAL	Used to indicate the 10MHz reference clock is set to External

4. Applications

The SCS16000/SCS16000J is suitable for use as a clock generator in a number of digital system applications, including serial data systems. The feature set is tailored specifically for clocking a Bit Error Ratio Test (BERT) system. Designers will also find it useful in developing systems which incorporate built in bit error ratio test capability.

The instrument can provide all the clock sources required for a BERT which does not have an integrated clock source, or to upgrade a basic BERT which only has a clean clock synthesizer to stress enabled, for performing jitter tolerance testing or general receiver characterization applications.

In a general BERT application, the outputs would be configured as follows:

Jittered (Main) Output is used to drive the pattern generator. Stress can be applied for jitter tolerance testing or other receiver characterization testing.

Delayed Output can be used to clock the error detector. The delay feature enabled the detector to synchronize with the pattern, and align to sampling at the center of the eye.

Divided Output can provide a sub rate of the clock to trigger a sampling oscilloscope. Most sampling scopes have maximum trigger rates which are substantially lower than the bandwidth of the sampler. When used in high data rate applications, the data clock must be divided down to a ratio within the maximum trigger rate. In addition, by setting the divider ratio to the exact pattern length, the output will be locked to the pattern. Using this signal to trigger the sampling scope allows the user to view and measure the actual bit stream, rather than presenting an "eye" of overlaid bits.

The divided output can also be used where a sub rate clock is required.

4.1. Stressed Pattern Generator

The SCS16000 can be used to clock a data pattern generator, such as the Centellax PPG12500, to form a stressed programmable pattern generator as shown in Figure 28. The result is ideal for jitter tolerance measurements and other receiver characterization which require specific patterns beyond PRBS.

Figure 28. Stressed programmable pattern generator configuration

To configure the system, connect the Jittered output from the SCS16000 to the clock input of the pattern generator as shown in Figure 28. If a PPG12500 is used, only a single ended clock is required. Either polarity of the clock output can be used.

If an error detector device is required, it can be clocked from the Delayed output of the SCS16000. The delay control can be used to center the detector sampling within the eye pattern

4.2. Stressed Parallel BERT

Combining the SCS16000 with the PCB12500 Parallel Channel BERT and associated generator and detector heads, will form a stressed multi-channel BERT. This solution is ideal for characterizing multi-lane serial data systems, as well as determining crosstalk susceptibility.

The PCB12500 has 5 ports for attaching either pattern generators or error detectors. One of the ports, designated Reference, can be configured to either share a clock or be independently clocked from the remaining 4 ports. This allows a single pattern generator to be stressed, while the error detector is non-stressed. The remaining ports can be used to drive active aggressors for crosstalk susceptibility testing.

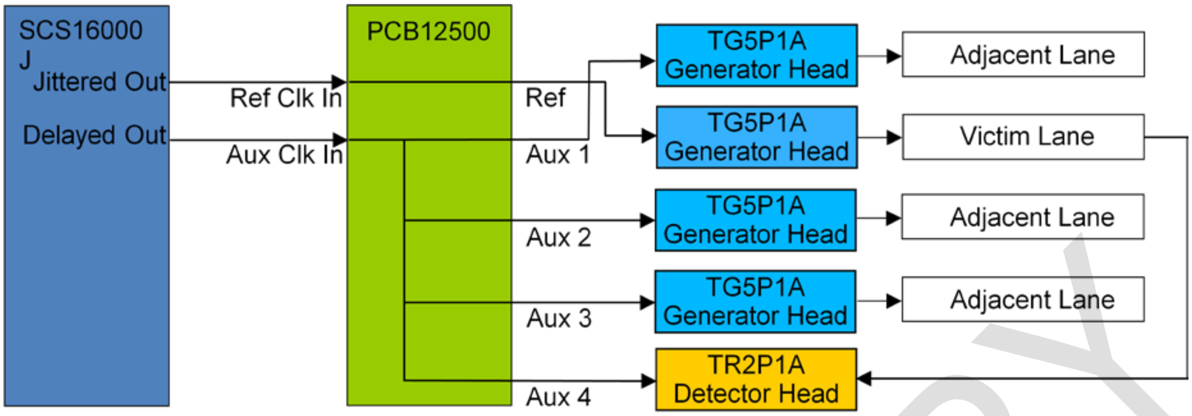


Figure 29. Typical crosstalk susceptibility setup

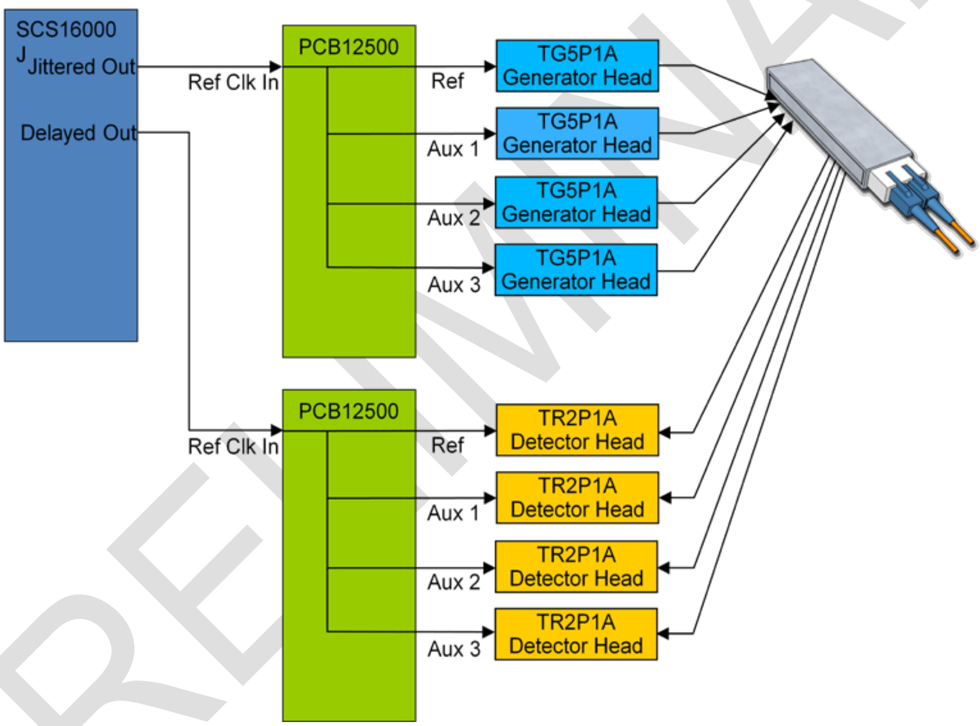


Figure 30. 4 X 10G QSFP jitter tolerance test setup

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5. Performance Specifications

Specifications describe the instrument's warranted performance. Non-warranted values are stated as typical. All specifications are valid in a range from 10 °C to 40 °C ambient temperatures after a 30-minute warm-up phase. Unless stated otherwise, all specifications are valid at the output of the included 36" high performance coax cables.

5.1. SCS16000/SCS16000J Specifications

Table 14 shows the SCS16000/SCS16000J specifications (non-stress).

Table 14. SCS16000/SCS16000J specifications

Parameter	Specification
Synthesizer	
Frequency Range	500 MHz to 16.0 GHz
Frequency Resolution	1 kHz
Outputs	Jitter (Stressed), Delay, and Divided (non-Stressed)
Output Configuration All Outputs	Differential, with amplitude, offset, and termination voltage adjustment (can be used single ended without terminating unused outputs)
Amplitude Range	300 mV to 1.7 Vp-p single ended
Offset Range	-2.4 V to +2.4 V, limited by termination voltage. See Figure 21. On divided clock output, this is only valid when the divide ratio is a power of 2.
Termination Voltage	-2.4 V to +2.4 V, limited by offset voltage. See Figure 21.
Rise Time (20% - 80%)	<20 ps
Intrinsic Jitter	<800 fs rms, integrated from 1 kHz to 100 MHz, for clock frequencies ≥ 1 GHz <1.2 ps rms for clock frequencies <1 GHz
Duty Cycle	
Jitter and Delay Outputs	50% ±5%
Divided Output	50% ±5% at divide ratios which are a power of 2. Duty factor may not be 50% at divide ratios which are not a power of 2. 50% ±10% when divide ratio is set to 1 for amplitudes ≥500 mV.
Frequency Stability	0.1 ppm
Frequency Accuracy	±20 ppm

Parameter	Specification
Reference Frequency	10.0 MHz, single ended output and input on rear panel
Input Amplitude	
Nominal	1 Vpp (4 dBm)
Operational Range	0.5 – 2 Vpp (-2 - +10 dBm)
Maximum Non-Destruct	5.0 Vpp (18 dBm)
Output Amplitude	1 Vpp typical, from 50 Ω, AC Coupled
External Clock	Single ended input can be substituted for internal synthesizer
External Clock Input Amplitude	
Nominal	1 Vpp (4 dBm)
Operational Range	0.6 – 2.0 Vpp (-0.45 – 10 dBm)
Maximum Non-Destruct	2.5 Vpp (12 dBm)
External Delayed Clock Input	Single ended input can be substituted for internal synthesizer
External Delayed Clock Input Amplitude	
Nominal	1 Vpp (4 dBm)
Operational Range	0.6 – 2.0 Vpp (-0.45 – 10 dBm)
Maximum Non-Destruct	2.5 Vpp (12 dBm)
Spread Spectrum Clock (SCS16000J only)	Phase deviation appears on all outputs
Deviation Range	0% to 1% (10,000 ppm)
Modulation Frequency Range	1 Hz to 50 kHz
Modulation Waveshape	Triangle
Deviation Direction	Down spread, Center spread, or Up spread
Divided Clock Divide Ratio	÷ 1 to 99,999,999, with no missing integers (Waveshape of divided clock slower than ≈ 1 MHz will be differentiated)
Delayed Clock Delay Range	0 to ±1,000 UI
Delayed Clock Delay Resolution	10 mUI

Table 16 shows the SCS16000 stress specifications.

Table 15. SCS16000 stress specifications

Parameter	Specification
SCS16000 Stress	
Sources	High frequency band: Sinusoidal Jitter 1 (SJ1) and externally injected high frequency jitter Low frequency band: Periodic Jitter (PJ), and externally injected low frequency jitter
Sinusoidal Jitter Configuration	Two modulator bands – high frequency or low frequency, user selected single sinusoidal jitter source in low frequency band
SJ Frequency Range	1 Hz to 200 MHz
SJ Modulation Range	Range of SJ1. Also maximum combined peak jitter of SJ1 + external jitter applied to high frequency band modulator.
Output Frequency 0.5 to 1 GHz	0.01 to 1.0 UI Pk for modulation frequency 1 Hz to 10 MHz, 0.01 to 0.5 UI Pk for modulation frequency >10 MHz to 50 MHz
Output Frequency >1 GHz to 3 GHz	0.01 to 1.0 UI Pk for modulation frequency 1 Hz to 100 MHz, 0.01 to 0.5 UI Pk for modulation frequency >100 MHz to 200 MHz
Output Frequency >3 GHz to 16 GHz	0.01 to 1.0 UI Pk for modulation frequency 1 Hz to 100 MHz, 0.01 to 0.7 UI Pk for modulation frequency >100 MHz to 200 MHz
External High Frequency Band Input	
Configuration	Wide band low deviation external modulation input. External input is summed with SJ1. High Frequency Band stress is not available when either Low Frequency PJ or External is selected.
Modulation Frequency Range	DC to at least 350 MHz, determined by high frequency modulator. -3 dB BW ≈ 320 MHz
Modulation Range	Peak sum of SJ and External input applied to high frequency modulation input is limited. Refer to SJ modulation range specification or Figure 31.
Low Frequency (High Deviation) Modulation Configuration	Periodic Jitter (PJ) or External input. SJ and high frequency external modulation sources are not available when either low frequency source is enabled.

Parameter	Specification
Low Frequency Modulation Frequency Range	
PJ External	1 Hz to 17 MHz 1 Hz to 4 MHz
Low Frequency PJ Modulation Range	
Main Clock Output	0.001 to 100 UI for frequency ≤62.5 kHz 0.001 to (6.25E6/ PJ Frequency) for frequency >62.5 kHz – 17 MHz (see Figure 31)
Low Frequency External Modulation Range	
Main Clock Output	0.001 to 50 UI for frequency ≤68.4 kHz 0.001 to (3.42E6/ PJ Frequency) for frequency >68.4 kHz – 4 MHz (see Figure 31)

Table 15 shows the SCS16000J stress specifications.

Table 16. SCS16000J stress specifications

Parameter	Specification
SCS16000J Stress	
Sources	High frequency band: Sinusoidal Jitter 1 (SJ1), Sinusoidal Jitter 2 (SJ2), Random Jitter (RJ), and externally injected high frequency jitter Low frequency band: Periodic Jitter (PJ), and externally injected low frequency jitter
Sinusoidal Jitter Configuration	Two modulator bands – high frequency or low frequency, user selected single sinusoidal jitter source in low frequency band
SJ Frequency Range	1 Hz to 200 MHz

Parameter	Specification
SJ Modulation Range	Range of SJ1 and SJ2. Also maximum combined peak jitter of SJ1 + SJ2 +RJ (peak) + external jitter applied to high frequency band modulator.
Output Frequency 0.5 to 1 GHz	0.01 to 1.0 UI Pk for modulation frequency 1 Hz to 10 MHz, 0.01 to 0.5 UI Pk for modulation frequency >10 MHz to 50 MHz
Output Frequency >1 GHz to 3 GHz	0.01 to 1.0 UI Pk for modulation frequency 1 Hz to 100 MHz, 0.01 to 0.5 UI Pk for modulation frequency >100 MHz to 200 MHz
Output Frequency >3 GHz to 16 GHz	0.01 to 1.0 UI Pk for modulation frequency 1 Hz to 100 MHz, 0.01 to 0.7 UI Pk for modulation frequency >100 MHz to 200 MHz
RJ Modulation Frequency Contour	Flat from DC to modulator band pass: -3 dB @ 320 MHz, single pole roll off to 500 MHz. Loop through allows user to customize contour by inserting HPF or LPF in loop on rear panel. Nominal impedance is 50 Ω. Filter insertion loss will lower RJ modulation depth below calibrated value.
RJ Modulation Range	0 to 75 mUI rms, can be set up to 150 mUI rms, to allow for insertion loss in external filters, but is uncalibrated for settings > 75 mUI. Peak sum of all SJ, RJ and External input applied to high frequency modulation input is limited. Refer to SJ modulation range specification or Figure 31.
RJ Crest Factor	14 minimum (p-p to rms ratio)

Parameter	Specification
External High Frequency Band Input	
Configuration	Wide band low deviation external modulation input. External input is summed with SJ1, SJ2, and RJ. High Frequency Band stress is not available when either Low Frequency PJ or External is selected.
Modulation Frequency Range	DC to at least 350 MHz, determined by high frequency modulator. -3 dB BW ≈ 320 MHz
Modulation Range	Peak sum of all SJ, RJ and External input applied to high frequency modulation input is limited. Refer to SJ modulation range specification or Figure 31.
Low Frequency (High Deviation) Modulation Configuration	Periodic Jitter (PJ) or External input. SJ, RJ and high frequency external modulation sources are not available when either low frequency source is enabled.
Low Frequency Modulation Frequency Range	
PJ External	1 Hz to 17 MHz 1 Hz to 4 MHz
Low Frequency PJ Modulation Range	
Main Clock Output	0.01 to 100 UI for frequency ≤62.5 kHz 0.01 to (6.25E6/ PJ Frequency) for frequency >62.5 kHz – 17 MHz (see Figure 31)
Low Frequency External Modulation Range	
Main Clock Output	0.01 to 50 UI for frequency ≤68.4 kHz 0.01 to (3.42E6/ Modulation Frequency) for frequency >68.4 kHz – 4 MHz (see Figure 31)

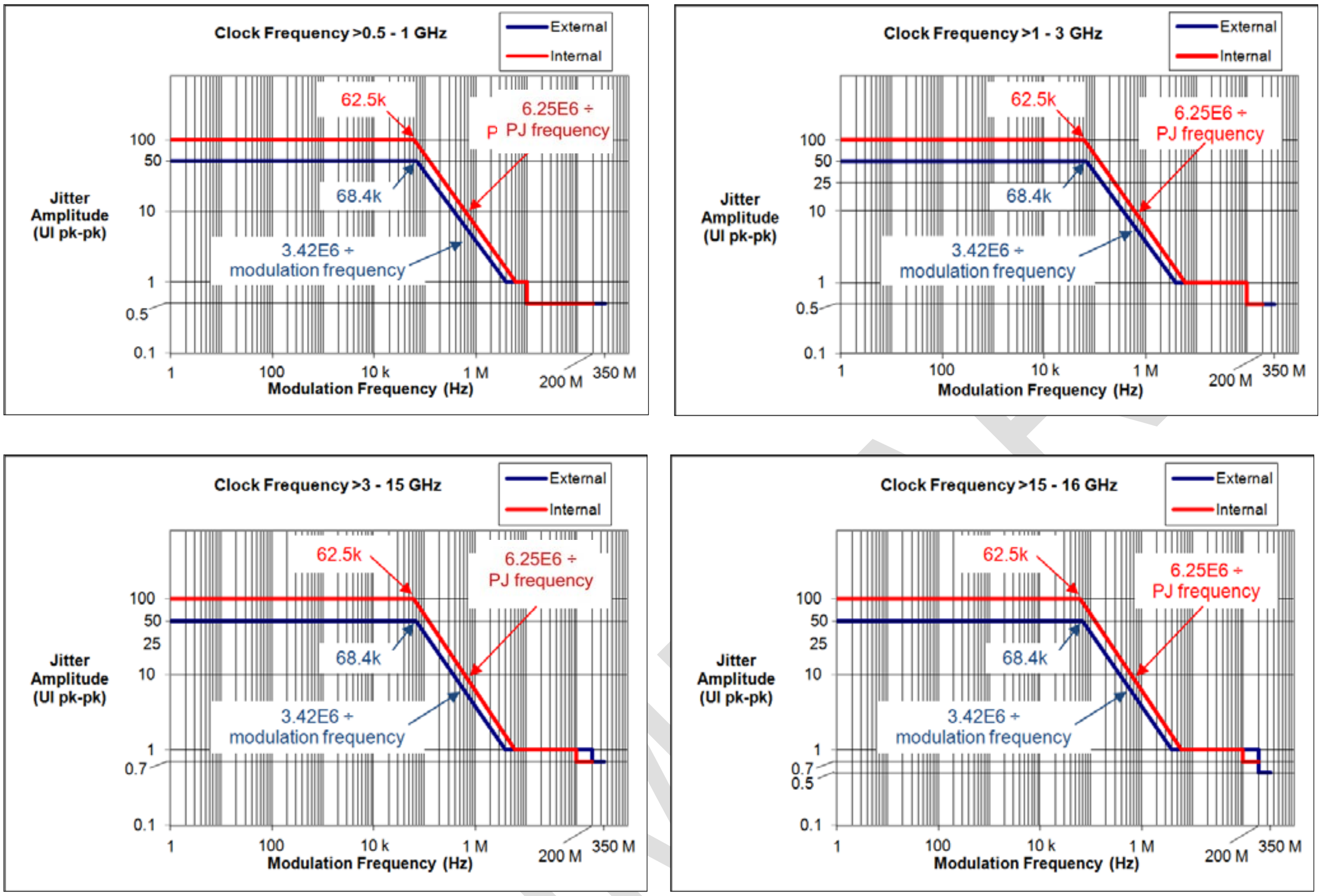

Figure 31. Internal and external – front panel clock outputs

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6. Remote Operation

The SCS16000/SCS16000J can be controlled and queried with the rear-panel GPIB or USB interface.

6.1. GPIB Interface

The GPIB interface complies with IEEE standard 488.2-1992. To learn more about the GPIB interface, consult the following books from the IEEE:

- The International Institute of Electrical and Electronic Engineers. *IEEE Standard 488.1-1987, IEEE Standard Digital Interface for Programmable Instrumentation.* New York, NY, 1987.
- The International Institute of Electrical and Electronic Engineers. *IEEE Standard 488.2-1987, IEEE Stand Codes, Formats, Protocols and Communication Commands for Use with ANSI/IEEE Std 488.1-1987.* New York, NY, 1987.

A GPIB interface requires that all devices on a common bus have different addresses. The address of the SCS16000/SCS16000J is set up using the System Settings menu. The range is 0 to 30.

The GPIB interface capabilities are described in Table 17.

Table 17: SCS16000/SCS16000J GPIB capabilities

Mnemonic	Function
SH1	Complete source handshake capability
AH1	Complete acceptor handshake capability
T6	Basic talker; serial poll; unaddressed to talk if addressed to listen; no talk only
L4	Basic listener; unaddressed to listen if addressed to talk; no listen only
SR1	Complete service request capability
RL2	Remote/local capability with local lockout (LLO)
PP0	No parallel poll capability
DC1	Device clear capability
DT1	Device trigger capability (accepted but ignored)
C0	No controller capability
E2	Tristate outputs (except the handshake line)

6.2. USB Interface

The USB interface connects to an external PC controller to control the SCS16000/SCS16000J. The USB interface allows the SCS16000/SCS16000J to be connected and disconnected without rebooting the computer or turning off the SCS16000/SCS16000J (hot swapping).

Connect a Type-A to Type-B 5 pin cable from the USB port of the PC controller to the USB port on the rear panel of the SCS16000/SCS16000J.

6.2.1. USB Driver

Installation of the appropriate driver is required. The SCS16000/SCS16000J USB port can be accessed from a PC as a virtual COM port (VCP). Virtual COM port drivers cause the USB device to appear as an additional COM port available to the PC. Application software can access the USB device in the same way as it would access a standard COM port.

The appropriate driver for several versions of Microsoft Windows® operating systems is included on a CD-ROM which is shipped with the instrument.

The SCS16000/SCS16000J uses a hardware interface IC manufactured by Future Technologies Devices International (FTDI). VCP drivers are available for several operating systems at their web site: www.ftdichip.com/FTDrivers.htm.

6.2.2. USB Programming Note

The FTDI chip, which enables serial port communication over a USB connection, boots at power-on, or preset, with the setting Local Echo = ON. The function returns a text string of each command sent over USB. It is recommended to set the Local Echo = OFF prior to sending any remote commands over USB. The command syntax to turn Local Echo OFF for the FTDI chip is:

```
!ECHO OFF
```

Progamming example:

```
# connect to SCS16000 and turn off local echo if using USB
# -address is "GPIB::18" for GPIB, "ASRL15" for COM15 (USB)
# -local echo may be on or off, which means the !ECHO OFF
#   command may be repeated back to us, this is tricky
print "connecting to " + address
scs = visa.instrument(address)
scs.clear
```

```
if (address.find("ASRL") != -1):
    scs.write("!ECHO OFF")
    scs.timeout = 1
    try:
        tmp = scs.read()
    except:
        scs.clear
    scs.timeout = timeout
```

6.3. Remote Command Syntax

The commands and queries are documented in the Backus-Naur Form notation, detailed in Table 18.

Table 18: Remote command and query syntax

Symbol	Meaning
<>	Defined element (e.g.: <arg>)
::=	Is defined as (e.g.: <arg> ::= argument)
|	Exclusive OR
{ }	One of this group is required
[ ]	Optional item
…	Previous elements may be repeated

6.3.1. Command Structure

The GPIB and USB interfaces allow commands that tell the instrument to take a specific action. In addition, these interfaces allow queries, which ask the instrument to return information.

Commands are composed of syntactic elements:

- Header – the command name; if it ends with a question mark, it's a query.
- Delimiter – a space ' ', colon ':', comma ',', or semi-colon ';'.
- Link – a command sub-function. Not all commands have links.
- Argument – a quantity, quality, or limit associated with the header or link.

Commands are case insensitive, although they are documented in an uppercase and lowercase manner that indicates the minimum characters required to make the command. The commands can be shortened to the minimum length illustrated by the uppercase letters in the documentation.

- The command
  - **:SOURce:FREQuency**
- Can be written in lowercase
  - **:source:frequency**
- And it can be shortened
  - **:SOUR:FREQ**

6.4. IEEE Common Commands

The IEEE 488.2 standard has a list of reserved commands that must be implemented by all instruments using the standard. The SCS16000/SCS16000J implements all of the required commands, listed in Table 19.

Table 19: IEEE common commands

Command	Function
*CLS	Clear status
*RST	Reset
*WAI	Wait to continue
*IDN?	Identification Query
*STB?	Status Byte Query
*TST?	Self Test Query
*ESR?	Event Status Register Query
*ESE	Event Status Enable Register Set
*ESE?	Event Status Enable Register Query
*OPC	Operation Complete clear flag
*OPC?	Operation Complete Query
*SRE	Service Request Enable Set
*SRE?	Service Request Enable Query
IEEE optional commands	
*SAV	Save
*RCL	Recall

6.5. SCPI Mandated Commands

The SCS16000/SCS16000J also conforms to the Standard Commands for Programmable Instrumentation (SCPI 1999.0) command set. The SCPI mandated commands that are implemented are listed in Table 20.

Table 20: SCPI mandated commands

Command	Function
:SYSTem:ERRor	Returns the oldest event/error number and message from error queue and removes it.
:SYSTem:VERSion	Returns SCPI protocol version number ("1999.0")
:SYSTem:ERRor:ALL	Returns all events/error log reports
:SYSTem:COUNt	Returns the number of errors in the queue.

6.6. SCPI Protocol Description

The SCS16000/SCS16000J supports a simple SCPI syntax. SCPI has an associated hierarchy with it. The top level is referred to as the Root mode. SCPI remembers the current hierarchy so you do not need to repeat it for subsequent commands.

6.6.1. SCPI Example

The capital letters in the commands denote the required subset of mnemonic for correct state control. The lower case letters are optional but if they are used they must be spelled correctly.

:OUTJitter:AMPLitude? *Query output jitter amplitude value.*

:OUTJitter:AMPLitude 500mV *Set output jitter amplitude value.*

AMPLitude? *Query output jitter amplitude value. Only the AMPLitude? command is required since it is part of the OUTJitter group.*

TERMination 135mV	*Set the termination voltage to 135 mV. Only the TERMination command is required since it is part of the OUTJitter group.*

6.7. SCPI Numeric Parameters and Optional Units

The following are examples of SCPI numeric parameters for SCPI commands that have numeric values:

.2	digits before decimal point not required
500.	digits after decimal point not required
500	no decimal point required
-1000	accepts negative '–' or positive '+' signs
200E-3	accepts uppercase 'E' or lowercase 'e' to specify exponent

The following are examples of optional units:

200 mV	mV used in place of e-3
5MHz	MHz used in place of e6
-1000UI	unit interval of negative 1000

6.8. SCS16000/SCS16000J Command Conventions

The following conventions are used in the following summary:

SOURce indicates that the SOUR characters are required and that the keyword may optionally appear as SOURCE instead. No other spellings are valid.

value is a placeholder in the command and is described elsewhere in the text for the command.

[unit] indicates that the unit placeholder is optional; it may or may not appear in the command.

string is a placeholder in the command and is described elsewhere in the text for the command.

ON | OFF indicates a choice may be made between ON or OFF.

{ ON | OFF } indicates that a choice *must* be made between ON or OFF; one or the other must appear in the command.

6.9. SCPI Standard Negative Event/Error Codes

The following table represents the SCPI standard event/errors used by the SCS16000/SCS16000J.

Table 21. SCPI standard negative event/error codes

Error/Event Code	Description
0, "No error"	Event/error queue is empty.
-100, "Command error"	Indicates that an undefined command was received via the SCPI interface.
-102, "Syntax error"	An unrecognized command or data type was encountered.
-103, "Invalid separator"	The parser was expecting a separator and encountered an illegal character.
-109, "Missing parameter"	Fewer parameters were received than required for the header.
-221, "Settings conflict"	A legal program data element was parsed but could not be executed due to current device
-222, "Data out of range"	A legal program data element was parsed but could not be executed because the value was outside the legal range as defined by the device.
-224, "Illegal parameter value"	Used where exact value, from a list of possibles, was expected.

Error/Event Code	Description
-400, "Query error"	Generic query error as defined in IEEE 488.2
-500, "Power on"	The instrument has detected an off to on transition in its power supply.
-600, "User request"	This event occurs when the instrument detects the activation of a user request local control.
-800, "Operation complete"	The instrument has completed all selected pending operations in accordance with the IEEE 488, 12.5.2 synchronization protocol.
-350, "Queue overflow"	If the queue overflows the last event/error in the queue is replaced with this error.

6.9.1. "Settings Conflict" Used for Settings Dependencies

As described in section 3.11.6, the SCS16000/SCS16000J has a number of settings which have a dependency on another setting.

From the front panel, the user is warned of these restrictions, and is given the opportunity to clear the conflict and carry out the user's request. However, the programming interface is not conducive to that behavior. Instead, the programming interface generates the "Settings Conflict" SCPI error if the controlling program has requested a value that cannot be achieved due to other dependent settings. For example, if the controlling program enables both SJ1 and SJ2, sets SJ1 to 0.4 UI, and then attempts to set SJ2 to 0.7 UI, the "Settings Conflict" error message will be generated.

The one exception to this rule is the relationship between PJ Frequency and PJ Amplitude. The PJ Amplitude is a function of the PJ Frequency. If the controlling program attempts to change the PJ Frequency such that it is incompatible with the current PJ Amplitude, the SCS16000/SCS16000J will respond with a AMPL_LIMIT_WARN instrument non-fatal error message (see Table 13), but will grant the PJ Frequency requested and set the PJ Amplitude to within valid range.

6.10. SCS16000/SCS16000J Device Commands

:OUTDelay:AMPLitude

Set the amplitude of the output delay logic level from 0.3 V to 1.7 V in 0.005 V increments. The optional units are V (default) and mV. The default value is 0.7 V.

Example
:OUTD:AMPL 750mV

:OUTDelay:AMPLitude?

Return the amplitude value of the output delay logic level. The range is 0.3 V to 1.7 V.

Example
:OUTD:AMPL?
0.750V

:OUTDelay:COUPling

Set the position of the internal switch to AC or DC. If set to AC, then offset and termination must be set to 0 V or a setting conflict error message will be generated.

Example
:OUTD:COUP DC

:OUTDelay:COUPling?

Return the position of the internal switch. The returned string is AC or DC.

Example
:OUTD:COUP?
DC

:OUTDelay:DELay

Set the output delay from -1000 UI to 1000 UI in 0.001 UI increments. The optional units are UI (Unit Interval) and mUI (milli Unit Interval). The default value/unit is 0 UI.

Example
:OUTD:DEL 1

:OUTDelay:DELay?

Return the value of the output delay. The data delay range is -1000 UI to 1000 UI.

Example
:OUTD:DEL?
1.000UI

:OUTDelay:OFFSet

Set the offset voltage of the output delay logic level from –2.4 V to +2.4 V in 0.005 V increments. The optional units are V (default) and mV. The default value/unit is 0 V.

Example
:OUTD:OFFS 2V

:OUTDelay:OFFSet?

Return the offset value of the output delay logic level. The range is –2.4 V to +2.4 V.

Example
:OUTD:OFFS?
2.000V

:OUTDelay:OUTPut

Turn the output delay clock ON or OFF. The default is OFF.

Example
:OUTD:OUTP on

:OUTDelay:OUTPut?

Return the status of the output delay clock. The returned string is either ON or OFF.

Example
:OUTD:OUTP?
ON

:OUTDelay:TERMination

Set the termination voltage of the output delay logic level from –2.4 V to +2.4 V in 0.005 V increments. The optional units are V (default) and mV. The default value/unit is 0 V.

Example
:OUTD:TERM 1.3V

:OUTDelay:TERMination?

Return the termination value of the output delay logic level. The range is –2.4 V to +2.4 V.

Example
:OUTD:TERM?
1.300V

:OUTJitter:AMPLitude

Set the amplitude of the clock signal at the clock outputs from 0.3 V to 1.7 V in 0.005 V increments. The optional units are V (default) and mV. The default value is 0.7 V.

Example
:OUTJ:AMPL 750mV

:OUTJitter:AMPLitude?

Return the amplitude of the clock signal at the clock outputs. The range is 0.3 V to 1.7 V.

Example
:OUTJ:AMPL?
0.750V

:OUTJitter:COUPling

Set the position of the internal switch to AC or DC. If set to AC, then offset and termination must be set to 0 V or a setting conflict error message will be returned.

Example
:OUTJ:COUP DC

:OUTJitter:COUPling?

Return the status of the internal switch. The returned string is AC or DC.

Example
:OUTJ:COUP?
DC

:OUTJitter:JITTer:EXTernal

Set jitter measurements to be made using a high or high deviation path. The settings are OFF, HIGHband or LOWband. The default is OFF.

Sinusoidal 1 jitter, Sinusoidal 2 jitter, random jitter, and external jitter (low deviation) can be enabled simultaneously. However, the sum of these paths cannot exceed 1 UI. The Sinusoidal periodic jitter path or external high deviation jitter path cannot be enabled if any of the other jitter paths are enabled.

Example
:OUTJ:JITT:EXT high

:OUTJitter:JITTer:EXTernal?

Return the status of the external jitter source band. The returned string is OFF, HIGHband, or LOWband.

Example
:OUTJ:JITT:EXT?
HIGH

:OUTJitter:JITTer:EXTernal:LBGain

Set the external low band range from 0.001 UI/V to 50 UI/V in 0.001 UI/V increments. The optional units are UI/V (Unit Interval) and mUI/V (milli Unit Interval). The default value/unit is 1 UI/V.

Example
:OUTJ:JITT:EXT:LBG 60UI

:OUTJitter:JITTer:EXTernal:LBGain?

Return the value of the external low band amplitude. The range is 0.001 UI/V to 50 UI/V.

Example
:OUTJ:JITT:EXT:LBG?
60UI/V

:OUTJitter:JITTer:PERiodic

Turn the periodic jitter output ON or OFF. The default is OFF.

Periodic jitter cannot be enabled if any of the other jitter sources are enabled.

Example
:OUTJ:JITT:PER on

:OUTJitter:JITTer:PERiodic?

Return the status of the periodic jitter. The returned string is either ON or OFF.

Example
:OUTJ:JITT:PER?
ON

:OUTJitter:JITTer: PERiodic:AMPLitude

Set the periodic jitter level from 0 UI to 100 UI in 0.001 UI increments. The optional units are UI (Unit Interval) and mUI (milli Unit Interval). The default value/unit is 0 UI. The PJ amplitude range is a function of PJ frequency.

Example
:OUTJ:JITT:PER:AMP 1UI

:OUTJitter:JITTer: PERiodic:AMPLitude?

Return the value of the periodic jitter amplitude. The range is 0 UI to 100 UI.

Example
:OUTJ:JITT:PER:AMP?
1.000UI

:OUTJitter:JITTer: PERiodic:FREQuency

Set the periodic jitter frequency from 1 Hz to 17 MHz in 1 Hz increments. The optional units are Hz, kHz, GHz, and MHz. The default value/unit is 00.100000 MHz. The PJ amplitude range is a function of PJ frequency. If the frequency is changed to a value incompatible with the current amplitude, the amplitude will automatically be adjusted to fit the range deviated by the desired frequency and a settings conflict error will be generated.

Example
:OUTJ:JITT:PER:FREQ 4MHz

:OUTJitter:JITTer: PERiodic:FREQuency?

Return the value of the periodic jitter frequency. The range is 1 Hz to 17 MHz.

Example
:OUTJ:JITT:PER:FREQ?
4MHz

:OUTJitter:JITTer:RANDom

Enable (ON) or disable (OFF) random jitter. The default is OFF.

SJ1, SJ2, RJ, and external jitter (low deviation) can be enabled simultaneously. RJ cannot be enabled if PJ or external jitter (lowband) are enabled.

Example
:OUTJ:JITT:RAND on

:OUTJitter:JITTer:RANDom?

Return the status of the random jitter source. The returned string is either ON or OFF.

Example
:OUTJ:JITT:RAND?
ON

:OUTJitter:JITTer:RANDom:AMPLitude

Set the random jitter level from 0 UI-rms to 0.150 UI-rms in 0.001 UI-rms increments. The optional units are UI-rms (Unit Interval-rms) and mUI-rms (milli Unit Interval). The default value/unit is 0 UI-rms. Setting the RJ amplitude to >0.107 UI-rms is allowed, but will result in an "uncalibrated" error.

Example
:OUTJ:JITT:RAND:AMPL 1UI-RMS

:OUTJitter:JITTer:RANDom:AMPLitude?

Return the value of the random level. The range is 0 UI-rms to 0.150 UI-rms.

Example
:OUTJ:JITT:RAND:AMPL?
0.100UI-rms

:OUTJitter:JITTer:SINusoidal1

Turn the SJ1 output ON or OFF. The default is OFF.

SJ1, SJ2, RJ, and external jitter (low deviation) can be enabled simultaneously. The sum of SJ1 and SJ2 cannot exceed 1.0 UI. SJ1 and SJ2 cannot be enabled if PJ or external jitter (lowband) is enabled.

Example
:OUTJ:JITT:SIN1 on

:OUTJitter:JITTer:SINusoidal1?

Return the status of SJ1. The returned string is either ON or OFF.

Example
:OUTJ:JITT:SIN1?
ON

:OUTJitter:JITTer:SINusoidal1:AMPLitude

Set the SJ1 level from 0 UI to 1.0 UI in 0.001 UI increments. The optional units are UI (Unit Interval) and mUI (milli Unit Interval). The default value/unit is 0 UI.

Example
:OUTJ:JITT:SIN1:AMPL 1UI

:OUTJitter:JITTer:SINusoidal1:AMPLitude?

Return the value of the SJ1 amplitude. The range is 0 UI to 1.0 UI.

Example
:OUTJ:JITT:SIN1:AMPL?
1.000UI

:OUTJitter:JITTer:SINusoidal1:FREQuency

Set the SJ1 frequency from 1 Hz to 200 MHz in 1 Hz increments. The optional units are Hz, kHz, GHz, and MHz. The default value/unit is 010.000000 MHz.

Example
:OUTJ:JITT:SIN1:FREQ 100MHz

:OUTJitter:JITTer:SINusoidal1:FREQuency?

Return the value of the SJ1 frequency. The range is 1 Hz to 200 MHz.

Example
:OUTJ:JITT:SIN1:FREQ?
100MHz

:OUTJitter:JITTer:SINusoidal2

Turn the sinusoidal 2 jitter output ON or OFF. The default is OFF.

SJ1, SJ2, RJ, and external jitter (low deviation) can be enabled simultaneously. However, the sum of SJ1 and SJ2 cannot exceed 1.0 UI. SJ1 and SJ2 cannot be enabled if PJ or external jitter (lowband) is enabled.

Example
:OUTJ:JITT:SIN2 on

:OUTJitter:JITTer:SINusoidal2?

Return the status of SJ2. The returned string is either ON or OFF.

Example
:OUTJ:JITT:SIN2?
ON

:OUTJitter:JITTer:SINusoidal2:AMPLitude

Set the SJ2 level from 0 UI to 1.0 UI in 0.001 UI increments. The optional units are UI (Unit Interval) and mUI (milli Unit Interval). The default value/unit is 0 UI.

Example
:OUTJ:JITT:SIN2:AMPL 1UI

:OUTJitter:JITTer:SINusoidal2:AMPLitude?

Return the value of the SJ2 amplitude. The range is 0 UI to 1.0 UI.

Example
:OUTJ:JITT:SIN2:AMPL?
1.000UI

:OUTJitter:JITTer:SINusoidal2:FREQuency

Set the SJ2 frequency from 1 Hz to 200 MHz in 1 Hz increments. The optional units are Hz, kHz, GHz, and MHz. The default value/unit is 010.000000 MHz.

Example
:OUTJ:JITT:SIN2:FREQ 100MHz

:OUTJitter:JITTer:SINusoidal2:FREQuency?

Return the value of the SJ2 frequency. The range is 1 Hz to 200 MHz.

Example
:OUTJ:JITT:SIN2:FREQ?
100MHz

:OUTJitter:OFFSet

Set the DC offset voltage at the clock outputs from –2.4 V to +2.4 V in 0.005 V increments. The optional units are V (default) and mV. The default value is 0 V.

Example
:OUTJ:OFFS 2V

:OUTJitter:OFFSet?

Return the DC offset voltage at the clock outputs. The range is –2.4 V to +2.4 V.

Example
:OUTJ:OFFS?
2.000V

:OUTJitter:OUTPut

Turn the output jitter clock ON or OFF. The default is OFF.

Example
:OUTJ:OUTP on

:OUTJitter:OUTPut?

Return the status of the output jitter clock. The returned string is either ON or OFF.

Example
:OUTJ:OUTP?
ON

:OUTJitter:TERMination

Set the DC output offset of the clock output to support the specified termination voltage of the 50Ω input port from –2.4 V to +2.4 V in 0.005 V increments. The optional units are V (default) and mV. The default value/unit is 0 V.

Example
:OUTJ:TERM 1.3V

:OUTJitter:TERMination?

Return the termination voltage of the 50Ω input port. The range is –2.4 V to +2.4 V.

Example
:OUTJ:TERM?
1.300V

:OUTSubrate:AMPLitude

Set the amplitude of the subrate output logic level from 0.3 V to 1.7 V in 0.005 V increments. The optional units are V (default) and mV. The default value is 0.7 V.

Example
:OUTS:AMPL 750mV

:OUTSubrate:AMPLitude?

Return the amplitude value of the subrate output logic level. The range is 0.3 V to 1.7 V.

Example
:OUTS:AMPL?
0.750V

:OUTSubrate:COUPling

Set the position of the internal switch to AC or DC. If set to AC, then offset and termination must be set to 0 V or a setting conflict error message will be generated.

Example
:OUTJ:COUP DC

:OUTSubrate:COUPling?

Return the status of the internal switch. The returned string is AC or DC.

Example
:OUTJ:COUP?
DC

:OUTSubrate:DIVider

Set the divider value from 1 to 99999999 in increments of 1. The default value is 4.

Example
:OUTS:DIV 4

:OUTSubrate:DIVider?

Return the divider value. The range is 1 to 99999999.

Example
:OUTS:DIV?
4

:OUTSubrate:OFFSet

Set the offset voltage of the subrate output logic level from –2.4 V to +2.4 V in 0.005 V increments. The optional units are V (default) and mV. The default value/unit is 0 V.

Example
:OUTS:OFFS 2V

:OUTSubrate:OFFSet?

Return the offset value of the subrate output logic level. The range is –2.4 V to +2.4 V.

Example
:OUTS:OFFS?
2.000V

:OUTSubrate:OUTPut

Turn the subrate output clock ON or OFF. The default is OFF.

Example
:OUTS:OUTP on

:OUTSubrate:OUTPut?

Return the status of the subrate output clock. The returned string is either ON or OFF.

Example
:OUTS:OUTP?
ON

:OUTSubrate:TERMination

Set the termination voltage of the subrate output logic level from –2.4 V to +2.4 V in 0.005 V increments. The optional units are V (default) and mV. The default value/unit is 0 V.

Example
:OUTS:TERM 1.3V

:OUTSubrate:TERMination?

Return the termination value of the subrate output logic level. The range is –2.4 V to +2.4 V.

Example
:OUTS:TERM?
1.300V

:SOURce:FREQuency

Set the source frequency from 500 MHz to 16000 MHz in 1 kHz increments. The optional units are Hz, kHz, MHz, and GHz. The default unit is GHz.

Example
:SOUR:FREQ 2GHz

:SOURce:FREQuency?

Return the value of the source frequency. The range is 500 MHz to 16000 MHz.

Example
:SOUR:FREQ?
2000MHz

:SOURce:FREQuency:CW

Set the source CW frequency from 500 MHz to 16000 MHz in 1 kHz increments. The optional units are Hz, kHz, MHz, and GHz. The default unit is Hz.

Example
:SOUR:FREQ:CW 2GHz

:SOURce:FREQuency:CW?

Return the value of the source CW frequency. The range is 500 MHz to 16000 MHz.

Example
:SOUR:FREQ:CW?
2000MHz

:SOURce:FREQuency:PATH

Set the frequency path to INTernal for using the internal source or EXTernal for using an external source. The default is INTernal. The SCS16000/SCS16000J should be disabled before setting the clock source to EXTernal.

Example
:SOUR:FREQ:PATH INT

Note: If the clock source is set to External without a valid clock signal connected, then the results from the :SOUR:FREQ? query may fluctuate or return "0000 Hz". In addition, a "FREQ/OOR" (frequency out of range) error may be generated. If either of these conditions is detected, check the external clock source.

SOURce:FREQuency:PATH?

Return the status of the source frequency path. The returned string is either INT (internal source) or EXT (external source).

Example
:SOUR:FREQ:PATH?
INT

:SOURce:ROSCillator:PATH

Set the frequency path of the reference oscillator to AUTO for sensing the reference source automatically, INTernal for using the internal reference source, or EXTernal for using an external reference source. The default is AUTO.

Example
:SOUR:ROSC:PATH EXT

Note: If the 10MHz Reference is set to Auto mode, whenever it switches between Internal and External, a message indicating the switch is generated ("REF,INTERNAL" and "REF,EXTERNAL") respectively. If the 10MHz Reference is using an External source and there is a loss of signal, a loss of signal error will be generated ("REF,LOS").

:SOURce: ROSCillator:PATH?

Return the status of the reference oscillator source frequency path. The returned string is AUTO (detect source automatically), INT (internal source), or EXT (external source).

Example
:SOUR:ROSC:PATH?
EXT

:SOURce:SSCLocking

Turn the spread spectrum clock ON or OFF. The default is OFF. The clock source must be set to INTernal before enabling the SCS16000/SCS16000J.

Example
:SOUR:SSCL on

:SOURce:SSCLocking?

Return the status of the spread spectrum clock. The returned string is either ON or OFF.

Example
:SOUR:SSCL?
ON

:SOURce:SSCLocking:DEViation

Set the spread spectrum clock deviation from 0 PPM (parts per million) to 10000 PPM in 1 PPM increments. The default value/unit is 5000 PPM.

Example
:SOUR:SSCL:DEV 10000ppm

:SOURce:SSCLocking:DEViation?

Return the deviation value of the spread spectrum clock. The range is 0 PPM (parts per million) to 10000 PPM.

Example
:SOUR:SSCL:DEV?
10000PPM

:SOURce:SSCLocking:FREQuency

Set the spread spectrum clock frequency from 1 Hz to 50000 Hz in 1 Hz increments. The optional units are Hz, kHz, and MHz. The default value/unit is 33000 Hz.

Example
:SOUR:SSCL:FREQ 50kHz

:SOURce:SSCLocking:FREQuency?

Return the value of the spread spectrum clock frequency. The range is 1 Hz to 50000 Hz.

Example
:SOUR:SSCL:FREQ?
50kHz

:SOURce:SSCLocking:TYPe

Set the spread spectrum clock to DOWN, UP, or CENTer. The default is DOWN.

Example
:SOUR:SSCL:TYP UP

:SOURce:SSCLocking:TYPe?

Return the status of the spread spectrum clock type. The returned string is DOWN, UP, or CENTer.

Example
:SOUR:SSCL:TYP?
UP

:SYSTem:DATE

Set the current date. The format is YYYY_MM_DD.

:SYSTem:DATE?

Return the current date.

:SYSTem:ERRor?

Return the oldest Event/Error Log Report.

Example
:SYST:ERR?
-222, "Data out of range"

:SYSTem:ERRor:ALL?

Return all Event/Error Log Reports.

Example
:SYST:ERR:ALL?
-100, "Command error", -222, "Data out of range"

:SYSTem:ERRor:COUNt?

Query the error/event queue for the number of unread items. As errors and events may occur at any time, more items may be present in the queue at the time it is read. If the queue is empty, the response is 0.

Example
:SYST:ERR:COUN?
0

:SYSTem:ERRor:NEXT?

Return the next Event/Error code. If the event/error queue is empty, the following is returned.

Example
:SYST:ERR:NEXT?
0, "No error"

:SYSTem:LLOCkout

Place the instrument in local lockout (remote mode) with front panel locked out. The user must use the below command to set the instrument back to local or power down to re-start the instrument.

Example
:SYST:LLOC

The following message is displayed on the front panel:

LOCAL LOCKOUT
FRONT PANEL DISABLED.

:SYSTem:LOCal

Places instrument from local lockout to local mode.

Example
:SYST:LOC

:SYSTem:PRESet

Execute a system preset. This command is the same as pressing the front panel Preset key.

:SYSTem:STATe:RECall

Recall a previously saved state from 1 to 5.

:SYSTem:STATe:SAVE

Save a system state to a storage number from 1 to 5.

:SYSTem:TIME

Set the current time. The format is HH_MM_SS.

:SYSTem:TIME?

Return the current time.

:SYSTem:VERSion?

Return current version of SCPI commands.

Example
:SYST:VERS?
1999.0

6.11. Command Summary

The SCS16000/SCS16000J device commands are summarized in Table 22.

Table 22: SCS16000/SCS16000J command summary

Command	Parameters / Results
:OUTDelay:AMPLitude	*value <unit>* ::= 0.3 V to 1.7 V, resolution = 0.005 V
:OUTDelay:AMPLitude?	
:OUTDelay:COUPling	{AC | DC}
:OUTDelay:COUPling?	
:OUTDelay:DELay	*value <unit>* ::= -1000 UI to 1000 UI, resolution=1 mUI
:OUTDelay:DELay?	
:OUTDelay:OFFSet	*value <unit>* ::= -2.4 V to +2.4 V, resolution = 0.005 V
:OUTDelay:OFFSet?	
:OUTDelay:TERMination	*value <unit>* ::= -2.4 V to +2.4 V, resolution = 0.005 V
:OUTDelay:TERMination?	
:OUTDelay:OUTPut	{ON | OFF}
:OUTDelay:OUTPut?	
:OUTJitter:AMPLitude	*value <unit>* ::= 0.3 V to 1.7 V, resolution = 0.005 V
:OUTJitter:AMPLitude?	
:OUTJitter:COUPling	{AC | DC}
:OUTJitter:COUPling?	
:OUTJitter:JITTer:EXTernal	{OFF | HIGHband | LOWband}
:OUTJitter:JITTer:EXTernal?	
:OUTJitter:JITTer:EXTernal:LBGain	*value <unit>* ::= 0.001 UI/V to 50 UI/V, resolution = 0.001 UI/V
:OUTJitter:JITTer:EXTernal:LBGain?	
:OUTJitter:JITTer:PERiodic	{ON | OFF}
:OUTJitter:JITTer:PERiodic?	
:OUTJitter:JITTer:PERiodic:AMPLitude	*value <unit>* ::= 0 UI to 62.5 UI, resolution=0.001 UI
:OUTJitter:JITTer:PERiodic:AMPLitude?	

Command	Parameters / Results
:OUTJitter:JITTer:PERiodic:FREQuency	*value <unit>* ::= 1 Hz to 17 MHz, resolution = 1 Hz
:OUTJitter:JITTer:PERiodic:FREQuency?	
:OUTJitter:JITTer:RANDom	{ON | OFF}
:OUTJitter:JITTer:RANDom?	
:OUTJitter:JITTer:RANDom:AMPLitude	*value <unit>* ::= 0 UI to 0.150 UI-rms, resolution=0.001 UI-rms
:OUTJitter:JITTer:RANDom:AMPLitude?	
:OUTJitter:JITTer:SINusoidal1	{ON | OFF}
:OUTJitter:JITTer:SINusoidal1?	
:OUTJitter:JITTer:SINusoidal1:AMPLitude	*value <unit>* ::= 0 UI to 1.0 UI, resolution=0.001 UI
:OUTJitter:JITTer:SINusoidal1:AMPLitude?	
:OUTJitter:JITTer:SINusoidal1:FREQuency	*value <unit>* ::= 1 Hz to 200 MHz, resolution = 1 Hz
:OUTJitter:JITTer:SINusoidal1:FREQuency?	
:OUTJitter:JITTer:SINusoidal2	{ON | OFF}
:OUTJitter:JITTer:SINusoidal2?	
:OUTJitter:JITTer:SINusoidal2:AMPLitude	*value <unit>* ::= 0 UI to 1.0 UI, resolution=0.001 UI
:OUTJitter:JITTer:SINusoidal2:AMPLitude?	
:OUTJitter:JITTer:SINusoidal2:FREQuency	*value <unit>* ::= 1 Hz to 200 MHz, resolution = 1 Hz
:OUTJitter:JITTer:SINusoidal2:FREQuency?	
:OUTJitter:OFFSet	*value <unit>* ::= -2.4 V to +2.4 V, resolution = 0.005 V
:OUTJitter:OFFSet?	
:OUTJitter:OUTPut	{ON | OFF}
:OUTJitter:OUTPut?	
:OUTJitter:TERMination	*value <unit>* ::= -2.4 V to +2.4 V, resolution = 0.005 V
:OUTJitter:TERMination?	
:OUTSubrate:AMPLitude	*value <unit>* ::= 0.3 V to 1.7 V, resolution = 0.005 V
:OUTSubrate:AMPLitude?	

Command	**Parameters / Results**
:OUTSubrate:DIVider	*value* ::= 1 to 99999999, resolution = 1
:OUTSubrate:DIVider?	
:OUTSubrate:OFFSet	*value* <*unit*> ::= -2.4 V to +2.4 V, resolution = 0.005 V
:OUTSubrate:OFFSet?	
:OUTSubrate:OUTPut	{ON | OFF}
:OUTSubrate:OUTPut?	
:OUTSubrate:TERMination	*value* <*unit*> ::= -2.4 V to +2.4 V, resolution = 0.005 V
:OUTSubrate:TERMination?	
:SOURce:FREQuency	*value* <*unit*> ::= 500 MHz to 16000 MHz, resolution = 1 kHz
:SOURce:FREQuency?	
:SOURce:FREQuency:CW	*value* <*unit*> ::= 500 MHz to 16000 MHz, resolution = 1 kHz
:SOURce:FREQuency:CW?	
:SOURce:FREQuency:PATH	{INTernal | EXTernal}
:SOURce:FREQuency:PATH?	
:SOURce:ROSCillator:PATH	{AUTO | INTernal | EXTernal}
:SOURce:ROSCillator:PATH?	
:SOURce:SSCLocking	{ON | OFF}
:SOURce:SSCLocking?	
:SOURce:SSCLocking:DEViation	*value* <*unit*> ::= 0 PPM to 10000 PPM, resolution = 1 PPM
:SOURce:SSCLocking:DEViation?	
:SOURce:SSCLocking:FREQuency	*value* <*unit*> ::= 1 Hz to 50000 Hz, resolution = 1 Hz
:SOURce:SSCLocking:FREQuency?	
:SOURce:SSCLocking:TYPe	{DOWN | UP | CENTer}
:SOURce:SSCLocking:TYPe?	
:SYSTem:DATE	Sets the current date
:SYSTem:DATE?	Responds with current date
:SYSTem:ERRor?	Responds with the oldest Event/Error log report
:SYSTem:ERRor:ALL?	Responds with all Event/Error log reports

Command	Parameters / Results
:SYSTem:ERRor:COUNt?	Queries the error/event queue for the number of unread items.
:SYSTem:ERRor:NEXT?	Gives the next Event/Error log report
:SYSTem:LLOCkout	Local lockout (panel locked out)
:SYSTem:LOCal	Places instrument in local mode
:SYSTem:PRESet	Execute a system preset.
:SYSTem:STATe:RECall	Recall a previously stored state.
:SYSTem:STATe:SAVE	Save a system state.
:SYSTem:TIME?	Responds with current time
:SYSTem:TIME	Set the current time
:SYSTem:VERSion?	Responds with current version of SCPI commands

6.12. Programming Example

The following programming example is written in Python, an open-source programming language that is free to use, even for commercial products. The open-source PyVISA package enables fast and easy GPIB and USB instrument control.

The example program below demonstrates some popular methods of interfacing with the SCS16000 instrument. Contact support@centellax.com if you have any additional questions or if you would like help programming our instruments.

```
# use the PyVISA plugin from http://pyvisa.sourceforge.net/
import visa

# instrument setup
address = "ASRL31" # "GPIB::18" for GPIB address 18, "ASRL15" for COM15
timeout = 1000     # default 1s timeout for queries
resetSCS = False   # option to reset the SCS after starting the program

# connect to SCS16000 and turn off local echo if using USB
# -address is "GPIB::18" for GPIB, "ASRL15" for COM15 (USB)
# -local echo may be on or off, which means the !ECHO OFF
#   command may be repeated back to us, this is tricky
print "connecting to " + address
scs = visa.instrument(address)
scs.clear
if (address.find("ASRL") != -1):
    scs.write("!ECHO OFF")
    scs.timeout = 1
    try:
        tmp = scs.read()
    except:
        scs.clear
    scs.timeout = timeout

# query instrument type
idn = scs.ask("*IDN?").strip("\n")
idnManufacturer, idnModel, idnSN, idnRev = idn.split(",")
idnModel = idnModel.upper().strip(" ")
idnSN = idnSN.strip(" ").lstrip("0")
if idnModel.find("SCS16000") != -1:
    if idnModel.find("J") != -1:
        scsJitter = True
    else:
        scsJitter = False
    print "found " + idnModel + " serial number " + idnSN
else:
    print "unrecognized instrument: " + idn
    exit

# reset the instrument, if desired
if resetSCS:
    print "resetting instrument:",
    scs.write("*RST")
```

```
    opc = scs.ask("*OPC?")
    print "done"

# clear any errors from the queue
def errchk():
    print "error queue:",
    esr = int(scs.ask("*ESR?").strip("\n"))
    if (esr != 0): print "*ESR? error #%d" % esr
    print scs.ask(":SYST:ERR:ALL?").strip("\n")
errchk()

# turn on internal clock and set frequency
print "setting clock:",
scs.write(":SOUR:FREQ:PATH INT")
opc = scs.ask("*OPC?")
print scs.ask(":SOUR:FREQ:PATH?").strip("\n"),
scs.write(":SOUR:FREQ %.3fGHz" % 10.3125)
opc = scs.ask("*OPC?")
print scs.ask(":SOUR:FREQ?").strip("\n")

# set delayed outputs on
print "delayed outputs:",
scs.write(":OUTD:OUTP ON")
print scs.ask(":OUTD:OUTP?").strip("\n"),
scs.write(":OUTD:AMPL 1V")
print scs.ask(":OUTD:AMPL?").strip("\n"),
scs.write(":OUTD:DEL 0.5UI")
opc = scs.ask("*OPC?")
print scs.ask(":OUTD:DEL?").strip("\n")

# set subrate outputs on
print "subrate outputs:",
scs.write(":OUTS:OUTP ON")
print scs.ask(":OUTS:OUTP?").strip("\n"),
scs.write(":OUTS:AMPL 1V")
print scs.ask(":OUTS:AMPL?").strip("\n"),
scs.write(":OUTS:DIV 64")
print scs.ask(":OUTS:DIV?").strip("\n")

# if jitter option enabled, apply some!
if scsJitter:
    # set jittered outputs on
    print "jittered outputs:",
    scs.write(":OUTJ:OUTP ON")
    print scs.ask(":OUTJ:OUTP?").strip("\n"),
    scs.write(":OUTJ:AMPL 1V")
    print scs.ask(":OUTJ:AMPL?").strip("\n")

    # turn on SSC: 33kHz 0/-0.5%
    print "SSC:",
    scs.write(":SOUR:SSCL ON")
    opc = scs.ask("*OPC?")
    print scs.ask(":SOUR:SSCL?").strip("\n"),
    scs.write(":SOUR:SSCL:FREQ 33kHz")
    print scs.ask(":SOUR:SSCL:FREQ?").strip("\n"),
    scs.write(":SOUR:SSCL:DEV 0.5pct")
    print scs.ask(":SOUR:SSCL:DEV?").strip("\n"),
```

```
scs.write(":SOUR:SSCL:TYP DOWN")
print scs.ask(":SOUR:SSCL:TYP?").strip("\n")

# turn off SJ1, SJ2, RJ
print "Jitter:",
scs.write(":OUTJ:JITT:PER OFF")
opc = scs.ask("*OPC?")
print scs.ask(":OUTJ:JITT:PER?").strip("\n"),
scs.write(":OUTJ:JITT:SIN1 OFF")
print scs.ask(":OUTJ:JITT:SIN1?").strip("\n"),
scs.write(":OUTJ:JITT:SIN2 OFF")
print scs.ask(":OUTJ:JITT:SIN2?").strip("\n"),
scs.write(":OUTJ:JITT:RAND OFF")
print scs.ask(":OUTJ:JITT:RAND?").strip("\n")

# turn on PJ and adjust to 3.645UI at 2.4MHz
print "PJ:",
scs.write(":OUTJ:JITT:PER ON")
opc = scs.ask("*OPC?")
print scs.ask(":OUTJ:JITT:PER?").strip("\n"),
scs.write(":OUTJ:JITT:PER:AMPL 0")
opc = scs.ask("*OPC?")
print scs.ask(":OUTJ:JITT:PER:AMPL?").strip("\n"),
scs.write(":OUTJ:JITT:PER:FREQ 2.4MHz")
print scs.ask(":OUTJ:JITT:PER:FREQ?").strip("\n").strip(" "),
scs.write(":OUTJ:JITT:PER:AMPL 3.645UI")
opc = scs.ask("*OPC?")
print scs.ask(":OUTJ:JITT:PER:AMPL?").strip("\n"),
# turn off PJ
scs.write(":OUTJ:JITT:PER OFF")
opc = scs.ask("*OPC?")
print scs.ask(":OUTJ:JITT:PER?").strip("\n")

# turn on SJ1 and adjust to 1.2UI at 200MHz
print "SJ1:",
scs.write(":OUTJ:JITT:SIN1 ON")
print scs.ask(":OUTJ:JITT:SIN1?").strip("\n"),
scs.write(":OUTJ:JITT:SIN1:AMPL 0")
print scs.ask(":OUTJ:JITT:SIN1:AMPL?").strip("\n"),
scs.write(":OUTJ:JITT:SIN1:FREQ 200MHz")
print scs.ask(":OUTJ:JITT:SIN1:FREQ?").strip("\n").strip(" "),
scs.write(":OUTJ:JITT:SIN1:AMPL 0.5UI")
print scs.ask(":OUTJ:JITT:SIN1:AMPL?").strip("\n")

# turn on SJ2 and adjust to 1.2UI at 150MHz
print "SJ2:",
scs.write(":OUTJ:JITT:SIN2 ON")
print scs.ask(":OUTJ:JITT:SIN2?").strip("\n"),
scs.write(":OUTJ:JITT:SIN2:AMPL 0")
print scs.ask(":OUTJ:JITT:SIN2:AMPL?").strip("\n"),
scs.write(":OUTJ:JITT:SIN2:FREQ 150MHz")
print scs.ask(":OUTJ:JITT:SIN2:FREQ?").strip("\n").strip(" "),
scs.write(":OUTJ:JITT:SIN2:AMPL 0.3UI")
print scs.ask(":OUTJ:JITT:SIN2:AMPL?").strip("\n")

# turn on RJ and adjust to 0.1UI
print "RJ:",
```

```
    scs.write(":OUTJ:JITT:RAND ON")
    print scs.ask(":OUTJ:JITT:RAND?").strip("\n"),
    scs.write(":OUTJ:JITT:RAND:AMPL 0.15UI")
    print scs.ask(":OUTJ:JITT:RAND:AMPL?").strip("\n")

# check errors one last time
errchk()
```

The program above generates the following output:

connecting to ASRL31
found SCS16000J serial number 205
error queue: 0, "No error"
setting clock: INT 10313000000 Hz
delayed outputs: ON 1.000V 0.500UI
subrate outputs: ON 1.000V 64
jittered outputs: ON 1.000V
SSC: ON 33000 Hz 5000PPM DOWN
Jitter: OFF OFF OFF OFF
PJ: ON 0.000UI 2400000 Hz 3.645UI OFF
SJ1: ON 0.000UI 200000000 Hz 0.500UI
SJ2: ON 0.000UI 150000000 Hz 0.300UI
RJ: ON 0.150UI-rms
error queue: 0, "No error"

6.13. Programming Tips

Some commands to control the SCS16000/SCS16000J may take a long time to execute completely. These are listed in Table 23.

Table 23: SCS16000/SCS16000J command that should be accompanied by *OPC? or *WAI

Command
:SOURce:FREQuency
:SOURce:FREQuency:CW
:SOURce:FREQuency:PATH
:OUTJitter:JITTer:PERiodic
:OUTJitter:JITTer:PERiodic:AMPLitude
:OUTJitter:JITTer:EXTernal
:OUTJitter:JITTer:EXTernal:LBGain
:OUTDelay:DELay
:SYSTem:PRESet
*RCL

In order to avoid issues when programming with these commands, such as bus timeout, the use of IEEE 488.2 commands *OPC? (Operation Complete Query) or *WAI (Wait to Continue) should be used. For example, a large change to the precision delay (using the :OUTDelay:DELay command) can take many seconds to complete, and the controlling program may want subsequent commands to wait until it has completed before proceeding.

With either solution, the bus timeout needs to be set appropriately. Timing for some SCS commands can be found in Section 6.13.3.

6.13.1. Example using *OPC?

The *OPC? query should be used to synchronize the host computer with the instrument. The *OPC? query does not return until the previous operation has been completed, thus allowing synchronization between the controlling program and instrument. Used in the example below, it causes the controlling program to wait until the delay setting command is complete before attempting to enable the Delayed Clock outputs. If the *OPC? query is not included after commands that may take a while to complete, then commands or queries issued ***after*** those commands may timeout.

```
scs.write(":SOUR:FREQ %.3fGHz" % 10.3125)
opc = scs.ask("*OPC?")
print scs.ask(":SOUR:FREQ?").strip("\n")
```

6.13.2. Example using *WAI

Alternatively, the *WAI command should be used to synchronize commands contained in a single line; it synchronizes the commands inside the instrument. *WAI prevents the instrument from processing further commands or queries until all pending operations are complete. The commands below accomplish the same objective as the previous example. The first command will be executed, the *WAI will delay until the command has been completed, and then the final command will be executed.

```
scs.write(":OUTD:DEL 0.5UI; *WAI; :OUTD:OUTP ON")
```

6.13.3. Communication Timeouts

Most SCPI commands of SCS16000/SCS16000J are processed quickly and return within milliseconds. A few commands require a longer time to take place and process.

The user should use "*OPC?" or "*WAI" after the SCPI command or "*OPC" followed by "*ESR?" for the commands listed in Table 23.

Furthermore, the bus interface timeout needs to be modified to ensure that all commands can complete without triggering the communication timeout for the following cases:

1. **Large delay change**

   Example: Set the delay of the delay outputs from the default state (0 UI) to 1000 UI.

   :OUTD:DEL 1000
   *OPC?

   It will take approximately **17 seconds** to set the delay from 0 UI to 1000 UI or from -1000 UI to 0 UI.

2. **System Preset**

   :SYST:PRES;*WAI

   This command will put the SCS16000J back into the default state. It will take approximately **9 seconds**.

   However, if the System Preset command is issued from a state of the instrument which has very large amount of delay as mentioned above, an additional time needed to set the delay back to 0UI should be added on top of the 9 seconds.

   For example: If the present instrument state has the delay set to 1000 UI. The command ":SYST:PRES;*WAI" will complete after **26 seconds.**

3. **Recall**

*RCL [x]
*OPC?

This command recalls the instrument's state from the register x (x = 1 to 5). It takes less than a second to complete. However, if the recalled state includes a large delay change as mentioned above, an additional time should be added in order to complete the task.

4. **Frequency source setting**

:SOUR:FREQ:PATH [INT|EXT]
*OPC?

A valid external clock should be applied at EXT CLK INPUT of the instrument before switching from internal to external state. If there is no valid external clock input applied, it will take approximately **6 seconds** to complete the switching from External to Internal state.

5. **External Jitter**

A valid external signal should be applied at the EXT JITTER INPUT of the instrument before switching from OFF to LOW or HIGH.

In the case when **no valid external signal is** applied:

a. It will take approximately **15 seconds** to complete the switching from OFF or Highband to Lowband state with command: ":OUTJ:JITT:EXT LOW;*WAI".

b. It will take approximately **5 seconds** to set a Lowband Gain value with command: ":OUTJ:JITT:EXT:LBG xx;*WAI".

c. It will take approximately **6 seconds** to complete to switch from Lowband to Highband state with command: ":OUTJ:JITT:EXT HIGH;*WAI".

6. **Periodic Jitter Amplitude**

Example: Set the amplitude of the periodic jitter to a large value, e.g. 100 UI.

:OUTJ:JITT:PER:AMPL 100
*OPC?

It will take approximately **42 seconds** to set the PJ amplitude from 0 UI to 100 UI at a PJ frequency = 1 Hz and about **18 seconds** at PJ freq = 19 Hz.

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7. Warranty/Product Service

CENTELLAX, Inc. (CENTELLAX) warrants that the test accessory products it manufactures are free from defective material and workmanship for a period of one (1) year subject to the following terms and conditions. CENTELLAX will remedy any such warranted defect subject to the following:

This warranty requires the product to be delivered to CENTELLAX intact for examination with an RMA number and with all transportation charges prepaid to the factory, within one (1) year from the date of sale to the original customer.

CENTELLAX will determine in its sole discretion when such defect exists.

CENTELLAX will return the repaired or replaced product to the customer at its cost unless the shipment needs to be expedited or the shipment is international, in which cases customer will pay for return shipment.

During the warranty period, CENTELLAX will, at its sole option, either repair or replace products which prove to be defective. This warranty does not extend to any CENTELLAX products which have been subject to misuse, neglect, accident, improper installation, or used in violation of operating instructions. This warranty does not extend to products which have been repaired, calibrated, or altered in any way by a facility that is not approved, in writing, by CENTELLAX to perform such work. This warranty does not apply to any product where the seals or serial number thereof has been removed, defaced or changed, nor to products not of our own manufacture.

THIS WARRANTY IS IN LIEU OF ALL OTHER WARRANTIES EXPRESSED OR IMPLIED FOR THE PRODUCTS AND ALL SUCH OTHER WARRANTIES ARE HEREBY EXPRESSLY EXCLUDED. CENTELLAX SPECIFICALLY DISCLAIMS THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

TO THE EXTENT ALLOWED BY LAW, THE REMEDIES PROVIDED HEREIN ARE THE CUSTOMER'S SOLE AND EXCLUSIVE REMEDIES. CENTELLAX SHALL NOT BE LIABLE FOR ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL OR CONSEQUENTIAL DAMAGES, WHETHER BASED ON CONTRACT, TORT OR ANY OTHER LEGAL THEORY.

CENTELLAX reserves the right to modify or change the warranty without notice.

All CENTELLAX trademarks and trade names are the property of CENTELLAX Inc.

Product Service

For information and pricing on standard factory service or yearly calibration service, please contact service@centellax.com.

Centellax, Inc.
3843 Brickway Blvd.
Suite 100
Santa Rosa, CA 95403

Centellax recommends this product be calibrated once a year.

7.1. Returning the SCS16000/SCS16000J to Centellax

If the SCS16000/SCS16000J fails system verification and you cannot correct the problem, return the SCS16000/SCS16000J to Centellax for repair following the steps shown below.

1 Record all symptoms.

2 Contact Centellax using the “Request an RMA” form at http://www.centellax.com/contact/request-rma.

3 Use the original packing material or similar packing material to ship the instrument to Centellax.

8. Appendix A: Preset State

The following settings are the default values after performing an instrument preset:

Table 24. Preset state

Setting	Preset State
Frequency	5 GHz
Clock Source	Internal
10 MHz Reference	Auto
SSC Deviation	5000 ppm
SSC Type	Down
SSC Frequency	33 kHz
SSC Enable	Off
Delay Clock Output Enable	Off
Delay Clock Amplitude	0.700 V
Delay Clock Offset	0 V
Delay Clock Termination	0 V
Delay Clock Coupling	AC
Delay Clock Delay	0.0 UI
Divided Clock Output Enable	Off
Divided Clock Amplitude	0.700 V
Divided Clock Offset	0 V
Divided Clock Termination	0 V
Divided Clock Coupling	AC
Divided Clock Divided	4
Jittered Clock Output Enable	Off
Jittered Clock Amplitude	0.700 V
Jittered Clock Offset	0 V
Jittered Clock Termination	0 V
Jittered Clock Coupling	AC
SJ1 Frequency	10 MHz
SJ1 Amplitude	0.0 UI
SJ1 Enable	Off
SJ2 Frequency	10 MHz

Setting	Preset State
SJ2 Amplitude	0.0 UI
SJ2 Enable	Off
PJ Frequency	100 kHz
PJ Amplitude	0.0 UI
PJ Enable	Off
RJ Amplitude	0 mUI-rms
RJ Enable	Off
External Jitter	Off
LBGain	1.0 UI/V

9. Appendix B: Rack Mounting

Rack mount kits are provided as an accessory. There are 2 rack options to choose from. One is for a single unit and the other is for 2 side-by-side units. If racking the PCB12500 next to the SCS16000/SCS16000J, rack the PCB12500 to the left of the SCS16000/SCS16000J. In either option, the instrument fits in an EIA 19" rack and occupies 2 rack units in height (with the feet removed).

OPTRCK – Single Unit Rack Mount Kit

OPTRCKD – Double Unit Rack Mount Kit

9.1. Installation Instructions for OPTRCK – Single Unit Rack Mount Kit

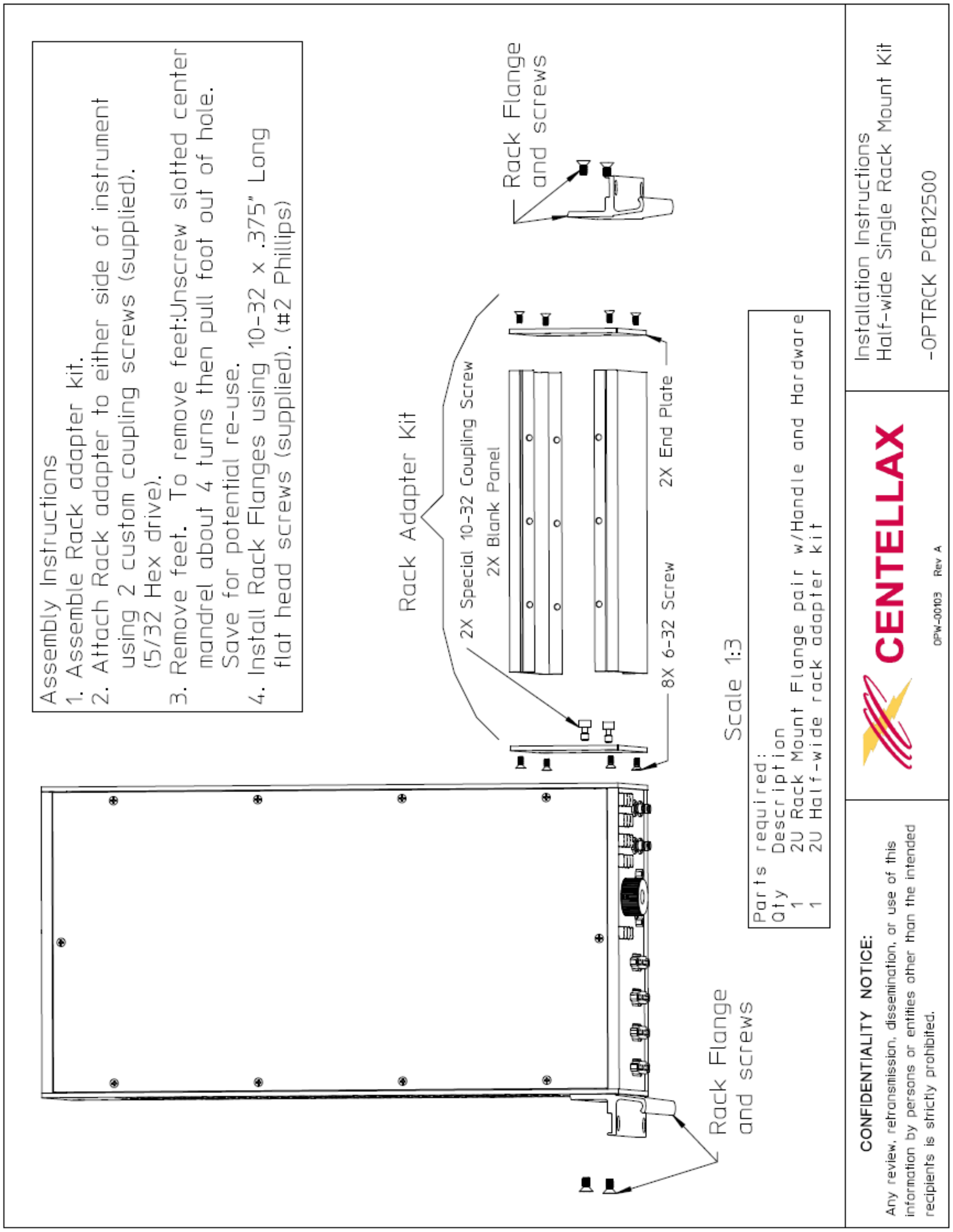

Figure 32. OPTRCK option installation

9.2. Installation Instructions for OPTRCKD – Double Unit Rack Mount Kit

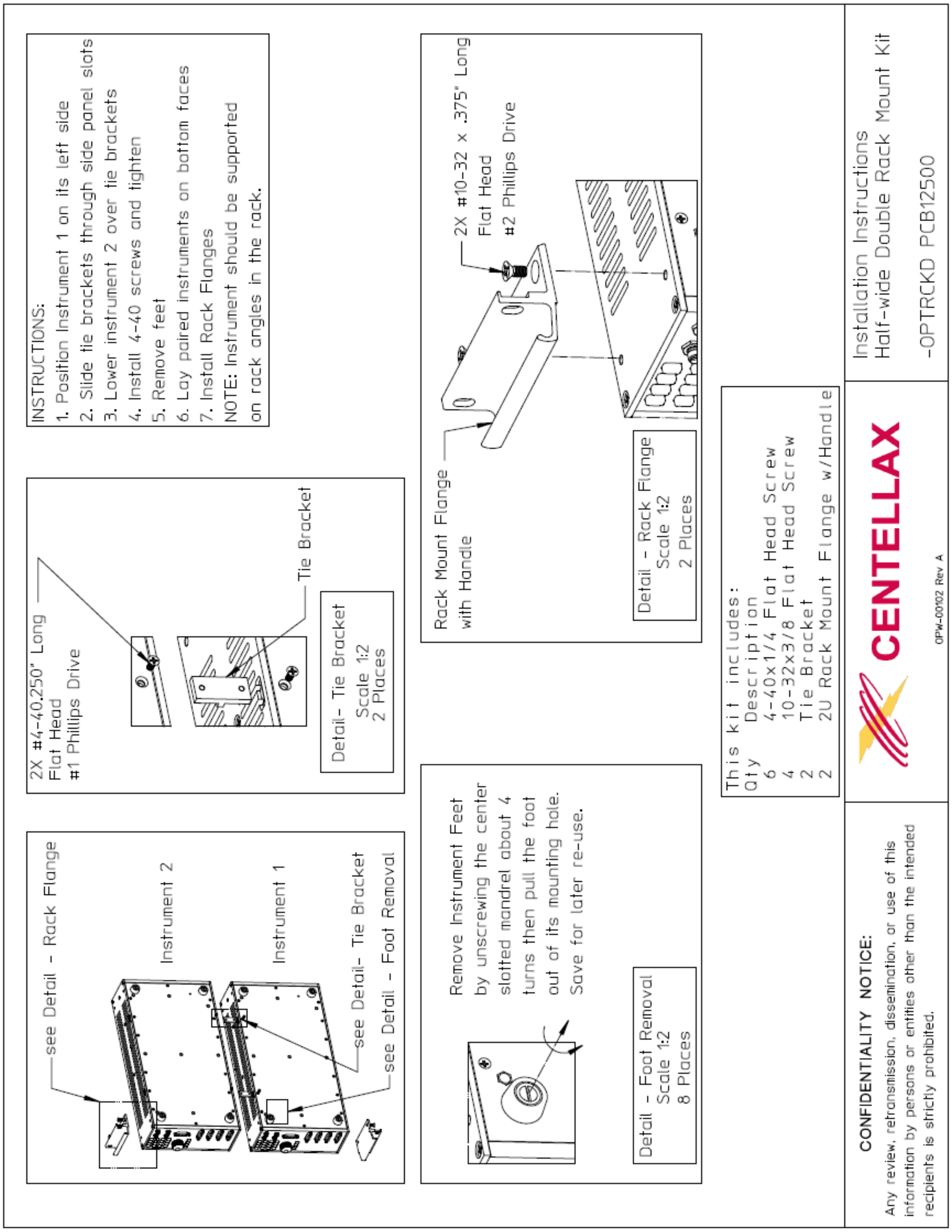

Figure 33. OPTRCKD Option Installation

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