Taehwan Kim

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INTERESTS & EXPERTIES

CMOS integrated circuit/VLSI design
Micro-architecture design for high-performance & energy-efficient xPUs
System-level study and implementation of multi-domain integrated systems (e.g. electronics-photonics)
Design automation techniques for advanced CMOS technologies
Application of new algorithms to old problems

EDUCATION

University of California, Berkeley *Aug. 2014 to Aug. 2019*

Ph.D. in Electrical Engineering and Computer Sciences (advisor: Vladimir Stojanović)

- Dissertation: Realization of Integrated Coherent LiDAR

Seoul National University *Mar. 2007 to Feb. 2014*

B.S. in Electrical and Computer Engineering & B.A. in Economics (double major)

EMPLOYMENT HISTORY

Senior SOC Design Engineer *Oct. 2021 to present*

Advanced Architecture Development Group, Intel Corporation, Hillsboro, OR

- Frontend micro-architecture design engineer for future high-performance x86 core product
  - Own the definition, tech readiness study, RTL development, power modeling, and documentation of fundamental building blocks & advanced power/performance features with the emphasis on the branch prediction unit
  - Collaborate with microprocessor architects to close realism gaps between architecture-level models versus RTL and come up with implementation-ready designs while meeting the power and performance goals
  - Collaborate with the verification team for the planning and execution of pre-silicon validation (e.g. test content development/failure analysis, behavioral modeling, coverage analysis, formal verification, etc.)
  - Collaborate with the physical design team to review static timing analysis results and optimize the RTL and floorplan to ensure timing convergence and meet power, performance, and area targets in leading-edge process nodes

Staff Research Scientist *Sep. 2019 to Oct. 2021*

PHY Research Lab, Intel Labs, Hillsboro, OR

- Research and development of silicon photonics-based energy efficient optical I/O (OIO) PHY with ultrahigh bandwidth density for future xPUs
  - Enabled photonics behavioral model framework for OIO system study & CMOS-photonics co-design and verification: Captured unique trade-offs in a DWDM system & interactions w/ the serdes/modulation format. Carried out a link-budget study (Ref: Sharma et al., JSSC 2021)
  - Owned problem formulation, system-level modeling, and design of integrated controller to enable in-situ monitor & stabilization mechanism for the microring-based transceiver in various operation scenarios against temperature drift and baseline wander. Delivered the IP subsystem in 28nm CMOS and lab-verified using the CMOS IC co-packaged with silicon photonics IC (Ref: Kim et al., US Patent Application 17/676,542, Li et al., JSSC 2020)
  - Established a lab testing system for photonic devices to ensure correlation between behavioral models vs. actual devices and to demonstrate system-level concepts prior to ASIC prototypes
  - Developed various soft IPs for serdes PHY (pattern gen, BER checker, CDR, EQ adaptation, control register interface) and carried out the physical design, while enabling AMS co-sim flow to verify their interactions to custom circuits.
  - Owned IP-level design, chip-level floorplaning/integration and DB delivery of 3 testchips in 16nm FinFET technology to collect silicon learnings for various OIO system building blocks.
  - Represent the team at multi-team workgroup on future prototyping plans leveraging advanced packaging.
  - Mentored a graduate intern to enable various OIO system-level studies.

- Process-portable analog mixed-signal collateral generation with Berkeley Analog Generator (BAG) for leading-edge nodes
  - Proposed and initiated the collaboration with the business unit to study the use of BAG for efficient physical design generation of AMS IPs with high re-use factor
  - Demonstrated feasibility & significant productivity gain through actual testchips on leading edge nodes. Completed formal tech transfer process
  - Presented a demo session at the internal conference & contributed to the training materials, consulted various BUs for broader adoption

Graduate Technical Intern *May. 2017 to Aug. 2018*

PHY Research Lab, Intel Labs, Hillsboro, OR

- Development and experimental verification of low-complexity polarization de-multiplexing schemes for 2x bandwidth density improvement of intensity-modulated direct-detection (IM-DD) optical communication (Ref: Kim et al., US Patent 11,126,018)

Graduate Student Researcher *Aug. 2014 to Aug. 2019*

Integrated Systems Group, University of California, Berkeley

- Thesis project: Realization of single-chip coherent LiDAR and free-space optical communication links leveraging wafer-scale 3D silicon photonics/CMOS integration technology
  - Comprehensive system and circuit-level trade-off analysis for FMCW LiDAR & free space link applications based on scalable beam-steering system using optical phased array/focal plane array
  - Constructed experimental setup for beam characterization and free-space system demonstration
  - Experimental demonstration of single-chip optical phased array system for solid-state beam-steering. Chip designed & fabricated using 65nm CMOS/300mm photonics 3D-integration platform (Ref: Kim et al., JSSC 2019)
  - Presented first experimental demonstration of fully-integrated coherent LiDAR system (Ref: Bhargava et al., VLSI 2019)
- Novel signal processing techniques for sensing
  - Developed and experimentally demonstrated optimal detection algorithm for long-range FMCW LiDAR operating in the range beyond the coherence distance by exploiting known laser spectral characteristics (Ref: Kim et al., ICASSP/CLEO 2018)
  - Developed and experimentally demonstrated artificial neural network-based framework for multi-dimensional super-resolution single-molecule localization fluorescent microscopy (STORM) (Ref: Kim et al., Nature Communications 2019)
- Model Predictive Control algorithm (MPC) based equalization of high-speed links

  Demonstration of transmitter-only equalization scheme for flexible, energy-efficient equalization of asymmetric high-speed interfaces (memory I/O, switches) (Ref: Kim et al., ASSCC 2016)

Undergraduate Researcher *Jun. 2012 to Feb. 2014*

Mixed-Signal IC and System Group, Seoul National University (Advisor: Jaeha Kim)

- Verification techniques for analog/mixed-signal circuits
  - Developed an algorithm to verify correctness of start-up behavior of coupled ring oscillators in presence of random variation. Implemented a Python-based tool for the detection of start-up failures in given oscillator design (Ref: Kim et al., ICCAD 2013)

PUBLICATIONS

S. Daneshgar, H. Li, **T. Kim**, G. Balamurugan, "A 128 Gb/s, 11.2 mW Single-Ended PAM4 Linear TIA With 2.7 μA_{rms} Input Noise in 22 nm FinFET CMOS," *IEEE Journal of Solid-State Circuits (JSSC)*, 2022.

J. Sharma, Z. Xuan, H. Li, **T. Kim**, R. Kumar, M. N. Sakib, C.-M. Hsu, C. Ma, H. Rong, G. Balamurugan, J. Jaussi, "Silicon Photonic Microring-Based 4 x 112 Gb/s WDM Transmitter With Photocurrent-Based Thermal Control in 28-nm CMOS," *IEEE Journal of Solid-State Circuits (JSSC)*, 2021.

T. Kim, C. Levy, M. Weiss, K. M. Nguyen, H. Fu, "Berkeley Analog Generator (BAG)–Efficient Analog Layout Generation and Process Migration," *Intel Design & Test Technology Conference (DTTC)*, 2021.

S. Daneshgar, H. Li, **T. Kim**, G. Balamurugan, "A 128 Gb/s PAM4 Linear TIA with 12.6 pA/$\sqrt{\text{Hz}}$ Noise Density in 22nm FinFET CMOS," *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2021.

H. Li, G. Balamurugan, **T. Kim**, M. N. Sakib, R. Kumar, H. Rong, J. Jaussi, B. Casper, "A 3-D-Integrated

Silicon Photonic Microring-Based 112-Gb/s PAM-4 Transmitter With Nonlinear Equalization and Thermal Control," *IEEE Journal of Solid-State Circuits (JSSC)*, 2020.

T. Kim, "Realization of Integrated Coherent LiDAR," *Ph. D. Thesis*, 2019.

T. Kim*, P. Bhargava*, C. V. Poulton*, J. Notaros, A. Yaacobi, E. Timurdogan, C. Baiocco, N. Fahrenkopf, S. Kruger, T. Ngai, Y. Timalsina, M. R. Watts, V. Stojanović, "A Single-Chip Optical Phased Array in a Wafer-Scale Silicon Photonics/CMOS 3D-Integration Platform," *IEEE Journal of Solid-State Circuits (JSSC)*, 2019. (*co-first authors)

T. Kim*, S. Moon*, K. Xu, "Information-Rich Localization Microscopy through Machine Learning," *Nature Communications*, 2019. (*co-first authors)

P. Bhargava*, **T. Kim***, C. V. Poulton*, J. Notaros, A. Yaacobi, E. Timurdogan, C. Baiocco, N. Fahrenkopf, S. Kruger, T. Ngai, Y. Timalsina, M. R. Watts, V. Stojanović, "Fully Integrated Coherent LiDAR in 3D-Integrated Silicon Photonics/65nm CMOS," *IEEE Symposium on VLSI Circuits*, 2019. (*co-first authors)

T. Kim, P. Bhargava, C. V. Poulton, J. Notaros, A. Yaacobi, E. Timurdogan, C. Baiocco, N. Fahrenkopf, S. Kruger, T. Ngai, Y. Timalsina, M. R. Watts, V. Stojanović, "A Single-Chip Optical Phased Array in a 3D-Integrated Silicon Photonics/65nm CMOS Technology," *IEEE International Solid-State Circuits Conference (ISSCC)*, 2019.

T. Kim, P. Bhargava, V. Stojanović, "Overcoming the Coherence Distance Barrier in Long-Range FMCW LIDAR," *Conference on Lasers and Electro-Optics (CLEO)*, 2018.

T. Kim, P. Bhargava, V. Stojanović, "Optimal Spectral Estimation and System Trade-Off in Long-Distance Frequency-Modulated Continuous-Wave LIDAR," *IEEE International Conference on Acoustics, Speech, and Signal Processing (ICASSP)*, 2018.

T. Kim, P. Bhargava, V. Stojanović, "A Model Predictive Control Equalization Transmitter for Asymmetric Interfaces in 28nm FDSOI, *IEEE Asian Solid-State Circuits Conference (ASSCC)*, 2016.

T. Kim, D.-G. Song, S. Youn, J. Park, H. Park, and J. Kim, "Verifying Start-Up Failures in Coupled Ring Oscillators in Presence of Variability Using Predictive Global Optimization," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, 2013.

J. Kim, J. Lee, D.-G. Song, **T. Kim**, K.-H. Kim, S. Jung, and S. Youn, "Discretization and Discrimination Methods for Design, Verification, and Testing of Analog/Mixed Signal Circuits," *Custom Integrated Circuits Conference (CICC)*, 2013.

PATENTS

T. Kim, H. LI, M. N. Sakib, H. Rong, G. Balamurugan, S. Gupta, J. Hong, N. Fediakine, "Ring Modulator Baseline Wander Compensation," US Patent Application 17/676,542.
D. Huang, S. Fathololoumi, M. N. Sakib, M. M. Najafabadi, C. Ma, D. Hui, **T. Kim**, L. Liao, H. Li, G. Balamurugan, H. Rong, A. Eftekhar, "Photonic wavelength division multiplexing (wdm) receiver with polarization diversity and/or low reflectance," US Patent Application 17/133,347.
T. Kim, G. Balamurugan, H. Li, H. Jayatilleka, "Polarization De-Multiplexing for Intensity-Modulated Direct-Detection (IM-DD) Optical Communications," US Patent 11,126,018.

HONORS & AWARDS

Intel Labs, Architecture & Design Research, Department Recognition Award	*2021*
Kwanjeong Scholarship for Abroad Studies	*2014-2019*
National Scholarship for Science and Engineering, Korea Science Foundation	*2007-2013*

TEACHING

Introduction to Digital Design and Integrated Circuits (EECS151/251A)	*Spring 2018*
Designing Information Devices and Systems I (EE16A)	*Spring 2019*

SKILLS

Deep experience in ASIC/VLSI tools, flows, and methods from high-level design to GDS delivery (both digital and analog/mixed-signal) in the context of research prototyping as well as product execution from a number of tapeout experiences
Verilog/SystemVerilog, Verilog-AMS, C/C++, Python, tcl, UNIX scripting, MATLAB, Simulink
Experience in research using Tensorflow (Ref: Kim et al., Nat. Comm., 2019)

MISC.

US permanent resident