Taehwan Kim

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RESEARCH INTERESTS

Electronic-photonic integrated systems for free-space communication/sensing
Novel reconstruction algorithms for sensing systems
Analog/mixed-signal integrated circuit design, high-performing/efficient IO technology

EDUCATION

University of California, Berkeley *Aug. 2014 to Present*
Ph.D. Student in Electrical Engineering and Computer Sciences

Seoul National University *Mar. 2007 to Feb. 2014*
B.S. in Electrical and Computer Engineering
B.A. in Economics (Double Major)

RESEARCH EXPERIENCE

Graduate Technical Intern *May. 2017 to present*
PHY Research Lab, Intel Labs, Santa Clara, CA

- Advanced system-level techniques for integrated optical links
  - US patent filed

Graduate Student Researcher *Aug. 2014 to present*
Integrated Systems Group, University of California, Berkeley (Advisor: Vladimir Stojanović)

- Free-space optical systems in electronic-photonic integration platform
  - Goal: realization of an integrated solution for ultra high-resolution FMCW LIDAR and free-space optical communication links leveraging silicon photonics technology
  - Developing system and circuit-level techniques for 1) laser modulation/synchronization (optical PLL for FMCW modulation/multi-laser synchronization) 2) scalable beam-steering system 3) FMCW detection algorithms for coherence distance limited systems
  - Various system-level budget analysis for LIDAR/communication applications
  - First tape-out done in early 2016 in 65nm 10LPe CMOS/300mm photonics 3D-integration platform
  - Optical PLL tape-out done in 2017 in 45nm SOI
- Model Predictive Control algorithm (MPC) based equalization of high-speed links
  - Demonstration of TX-side equalization scheme based on channel models for flexible, energy-efficient equalization of asymmetric high-speed interfaces (e.g. processor-memory, switches)
  - Built/measured chips in 28nm FDSOI & 45nm SOI, paper accepted

Undergraduate Researcher *Jun. 2012 to Feb. 2014*
Mixed-Signal IC and System Group, Seoul National University (Advisor: Jaeha Kim)

- Formal verification of analog/mixed-signal circuits
  - Developed an algorithm to verify correctness of start-up behavior of ring oscillators in presence of variability
  - Implemented GCHECK: a Python-based tool for detection of start-up failures of coupled ring oscillators (transferred to Samsung Electronics, patent issued)
- Variability-aware circuit optimization
  - Developed global optimizer for analog/mixed-signal circuits based on statistical metamodeling

PUBLICATIONS

T. Kim, P. Bhargava, V. Stojanović, "Overcoming the Coherence Distance Barrier in Long-Range FMCW LIDAR," *Conference on Lasers and Electro-Optics (CLEO)*, 2018.

T. Kim, P. Bhargava, V. Stojanović, "Optimal Spectral Estimation and System Trade-Off in Long-Distance Frequency-Modulated Continuous-Wave LIDAR," *IEEE International Conference on Acoustics, Speech, and Signal Processing (ICASSP)*, 2018.

T. Kim, P. Bhargava, V. Stojanović, "A Model Predictive Control Equalization Transmitter for Asymmetric Interfaces in 28nm FDSOI, *IEEE Asian Solid-State Circuits Conference (ASSCC)*, 2016.

T. Kim, D.-G. Song, S. Youn, J. Park, H. Park, and J. Kim, "Verifying Start-Up Failures in Coupled Ring Oscillators in Presence of Variability Using Predictive Global Optimization," *IEEE/ACM International*

Conference on Computer-Aided Design (ICCAD), 2013.

J. Kim, J. Lee, D.-G. Song, **T. Kim**, K.-H. Kim, S. Jung, and S. Youn, "Discretization and Discrimination Methods for Design, Verification, and Testing of Analog/Mixed Signal Circuits," *Custom Integrated Circuits Conference (CICC)*, 2013.

HONORS & AWARDS

Kwanjeong Scholarship for Abroad Studies *2014-2018*

National Scholarship for Science and Engineering, Korea Science Foundation *2007-2013*

SKILLS

Languages: C, C++, Python, Verilog, Verilog-A

Tools: Custom IP block and VLSI design/verification tools (Virtuoso, ADS, DC, ICC, RC, SOC-ENC, Calibre), MATLAB