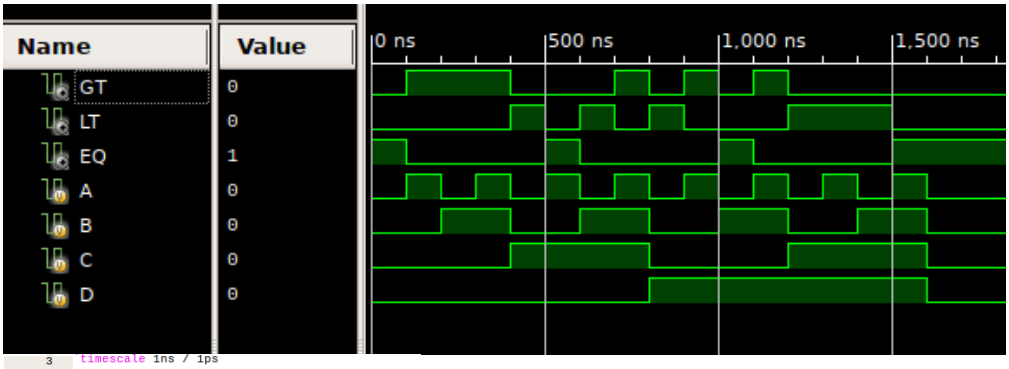
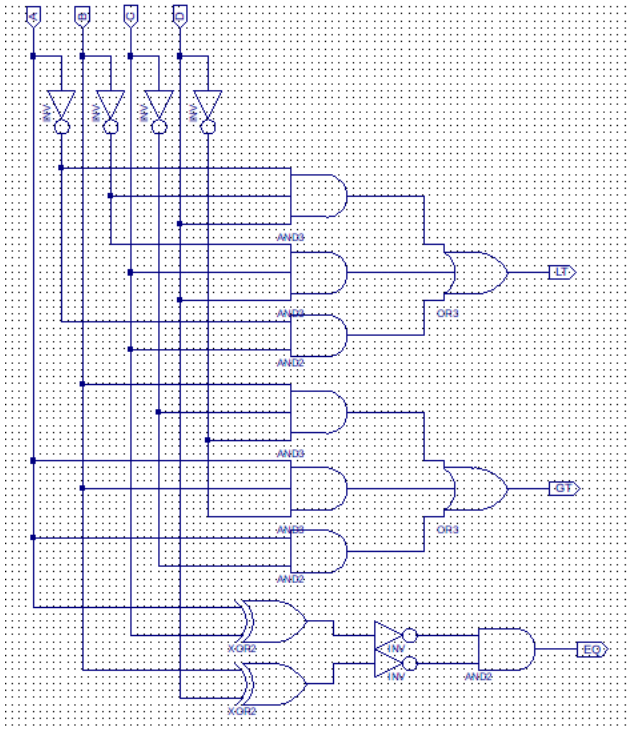
LDLAB_220329_002_TEAM20_TAEHYUN YANG_2021-14284

1. Team Work

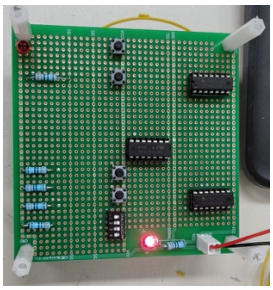
Lab Results



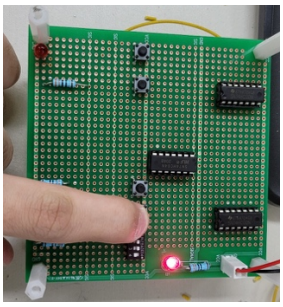

```
3   `timescale 1ns / 1ps
4
5   module comparator_comparator_sch_tb();
6
7   // Inputs
8      reg A;
9      reg B;
10     reg C;
11     reg D;
12
13  // Output
14     wire GT;
15     wire LT;
16     wire EQ;
17
18  // Bidirs
19
20  integer i;
21
22  // Instantiate the UUT
23     comparator UUT (
24        .GT(GT),
25        .LT(LT),
26        .EQ(EQ),
27        .A(A),
28        .B(B),
29        .C(C),
30        .D(D)
31     );
32  // Initialize Inputs
33     initial begin
34        for(i = 0; i<16; i=i+1) begin
35        A = i&1;
36        B = (i&2) >> 1;
37        C = (i&4) >> 2;
38        D = (i&8) >> 3;
39        #100;
40        end
41
42        A = 0;
43        B = 0;
44        C = 0;
45        D = 0;
46
47     end
48  endmodule
49
```



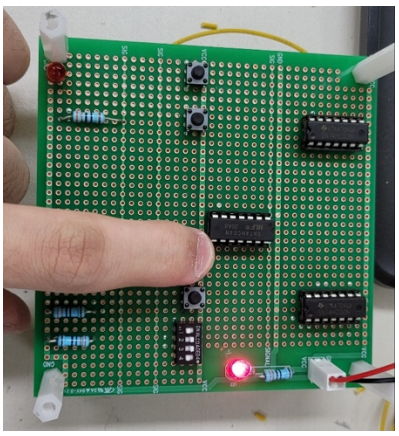
Input:0000 Output: 0



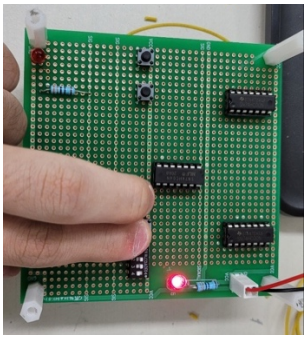
Input:0001 Output: 0



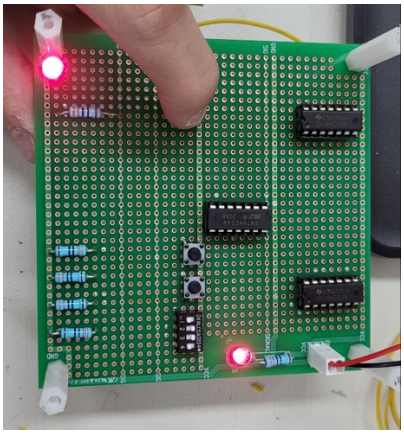
Input:0010 Output: 0



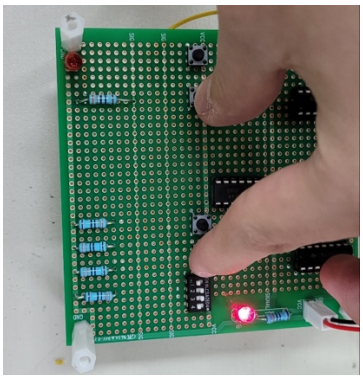
Input:0011 Output: 0



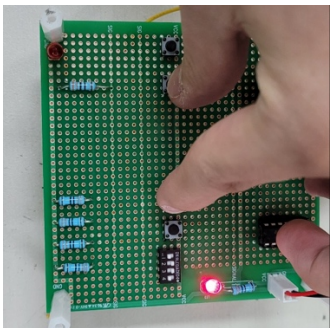
Input:0100 Output: 1



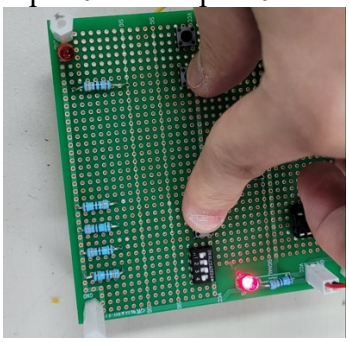
Input:0101 Output: 1



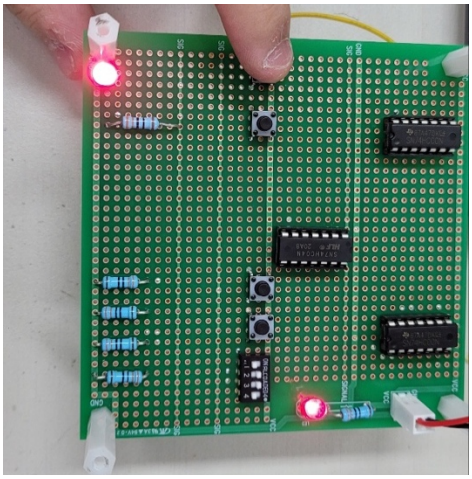
Input:0110 Output: 0



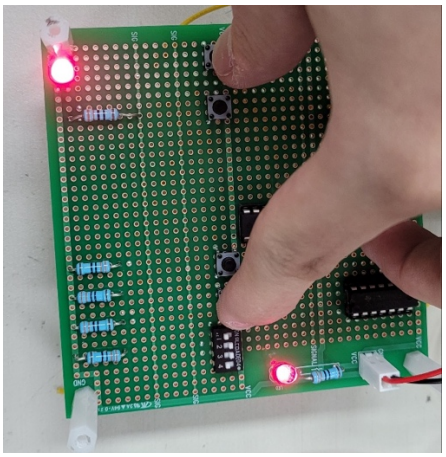
Input:0111 Output: 0



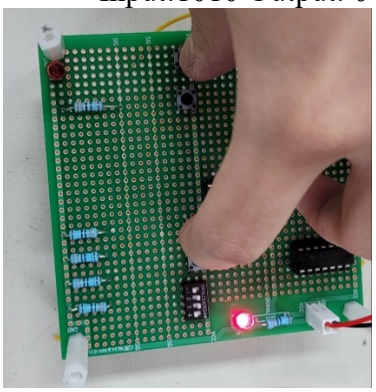
Input:1000 Output: 1



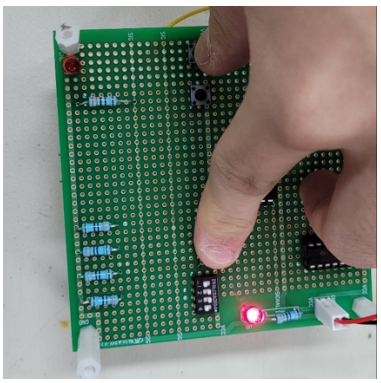
Input:1001 Output: 1



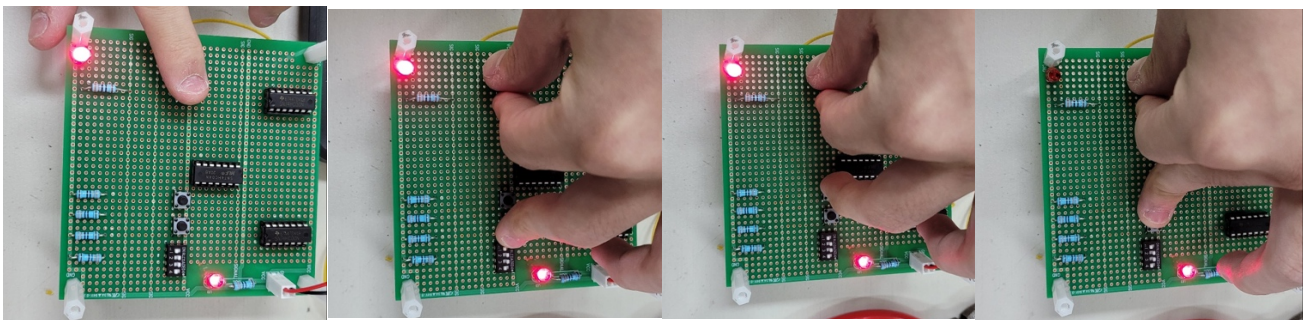
Input:1010 Output: 0



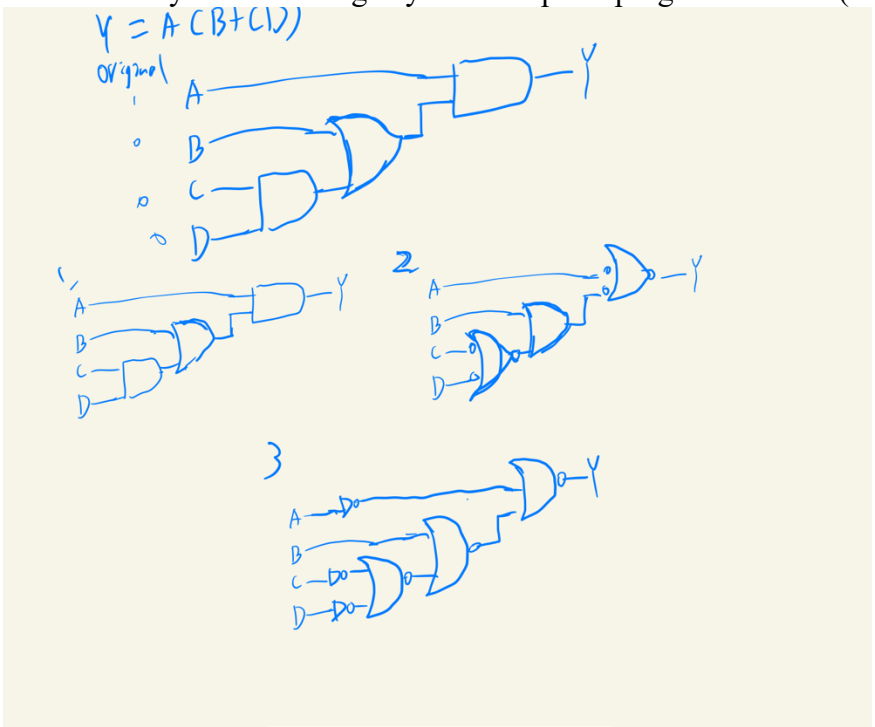
Input:1011 Output: 0



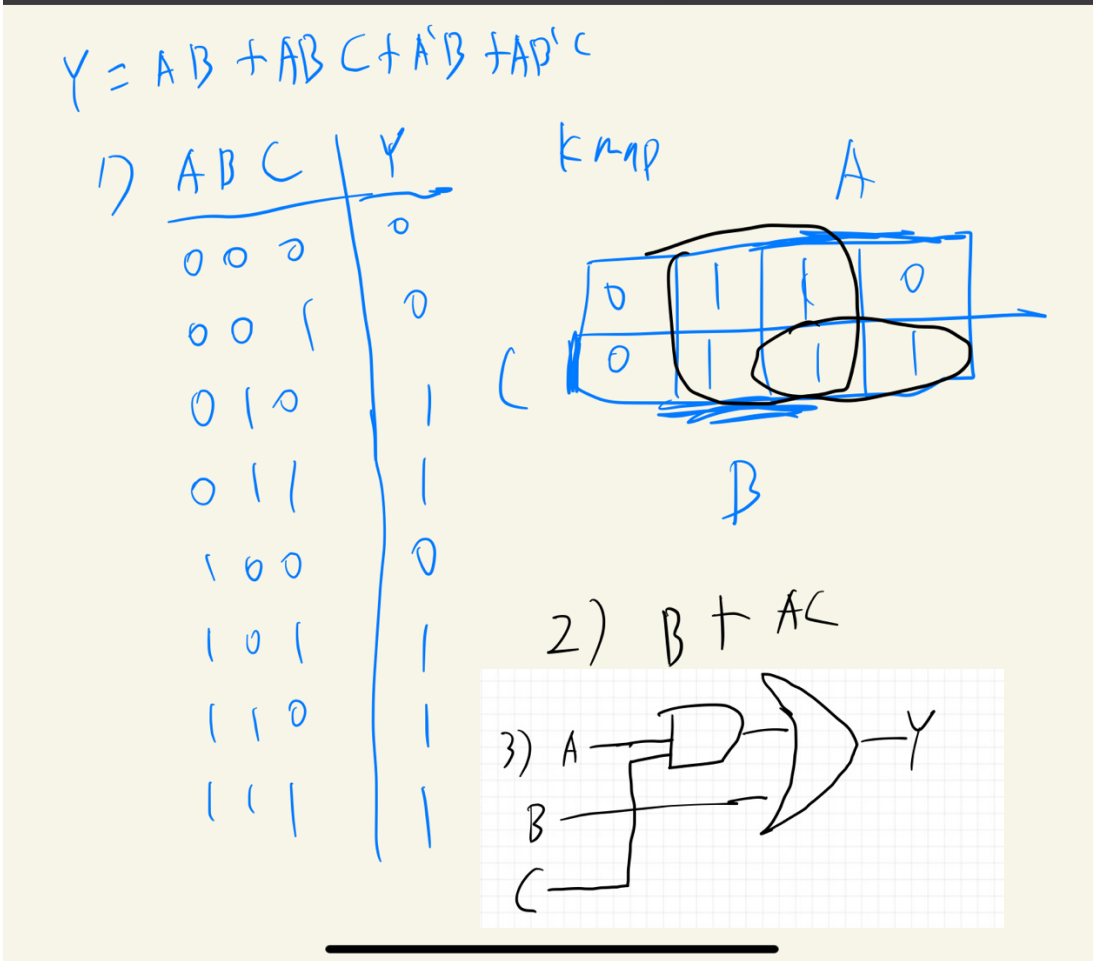
Input:1100 Output: 1 Input:1101 Output: 1 Input:1110 Output: 1 Input:1111 Output: 0



2. [Individual] Draw a circuit diagram for the below formula using ONLY NOR and NOT gates. You can draw it by hand or using any of a computer program. - Y = A(B+CD)

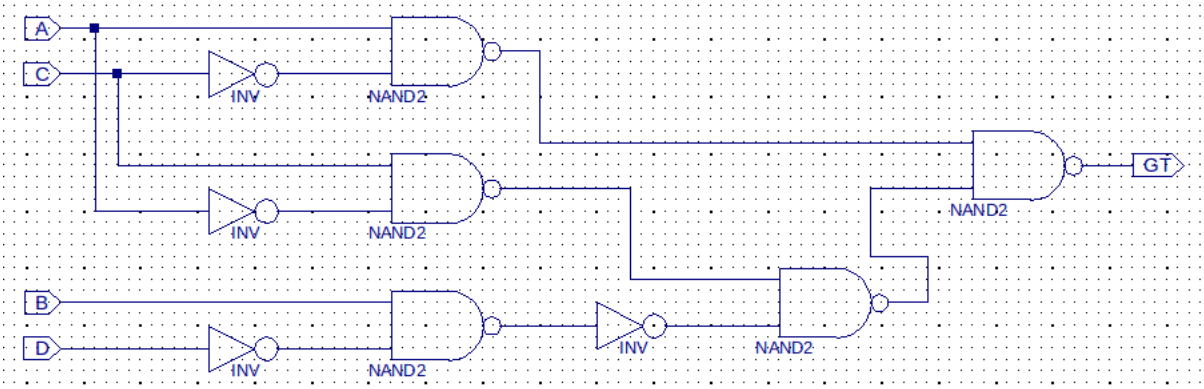


3. [Individual] Y = AB + ABC + A'B + AB'C (1) Make a truth table (2) Minimize # of operators (3) Draw a circuit diagram



4. How can we reduce more costs in GT circuit on a universal board? (Optional) - This question is for discussion. (If you don't have any discussion, think about this)

We actually did reduce costs by changing the schematic:



Instead of using 3 input AND gates and 3 input OR gates, we actually optimized the schematic so that we only need NAND and NOT gates. We did so by using two level logic complemented inputs, changing AND gates to NORS and applying inverse gates to OR gates. Doing so, we only had to use 1 7404 Gates and 2 7400 Gates because we needed 4 NOT gates and 5 2 input NOR Gates. However, our switch input was constantly shorted and didn't seem to work, therefore we replaced them with push switches. Although we used different gates, we didn't change the overall logic, therefore the GT function still worked.