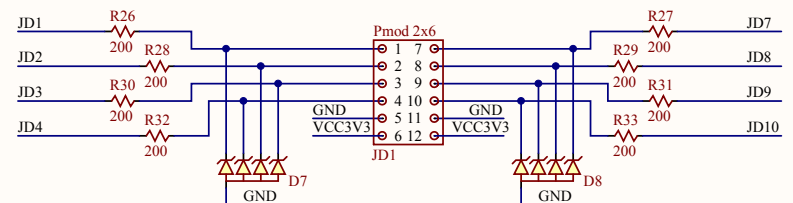
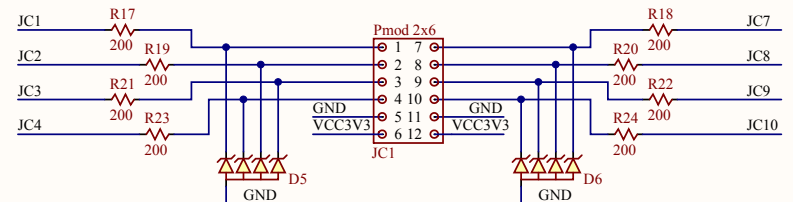
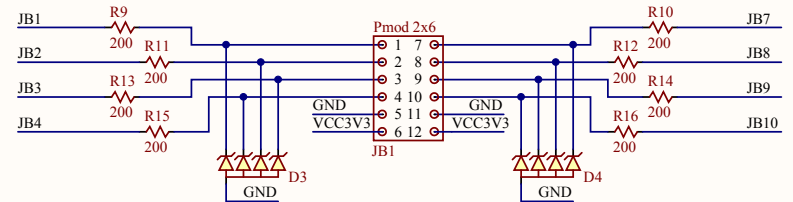
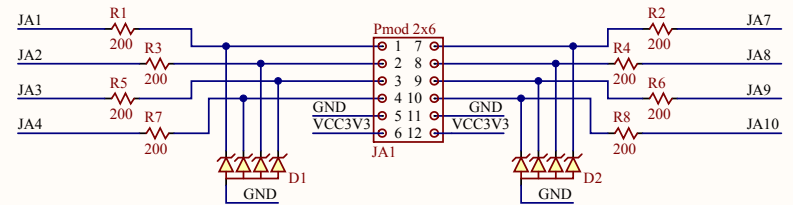
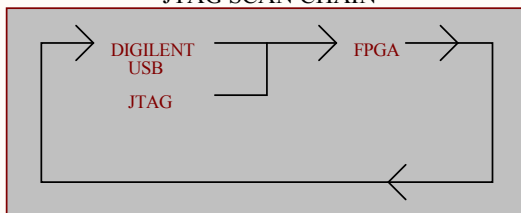
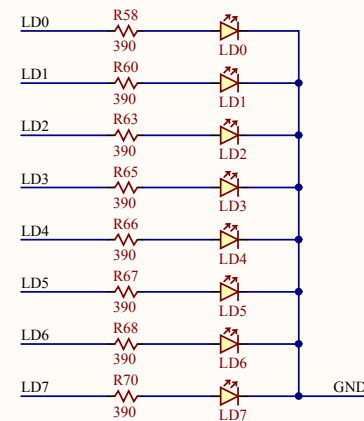
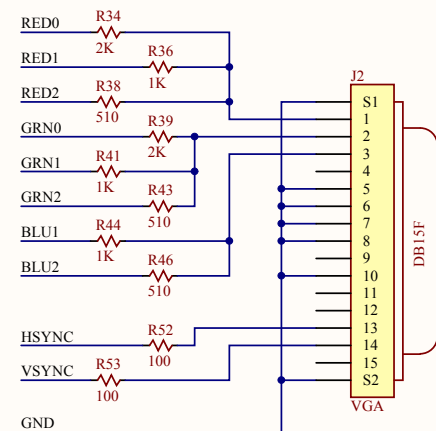
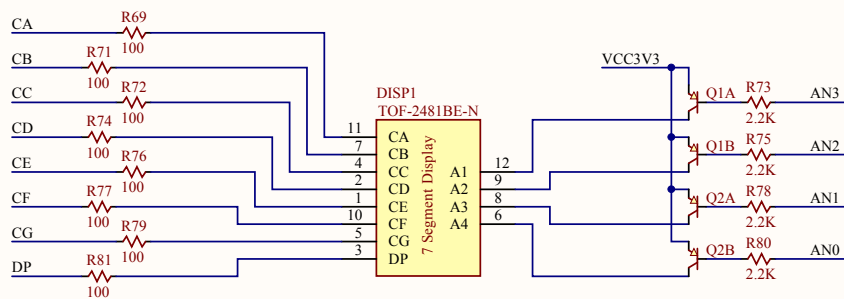
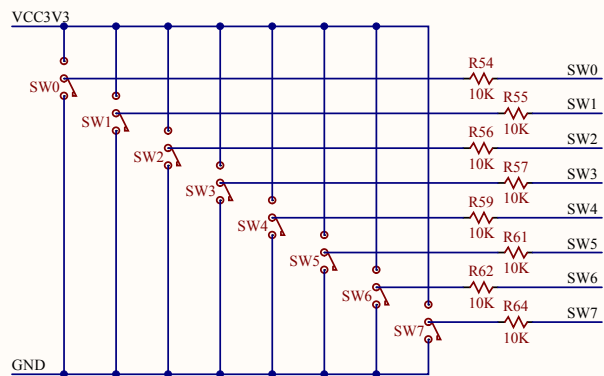
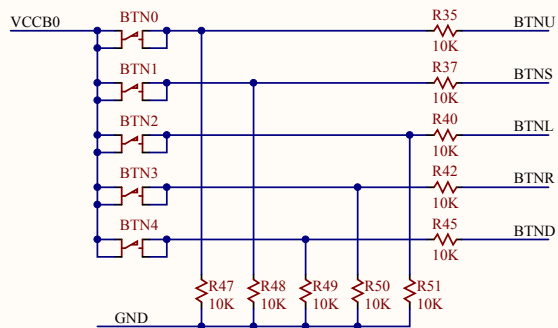


### JTAG SCAN CHAIN

Foot  
F1  
Foot  
F2  
Foot  
F3  
Foot  
F4



Title <b>Nexys III</b>		Rev <b>B.0</b> Copyright 2011
Circuit Expansion Header and IO		
Doc# 500-182		
Engineer CC		
Author GMA		
Date 2/17/2011		
Sheet# 1 out of 10		

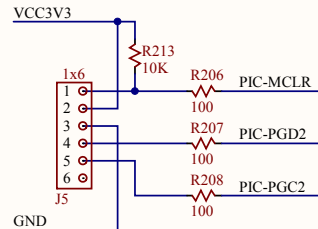
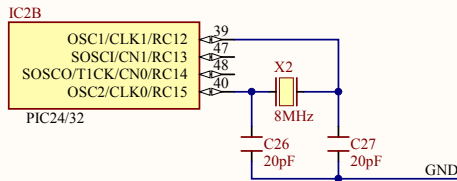
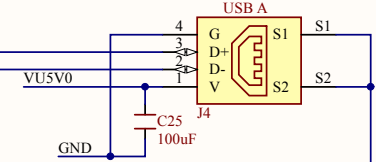
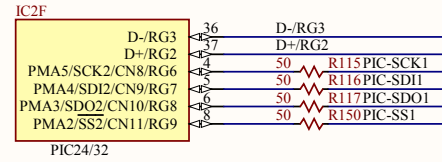
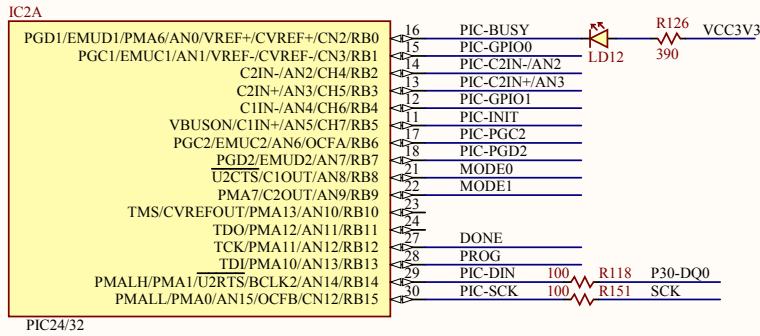


Title <b>Nexys III</b>		Rev <b>B.0</b> Copyright 2011
Circuit General IO		
Doc# 500-182		
Engineer CC		
Author GMA		
Date 2/17/2011		
Sheet# 2 out of 10		

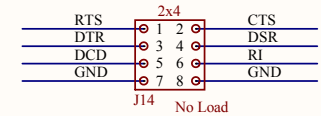
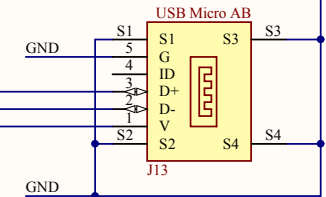
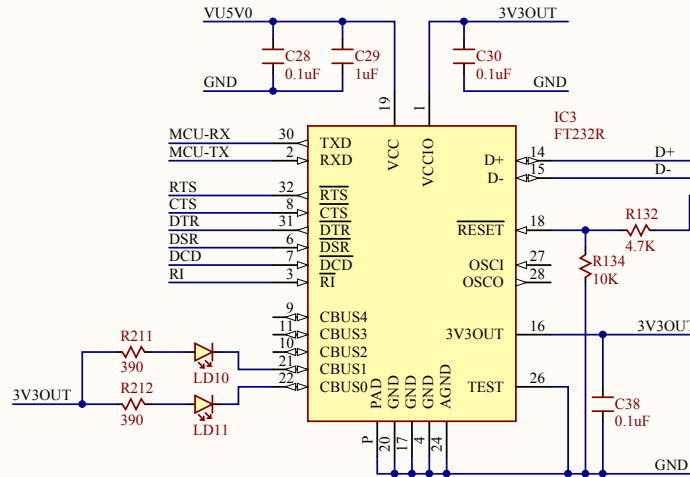
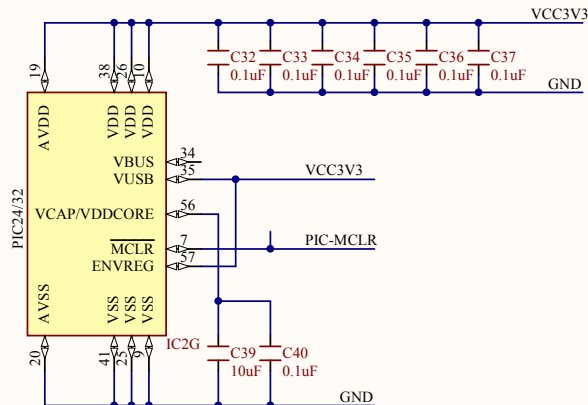
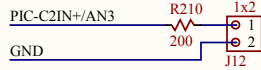
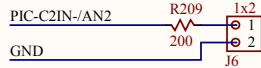



**DIGILENT**  
BEYOND THEORY

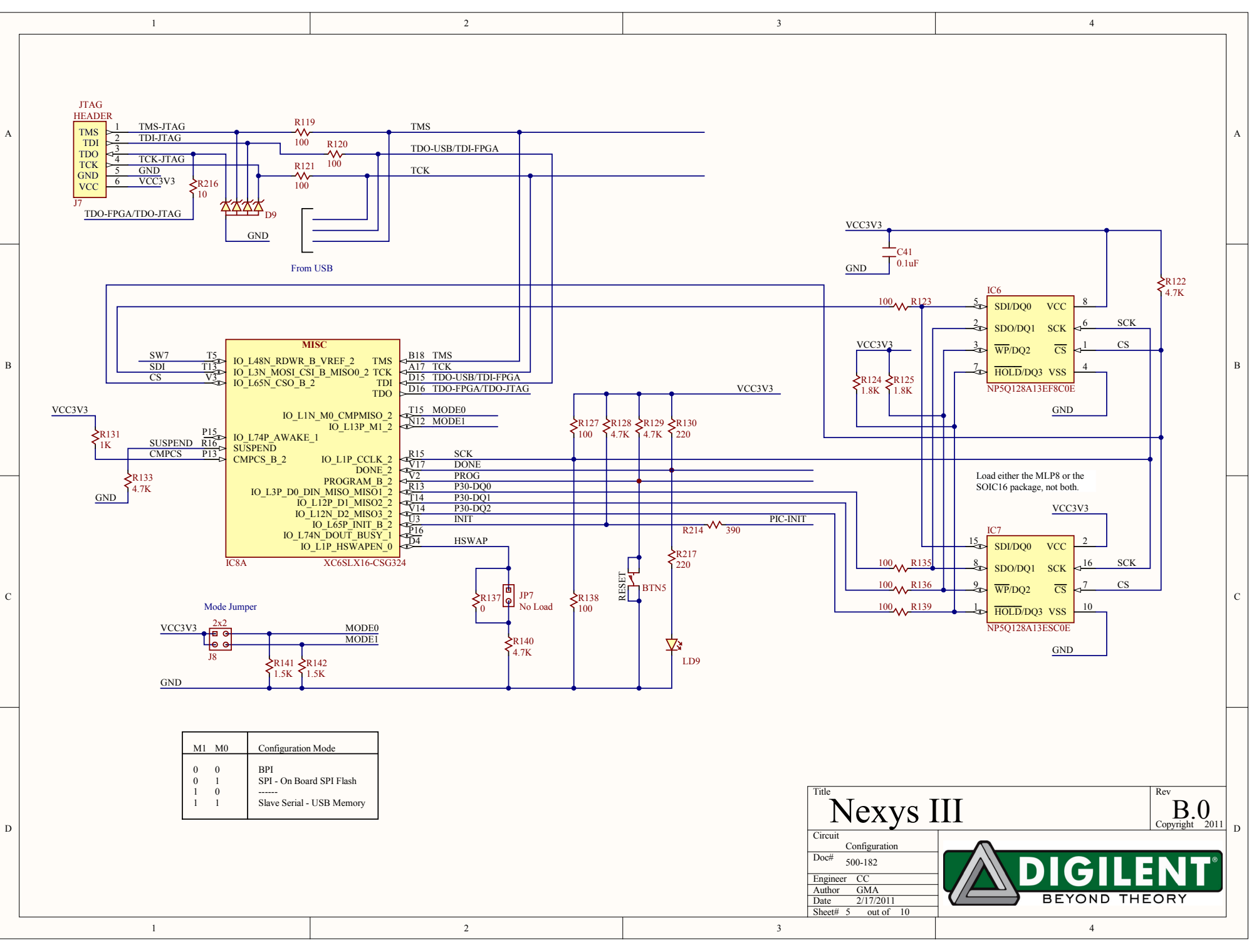




#### ANALOG HEADERS



Title <b>Nexys III</b>		Rev <b>B.0</b> Copyright 2011
Circuit USB Host		
Doc# 500-182		
Engineer CC		
Author GMA		
Date 2/17/2011		
Sheet# 4 out of 10		



M1	M0	Configuration Mode
0	0	BPI
0	1	SPI - On Board SPI Flash
1	0	-----
1	1	Slave Serial - USB Memory

Title

Nexys III

Rev

B.0

Copyright

2011

Circuit

Configuration

Doc#

500-182

Engineer

CC

Author


GMA

Date

2/17/2011

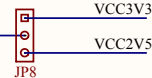
Sheet#

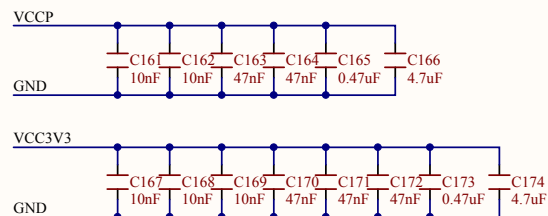
5 out of 10




**DIGILENT**  
BEYOND THEORY



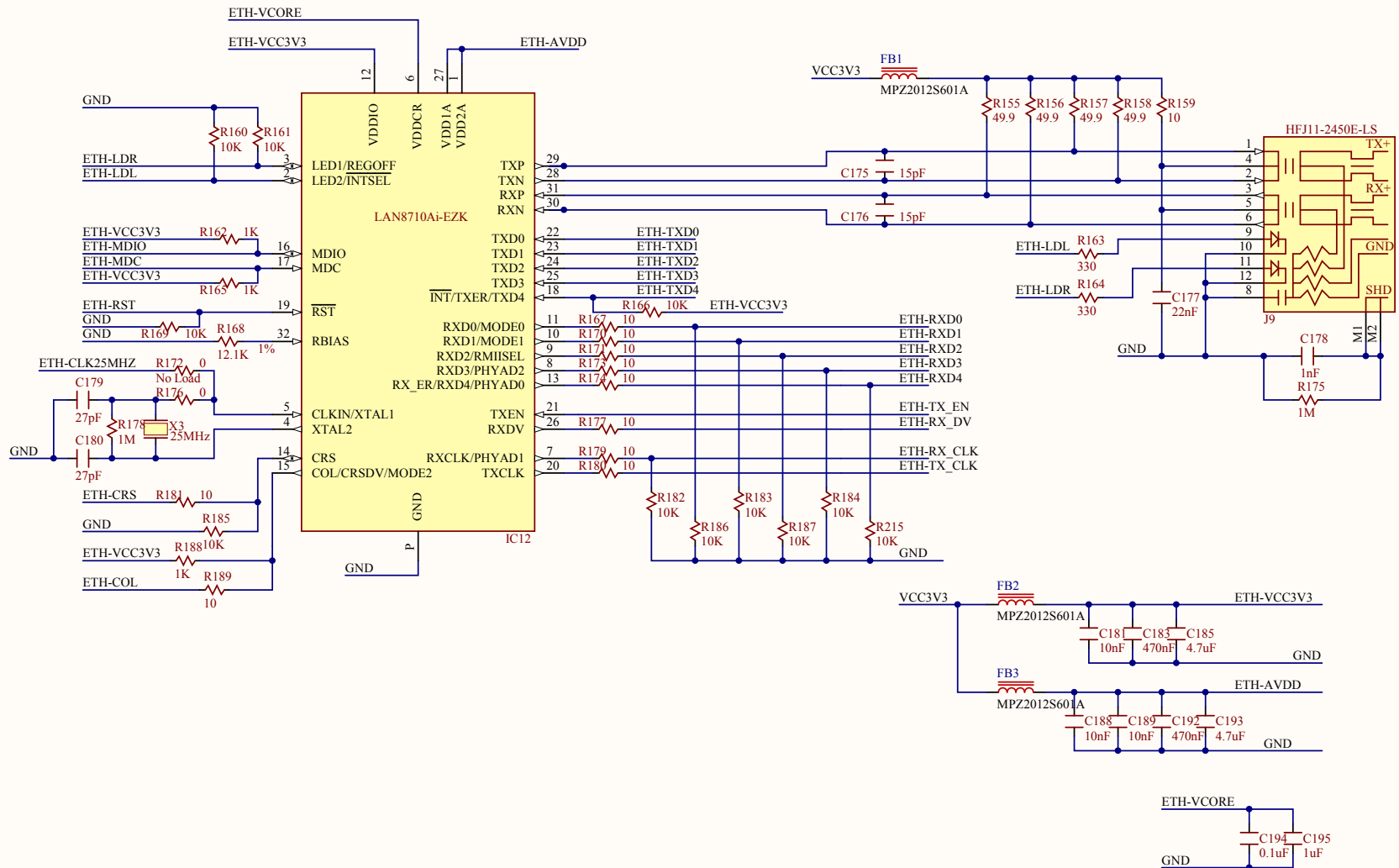



[illegible]

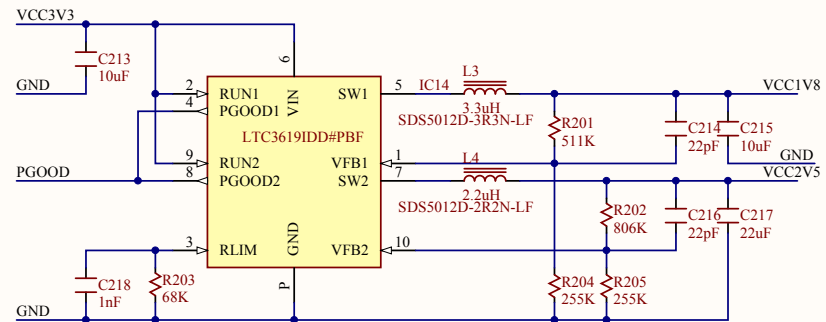
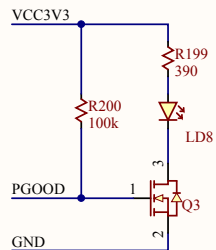
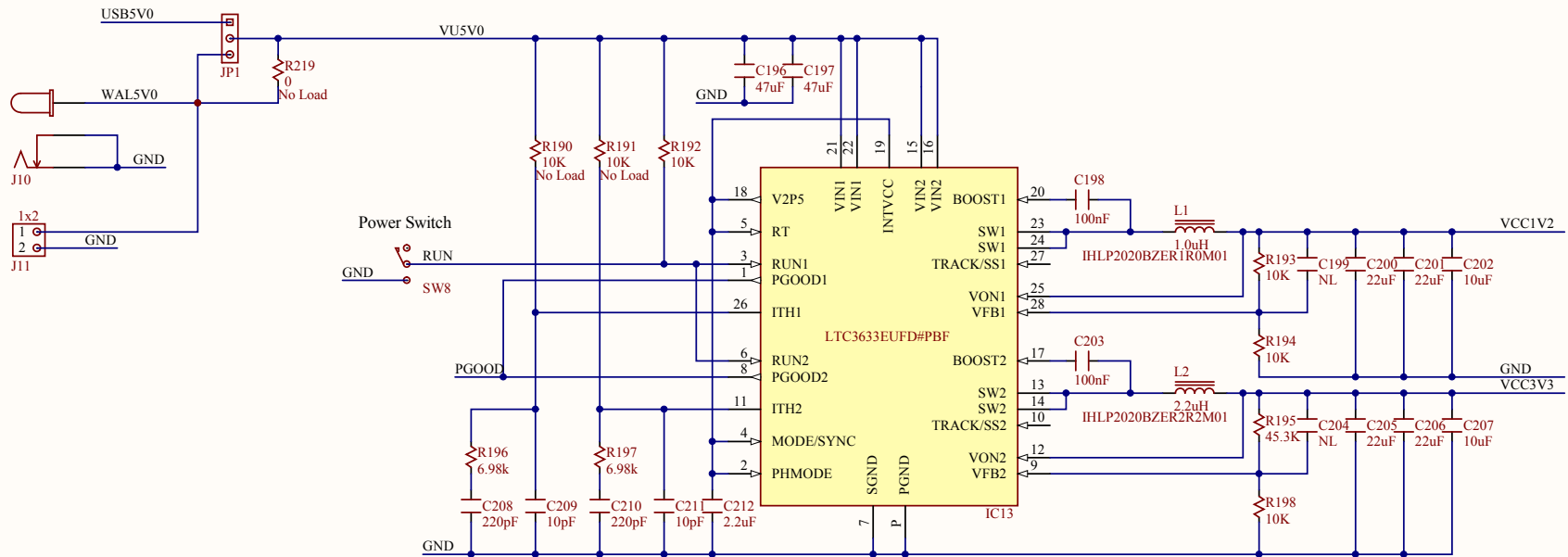
Title <b>Nexys III</b>		Rev <b>B.0</b> Copyright 2011
Circuit	Memory	
Doc#	500-182	
Engineer	CC	
Author	GMA	
Date	2/17/2011	
Sheet#	8 out of 10	



## ETHERNET



Title <b>Nexys III</b>		Rev <b>B.0</b> Copyright 2011
Circuit Ethernet		
Doc# 500-182		
Engineer CC		
Author GMA		
Date 2/17/2011		
Sheet# 9 out of 10		



Title		Rev	
Nexys III		B.0	
Circuit		Copyright 2011	
Power			
Doc#			
500-182			
Engineer			
CC			
Author			
GMA			
Date			
2/17/2011			
Sheet#			
10 out of 10			

