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1  /*
2  * system.h - SOPC Builder system and BSP software package information
3  *
4  * Machine generated for CPU 'nios' in SOPC Builder design 'sopc_scope_sys'
5  * SOPC Builder design path: C:/Users/tago/Dropbox/OUT/EE52/quartus/sopc_scope_sys.sopcinfo
6  *
7  * Generated: Wed Jun 11 15:26:36 PDT 2014
8  */
9
10 /*
11 * DO NOT MODIFY THIS FILE
12 *
13 * Changing this file will have subtle consequences
14 * which will almost certainly lead to a nonfunctioning
15 * system. If you do modify this file, be aware that your
16 * changes will be overwritten and lost when this file
17 * is generated again.
18 *
19 * DO NOT MODIFY THIS FILE
20 */
21
22 /*
23 * License Agreement
24 *
25 * Copyright (c) 2008
26 * Altera Corporation, San Jose, California, USA.
27 * All rights reserved.
28 *
29 * Permission is hereby granted, free of charge, to any person obtaining a
30 * copy of this software and associated documentation files (the "Software"),
31 * to deal in the Software without restriction, including without limitation
32 * the rights to use, copy, modify, merge, publish, distribute, sublicense,
33 * and/or sell copies of the Software, and to permit persons to whom the
34 * Software is furnished to do so, subject to the following conditions:
35 *
36 * The above copyright notice and this permission notice shall be included in
37 * all copies or substantial portions of the Software.
38 *
39 * THE SOFTWARE IS PROVIDED "AS IS", WITHOUT WARRANTY OF ANY KIND, EXPRESS OR
40 * IMPLIED, INCLUDING BUT NOT LIMITED TO THE WARRANTIES OF MERCHANTABILITY,
41 * FITNESS FOR A PARTICULAR PURPOSE AND NONINFRINGEMENT. IN NO EVENT SHALL THE
42 * AUTHORS OR COPYRIGHT HOLDERS BE LIABLE FOR ANY CLAIM, DAMAGES OR OTHER
43 * LIABILITY, WHETHER IN AN ACTION OF CONTRACT, TORT OR OTHERWISE, ARISING
44 * FROM, OUT OF OR IN CONNECTION WITH THE SOFTWARE OR THE USE OR OTHER
45 * DEALINGS IN THE SOFTWARE.
46 *
47 * This agreement shall be governed in all respects by the laws of the State
48 * of California and by the laws of the United States of America.
49 */
50
51 #ifndef __SYSTEM_H_
52 #define __SYSTEM_H_
53
54 /* Include definitions from linker script generator */
55 #include "linker.h"
56
57
58 /*
59 * CPU configuration
60 *
61 */
62
63 #define ALT_CPU_ARCHITECTURE "altera_nios2_qsys"
64 #define ALT_CPU_BIG_ENDIAN 0
65 #define ALT_CPU_BREAK_ADDR 0x00240820
66 #define ALT_CPU_CPU_FREQ 50000000u
67 #define ALT_CPU_CPU_ID_SIZE 1
68 #define ALT_CPU_CPU_ID_VALUE 0x00000000
69 #define ALT_CPU_CPU_IMPLEMENTATION "tiny"
70 #define ALT_CPU_DATA_ADDR_WIDTH 0x16
71 #define ALT_CPU_DCACHE_LINE_SIZE 0
72 #define ALT_CPU_DCACHE_LINE_SIZE_LOG2 0
73 #define ALT_CPU_DCACHE_SIZE 0
74 #define ALT_CPU_EXCEPTION_ADDR 0x00180020
75 #define ALT_CPU_FLUSHDA_SUPPORTED

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76 #define ALT_CPU_FREQ 50000000
77 #define ALT_CPU_HARDWARE_DIVIDE_PRESENT 0
78 #define ALT_CPU_HARDWARE_MULTIPLY_PRESENT 0
79 #define ALT_CPU_HARDWARE_MULX_PRESENT 0
80 #define ALT_CPU_HAS_DEBUG_CORE 1
81 #define ALT_CPU_HAS_DEBUG_STUB
82 #define ALT_CPU_HAS_JMPI_INSTRUCTION
83 #define ALT_CPU_ICACHE_LINE_SIZE 0
84 #define ALT_CPU_ICACHE_LINE_SIZE_LOG2 0
85 #define ALT_CPU_ICACHE_SIZE 0
86 #define ALT_CPU_INST_ADDR_WIDTH 0x16
87 #define ALT_CPU_NAME "nios"
88 #define ALT_CPU_RESET_ADDR 0x00180000
89
90
91 /*
92  * CPU configuration (with legacy prefix - don't use these anymore)
93  *
94  */
95
96 #define NIOS2_BIG_ENDIAN 0
97 #define NIOS2_BREAK_ADDR 0x00240820
98 #define NIOS2_CPU_FREQ 50000000u
99 #define NIOS2_CPU_ID_SIZE 1
100 #define NIOS2_CPU_ID_VALUE 0x00000000
101 #define NIOS2_CPU_IMPLEMENTATION "tiny"
102 #define NIOS2_DATA_ADDR_WIDTH 0x16
103 #define NIOS2_DCACHE_LINE_SIZE 0
104 #define NIOS2_DCACHE_LINE_SIZE_LOG2 0
105 #define NIOS2_DCACHE_SIZE 0
106 #define NIOS2_EXCEPTION_ADDR 0x00180020
107 #define NIOS2_FLUSHDA_SUPPORTED
108 #define NIOS2_HARDWARE_DIVIDE_PRESENT 0
109 #define NIOS2_HARDWARE_MULTIPLY_PRESENT 0
110 #define NIOS2_HARDWARE_MULX_PRESENT 0
111 #define NIOS2_HAS_DEBUG_CORE 1
112 #define NIOS2_HAS_DEBUG_STUB
113 #define NIOS2_HAS_JMPI_INSTRUCTION
114 #define NIOS2_ICACHE_LINE_SIZE 0
115 #define NIOS2_ICACHE_LINE_SIZE_LOG2 0
116 #define NIOS2_ICACHE_SIZE 0
117 #define NIOS2_INST_ADDR_WIDTH 0x16
118 #define NIOS2_RESET_ADDR 0x00180000
119
120
121 /*
122  * Define for each module class mastered by the CPU
123  *
124  */
125
126 #define __ALTERA_AVALON_JTAG_UART
127 #define __ALTERA_AVALON_PIO
128 #define __ALTERA_GENERIC_TRISTATE_CONTROLLER
129 #define __ALTERA_NIOS2_QSYS
130
131
132 /*
133  * System configuration
134  *
135  */
136
137 #define ALT_DEVICE_FAMILY "Cyclone III"
138 #define ALT_ENHANCED_INTERRUPT_API_PRESENT
139 #define ALT_IRQ_BASE NULL
140 #define ALT_LOG_PORT "/dev/null"
141 #define ALT_LOG_PORT_BASE 0x0
142 #define ALT_LOG_PORT_DEV null
143 #define ALT_LOG_PORT_TYPE ""
144 #define ALT_NUM_EXTERNAL_INTERRUPT_CONTROLLERS 0
145 #define ALT_NUM_INTERNAL_INTERRUPT_CONTROLLERS 1
146 #define ALT_NUM_INTERRUPT_CONTROLLERS 1
147 #define ALT_STDERR "/dev/jtag"
148 #define ALT_STDERR_BASE 0x241180
149 #define ALT_STDERR_DEV jtag
150 #define ALT_STDERR_IS_JTAG_UART

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151 #define ALT_STDERR_PRESENT
152 #define ALT_STDERR_TYPE "altera_avalon_jtag_uart"
153 #define ALT_STDIN "/dev/jtag"
154 #define ALT_STDIN_BASE 0x241180
155 #define ALT_STDIN_DEV jtag
156 #define ALT_STDIN_IS_JTAG_UART
157 #define ALT_STDIN_PRESENT
158 #define ALT_STDIN_TYPE "altera_avalon_jtag_uart"
159 #define ALT_STDOUT "/dev/jtag"
160 #define ALT_STDOUT_BASE 0x241180
161 #define ALT_STDOUT_DEV jtag
162 #define ALT_STDOUT_IS_JTAG_UART
163 #define ALT_STDOUT_PRESENT
164 #define ALT_STDOUT_TYPE "altera_avalon_jtag_uart"
165 #define ALT_SYSTEM_NAME "sopc_scope_sys"
166
167
168 /*
169  * fifo_data configuration
170  *
171  */
172
173 #define ALT_MODULE_CLASS_fifo_data altera_avalon_pio
174 #define FIFO_DATA_BASE 0x241140
175 #define FIFO_DATA_BIT_CLEARING_EDGE_REGISTER 0
176 #define FIFO_DATA_BIT_MODIFYING_OUTPUT_REGISTER 0
177 #define FIFO_DATA_CAPTURE 0
178 #define FIFO_DATA_DATA_WIDTH 8
179 #define FIFO_DATA_DO_TEST_BENCH_WIRING 0
180 #define FIFO_DATA_DRIVEN_SIM_VALUE 0
181 #define FIFO_DATA_EDGE_TYPE "NONE"
182 #define FIFO_DATA_FREQ 50000000
183 #define FIFO_DATA_HAS_IN 1
184 #define FIFO_DATA_HAS_OUT 0
185 #define FIFO_DATA_HAS_TRI 0
186 #define FIFO_DATA_IRQ -1
187 #define FIFO_DATA_IRQ_INTERRUPT_CONTROLLER_ID -1
188 #define FIFO_DATA_IRQ_TYPE "NONE"
189 #define FIFO_DATA_NAME "/dev/fifo_data"
190 #define FIFO_DATA_RESET_VALUE 0
191 #define FIFO_DATA_SPAN 16
192 #define FIFO_DATA_TYPE "altera_avalon_pio"
193
194
195 /*
196  * fifo_full configuration
197  *
198  */
199
200 #define ALT_MODULE_CLASS_fifo_full altera_avalon_pio
201 #define FIFO_FULL_BASE 0x241130
202 #define FIFO_FULL_BIT_CLEARING_EDGE_REGISTER 0
203 #define FIFO_FULL_BIT_MODIFYING_OUTPUT_REGISTER 0
204 #define FIFO_FULL_CAPTURE 1
205 #define FIFO_FULL_DATA_WIDTH 1
206 #define FIFO_FULL_DO_TEST_BENCH_WIRING 0
207 #define FIFO_FULL_DRIVEN_SIM_VALUE 0
208 #define FIFO_FULL_EDGE_TYPE "RISING"
209 #define FIFO_FULL_FREQ 50000000
210 #define FIFO_FULL_HAS_IN 1
211 #define FIFO_FULL_HAS_OUT 0
212 #define FIFO_FULL_HAS_TRI 0
213 #define FIFO_FULL_IRQ 4
214 #define FIFO_FULL_IRQ_INTERRUPT_CONTROLLER_ID 0
215 #define FIFO_FULL_IRQ_TYPE "EDGE"
216 #define FIFO_FULL_NAME "/dev/fifo_full"
217 #define FIFO_FULL_RESET_VALUE 0
218 #define FIFO_FULL_SPAN 16
219 #define FIFO_FULL_TYPE "altera_avalon_pio"
220
221
222 /*
223  * hal configuration
224  *
225  */

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226
227 #define ALT_MAX_FD 32
228 #define ALT_SYS_CLK none
229 #define ALT_TIMESTAMP_CLK none
230
231
232 /*
233  * jtag configuration
234  *
235  */
236
237 #define ALT_MODULE_CLASS_jtag altera_avalon_jtag_uart
238 #define JTAG_BASE 0x241180
239 #define JTAG_IRQ 0
240 #define JTAG_IRQ_INTERRUPT_CONTROLLER_ID 0
241 #define JTAG_NAME "/dev/jtag"
242 #define JTAG_READ_DEPTH 64
243 #define JTAG_READ_THRESHOLD 8
244 #define JTAG_SPAN 8
245 #define JTAG_TYPE "altera_avalon_jtag_uart"
246 #define JTAG_WRITE_DEPTH 64
247 #define JTAG_WRITE_THRESHOLD 8
248
249
250 /*
251  * pio_0 configuration
252  *
253  */
254
255 #define ALT_MODULE_CLASS_pio_0 altera_avalon_pio
256 #define PIO_0_BASE 0x2410a0
257 #define PIO_0_BIT_CLEARING_EDGE_REGISTER 1
258 #define PIO_0_BIT_MODIFYING_OUTPUT_REGISTER 1
259 #define PIO_0_CAPTURE 1
260 #define PIO_0_DATA_WIDTH 6
261 #define PIO_0_DO_TEST_BENCH_WIRING 0
262 #define PIO_0_DRIVEN_SIM_VALUE 0
263 #define PIO_0_EDGE_TYPE "FALLING"
264 #define PIO_0_FREQ 50000000
265 #define PIO_0_HAS_IN 1
266 #define PIO_0_HAS_OUT 0
267 #define PIO_0_HAS_TRI 0
268 #define PIO_0_IRQ 1
269 #define PIO_0_IRQ_INTERRUPT_CONTROLLER_ID 0
270 #define PIO_0_IRQ_TYPE "EDGE"
271 #define PIO_0_NAME "/dev/pio_0"
272 #define PIO_0_RESET_VALUE 0
273 #define PIO_0_SPAN 32
274 #define PIO_0_TYPE "altera_avalon_pio"
275
276
277 /*
278  * ram configuration
279  *
280  */
281
282 #define ALT_MODULE_CLASS_ram altera_generic_tristate_controller
283 #define RAM_BASE 0x220000
284 #define RAM_IRQ -1
285 #define RAM_IRQ_INTERRUPT_CONTROLLER_ID -1
286 #define RAM_NAME "/dev/ram"
287 #define RAM_SPAN 131072
288 #define RAM_TYPE "altera_generic_tristate_controller"
289
290
291 /*
292  * rom configuration
293  *
294  */
295
296 #define ALT_MODULE_CLASS_rom altera_generic_tristate_controller
297 #define ROM_BASE 0x180000
298 #define ROM_IRQ -1
299 #define ROM_IRQ_INTERRUPT_CONTROLLER_ID -1
300 #define ROM_NAME "/dev/rom"

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```

301 #define ROM_SPAN 524288
302 #define ROM_TYPE "altera_generic_tristate_controller"
303
304
305 /*
306  * trig_ctrl configuration
307  *
308  */
309
310 #define ALT_MODULE_CLASS_trig_ctrl altera_avalon_pio
311 #define TRIG_CTRL_BASE 0x241060
312 #define TRIG_CTRL_BIT_CLEARING_EDGE_REGISTER 0
313 #define TRIG_CTRL_BIT_MODIFYING_OUTPUT_REGISTER 1
314 #define TRIG_CTRL_CAPTURE 0
315 #define TRIG_CTRL_DATA_WIDTH 5
316 #define TRIG_CTRL_DO_TEST_BENCH_WIRING 0
317 #define TRIG_CTRL_DRIVEN_SIM_VALUE 0
318 #define TRIG_CTRL_EDGE_TYPE "NONE"
319 #define TRIG_CTRL_FREQ 50000000
320 #define TRIG_CTRL_HAS_IN 0
321 #define TRIG_CTRL_HAS_OUT 1
322 #define TRIG_CTRL_HAS_TRI 0
323 #define TRIG_CTRL_IRQ -1
324 #define TRIG_CTRL_IRQ_INTERRUPT_CONTROLLER_ID -1
325 #define TRIG_CTRL_IRQ_TYPE "NONE"
326 #define TRIG_CTRL_NAME "/dev/trig_ctrl"
327 #define TRIG_CTRL_RESET_VALUE 3
328 #define TRIG_CTRL_SPAN 32
329 #define TRIG_CTRL_TYPE "altera_avalon_pio"
330
331
332 /*
333  * trig_delay configuration
334  *
335  */
336
337 #define ALT_MODULE_CLASS_trig_delay altera_avalon_pio
338 #define TRIG_DELAY_BASE 0x241120
339 #define TRIG_DELAY_BIT_CLEARING_EDGE_REGISTER 0
340 #define TRIG_DELAY_BIT_MODIFYING_OUTPUT_REGISTER 0
341 #define TRIG_DELAY_CAPTURE 0
342 #define TRIG_DELAY_DATA_WIDTH 32
343 #define TRIG_DELAY_DO_TEST_BENCH_WIRING 0
344 #define TRIG_DELAY_DRIVEN_SIM_VALUE 0
345 #define TRIG_DELAY_EDGE_TYPE "NONE"
346 #define TRIG_DELAY_FREQ 50000000
347 #define TRIG_DELAY_HAS_IN 0
348 #define TRIG_DELAY_HAS_OUT 1
349 #define TRIG_DELAY_HAS_TRI 0
350 #define TRIG_DELAY_IRQ -1
351 #define TRIG_DELAY_IRQ_INTERRUPT_CONTROLLER_ID -1
352 #define TRIG_DELAY_IRQ_TYPE "NONE"
353 #define TRIG_DELAY_NAME "/dev/trig_delay"
354 #define TRIG_DELAY_RESET_VALUE 1
355 #define TRIG_DELAY_SPAN 16
356 #define TRIG_DELAY_TYPE "altera_avalon_pio"
357
358
359 /*
360  * trig_level configuration
361  *
362  */
363
364 #define ALT_MODULE_CLASS_trig_level altera_avalon_pio
365 #define TRIG_LEVEL_BASE 0x241150
366 #define TRIG_LEVEL_BIT_CLEARING_EDGE_REGISTER 0
367 #define TRIG_LEVEL_BIT_MODIFYING_OUTPUT_REGISTER 0
368 #define TRIG_LEVEL_CAPTURE 0
369 #define TRIG_LEVEL_DATA_WIDTH 8
370 #define TRIG_LEVEL_DO_TEST_BENCH_WIRING 0
371 #define TRIG_LEVEL_DRIVEN_SIM_VALUE 0
372 #define TRIG_LEVEL_EDGE_TYPE "NONE"
373 #define TRIG_LEVEL_FREQ 50000000
374 #define TRIG_LEVEL_HAS_IN 0
375 #define TRIG_LEVEL_HAS_OUT 1

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```

376 #define TRIG_LEVEL_HAS_TRI 0
377 #define TRIG_LEVEL_IRQ -1
378 #define TRIG_LEVEL_IRQ_INTERRUPT_CONTROLLER_ID -1
379 #define TRIG_LEVEL_IRQ_TYPE "NONE"
380 #define TRIG_LEVEL_NAME "/dev/trig_level"
381 #define TRIG_LEVEL_RESET_VALUE 0
382 #define TRIG_LEVEL_SPAN 16
383 #define TRIG_LEVEL_TYPE "altera_avalon_pio"
384
385
386 /*
387  * trig_period configuration
388  *
389  */
390
391 #define ALT_MODULE_CLASS_trig_period altera_avalon_pio
392 #define TRIG_PERIOD_BASE 0x241160
393 #define TRIG_PERIOD_BIT_CLEARING_EDGE_REGISTER 0
394 #define TRIG_PERIOD_BIT_MODIFYING_OUTPUT_REGISTER 0
395 #define TRIG_PERIOD_CAPTURE 0
396 #define TRIG_PERIOD_DATA_WIDTH 32
397 #define TRIG_PERIOD_DO_TEST_BENCH_WIRING 0
398 #define TRIG_PERIOD_DRIVEN_SIM_VALUE 0
399 #define TRIG_PERIOD_EDGE_TYPE "NONE"
400 #define TRIG_PERIOD_FREQ 50000000
401 #define TRIG_PERIOD_HAS_IN 0
402 #define TRIG_PERIOD_HAS_OUT 1
403 #define TRIG_PERIOD_HAS_TRI 0
404 #define TRIG_PERIOD_IRQ -1
405 #define TRIG_PERIOD_IRQ_INTERRUPT_CONTROLLER_ID -1
406 #define TRIG_PERIOD_IRQ_TYPE "NONE"
407 #define TRIG_PERIOD_NAME "/dev/trig_period"
408 #define TRIG_PERIOD_RESET_VALUE 1
409 #define TRIG_PERIOD_SPAN 16
410 #define TRIG_PERIOD_TYPE "altera_avalon_pio"
411
412
413 /*
414  * vram configuration
415  *
416  */
417
418 #define ALT_MODULE_CLASS_vram altera_generic_tristate_controller
419 #define VRAM_BASE 0x0
420 #define VRAM_IRQ -1
421 #define VRAM_IRQ_INTERRUPT_CONTROLLER_ID -1
422 #define VRAM_NAME "/dev/vram"
423 #define VRAM_SPAN 1048576
424 #define VRAM_TYPE "altera_generic_tristate_controller"
425
426 #endif /* __SYSTEM_H_ */
427

```