General Data

SYMBOL	DEFINITION	DESCRIPTION	MIN	MAX	NOTES
t_{BIO}		Buffer I/O Delay		4.5ns	
t_{prop}		FPGA Propagation Delay		2ns	
t_{CLK}		DCLK Period	66.7ns		
H		HSync Cycle - 2100			
t_{VP}		VSync Pulse Width - 10 H			
t_{VB}		VSync Back Porch - 2 H			
t_{VD}		VSync Display Period - 272 H			
t_{VF}		VSync Front Porch - 2 H			
t_{HP}		HSync Pulse Width - 164 CLKS	260ns	4.33us	
t_{HB}		HSync Back Porch - 8 CLKS			
t_{HD}		HSync Display Period - 1920 CLKS			
t_{HF}		HSync Front Porch - 8 CLKS			
t_{SCA}		VRAM Access Time (from SC)		15ns	
t_{SOH}		VRAM Serial Output Hold Time (rom SC)	3ns		
t_{DS}		Data Setup Time	10ns		
t_{DH}		Data Hold Time	10ns		
t_{VS}		VSync Setup Time	10ns		
t_{HS}		HSync Setup Time	10ns		

General Data continued...

SYMBOL	DEFINITION	DESCRIPTION	MIN	MAX	NOTES
t_{SC}		Serial Clock Pulse Width	5ns		
t_{SCC}		Serial Clock Period	18ns		