General Data

SYMBOL	DEFINITION	DESCRIPTION	MIN	MAX	NOTES
t_{prop}		Propagation delay of FPGA	0ns	2ns	
t_{BIO}		Buffer input-output delay		4.5ns	
t_{BOE}		Buffer output enable		6.5ns	
t_{LZ}		Chip selection to output enable		10ns	
t_{AA}		Address access time		85ns	
t_{RC}		Read cycle time	85ns		
t_{HZ}		Chip deselection to output high-Z		30ns	
t_{OH}		Output hold from address change	10ns		