General Data

SYMBOL	DEFINITION	DESCRIPTION	MIN	MAX	NOTES
t_{prop}		Propagation delay of FPGA	0ns	2ns	
t_{buff}		Buffer output delay		4.5ns	
t_{ACC}		Address to Data Valid delay		120ns	
t_{CE}		Chip Enable to Data Valid delay		120ns	
t_{RC}		Address stable hold time	120ns		
t_{DF}		Chip enable to output high-Z delay		16ns	
t_{OH}		Outputhold time from address/CE	0ns	0	