SN54LVT16245B, SN74LVT16245B
3.3-V ABT 16-BIT BUS TRANSCEIVERS
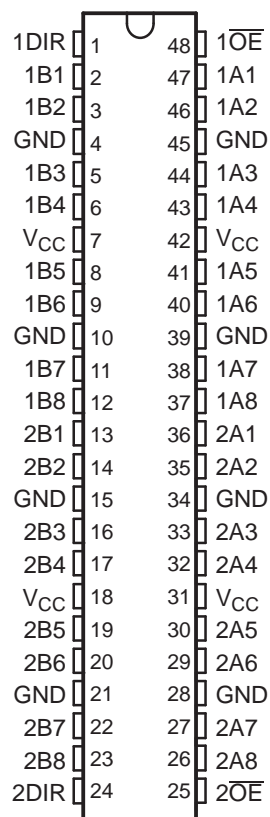# WITH 3-STATE OUTPUTS

FEATURES

- **Member of the Texas Instruments Widebus™ Family**
- **State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static-Power Dissipation**
- **Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Support Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **I_{off} and Power-Up 3-State Support Hot Insertion**
- **Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
    - **2000-V Human-Body Model (A114-A)**
    - **200-V Machine Model (A115-A)**
    - **1000-V Charged-Device Model (C101)**

SN54LVT16245B . . . WD PACKAGE
SN74LVT16245B . . . DGG, DGV, OR DL PACKAGE
(TOP VIEW)

1DIR	1	48	1$\overline{OE}$
1B1	2	47	1A1
1B2	3	46	1A2
GND	4	45	GND
1B3	5	44	1A3
1B4	6	43	1A4
V_{CC}	7	42	V_{CC}
1B5	8	41	1A5
1B6	9	40	1A6
GND	10	39	GND
1B7	11	38	1A7
1B8	12	37	1A8
2B1	13	36	2A1
2B2	14	35	2A2
GND	15	34	GND
2B3	16	33	2A3
2B4	17	32	2A4
V_{CC}	18	31	V_{CC}
2B5	19	30	2A5
2B6	20	29	2A6
GND	21	28	GND
2B7	22	27	2A7
2B8	23	26	2A8
2DIR	24	25	2$\overline{OE}$

DESCRIPTION/ORDERING INFORMATION

ORDERING INFORMATION

T_A	PACKAGE[1]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	FBGA – GRD	Reel of 1000	SN74LVT16245BGRDR	VD245B
	FBGA – ZRD (Pb-free)		SN74LVT16245BZRDR	
	SSOP – DL	Tube of 25	SN74LVT16245BDL	LVT16245B
			SN74LVT16245BDLG4	
		Reel of 1000	SN74LVT16245BDLR	
			74LVT16245BDLRG4	
	TSSOP – DGG	Reel of 2000	SN74LVT16245BDGGR	LVT16245B
			74LVT16245BDGGRE4	
	TVSOP – DGV	Reel of 2000	SN74LVT16245BDGVR	VD245B
			74LVT16245BDGVRE4	
	VFBGA – GQL	Reel of 1000	SN74LVT16245BGQLR	VD245B
	VFBGA – ZQL (Pb-free)		SN74LVT16245BZQLR	
−55°C to 125°C	CFP – WD	Tube	SNJ54LVT16245BWD	SNJ54LVT16245BWD

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

![warning symbol] Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments.

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

The 'LVT16245B devices are 16-bit (dual-octal) noninverting 3-state transceivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

These devices are designed for asynchronous communication between two data buses. The logic levels of the direction-control (DIR) input and the output-enable ($\overline{OE}$) input activate either the B-port outputs or the A-port outputs or place both output ports into the high-impedance mode. The device transmits data from the A bus to the B bus when the B-port outputs are activated, and from the B bus to the A bus when the A-port outputs are activated. The input circuitry on both A and B ports is always active and must have a logic HIGH or LOW level applied to prevent excess I_{CC} and I_{CCZ}.

When V_{CC} is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.
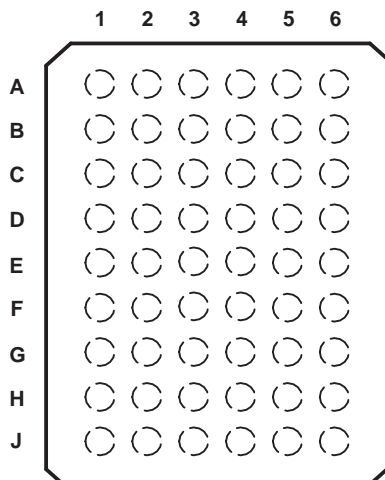
GQL OR ZQL PACKAGE
(TOP VIEW)
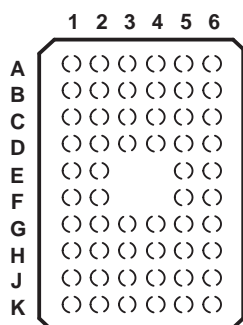
TERMINAL ASSIGNMENTS[1]
(56-Ball GQL/ZQL Package)

	1	2	3	4	5	6
A	1DIR	NC	NC	NC	NC	1$\overline{OE}$
B	1B2	1B1	GND	GND	1A1	1A2
C	1B4	1B3	V_{CC}	V_{CC}	1A3	1A4
D	1B6	1B5	GND	GND	1A5	1A6
E	1B8	1B7			1A7	1A8
F	2B1	2B2			2A2	2A1
G	2B3	2B4	GND	GND	2A4	2A3
H	2B5	2B6	V_{CC}	V_{CC}	2A6	2A5
J	2B7	2B8	GND	GND	2A8	2A7
K	2DIR	NC	NC	NC	NC	2$\overline{OE}$

(1)   NC – No internal connection

GRD OR ZRD PACKAGE
(TOP VIEW)

TERMINAL ASSIGNMENTS[1]
(54-Ball GRD/ZRD Package)

	1	2	3	4	5	6
A	1B1	NC	1DIR	1$\overline{OE}$	NC	1A1
B	1B3	1B2	NC	NC	1A2	1A3
C	1B5	1B4	V_{CC}	V_{CC}	1A4	1A5
D	1B7	1B6	GND	GND	1A6	1A7
E	2B1	1B8	GND	GND	1A8	2A1
F	2B3	2B2	GND	GND	2A2	2A3
G	2B5	2B4	V_{CC}	V_{CC}	2A4	2A5
H	2B7	2B6	NC	NC	2A6	2A7
J	2B8	NC	2DIR	2$\overline{OE}$	NC	2A8

(1)   NC – No internal connection

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FUNCTION TABLE[1]
(each 8-bit section)

CONTROL INPUTS		OUTPUT CIRCUITS		OPERATION
$\overline{OE}$	DIR	A PORT	B PORT	
L	L	Enabled	Hi-Z	B data to A bus
L	H	Hi-Z	Enabled	A data to B bus
H	X	Hi-Z	Hi-Z	Isolation

(1) Input circuits of the data I/Os always are active.

LOGIC DIAGRAM (POSITIVE LOGIC)
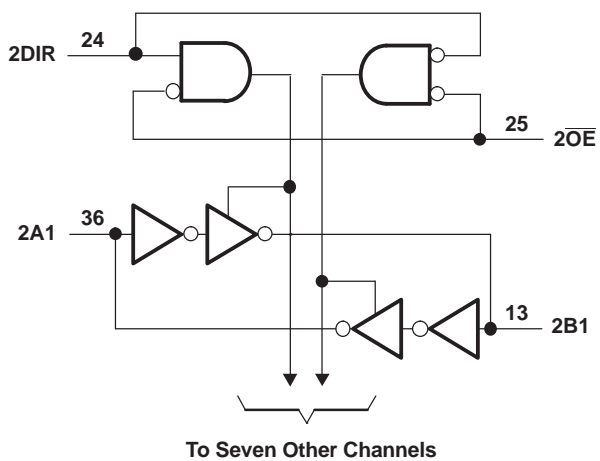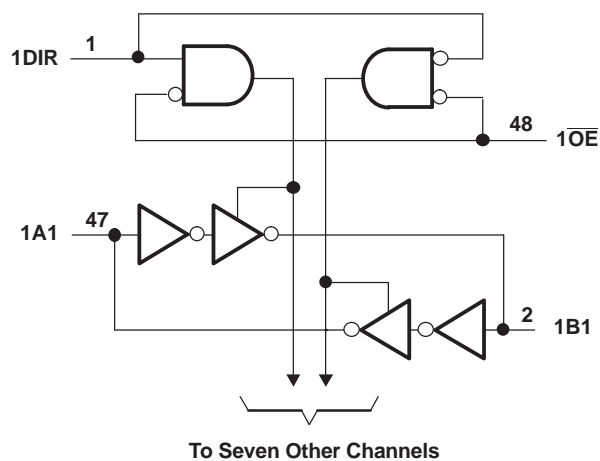
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Absolute Maximum Ratings[1]

over recommended operating free-air temperature range (unless otherwise noted)

			MIN	**MAX**	**UNIT**
V_{CC}	Supply voltage range		−0.5	4.6	V
V_I	Input voltage range[2]		−0.5	7	V
V_O	Voltage range applied to any output in the high-impedance or power-off state[2]		−0.5	7	V
V_O	Voltage range applied to any output in the high state[2]		−0.5	V_{CC} + 0.5	V
I_O	Current into any output in the low state	SN54LVT16245B		96	mA
		SN74LVT16245B		128	
I_O	Current into any output in the high state[3]	SN54LVT16245B		48	mA
		SN74LVT16245B		64	
I_{IK}	Input clamp current	$V_I < 0$		−50	mA
I_{OK}	Output clamp current	$V_O < 0$		−50	mA
θ_{JA}	Package thermal impedance[4]	DGG package		70	°C/W
		DGV package		58	
		DL package		63	
		GQL/ZQL package		42	
		GRD/ZRD package		36	
T_{stg}	Storage temperature range		−65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) This current flows only when the output is in the high state and $V_O > V_{CC}$.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions[1]

			SN54LVT16245B[2]		SN74LVT16245B		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200		200		μs/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

(1) All unused or undriven (floating) inputs (I/Os) of the device must be held at logic HIGH or LOW (preferably V_{CC} or GND) to ensure
     proper device operation and minimize power. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature
     number SCBA004.
(2) Product preview

SN54LVT16245B, SN74LVT16245B
3.3-V ABT 16-BIT BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS
SCBS715E−FEBRUARY 2000−REVISED NOVEMBER 2006

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Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54LVT16245B[1]			SN74LVT16245B			UNIT
				MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
V_{IK}		V_{CC} = 2.7 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 2.7 to 3.6 V,	I_{OH} = −100 µA	V_{CC} − 0.2			V_{CC} − 0.2			V
		V_{CC} = 2.7 V,	I_{OH} = −8 mA	2.4			2.4			
		V_{CC} = 3 V	I_{OH} = −24 mA	2						
			I_{OH} = −32 mA				2			
V_{OL}		V_{CC} = 2.7 V	I_{OL} = 100 µA			0.2			0.2	V
			I_{OL} = 24 mA			0.5			0.5	
		V_{CC} = 3 V	I_{OL} = 16 mA			0.4			0.4	
			I_{OL} = 32 mA			0.5			0.5	
			I_{OL} = 48 mA			0.55				
			I_{OL} = 64 mA						0.55	
I_I	Control inputs	V_{CC} = 3.6 V,	V_I = V_{CC} or GND			±1			±1	µA
		V_{CC} = 0 or 3.6 V,	V_I = 5.5 V			10			10	
	A or B port[3]	V_{CC} = 3.6 V	V_I = 5.5 V			20			20	
			V_I = V_{CC}			5			1	
			V_I = 0			−5			−5	
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 4.5 V						±100	µA
I_{OZPU}		V_{CC} = 0 to 1.5 V, V_O = 0.5 V to 3 V, $\overline{OE}$ = don't care				±100[4]			±100	µA
I_{OZPD}		V_{CC} = 1.5 V to 0, V_O = 0.5 V to 3 V, $\overline{OE}$ = don't care				±100[4]			±100	µA
I_{CC}		V_{CC} = 3.6 V, I_O = 0, V_I = V_{CC} or GND	Outputs high			0.19			0.19	mA
			Outputs low			5			5	
			Outputs disabled			0.19			0.19	
ΔI_{CC}[5]		V_{CC} = 3 V to 3.6 V, One input at V_{CC} − 0.6 V, Other inputs at V_{CC} or GND				0.2			0.2	mA
C_i		V_I = 3 V or 0			4			4		pF
C_{io}		V_O = 3 V or 0			10			10		pF

(1) Product preview
(2) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
(3) Unused pins at V_{CC} or GND.
(4) On products compliant to MIL-PRF-38535, this parameter is not production tested.
(5) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.
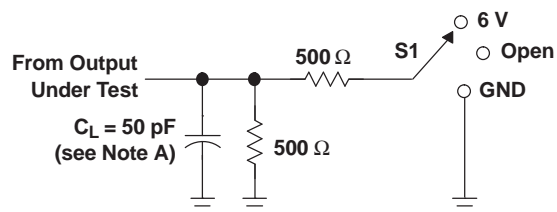
Switching Characteristics

over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT16245B[1]				SN74LVT16245B					UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP[2]	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	0.5	4.5		4.6	1.5	2.3	3.3		3.7	ns
t_{PHL}			0.5	4.4		3.9	1.3	2.1	3.3		3.5	
t_{PZH}	$\overline{OE}$	A or B	0.5	6.5		6.6	1.5	2.8	4.5		5.3	ns
t_{PZL}			0.5	5.4		6.2	1.6	2.9	4.6		5.2	
t_{PHZ}	$\overline{OE}$	A or B	1	6.8		7	2.3	3.7	5.1		5.5	ns
t_{PLZ}			1	6.2		6.3	2.2	3.5	5.1		5.4	
$t_{sk(LH)}$									0.5			ns
$t_{sk(HL)}$									0.5			

(1) Product preview
(2) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

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PARAMETER MEASUREMENT INFORMATION

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT
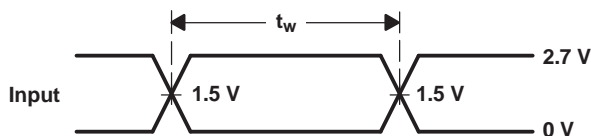
VOLTAGE WAVEFORMS
PULSE DURATION
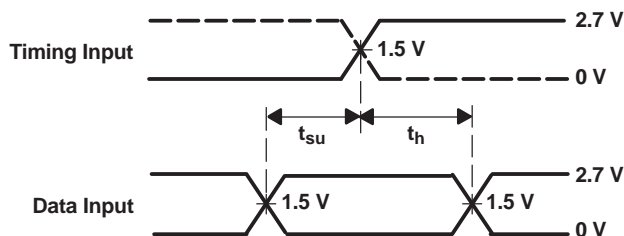
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS
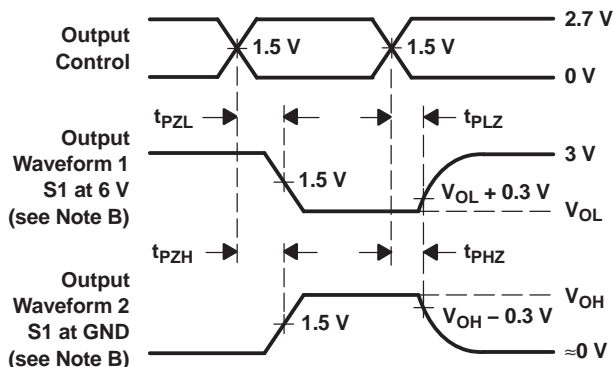
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
    Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
 D. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
74LVT16245BDGGRE4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74LVT16245BDGVRE4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74LVT16245BDLRG4	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVT16245BDGGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVT16245BDGVR	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVT16245BDL	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVT16245BDLG4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVT16245BDLR	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVT16245BGQLR	NRND	BGA MICROSTAR JUNIOR	GQL	56	1000	TBD	SNPB	Level-1-240C-UNLIM
SN74LVT16245BGRDR	ACTIVE	BGA MICROSTAR JUNIOR	GRD	54	1000	TBD	SNPB	Level-1-240C-UNLIM
SN74LVT16245BZQLR	ACTIVE	BGA MICROSTAR JUNIOR	ZQL	56	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
SN74LVT16245BZRDR	ACTIVE	BGA MICROSTAR JUNIOR	ZRD	54	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder
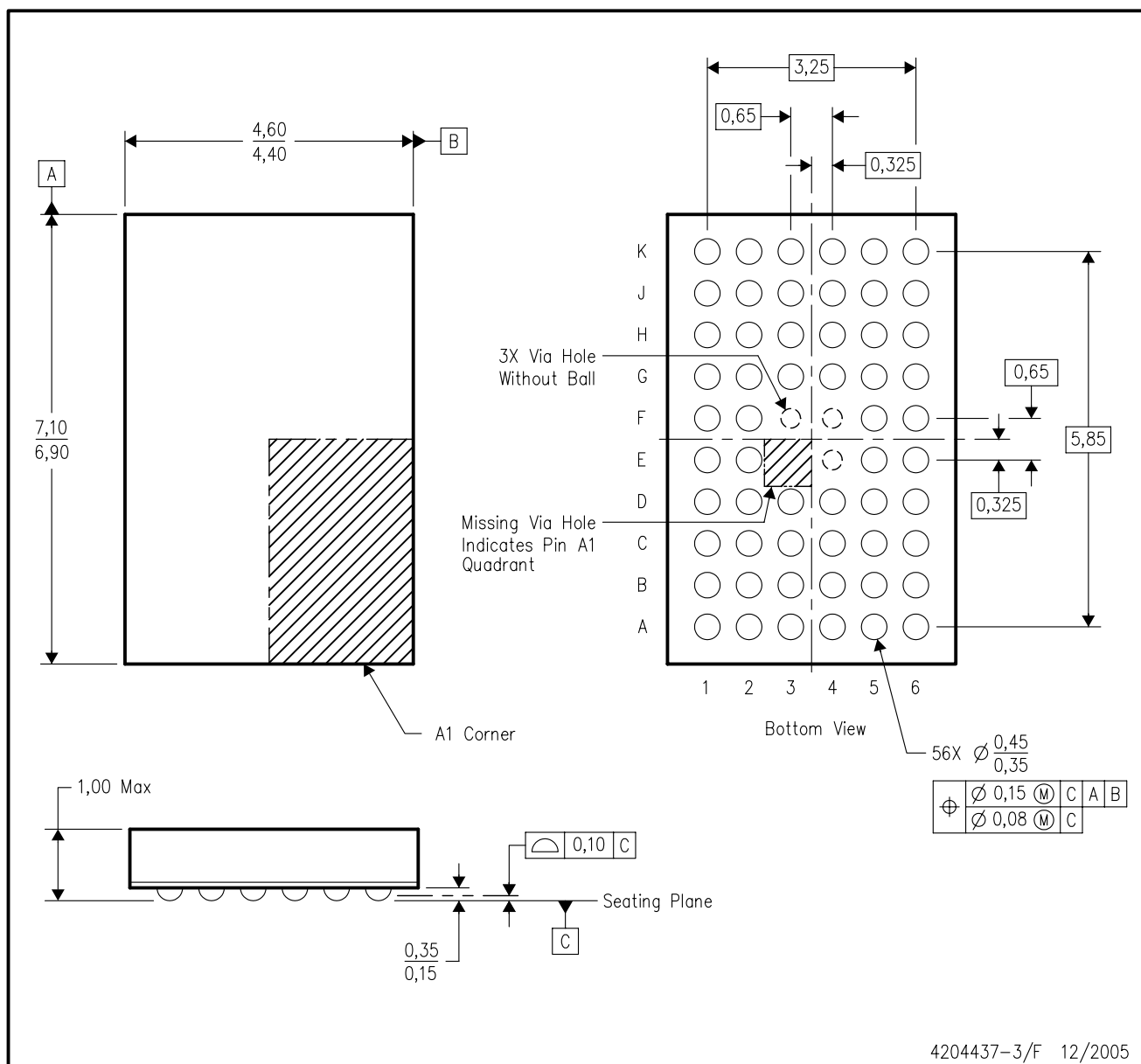
temperature.

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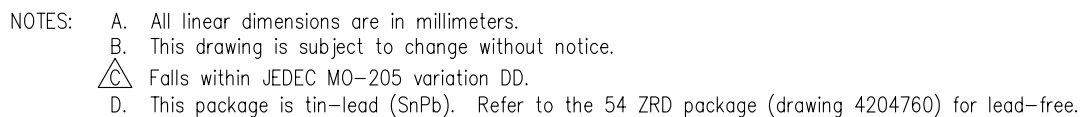
ZQL (R−PBGA−N56)

PLASTIC BALL GRID ARRAY

3,25

0,65

0,325

4,60
4,40

A

B

7,10
6,90

K
J
H
G
F
E
D
C
B
A

3X Via Hole
Without Ball

0,65

5,85

0,325

Missing Via Hole
Indicates Pin A1
Quadrant

A1 Corner

1 2 3 4 5 6

Bottom View

56X Ø 0,45
0,35

⊕	Ø 0,15 Ⓜ	C	A	B
	Ø 0,08 Ⓜ	C		

1,00 Max
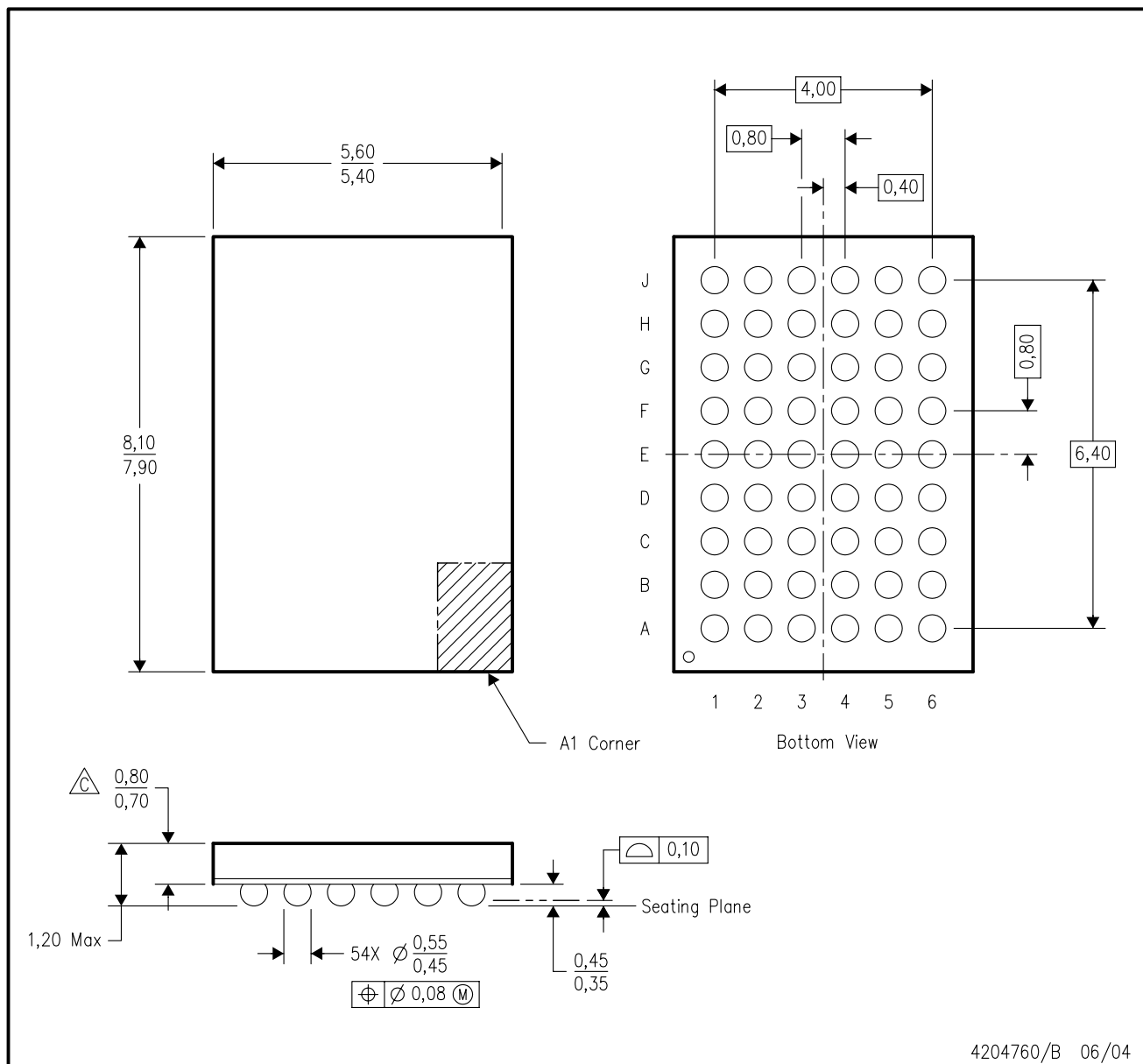
0,10 C

Seating Plane

0,35
0,15

C

4204437−3/F   12/2005

NOTES: A.   All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.   This drawing is subject to change without notice.
         C.   Falls within JEDEC MO−225 variation BA.
         D.   This package is lead−free. Refer to the 56 GQL package (drawing 4200583) for tin−lead (SnPb).

GRD (R-PBGA-N54)   PLASTIC BALL GRID ARRAY

A1 Corner

Bottom View

Seating Plane

54X Ø $\frac{0.55}{0.45}$

⊕ Ø 0,08 Ⓜ

4204759/B 06/04

NOTES: A. All linear dimensions are in millimeters.
         B. This drawing is subject to change without notice.
         C. Falls within JEDEC MO-205 variation DD.
         D. This package is tin-lead (SnPb). Refer to the 54 ZRD package (drawing 4204760) for lead-free.

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ZRD (R−PBGA−N54)   PLASTIC BALL GRID ARRAY

5,60
5,40

8,10
7,90

A1 Corner

4,00

0,80

0,40

J
H
G
F
E
D
C
B
A

1 2 3 4 5 6

Bottom View

0,80

6,40

ⓒ
0,80
0,70

1,20 Max

54X Ø 0,55
         0,45

⊕ Ø 0,08 Ⓜ

0,10

Seating Plane

0,45
0,35

4204760/B 06/04

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
      ⓒ C.   Falls within JEDEC MO−205 variation DD.
         D.   This package is lead−free. Refer to the 54 GRD package (drawing 4204759) for tin−lead (SnPb).

DGV (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN

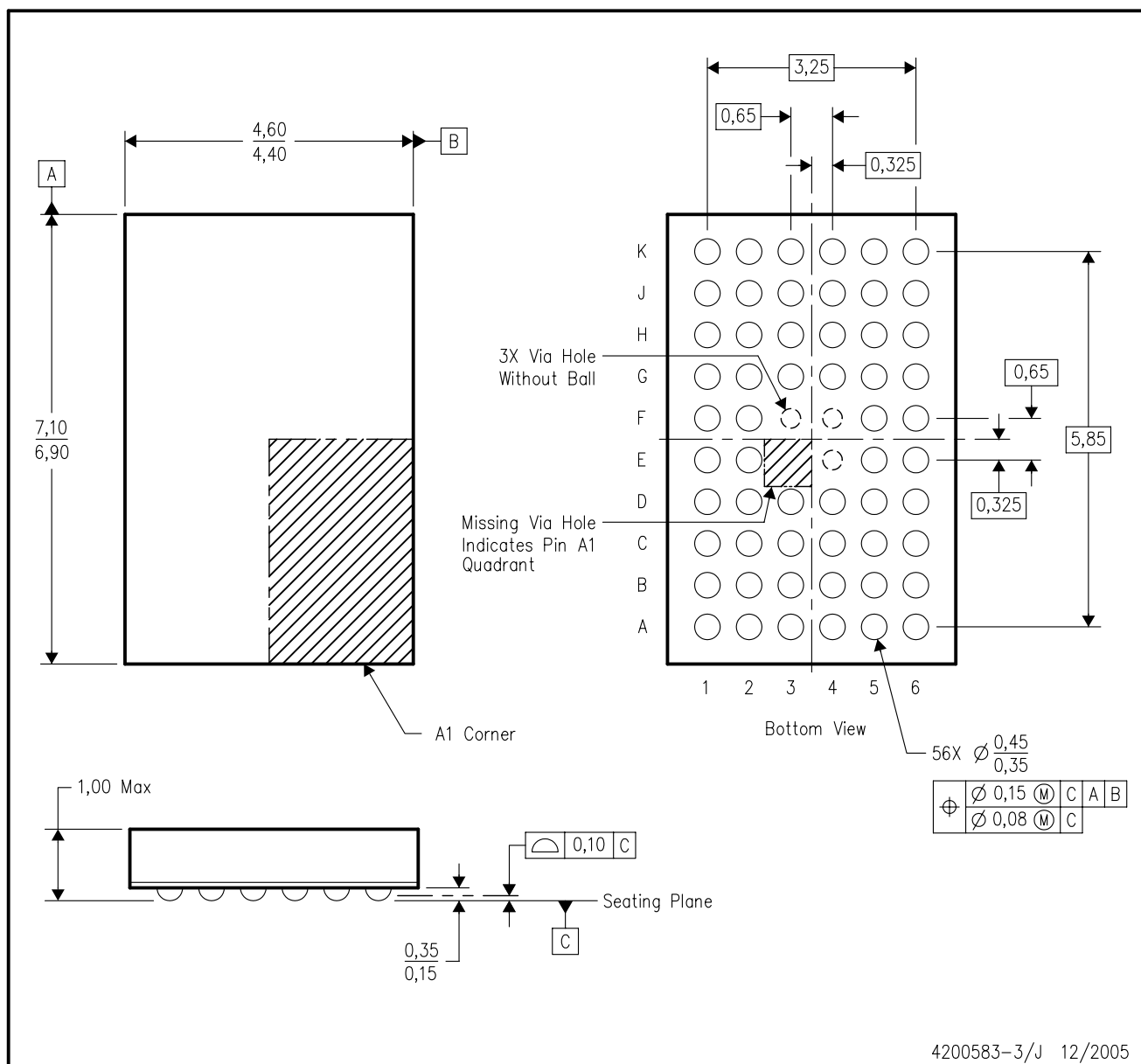| PINS ** DIM	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

TEXAS INSTRUMENTS

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GQL (R−PBGA−N56)   PLASTIC BALL GRID ARRAY

4,60 / 4,40   B

A

7,10 / 6,90

A1 Corner

1,00 Max

0,10 C

Seating Plane

0,35 / 0,15

C

3,25

0,65

0,325

K
J
H
G
F
E
D
C
B
A

1 2 3 4 5 6

Bottom View

3X Via Hole Without Ball

Missing Via Hole Indicates Pin A1 Quadrant

0,65

5,85

0,325

56X Ø 0,45 / 0,35

⌖ Ø 0,15 Ⓜ C A B
   Ø 0,08 Ⓜ C
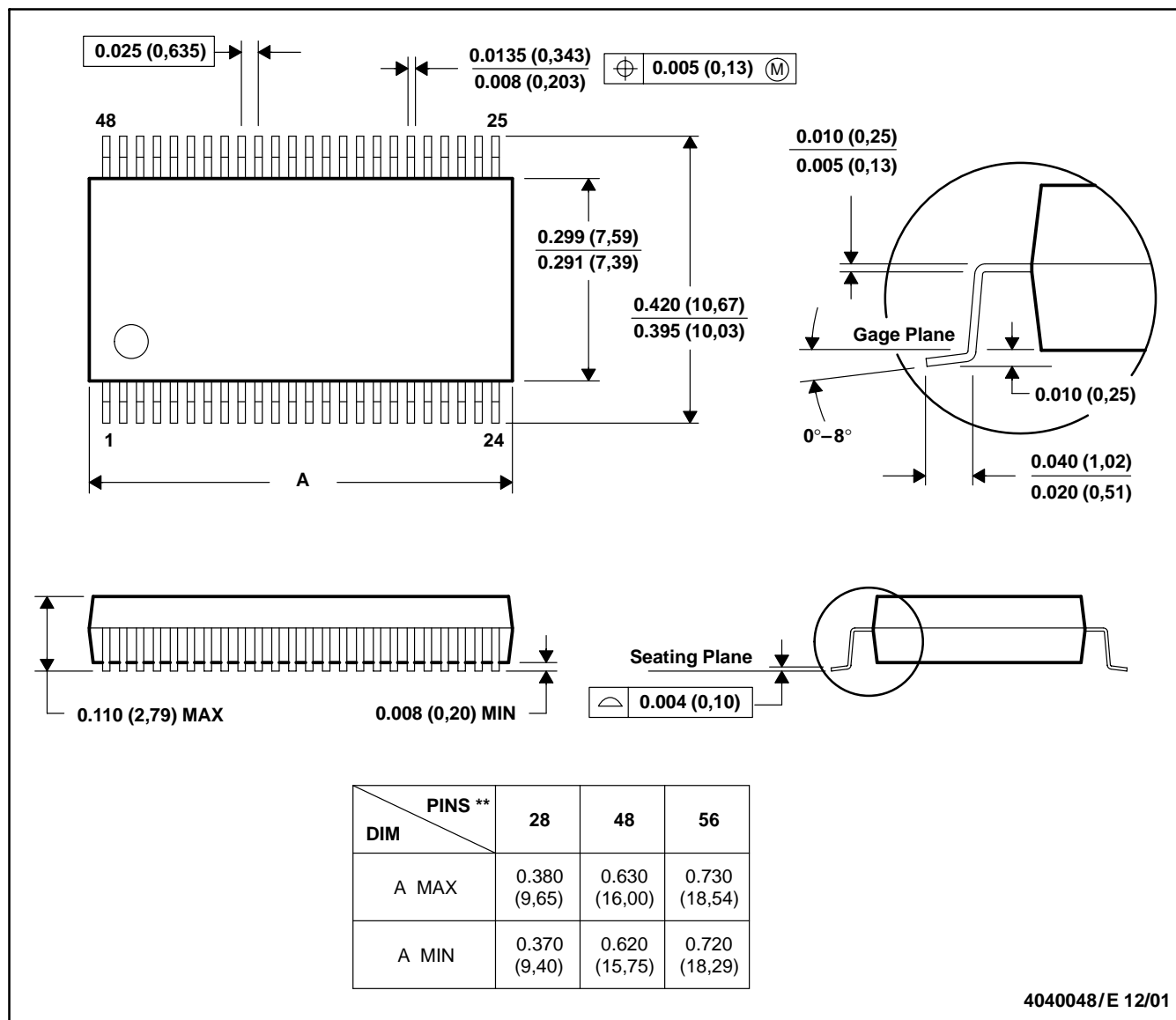
4200583−3/J 12/2005

NOTES: A.   All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.   This drawing is subject to change without notice.
         C.   Falls within JEDEC MO−225 variation BA.
         D.   This package is tin−lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead−free.

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DL (R-PDSO-G**)   PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN

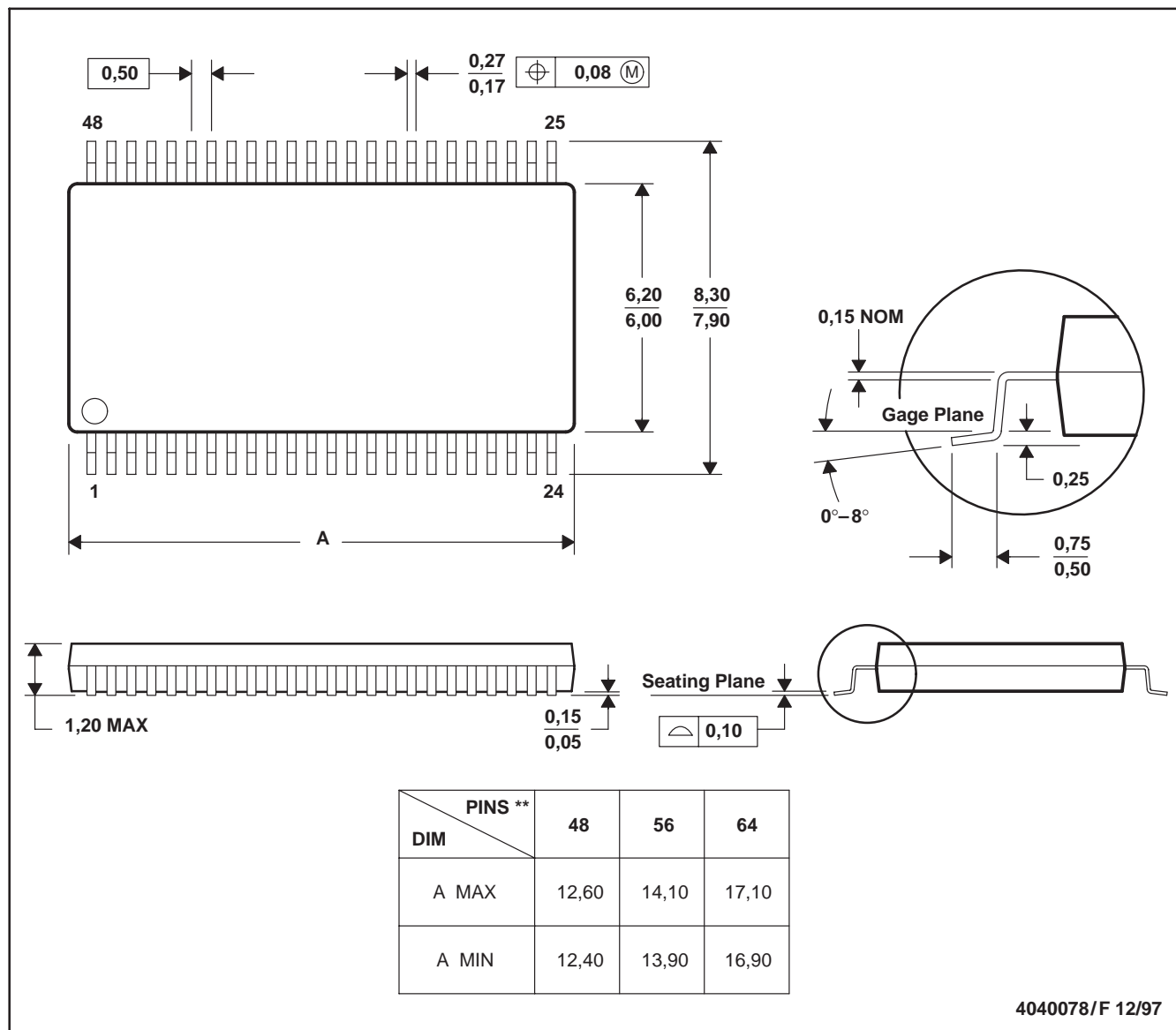| PINS ** | 28 | 48 | 56 |
DIM			
A MAX	0.380 (9,65)	0.630 (16,00)	0.730 (18,54)
A MIN	0.370 (9,40)	0.620 (15,75)	0.720 (18,29)

4040048 / E 12/01

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO-118

DGG (R-PDSO-G)**   **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN

		PINS **		
DIM		48	56	64
A MAX		12,60	14,10	17,10
A MIN		12,40	13,90	16,90

4040078 / F 12/97

NOTES: A. All linear dimensions are in millimeters.
      B. This drawing is subject to change without notice.
      C. Body dimensions do not include mold protrusion not to exceed 0,15.
      D. Falls within JEDEC MO-153

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