General Data

SYMBOL	DEFINITION	DESCRIPTION	MIN	MAX	NOTES
t_{prop}		FPGA Propagation Delay	0	2ns	
t_{BIO}		Buffer Input-Output Delay		4.5ns	
t_{BOE}		Buffer Output Enable Delay		6.5ns	
t_{CW}		Chip selection to end of write ($\overline{CS1}$, CS2 hold time)	75ns		
t_{WC}		Write cycle time	85ns		
t_{WP}		Write pulse width ($\overline{WE}$ hold time)	55ns		
t_{AS}		Address setup time	0ns		
t_{WHZ}		Write output to high-Z (don't drive data during this delay)		30ns	
t_{DW}		Data to write setup time	30ns		
t_{DH}		Data hold from write time	0ns		
t_{WR}		Write recovery time	0ns		
t_{OHZ}		Output disable to output high-Z delay		25ns	