DESIGN OF A DICE GAME

Digital Logic Design Project | Bu-Ali Sina – 4041

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Introduciton

This project's purpose is to familiarize you with the methods of digital design through a hands-on task. In groups of two, you will use VHDL to create a simple dice game, gaining experience in RTL design, I/O interfacing, and system integration. While **a functional implementation is the top priority**, you should also explore design tradeoffs by optimizing your system for minimal resource cost and maximum performance.

Your first step in this project is to translate the high-level specifications into a hardware plan using tools like state machines and block diagrams. While we have provided most of these for you, remember that this planning phase is critical to avoid major delays during implementation. After coding the VHDL and building a working system—which is your primary goal—you will then optimize your design for speed and resource efficiency. This entire process will give you a solid understanding of the basic digital hardware development cycle.

Project Specification

You will design and implement the dice game **Craps**. To simulate the roll of two six-sided dice, you must use **two pseudo-random counters**. The outcome of the game will be based on the sum of their values (2 to 12), according to the rules below.

1. On the first roll, the player wins if the sum is 7 or 11, and loses if the sum is 2, 3, or 12. Any other sum becomes the **point**, and the game continues to the next roll.
2. For all subsequent rolls, the player wins by rolling the **point** again and loses by rolling a 7. If any other number is rolled, the player must continue rolling.

Data path

The datapath shown in Figure 1 implements the game's rules using an adder, a register to store the **point**, a comparator, and logic to determine win/loss conditions.

You **must test each component individually**, then integrate them to build and test the complete datapath. Your report **must include annotated simulation waveforms that verify the correct functionality of both the individual components and the final, integrated circuit**.

FSM

Next, **design and simulate the Finite State Machine (FSM) that will act as the system's controller**. You must debug the FSM until it works correctly and **include its annotated simulation waveform in your report**.

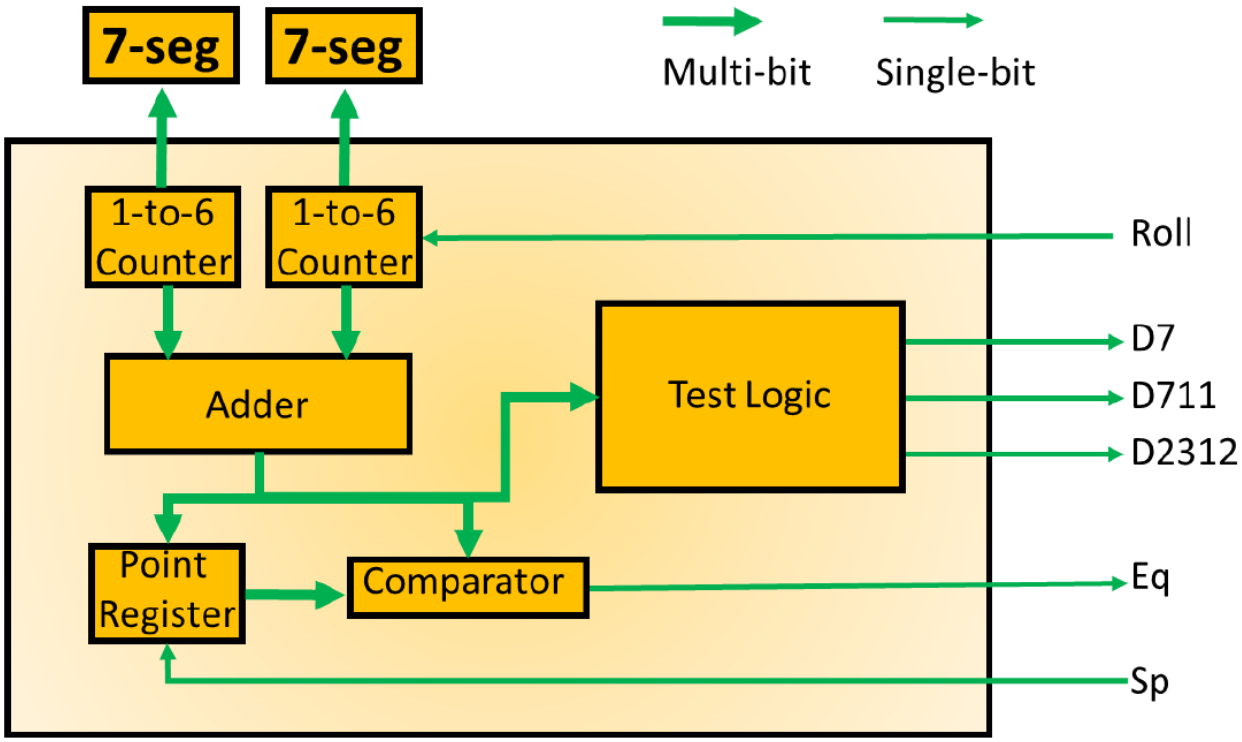

Figure 1: Data path

Complete system

Finally, integrate your verified controller and datapath to build the complete system as shown in Figure 2.

The system is controlled by two debounced push buttons: **Reset** and **Roll**. Outputs are shown on **two 7-segment displays** (for dice values) and **two LEDs for Win and Lose**. To begin a new game **Reset** is pressed. To roll the dice, The **Roll** button is pressed and held; the dice values are captured and displayed upon its release. If neither the **Win** nor **Lose** LED is lit, the player must roll again. After a win or loss, the game halts until "Reset" is pressed to start over.

Signals values are defined as follows:

- D7 = 1 if the sum of the dice is 7
- D711 = 1 if the sum of the dice is 7 or 11,
- D2312 = 1 if the sum of the dice is 2, 3, or 12,
- Eq = 1 if the sum of the dice equals the number stored in the point register,
- Roll = 1 enables the dice counters,
- Sp = 1 causes the sum to be stored in the point register,
- Win = 1 turns on the win light,

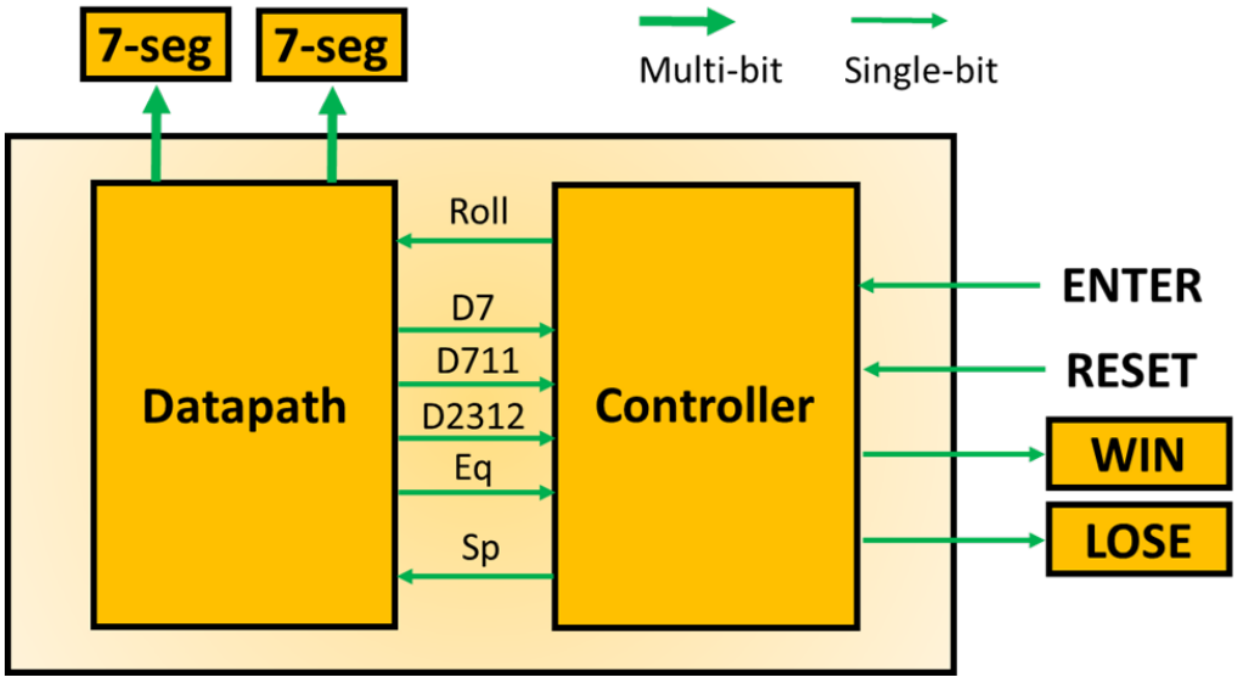

Figure 2: Complete system

- Lose = 1 turns on the lose light.

Debug and simulate this final design until it functions correctly. Once it is working, you **must include an annotated simulation waveform for the full system in your report** and prepare to demonstrate your project to the TA.

Evaluation Criteria

Datapath (75% Total):

- Counters 15%
- 7 Segment 15%
- Adder 10%
- Point Register 10%
- Comparator 10%
- Test Logic 15%
  - D7 5%
  - D711 5%
  - D2312 5%

Controller (25% Total)

Extra: Minimize the cost of circuit

Acknowledgments

This work is adapted from “Final Project: Design of a Dice Game” by Dalhouse University, available at http://mems.ece.dal.ca/eced4260/lab4.pdf.