UNIVERSITY OF TEHRAN
Electrical and Computer Engineering Department
ECE 367, Digital Logic Circuits – Fall 1397
Computer Assignment 6
RTL Processing Element Design and Implementation
Due week 15 of the semester

Taylor series is one of well-known methods to compute mathematical functions such as *sin(x)*, *cos(x)*, *exp*, etc. In this problem you are to design a sequential circuit that computes an approximation of *tan x* using the first 8 terms of its Taylor expansion. The numbers B_{2n} are Bernoulli numbers.

$$\tan x = \sum_{n=1}^{\infty} \frac{B_{2n}(-4)^n\,(1-4^n)}{(2n)!}\,x^{2n-1} \qquad = x + \frac{x^3}{3} + \frac{2x^5}{15} + \cdots \qquad \text{for } |x| < \frac{\pi}{2}$$

$$\tan x = x + \tfrac{1}{3}x^3 + \tfrac{2}{15}x^5 + \tfrac{17}{315}x^7 + \tfrac{62}{2835}x^9 + \ldots$$

The algorithm you chose to implement should use an array multiplier and a ROM for series coefficients.

Shown below is the block diagram of the module approximating *tan()*. The module accepts a 16-bit fixed point value on *x* between 0 and π/2 after *start* is asserted. After that, computation is started. During the computation, the *busy* signal is asserted. After the completion of the computation, the result becomes available on output *y*, *busy* is deactivated, and *ready* is issued.

As mentioned, *x* is between 0 and π/2, and all numbers are represented in 16-bit fixed point format. In addition, a 16-bit fixed point adder and a 16-bit fixed point array multiplier are available as datapath components. The series coefficients must be pre-calculated and stored in a combinational lookup table. The table has four address lines and a 16-bit data output.

A) Generate a ROM in Quartus II for the required memory of factorial calculations.
B) Design the datapath of module *tan(x)*, and implement it in Quartus II.
C) Write a Verilog description for the controller of module *tan(x)*.
D) Complete the datapath and controller of your circuit and develop a testbench for it.