UNIVERSITY OF TEHRAN
Electrical and Computer Engineering Department
Digital Logic Design, ECE 367, Fall 1397
Computer Assignment 3
Small-scale RT Level Components, Iterative Logic
Week 7

Name:
Date:

The problem for this assignment is a circuit that calculates the number of 1's on its data inputs. The circuit that is to be designed has 127 inputs, and it is built of cascadable modules in a regular structure.

1. The OC3 circuit that you designed in CA1 was a simple full-adder or a 1-bit adder. Based on delay values from this circuit, write a parametrized n-bit adder that uses n to adjust the size and delay value of the adder. The adder module uses **#parameter(…)** construct in its header part. For the delay values assume the adder is realized as a Ripple-carry adder.
2. Test the adder of Part 1 for n value of 4 using a Verilog testbench. Use constructs such as **repeat** and **$random()** for test data generation.
3. Using Verilog **generate** statement wire n-bit adders (where n is 1 to 6) in a tree structure to build a 127-bit one's counter.
4. Test your design of Part 3 for functionality and timing using a Verilog testbench. Among other tests, in the testbench generate a 127 bit Marchinbg-1 data generator for providing data to your counter.