UNIVERSITY OF TEHRAN
Electrical and Computer Engineering Department
Digital Logic Design, ECE 367, Fall 1397
Computer Assignment 2
Gate, and Expressions in Verilog
Week 5

Name:
Date:

The problem for this assignment is a circuit that calculates the number of 1's on its data inputs. The circuit that you start with has three inputs (n=2) and it is cascadable to build any circuit with 2^n-1 inputs. Assume complement of all inputs are available and use Verilog ~ operation for getting the complement of circuit primary inputs.

1. Using several copies of OC3 of Part 2 of Computer Assignment 1 in a structural fashion, build a circuit for counting the number of ones on its seven data inputs (n is 3). We refer to this circuit as an OC7 circuit.
2. Repeat the above, but use the OC3 circuit described using **assign** statements (circuit of Part 6 of Computer Assignment 1).
3. Generate a testbench for the circuits of Part 1 and Part 2, and compare the timings.
4. Now design an OC15 circuit (n=4), using OC7 and OC3 circuits of Part 1 of this assignment and Part 2 of Computer Assignment 1. Test this circuit and calculate its worst case delay.