

Analog IC Cheat Sheet

1

1 Introduction

$$\text{Voltage gain } (A_v) \equiv \frac{v_o}{v_i} \quad (1)$$

$$\text{Current gain } (A_i) \equiv \frac{i_o}{i_i} \quad (2)$$

$$\text{Power gain } (A_p) \equiv \frac{\text{load power } (P_L)}{\text{input power } (P_I)} = \frac{v_o i_o}{v_i i_i} A_p = A_v A_i \quad (3)$$

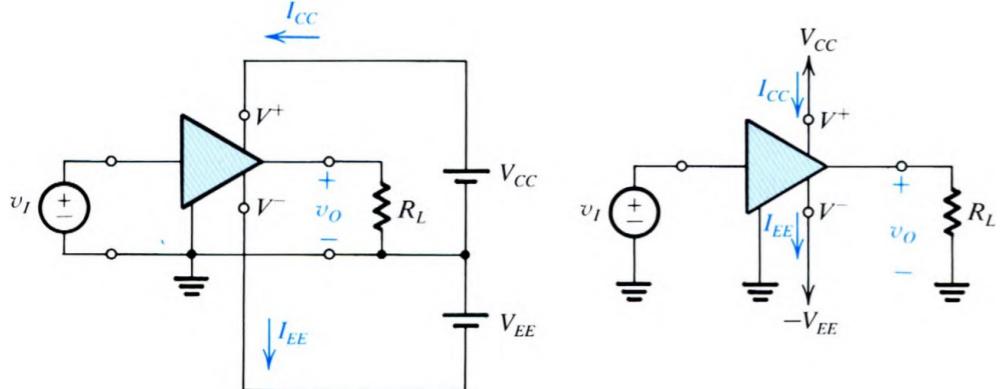
$$\text{Voltage gain in decibels} = 20 \log |A_v| \text{ dB} \quad (4)$$

$$\text{Current gain in decibels} = 20 \log |A_i| \text{ dB} \quad (5)$$

$$\text{Power gain in decibels} = 10 \log A_p \text{ dB} \quad (6)$$

Voltage, Current $\rightarrow 20$, Power $\rightarrow 10$

$$A_P(\text{dB}) = \frac{1}{2} (A_v(\text{dB}) + A_i(\text{dB})) \quad (7)$$



$$V_{\text{rms}} = \frac{V_{\text{peak}}}{\sqrt{2}} \quad (8)$$

The input power

$$P_I = V_i \text{ rms} I_i \text{ rms} = \frac{V_i \text{ peak} I_i \text{ peak}}{\sqrt{2} \times \sqrt{2}} = \frac{V_i \text{ peak} I_i \text{ peak}}{2} \quad (9)$$

The load power :

$$P_{\text{load}} = V_o \text{ rms} I_o \text{ rms} = I_o^2 \text{ rms} \times R_L = \frac{V_o^2 \text{ rms}}{R_L} \quad (10)$$

the dc power delivered to the amplifier

¹Taha Ahmed (Differential amplifiers not included)

$$P_{\text{dc}} = V_{CC} I_{CC} + V_{EE} I_{EE} \quad (11)$$

, the power-balance equation for the amplifier (conservation of power)

$$P_{\text{dc}} + P_I = P_L + P_{\text{dissipated}} \quad (12)$$

the amplifier power efficiency

$$\eta = \frac{P_L}{P_{\text{dc}} + P_I} \times 100 \equiv \frac{P_L}{P_{\text{dc}}} \times 100 \quad (13)$$

1. Q Consider a microphone producing a sinusoidal signal that is 400-mV peak $\rightarrow v_i$. It delivers 10- μ A peak sinusoidal current $\rightarrow i_i$ to an amplifier that operates from ± 1 -V power supplies $\rightarrow V_{CC}, V_{EE}$. The amplifier delivers a 0.8 – V peak sinusoidal $\rightarrow v_o$ to a speaker load with $32 - \Omega$ resistance $\rightarrow R_L$. The amplifier draws a current of 30 mA $\rightarrow I_{\text{dc}}$ from each of its two power supplies.

Find the voltage gain, $\rightarrow A_v$

the current gain, $\rightarrow A_i$

the power gain, $\rightarrow A_p$

the power drawn from the dc supplies, $\rightarrow P_{\text{dc}}$

the power dissipated in the amplifier, $\rightarrow P_{\text{dissipated}}$

and the amplifier efficiency. $\rightarrow \eta$

1. A How to solve?

$$A_v = \frac{v_o}{v_i} \quad A_v = 20 \log \frac{v_o}{v_i} = \text{dB}$$

$$A_i = \frac{I_o}{I_i} = \frac{v_o \times R_L}{I_i} = \text{dB} \quad A_i = 20 \log \frac{v_o}{I_i} = \text{dB}$$

$$P_L = V_{o \text{ rms}} I_{o \text{ rms}} = \frac{v_o i_o}{\sqrt{2}} = \text{mW}$$

$$P_I = V_{i \text{ rms}} I_{i \text{ rms}} = \frac{v_i i_i}{\sqrt{2} \sqrt{2}} = \text{W}$$

$$A_p = A_v A_i \quad A_p = 10 \log A_v A_i = \text{dB}$$

$$P_{\text{dc}} = V_{EE} I_{\text{dc}} + V_{CC} I_{\text{dc}} = \text{mW}$$

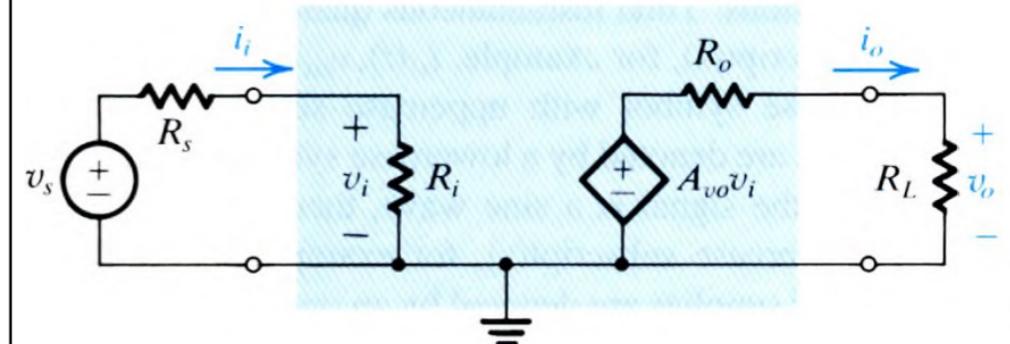
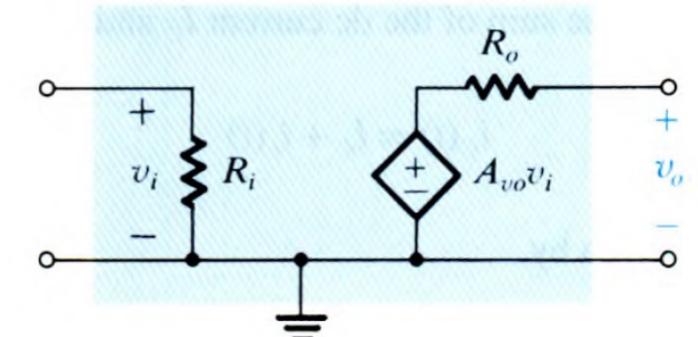
$$P_{\text{dissipated}} = P_{\text{dc}} + P_I - P_L = \text{mW}$$

$$\eta = \frac{P_L}{P_{\text{dc}}} \times 100 = \% \quad (14)$$

To avoid saturation

$$\frac{L_-}{A_v} \leq v_i \leq \frac{L_+}{A_v} \quad (14)$$

2 Circuit Models for Amplifiers



R_i : input resistance (ideally ∞)

R_o : output resistance (ideally 0)

A_v : voltage gain

A_{vo} : Open circuit voltage gain

(in case of no R_L)

$$v_o = A_{vo} v_i \quad (15)$$

$$= A_{vo} v_s \text{ (in case of no } R_s) \quad (16)$$

(in case of R_L)

$$v_o = A_{vo} v_i \frac{R_L}{R_L + R_o} \quad (17)$$

$$v_i = v_s \frac{R_i}{R_i + R_s} \quad (18)$$

$$A_v \equiv \frac{v_o}{v_i} = A_{vo} \frac{R_L}{R_L + R_o} \quad (\text{therefore : } A_v < A_{vo}) \quad (19)$$

(overall voltage gain:)

$$\frac{v_o}{v_s} = A_{vo} \frac{R_i}{R_i + R_s} \frac{R_L}{R_L + R_o} = A_v \frac{R_i}{R_i + R_s} \quad (20)$$

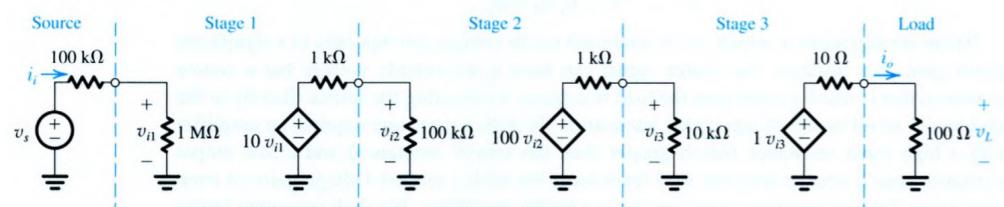
$$\frac{v_o}{v_s} = A_{vo} \frac{R_i}{R_i + R_s} \frac{R_L}{R_L + R_o} = A_v \frac{R_i}{R_i + R_s} \quad (21)$$

3 Cascaded Amplifier

The overall gain of an amplifier of n stages :

$$A_v = A_{v1} \times A_{v2} \times A_{v3} \times \cdots \times A_{vn} \quad (22)$$

2. Q The following figure depicts an amplifier composed of a cascade of three stages. The amplifier is fed by a signal source with a source resistance of $100 \text{ k}\Omega$ and delivers its output into a load resistance of 100Ω . The first stage has a relatively high input resistance and a modest gain factor of 10. The second stage has a higher gain factor but lower input resistance. Finally, the last, or output, stage has unity gain but a low output resistance.



Find:

1) the overall voltage gain i.e. $\frac{v_L}{v_s}$

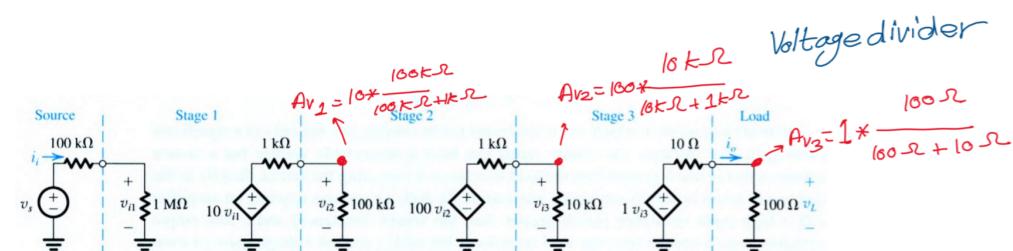
2) the current gain

3) the power gain.

2. A

How to solve ?

Find A_{v1}, A_{v2}, A_{v3}



The total gain

$$A_v \equiv \frac{v_L}{v_s} = A_{v1} A_{v2} A_{v3} = \checkmark$$

In decibels

$$A_v (\text{dB}) = 20 \log \checkmark = \checkmark \text{ dB}$$

To find the voltage gain from source to load, we multiply A_v by the factor representing the loss of gain at the input; that is,

$$\begin{aligned} \frac{v_L}{v_s} &= \frac{v_L}{v_{i1}} \frac{v_{i1}}{v_s} = A_v \frac{v_{i1}}{v_s} \\ &= \checkmark \times \frac{1\text{M}\Omega}{1\text{M}\Omega + 100\text{k}\Omega} \end{aligned}$$

In decibels

$$\frac{v_L}{v_s} = 20 \log \checkmark = \checkmark \text{ dB}$$

2) The current gain is found as follows:

$$A_i \equiv \frac{i_o}{i_i} = \frac{v_L/100\Omega}{v_{i1}/1\text{M}\Omega} = 10^4 \times A_v = \checkmark \text{ A/A}$$

In decibels

$$A_i (\text{dB}) = 20 \log \checkmark = \checkmark \text{ dB}$$

3) The power gain

$$\begin{aligned} A_p \equiv \frac{P_L}{P_I} &= \frac{v_L i_o}{v_{i1} i_i} \\ &= A_v A_i = \checkmark \times \checkmark = \checkmark \end{aligned}$$

$$A_p (\text{dB}) = 10 \log(6.69 \times 10^9) = 98.25 \text{ dB}$$

3. Q Voltage amplifier delivers 200 mV across a load resistance of $1 \text{ k}\Omega$, it is found that the output voltage decreased by 5mV when the load resistance decreased to 780Ω . What the values of open circuit output voltage and output resistance of the amplifier

Consider an amplifier with the following values:

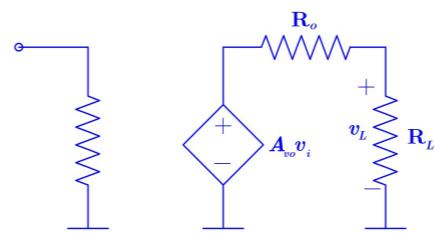
Find the output resistance and the voltage gain, then draw a graph represents the relation between R_L and V_L

3. A

Note that :

When $R_L = 780\Omega$, $V_L = 195\text{mV}$

When $R_L = 1000\Omega$, $V_L = 200\text{mV}$



$$v_L = A_{vo} v_i \frac{R_L}{R_L + R_o}$$

substitute twice (two equations, two unknowns)

$$\therefore 0.195 = A_{vo} v_i \frac{780}{780 + R_o}$$

$$\therefore 0.2 = A_{vo} v_i \frac{1000}{1000 + R_o}$$

divide (1) by (2)

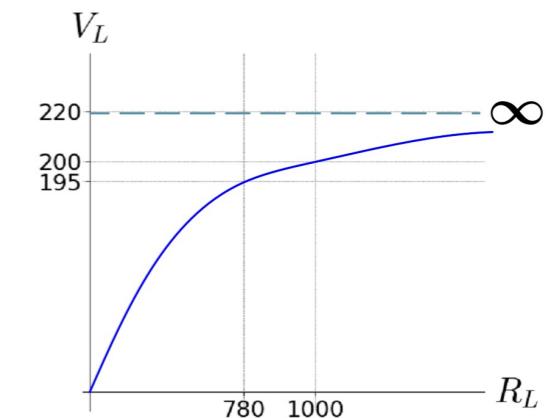
$$\therefore 0.975 = \frac{780}{780 + R_o} \times \frac{1000 + R_o}{1000}$$

$$\therefore R_o = 100\Omega$$

Substitute in (1)

$$\therefore 0.195 = A_{vo} v_i \frac{780}{780 + 100}$$

$\therefore A_{vo} v_i = 0.22$ (open circuit voltage gain (when $R_L \rightarrow \infty$, $v_L \rightarrow 220 \text{ mV}$))



MOSTFET

threshold voltage (V_t) : The value of v_{GS} at which a sufficient number of mobile electrons accumulate under the gate to form a conducting channel

overdrive voltage (v_{OV}) (aka overdrive voltage) : The excess of v_{GS} over V_t

$$v_{ov} \equiv v_{GS} - V_t \quad (23)$$

We can express the magnitude of the electron charge in the channel by

$$|Q| = C_{ox}(WL)v_{ov} \quad (24)$$

where

C_{ox} : the oxide capacitance, (F/m^2)

W : width of the channel

L : the length of the channel

oxide capacitance (C_{ox}): capacitance of the parallel-plate capacitor per unit gate area

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

where

ϵ_{ox} : permittivity of the silicon dioxide

t_{ox} : oxide thickness

4. Q Calculate the oxide capacitance, total capacitance For a MOSFET fabricated in this technology with a channel length $L = 0.18 \mu\text{m}$, width $W = 0.72 \mu\text{m}$ and oxide thickness 4 nm, given that the permittivity of the silicon dioxide equals $3.45 \times 10^{-11} \text{ F/m}$

4. A

How to solve ?

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \text{✓ F/m}^2$$

$$C = C_{ox}WL = \text{✓ F}$$

process transconductance (k'_n): The product of each of μ_n and C_{ox} (note the subscript n denotes n channel)

$$k'_n = \mu_n C_{ox}$$

aspect ratio $(\frac{W}{L})$: the channel width W divided by the channel length L . It is a dimensionless quantity that is determined by the device design

MOSFET transconductance parameter (k_n): The product of the process transconductance parameter (k'_n) and the transistor aspect ratio $(\frac{W}{L})$

$$k_n = k'_n(W/L) = (\mu_n C_{ox})(W/L) \quad (25)$$

The $i_D - v_{GS}$ Characteristic

When the MOSFET is used to design an amplifier, it is operated in the saturation region as a voltage-controlled current source with the control relationship described by

$$i_D = \frac{1}{2} k'_n \left(\frac{W}{L} \right) (v_{GS} - V_t)^2 \quad (26)$$

or in terms of v_{OV}

$$i_D = \frac{1}{2} k'_n \left(\frac{W}{L} \right) v_{OV}^2$$

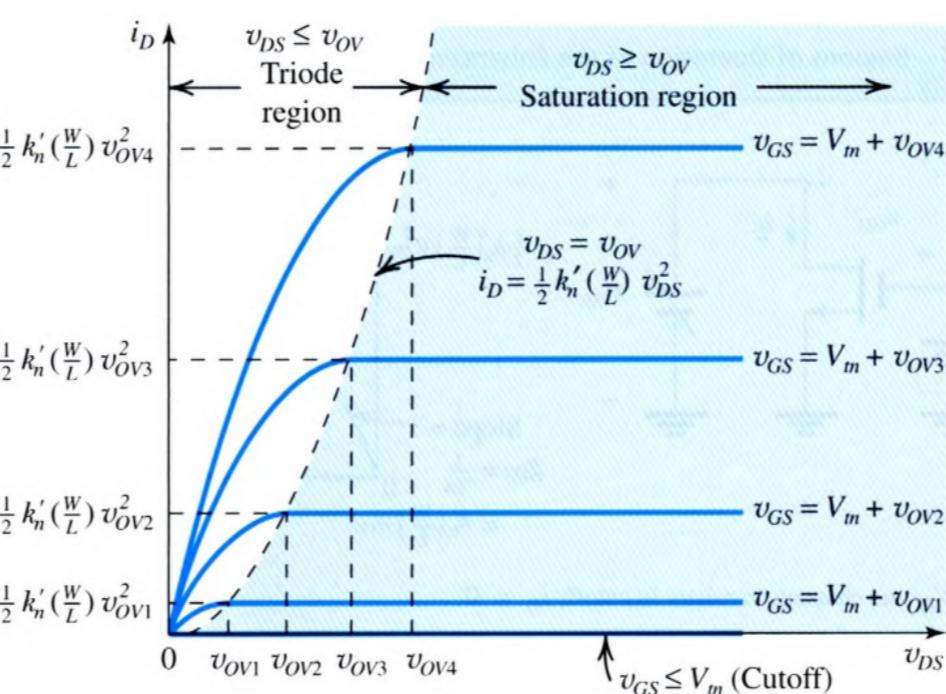


Figure 1: The $i_D - v_{DS}$ characteristics for an enhancement-type NMOS transistor.

in practice, increasing v_{DS} beyond a certain point causes the channel pinch-off point to move slightly away from the drain. This reduces the channel length, resulting in channel-length modulation, and causes i_D to increase with v_{DS}

$$i_D = \frac{1}{2} k'_n \left(\frac{W}{L} \right) (v_{GS} - V_{tn})^2 (1 + \lambda v_{DS}) \quad (27)$$

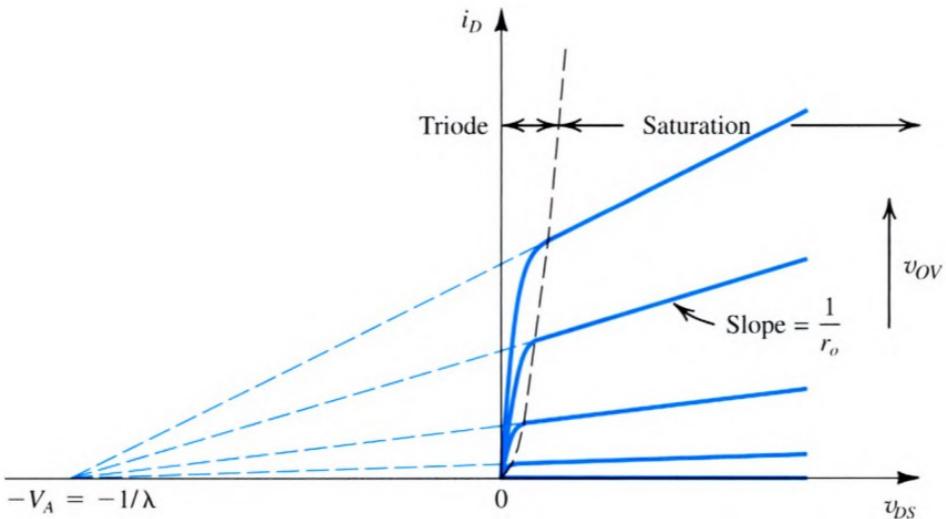


Figure 2: Effect of v_{DS} on i_D in the saturation region. The MOSFET parameter V_A depends on the process technology and, for a given process, is proportional to the channel length L .

from the previous figure:

$$i_D = 0 \quad \therefore (1 + \lambda v_{DS} = 0) \quad (28)$$

$$\therefore v_{DS} = \frac{-1}{\lambda} \quad V_A = V'_A L \quad (29)$$

where

V'_A : process-technology dependent (constant) $\left(\frac{V}{\mu\text{m}} \right)$ (range of $5 \left(\frac{V}{\mu\text{m}} \right)$ to $50 \left(\frac{V}{\mu\text{m}} \right)$)

V_A : Early voltage

3.1 Large-signal, equivalent-circuit model of the n -channel MOSFET

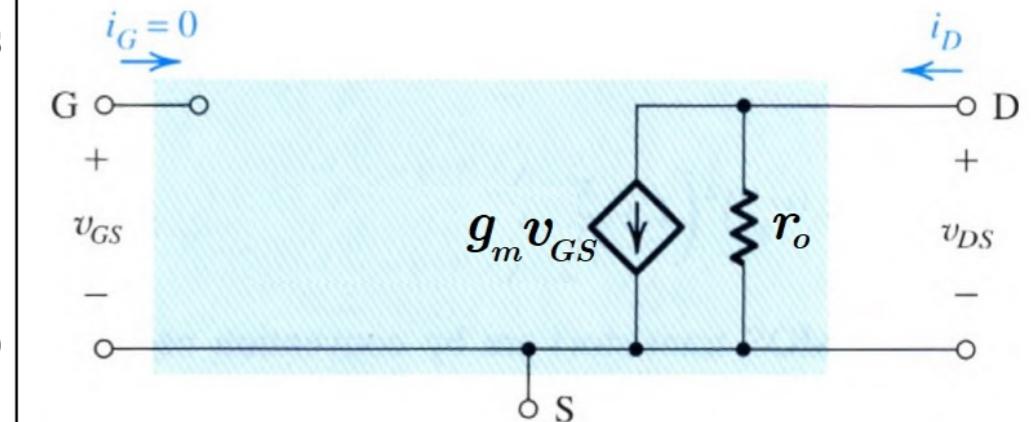


Figure 3: Large-signal, equivalent-circuit model of the n -channel MOSFET in saturation, incorporating the output resistance r_o . The output resistance models the linear dependence of i_D on v_{DS} and is given by)

the relation between v_{GS} and the current i_D can be models using g_m (transconductance)

$$g_m \equiv \frac{\partial i_D}{\partial v_{GS}} = \frac{\Delta i_D}{\Delta v_{GS}} = \frac{2i_d}{V_{OV}} \quad (30)$$

Defining the output resistance r_o

$$r_o \equiv \left. \frac{\partial v_{DS}}{\partial i_D} \right|_{v_{GS} \text{ constant}} \quad \therefore r_o = \frac{V_A}{i'_D} \quad (31)$$

where i_D is the drain current without channel-length modulation taken into account; that is:

$$i_D = \frac{1}{2} k'_n \left(\frac{W}{L} \right) (v_{GS} - V_{tn})^2 \quad (32)$$

5. Q Compare between n -channel MOSFET and p -channel MOSFET

	<i>n</i> -channel MOSFET	<i>p</i> -channel MOSFET
Symbol		
polarity of V_t	$V_{tn} \rightarrow$ positive	$V_{tp} \rightarrow$ negative
v_{OV}	$v_{OV} \equiv v_{GS} - V_{tp}$ +ve +ve +ve	$v_{OV} \equiv v_{GS} - V_{tp}$ -ve -ve -ve
In Saturation	$v_{DS} \geq v_{OV}$	$v_{DS} \leq v_{OV}$

5. A

6. Q for the following circuit , find the labeled node voltages. The NMOS transistors have $V_t = 0.9$ V and $k'_n(W/L) = 1.5$ mA/V².

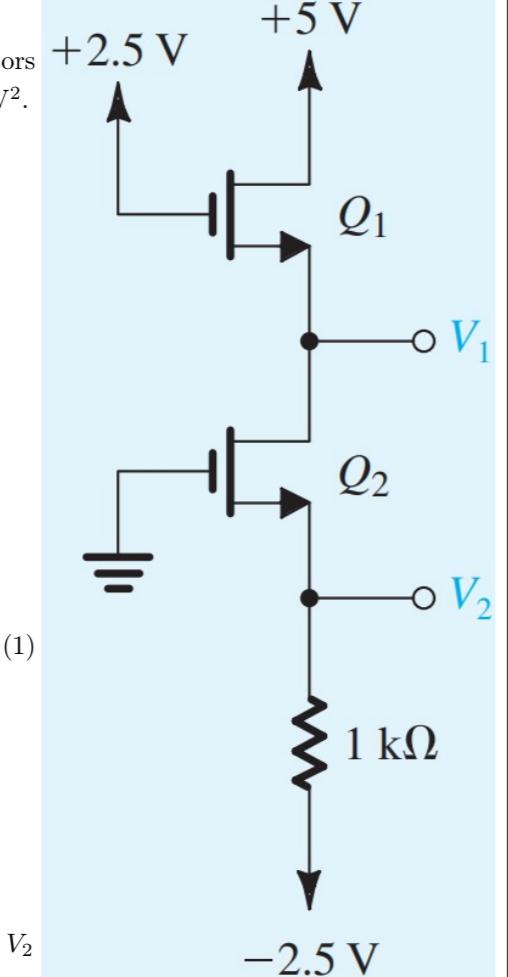
How to solve ?

Get

$$i_{D1} = \frac{1}{2}k'_n \left(\frac{W}{L} \right) (v_{GS} - V_t)^2$$

$$i_{D2} = \frac{1}{2}k'_n \left(\frac{W}{L} \right) (v_{GS} - V_t)^2$$

$$i_{D2} = \frac{V_2 - (-2.5)}{1000} = V_2 + 2.5 \text{ mA}$$



$$V_{GS} = V_G - V_S$$

$$\text{For } Q_1, V_{GS} = 2.5 - V_1$$

$$\text{For } Q_2, V_{GS} = 0 - V_2$$

Equate

 i_{D1} with i_{D2} to get a relation between V_1, V_2 Equate the two equations of i_{D2} to get V_2

7. Q for the following circuit , find the labeled node voltages. The NMOS transistors have $V_t = 0.9$ V and $k'_n(W/L) = 1.5$ mA/V².

How to solve?

Get

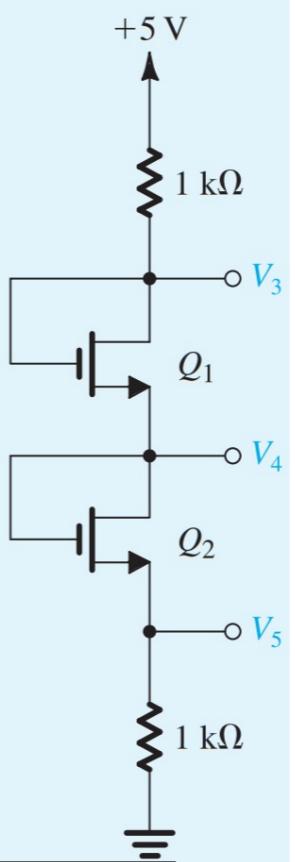
Get

$$i_{D1} = \frac{1}{2}k'_n \left(\frac{W}{L} \right) (v_{GS} - V_t)^2$$

$$i_{D2} = \frac{1}{2}k'_n \left(\frac{W}{L} \right) (v_{GS} - V_t)^2$$

$$i_{D2} = \frac{V_3 - (0)}{1000} = V_5 \text{ mA}$$

$$i_{D1} = \frac{5 - (V_3)}{1000} = 5 - V_3 \text{ mA}$$

Equate i_{D1} with i_{D2} 

Divide the two equations :

$$\frac{i_{D1}}{i_{D2}} = \checkmark$$

Relation between i_{D1} and i_{D2} is $i_{D1} = 1.5i_{D2}$

$$i_{D1} + i_{D2} = 200\mu\text{A}$$

$$\checkmark i_{D2} + i_{D2} = 200 \times 10^{-6} \text{ A}$$

$$i_{D2} = \checkmark \mu\text{A}$$

$$i_{D1} = \checkmark \mu\text{A}$$

Get

$$i_{D1} = \frac{1 - V_1}{5 \times 10^3} \text{ A}$$

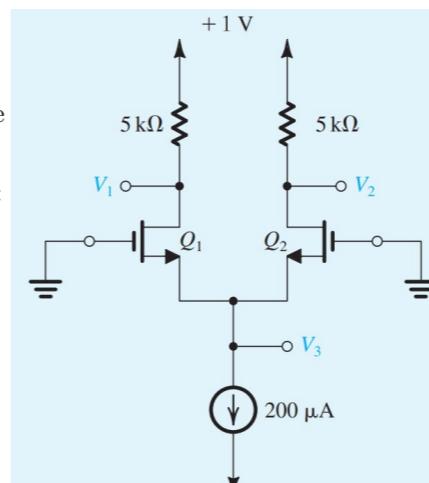
$$i_{D1} = \frac{1}{2}k'_n(W/L)_1 (v_G - V_t)^2$$

And get

 i_{D1}, i_{D2} from the ohms law then substitute

4 MOSFET Circuit Model

4.1 The π Equivalent-Circuit Model



8. Q In the circuit of the following figure , transistors and Q_2 have $V_t = 0.5V$, and the process transconductance parameter $k'_n = 400\mu\text{A}/\text{V}^2$ Find V_1, V_2 , and V_3 for each of the following cases:

- a) $(W/L)_1 = (W/L)_2 = 10$
- b) $(W/L)_1 = 1.5(W/L)_2 = 10$

8. A How to solve?

A) Due to the similarity of the circuit :

$$i_{D1} + i_{D2} = 200\mu\text{A}$$

Therefore Drain current $i_{D1} = i_{D2}$ is $100\mu\text{A}$, and $V_1 = V_2$

Get

$$i_{D1} = \frac{1 - V_1}{5 \times 10^3} \text{ A}$$

$$i_{D1} = \frac{1}{2}k'_n(W/L)_1 (v_G - V_t)^2$$

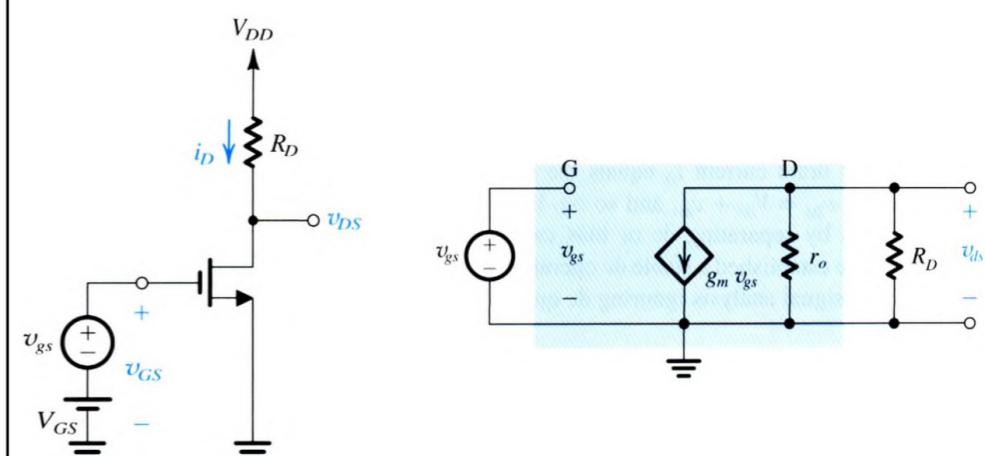
substitute with $i_{D1} = 100\mu\text{A}$ in both equations

$$\text{b) } (W/L)_1 = 10$$

$$(W/L)_2 = 6.66$$

$$i_{D1} = \frac{1}{2}k'_n(W/L)_1 (v_{GS} - V_t)^2$$

$$i_{D2} = \frac{1}{2}k'_n(W/L)_2 (v_{GS} - V_t)^2$$

Figure 4: Small-signal equivalent π model .

4.2 The T Equivalent-Circuit Model

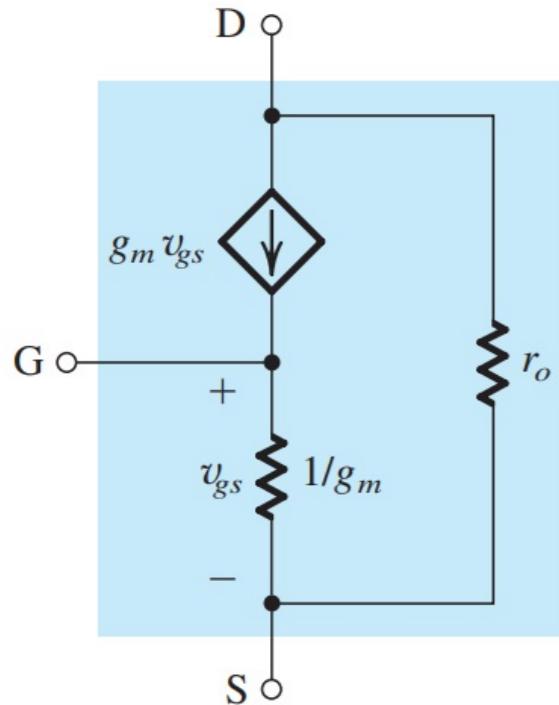


Figure 5: Small-signal equivalent T model .

5 The Three Basic Configurations of MOSFET Circuits

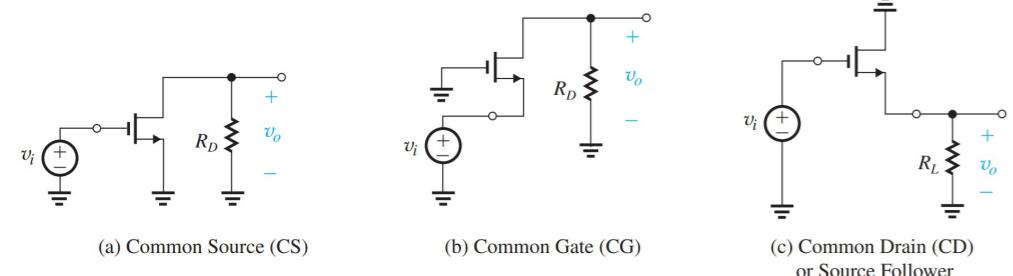


Figure 6: The basic configurations of transistor amplifiers

5.1 The Common-Source (CS) Amplifiers

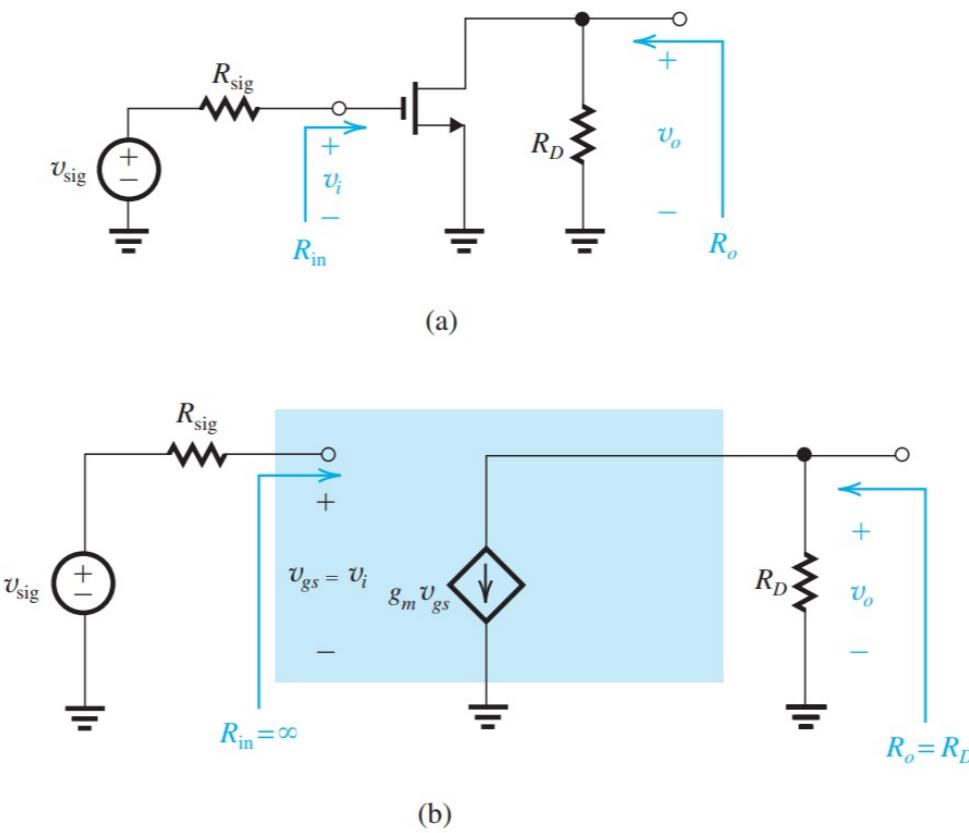


Figure 7: (a) Common-source amplifier fed with a signal v_{sig} from a generator with a resistance R_{sig} (b) The common-source amplifier with the MOSFET replaced with its π model.

from the circuit model:

$$R_{in} = \infty \quad (33)$$

$$v_{sig} = v_i = v_{gs} \quad (34)$$

$$v_o = -g_m v_{gs} R_D \quad (35)$$

$$A_{vo} \equiv \frac{v_o}{v_i} = \frac{-g_m v_{gs} R_D}{v_{gs}} = -g_m R_D \quad (36)$$

$$R_o = R_D \quad (37)$$

If a load resistance R_L is connected across R_D , the voltage gain A_v can be obtained from

$$A_v = A_{vo} \frac{R_L}{R_L + R_o} = -g_m R_D \frac{R_L}{R_L + R_o} = -g_m (R_D \| R_L) \quad (38)$$

since $R_{in} = \infty$ and thus $v_i = v_{sig}$, the overall voltage gain G_v is equal to A_v .

$$G_v \equiv \frac{v_o}{v_{sig}} = -g_m (R_D \| R_L) \quad (39)$$

5.2 The Common-Gate (CG) Amplifiers

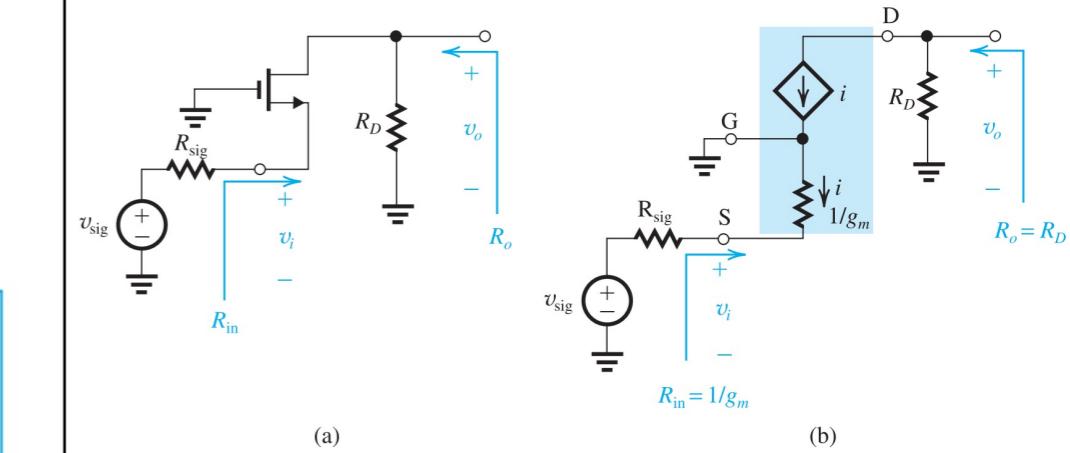


Figure 8: (a) Common-gate amplifier (b) Equivalent circuit of the common-gate replaced with its T model.

$$R_{in} = \frac{1}{g_m} \quad (40)$$

$$v_o = -i R_D \quad (41)$$

$$i = -\frac{v_i}{1/g_m} \quad (42)$$

$$v_i = -i \times 1/g_m \quad (43)$$

$$A_{vo} \equiv \frac{v_o}{v_i} = \frac{-i R_D}{-i \times 1/g_m} = g_m R_D \quad (44)$$

$$R_o = R_D \quad (45)$$

$$\frac{v_i}{v_{sig}} = \frac{R_{in}}{R_{in} + R_{sig}} = \frac{1/g_m}{1/g_m + R_{sig}} \quad (46)$$

$$G_v = \frac{v_o}{v_{sig}} = \frac{v_i}{v_{sig}} \times \frac{v_o}{v_i} \quad (47)$$

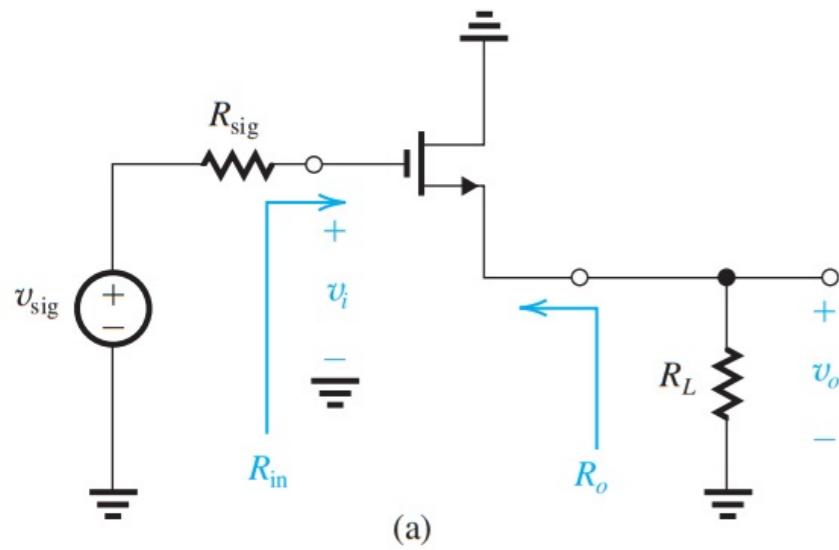
In case of resistance R_L connected at the output

$$\frac{v_o}{v_i} = g_m (R_D \| R_L) \quad (48)$$

$$G_v = \frac{1/g_m}{R_{sig} + 1/g_m} [g_m (R_D \| R_L)] \quad (49)$$

$$\therefore G_v = \frac{R_D \| R_L}{R_{sig} + 1/g_m} \quad (50)$$

5.3 The Common-Drain (CD) Amplifiers (Source Follower)



since $R_{in} = \infty$ and thus $v_i = v_{sig}$, the overall voltage gain G_v is equal to A_v

$$A_{vo} = 1$$

$$R_o = 1/g_m$$

$$G_v = A_v = \frac{R_L}{R_L + 1/g_m}$$

6 The MOS Current Mirror

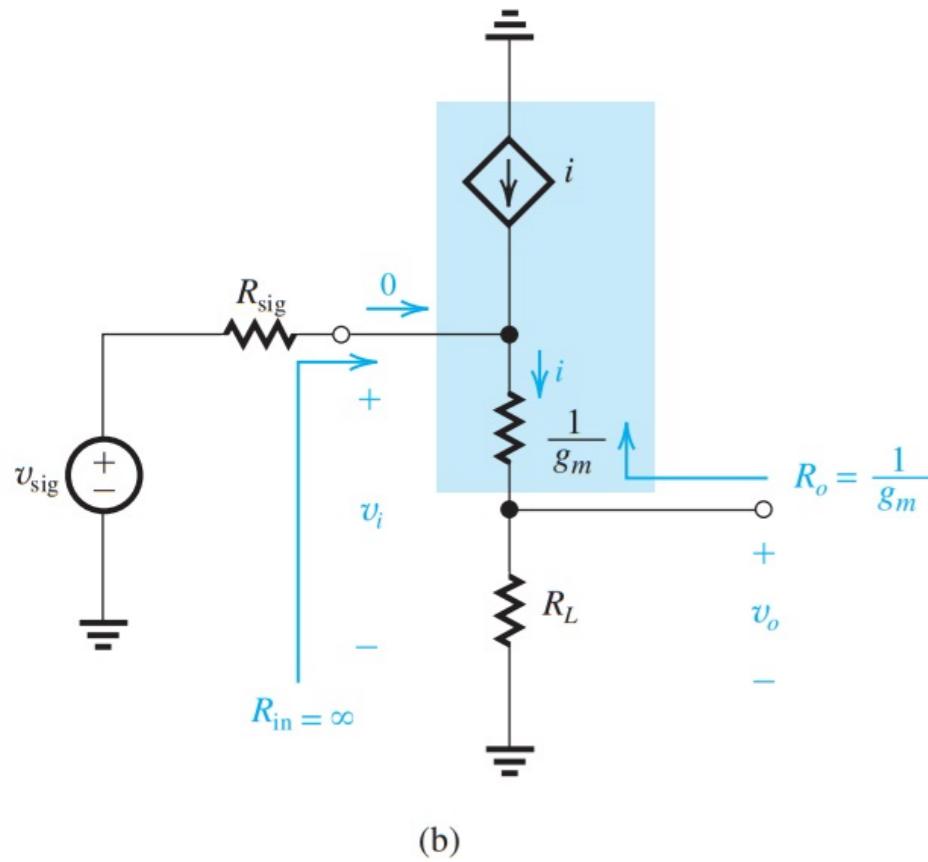


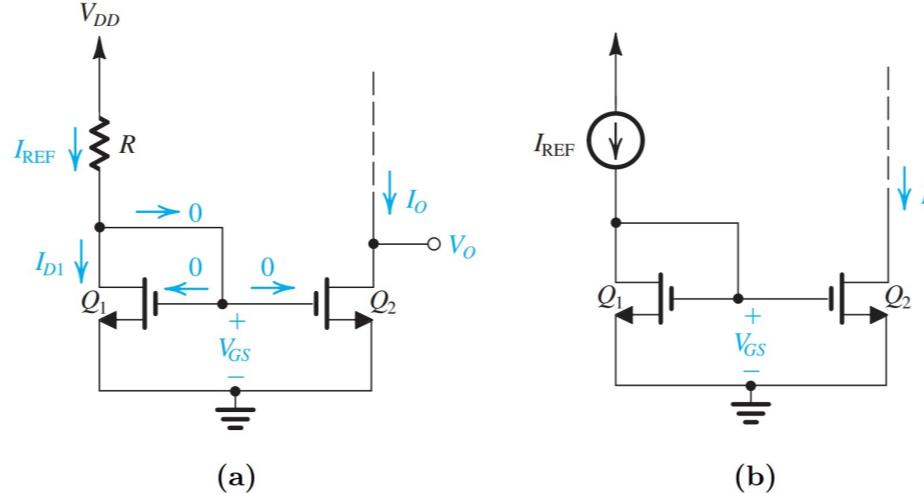
Figure 10: (a) Circuit for a basic MOSFET constant current source ; (b) Basic MOSFET current mirror.

Figure 9: (a) Common-drain amplifier or source follower (b) Equivalent circuit of the source follower obtained by replacing the MOSFET with its T model.

$$R_{\text{in}} = \infty \quad (\text{input current} = 0)$$

$$A_v \equiv \frac{v_o}{v_i} = \frac{R_L}{R_L + 1/g_m} \quad (52)$$

Setting $R_L = \infty$, we obtain :



The output resistance of $Q_2 = r_{o2}$,

$$\frac{I_O}{I_{\text{REF}}} = \frac{(W/L)_2}{(W/L)_1} \quad (56)$$

and where V_{A2} is the Early voltage of Q_2 .

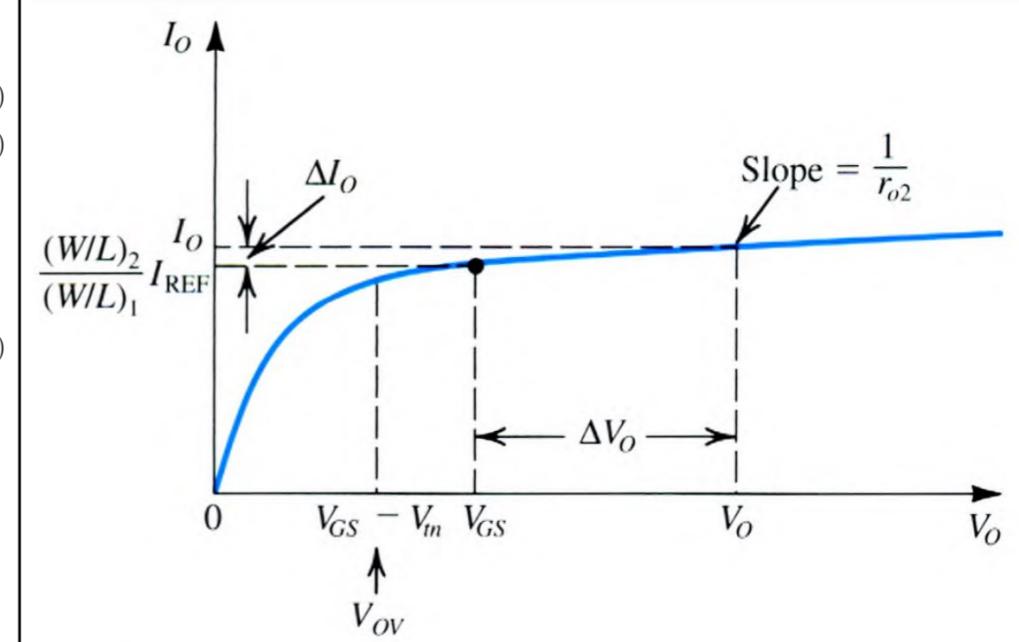


Figure 11: Output characteristic of the current mirror

9. Q Given $V_{DD} = 3$ V and using $I_{REF} = 100\mu A$, design the current source circuit to obtain an output current whose nominal value is $100\mu A$. Find R if Q_1 and Q_2 are matched and have channel lengths of $1\mu m$, channel widths of $10\mu m$, $V_t = 0.7$ V, and $k'_n = 200\mu A/V^2$. What is the lowest possible value of V_o ? Assuming that for this process technology, the Early voltage $V'_A = 20$ V/ μm , find the output resistance of the current source. Also, find the change in output current resulting from a $+1 - V$ change in V_o .

9. A How to solve

get V_{OU}

$$I_{D1} = I_{\text{REF}} = \frac{1}{2} k'_n \left(\frac{W}{L} \right)_1 V_{OV}^2$$

$V_{OV} = \checkmark$

get V_{GS}

$$V_{GS} = V_t + V_{OV} = \checkmark \text{ V}$$

$$R = \frac{V_{DD} - V_{GS}}{I_{BEE}} = \checkmark \Omega$$

$$V_{O \text{ min}} = V_{OW}$$

Early voltage $V'_A = 20$ V/ μm and $L = 1\mu\text{m}$, \therefore

$$V_A = 20 \times 1 = 20 \text{ V}$$

$$r_{o2} \frac{V_A}{I_O|_{\text{nominal}}} = \checkmark \Omega$$

the change in output current resulting from a $+1 - V$ change in V_o .

$$\Delta I_O = \frac{\Delta V_O}{r_{c2}} = \frac{1 \text{ V}}{r_{c2}} = \checkmark \mu\text{A}$$

Once a constant current has been generated, it can be replicated to provide dc bias or load currents for the various amplifier stages in an IC. Current mirrors can obviously be used to implement this current-steering function.

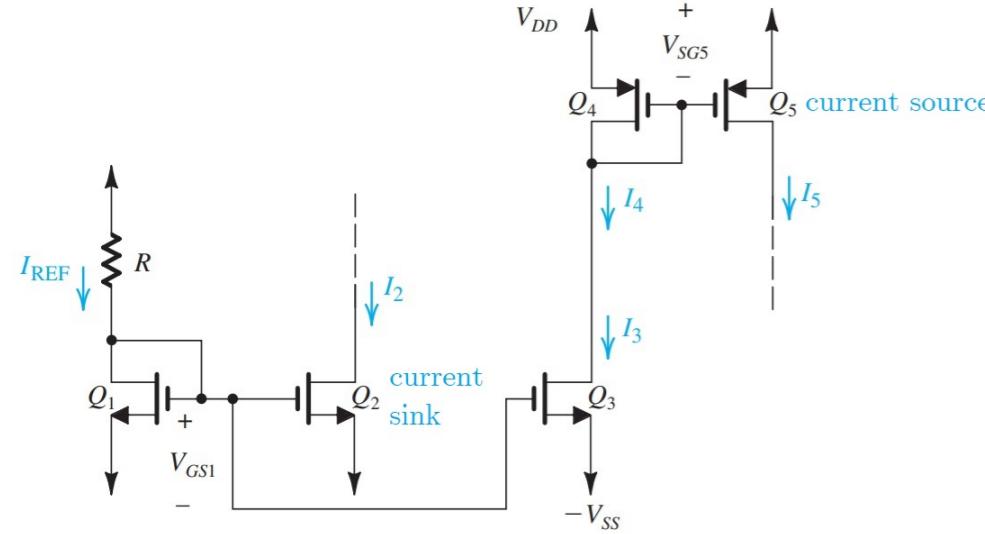


Figure 12: A current-steering circuit

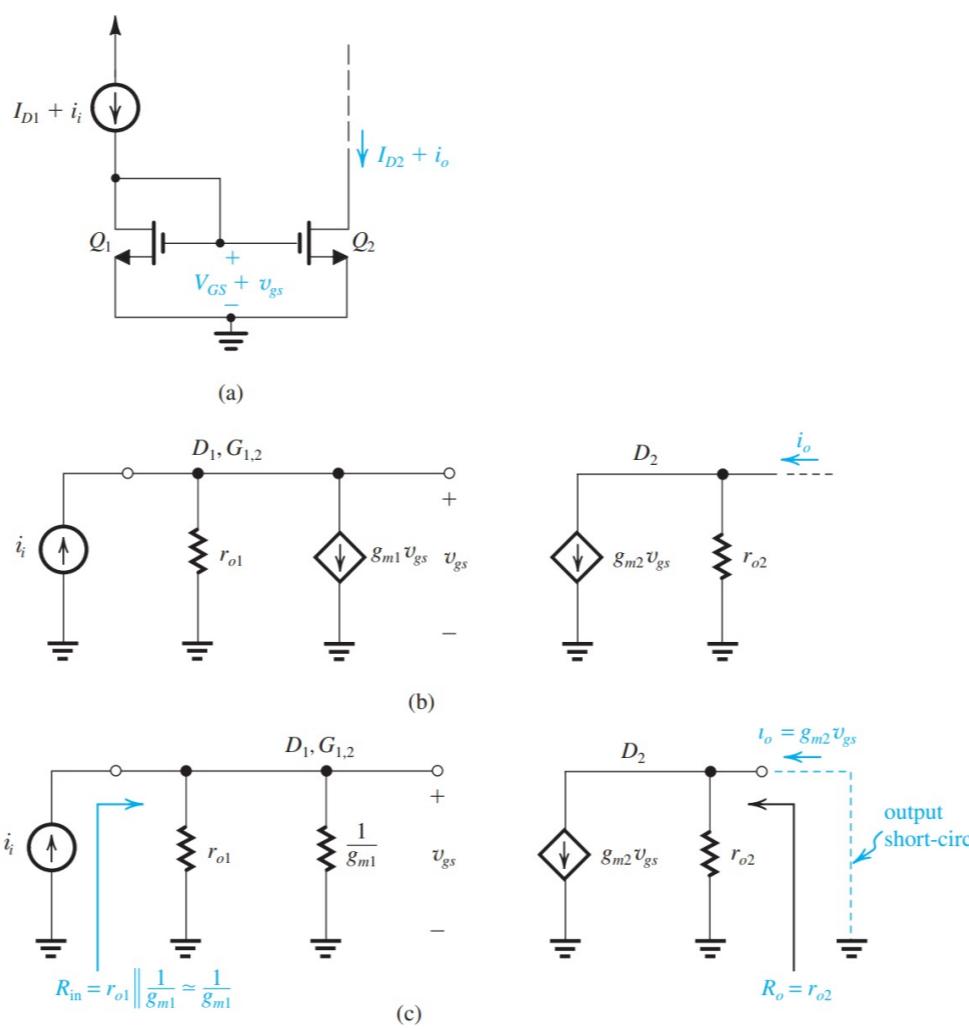


Figure 13: Obtaining the small-signal parameters of the MOS current mirror as a current amplifier.

Input resistance

$$R_{in} = r_{o1} \parallel \frac{1}{g_{m1}} \simeq \frac{1}{g_{m1}} \quad (61)$$

Output resistance

$$R_o = r_{o2} \quad (62)$$

Short circuit current gain

$$A_{is} = \left. \frac{i_o}{i_i} \right|_{v_{d2}=0} = \frac{g_{m2}v_{gs}}{i_i} \simeq \frac{g_{m2}i_i/g_{m1}}{i_i} \quad (63)$$

Thus :

$$A_{is} = \frac{g_{m2}}{g_{m1}} \quad (64)$$

Substituting for $g_{m1,2} = \mu_n C_{ox} (W/L)_{1,2} V_{OV}$, where V_{OV} is the overdrive voltage at which Q_1 and Q_2 are operating, yields for the short-circuit current gain

$$A_{is} = \frac{(W/L)_2}{(W/L)_1} \quad (65)$$

We conclude that the current mirror is an excellent current amplifier: It has a relatively low input resistance ($1/g_{m1}$), a relatively high output resistance (r_{o2}), and a gain determined by the aspect ratios of the MOSFETs.

Basic gain cell

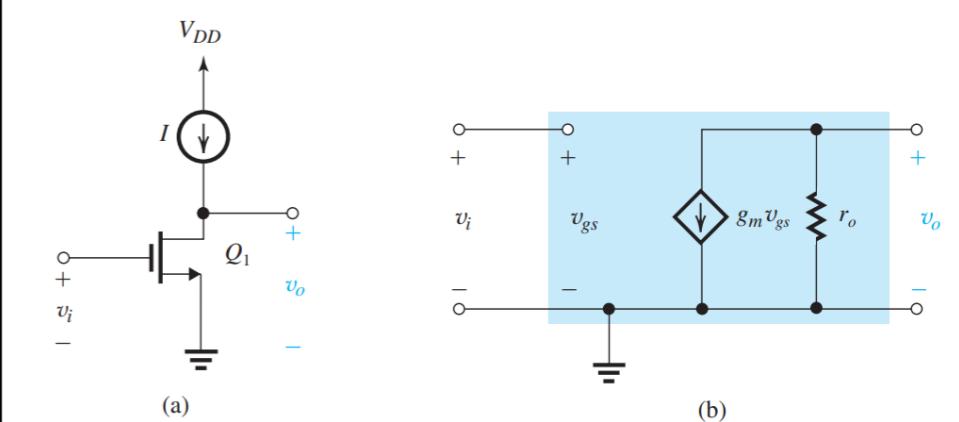


Figure 14: The basic gain cells of IC amplifiers: (a) current-source- or active-loaded common-source amplifier; (b) small-signal equivalent circuit of (a).

$$I_2 = I_{REF} \frac{(W/L)_2}{(W/L)_1} \quad (58)$$

$$I_3 = I_{REF} \frac{(W/L)_3}{(W/L)_1} \quad (59)$$

$$I_5 = I_4 \frac{(W/L)_5}{(W/L)_4} \quad (60)$$

6.1 Small-Signal Operation of Current Mirrors

In addition to their use in biasing, current mirrors are sometimes employed as current amplifiers.

$$R_{in} = \infty \quad (66)$$

$$A_{vo} = -g_m r_o \quad (67)$$

$$R_o = r_o \quad (68)$$

6.2 Effect of the Output Resistance of the Current-Source Load

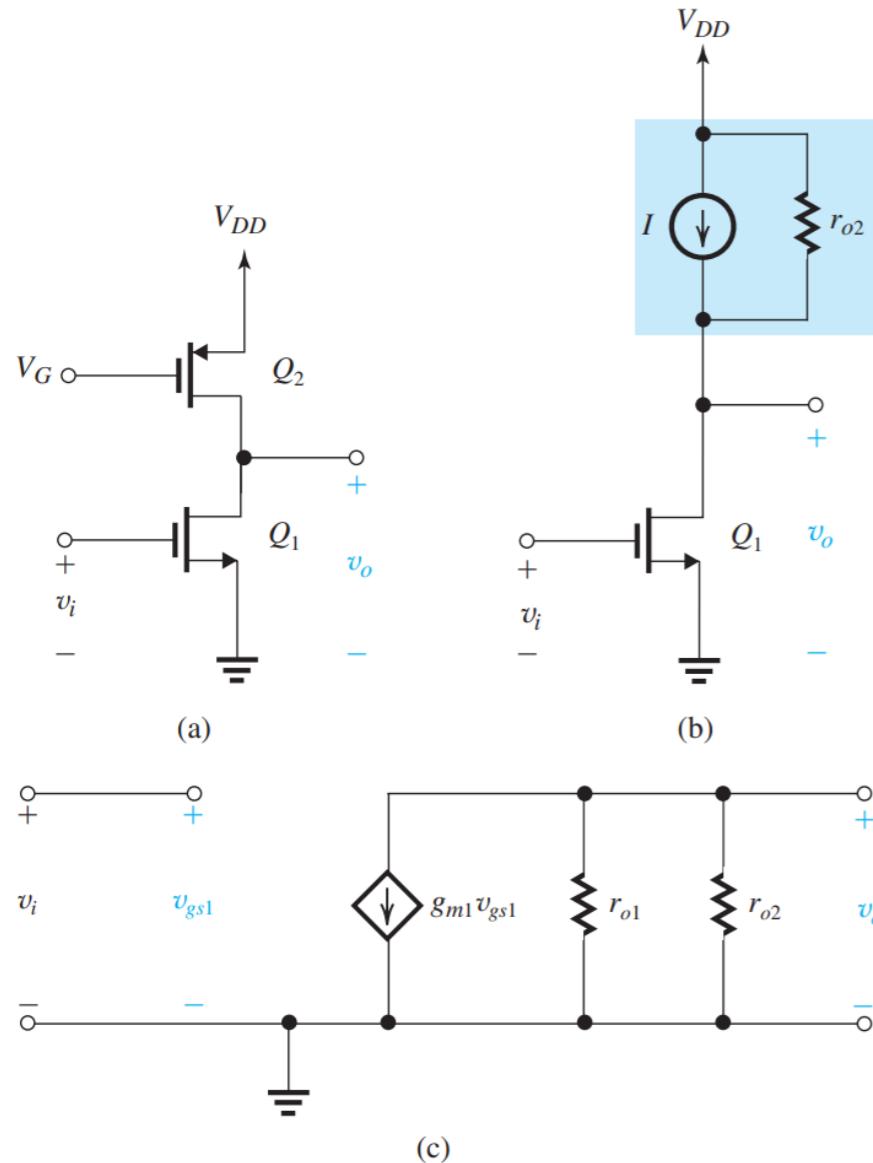


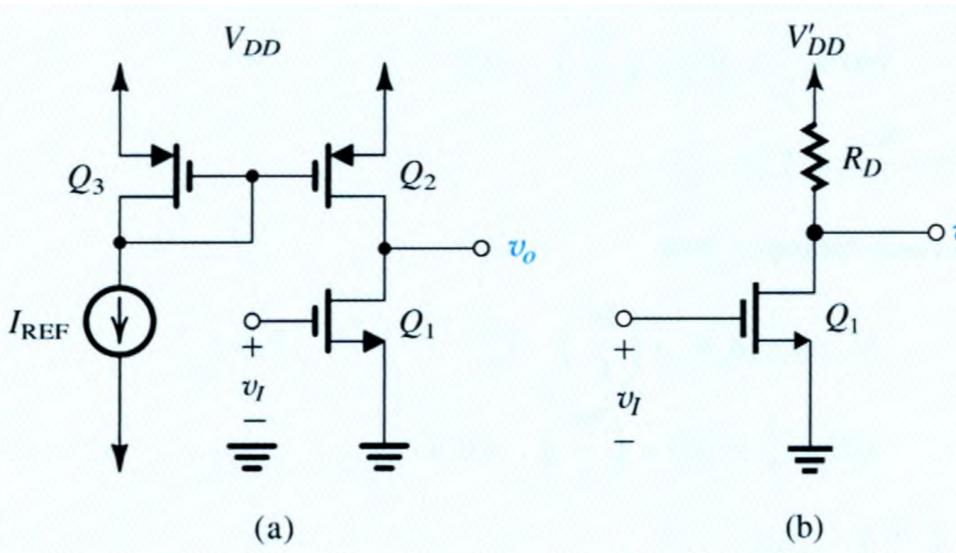
Figure 15: (a) The CS amplifier with the current-source load implemented with a *p*-channel MOSFET \$Q_2\$; (b) the circuit with \$Q_2\$ replaced with its large-signal model; and (c) small-signal equivalent circuit of the amplifier.

$$A_{vo} = -g_{m1}(r_{o1}||r_{o2}) \quad (69)$$

$$\text{If } r_{o1} = r_{o2} \quad (70)$$

$$\therefore A_{vo} = -\frac{1}{2}g_m r_o \quad (71)$$

10. Q A practical circuit implementation of the common-source amplifier with a current-source load is shown in the following figure. Here the current-source transistor \$Q_2\$ is the output transistor of a current mirror formed by \$Q_2\$ and \$Q_3\$ and fed with a reference current \$I_{REF}\$. Assume that \$Q_2\$ and \$Q_3\$ are matched.



Let \$V_{DD} = 1.8\$ V, \$V_{tn} = -V_{tp} = 0.5\$ V, \$\mu_n C_{ox} = 4\mu_p C_{ox} = 400\mu\text{A}/\text{V}^2\$, \$|V_A| = 5\$ V for all transistors, and \$I_{REF} = 100\mu\text{A}\$.

- (a) Find the dc component of \$v_1\$, and the \$W/L\$ ratios so that all transistors operate at \$|V_{ov}| = 0.2\$ V.
- (b) Determine the small-signal voltage gain.
- (c) What is the allowable range of signal swing at the output for almost-linear operation?
- (d) If the current-source load is replaced with a resistance \$R_D\$ connected to a power supply \$V'_DD\$ as shown in the figure, find the value of \$R_D\$ and \$V'_DD\$ to keep \$I_D\$, the voltage gain, and the output signal swing unchanged.

10. A

- (a) To operate \$Q_1\$ and \$V_{OV} = 0.2\$ V, \$V_{GS1}\$ must be

$$V_{GS1} = V_{tn} + V_{OV} = 0.5 + 0.2 = 0.7 \text{ V}$$

and thus the dc component of \$v_1\$ must be

$$V_I = V_{GS1} = 0.7 \text{ V}$$

Next, we determine \$(W/L)\$, from

$$I_{D1} = \frac{1}{2} (\mu_n C_{ox}) \left(\frac{W}{L} \right)_1 V_{OV}^2$$

Substituting \$I_{D1} = I_{REF} = 100\mu\text{A}\$,

$$\begin{aligned} 100 &= \frac{1}{2} \times 400 \times \left(\frac{W}{L} \right)_1 \times 0.2^2 \\ \Rightarrow \left(\frac{W}{L} \right)_1 &= 12.5 \end{aligned}$$

The \$W/L\$ ratios for \$Q_2\$ and \$Q_3\$ can now be found from

$$\begin{aligned} I_{D2,3} &= \frac{1}{2} (\mu_p C_{ox}) \left(\frac{W}{L} \right)_{2,3} V_{OV}^2 \\ 100 &= \frac{1}{2} \times 100 \times \left(\frac{W}{L} \right)_{2,3} \times 0.2^2 \\ \Rightarrow \left(\frac{W}{L} \right)_{2,3} &= 50 \end{aligned}$$

(b) To obtain the small-voltage signal voltage gain, we first determine the small-signal parameters \$g_{m1} : r_{o1}\$, and \$r_{o2}\$ as follows:

$$\begin{aligned} g_{m1} &= \frac{2I_{D1}}{V_{OV1}} = \frac{2 \times 0.1 \text{ mA}}{0.2 \text{ V}} = 1 \text{ mA/V} \\ r_{o1} &= \frac{V_{A1}}{I_{D1}} = \frac{5 \text{ V}}{0.1 \text{ mA}} = 50 \text{k}\Omega \\ r_{o2} &= \frac{|V_{A2}|}{I_{D2}} = \frac{5 \text{ V}}{0.1 \text{ mA}} = 50 \text{k}\Omega \end{aligned}$$

The voltage gain \$A_v\$ can now be found as

$$\begin{aligned} A_v &= -g_{m1} (r_{o1}||r_{o2}) \\ &= -1(50||50) \\ &= -25 \text{ V/V} \end{aligned}$$

(c) The upper limit of the output signal swing is determined by \$Q_2\$ leaving the saturation region. This will occur if \$v_O\$ reaches \$V_{DD} - |V_{OV2}|\$, thus

$$v_{O\max} = 1.8 - 0.2 = 1.6 \text{ V}$$

The lower limit of the output signal swing is determined by \$Q_1\$ leaving the saturation region. This will occur if \$v_0\$ falls below \$V_{OV1}\$, thus

$$v_{0\min} = 0.2 \text{ V}$$

Thus, the range of linear signal swing at the output is given by

$$0.2 \text{ V} \leq v_o \leq 1.6 \text{ V}$$

(d) If the current-source load is replaced with a resistance \$R_D\$ as in Fig. 8.16(b), to keep the gain unchanged,

$$R_D = r_{o2} = 50 \text{k}\Omega$$

To keep the output signal swing unchanged, we bias \$Q_1\$ so that \$V_{DS1}\$ is equal to the mid point of the output swing, that is,

$$V_{DS1} = 0.9 \text{ V}$$

Now, for \$I_D\$ to be the same as before, that is, \$I_D = 0.1\$ mA, the new supply voltage must be,

$$\begin{aligned} V'_{DD} &= V_{DS1} + I_D R_D \\ &= 0.9 + 0.1 \times 50 = 5.9 \text{ V} \end{aligned}$$

which is much larger than the supply voltage possible with this $0.18 - \mu\text{m}$ CMOS technology (1.8 V). Needless to say, fabricating a $50\text{k}\Omega$ resistance with precise value on the IC is an expensive endeavor. This illustrates the need for using current-source loads.

7 The Common-Gate and Common-Base Amplifiers as Current Buffers

7.1 The CG Circuit

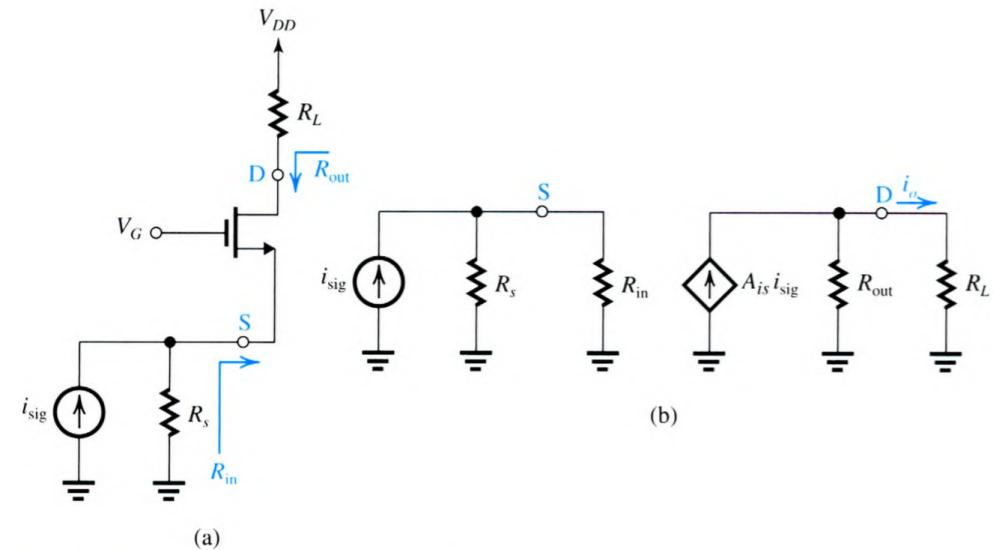


Figure 16: (a) A CG amplifier with the bias arrangement only partially shown, (b) Equivalent circuit model of the CG amplifier in (a).

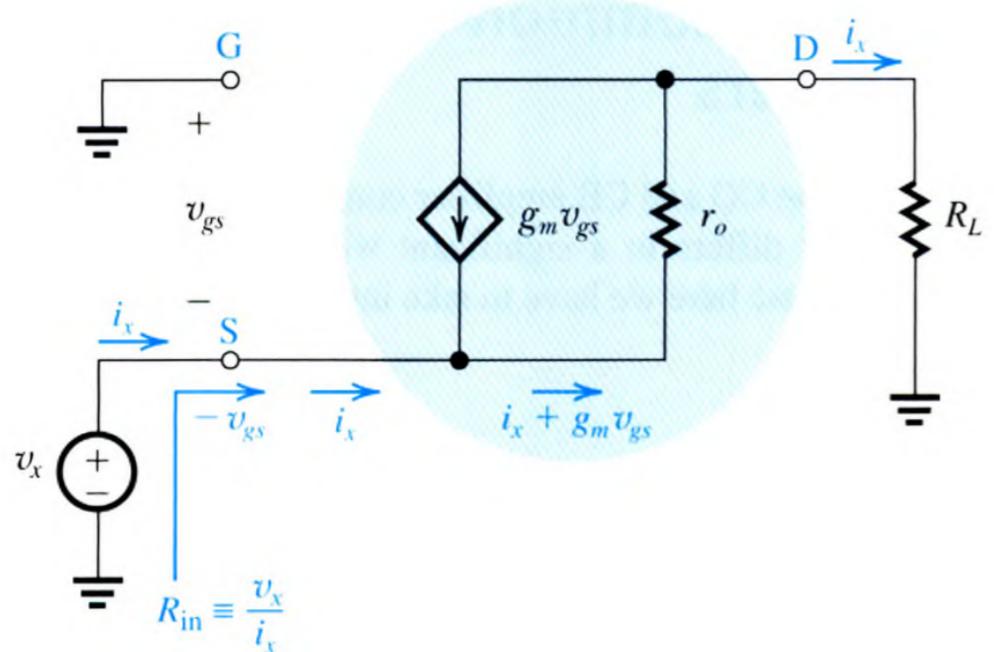


Figure 17: Determining the input resistance R_{in} of the CG amplifier.

Input resistance :

$$R_{\text{in}} = \frac{v_x}{i_x}$$

Some of the analysis is shown in Fig. 4. Now, writing a loop equation for the loop comprising v_x , r_o , and R_L gives

$$v_x = (i_x + g_m v_{gs}) r_o + i_x R_L$$

Since the voltage at the source node v_x is equal to $-v_{gs}$, we can replace v_{gs} by $-v_x$ and rearrange terms to obtain $R_{\text{in}} \equiv v_x/i_x$

$$R_{\text{in}} = \frac{r_o + R_L}{g_m r_o + 1}$$

For $g_m r_o \gg 1$

$$R_{\text{in}} \simeq \frac{1}{g_m} + \frac{R_L}{g_m r_o}$$

short circuit gain

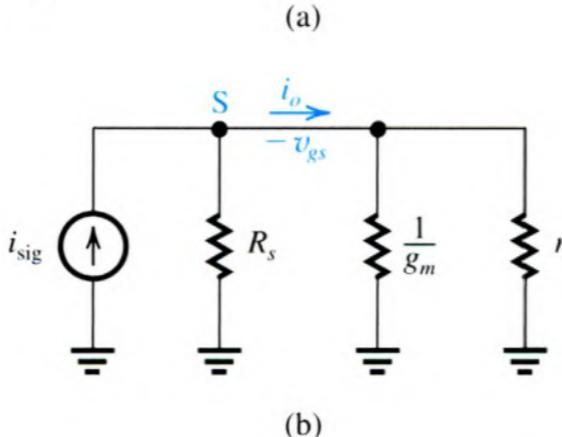
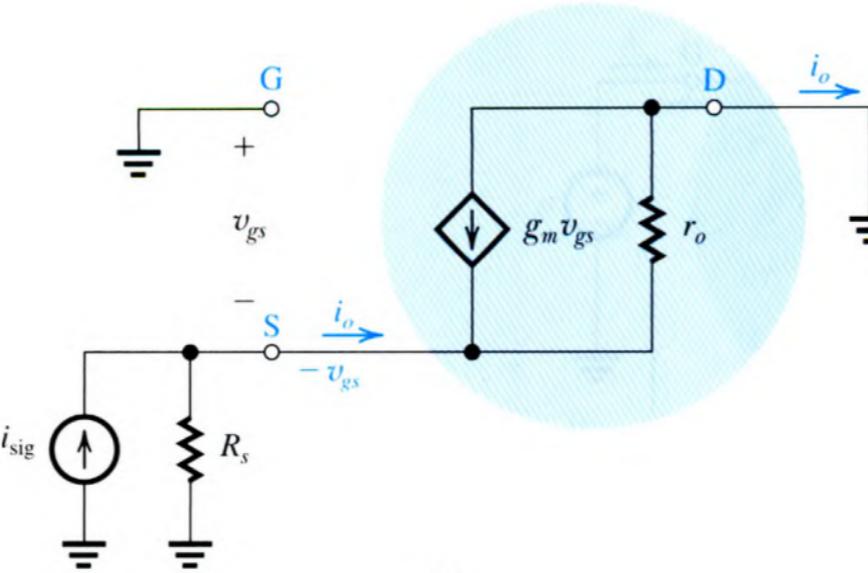


Figure 18: (a) Determining the short-circuit current gain $A_{is} = i_o / i_{\text{sig}}$ of the CG amplifier, (b) A simplified version of the circuit in (a).

$$A_{is} \equiv \frac{i_o}{i_{\text{sig}}}$$

circuit shown in Fig. 5, from which we can find i_o/i_{sig} by using the current-divider rule:

$$A_{is} \equiv \frac{i_o}{i_{\text{sig}}} = \frac{g_m + \frac{1}{r_o}}{g_m + \frac{1}{r_o} + \frac{1}{R_s}}$$

Thus,

$$A_{is} = \frac{1 + \frac{1}{g_m r_o}}{1 + \frac{1}{g_m r_o} + \frac{1}{g_m R_s}}$$

For $g_m r_o \gg 1$ and $g_m R_s \gg 1$

$$A_{is} \simeq 1$$

which is an important characteristic of a current buffer.

Output Resistance

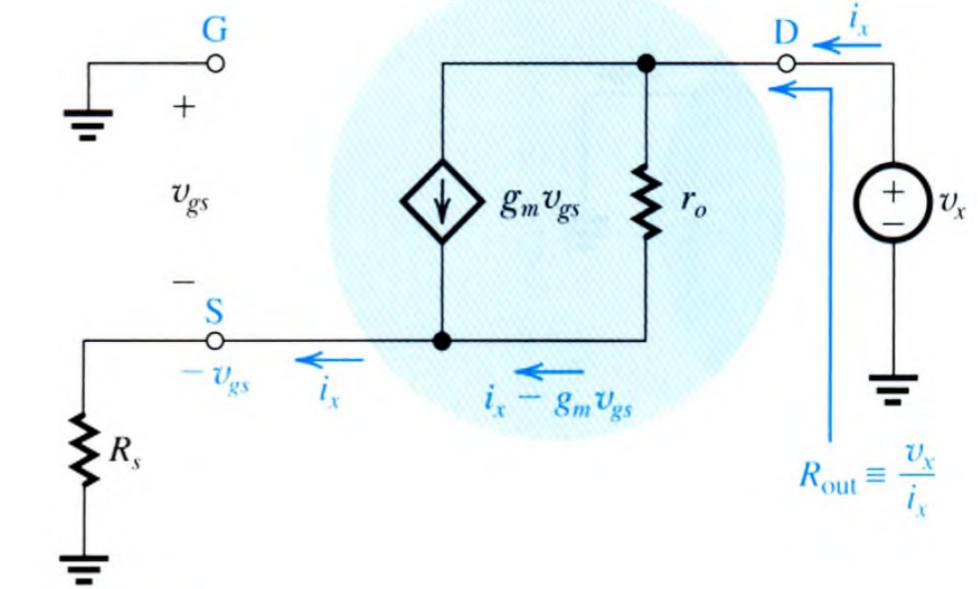


Figure 19: Determining the output resistance R_{out} of the CG amplifier.

$$R_{\text{out}} = \frac{v_x}{i_x}$$

Some of the analysis is shown in Fig. 6. Now, a loop equation for the loop comprising v_x , r_o , and R_s gives

$$v_x = (i_x - g_m v_{gs}) r_o + i_x R_s$$

Notice that the voltage at the source terminal is $-v_{gs}$ and thus can also be expressed as

$$-v_{gs} = i_x R_s$$

Substituting this value for v_{gs} in the previous equation and rearranging terms to obtain $R_{\text{out}} \equiv v_x/i_x$ yields

$$R_{\text{out}} = r_o + R_s + g_m r_o R_s$$

which can be written in the alternate form

$$R_{\text{out}} = r_o + (1 + g_m r_o) R_s$$

For $g_m r_o \gg 1$

$$R_{\text{out}} \simeq r_o + (g_m r_o) R_s$$

and if we also have $g_m R_s \gg 1$, then

$$R_{\text{out}} \simeq (g_m r_o) R_s$$

7.2 Summary

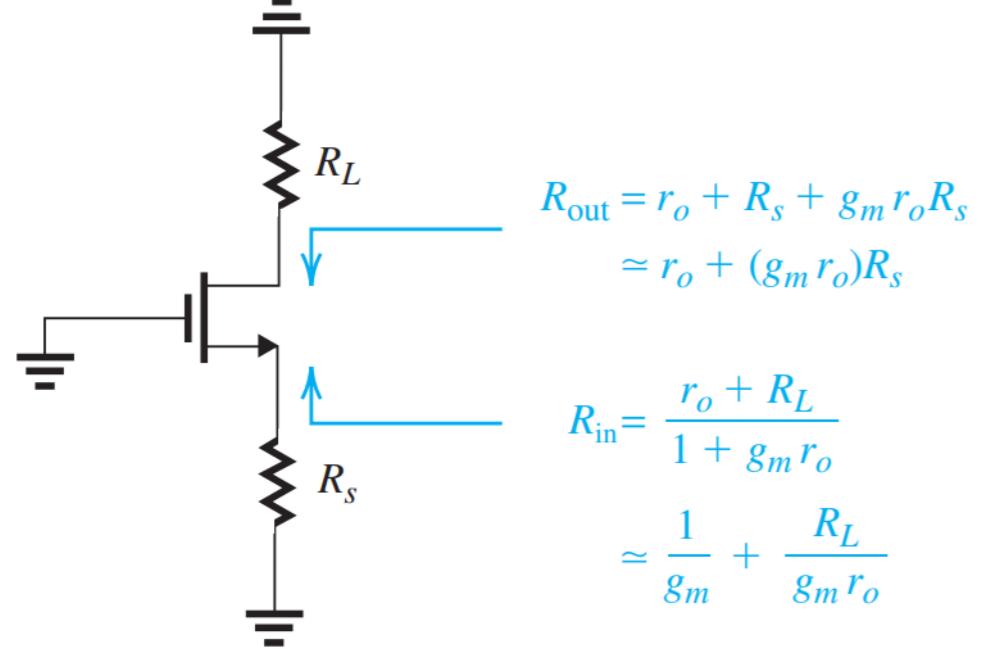


Figure 20: The impedance transformation properties of the common-gate amplifier. Depending on the values of R_s and R_L , we can sometimes write $R_{\text{in}} \approx R_L/(g_m r_o)$ and $R_o \approx R_s(g_m r_o)$. However, such approximations are not always justified.

8 MOSFET Cascode Amplifier

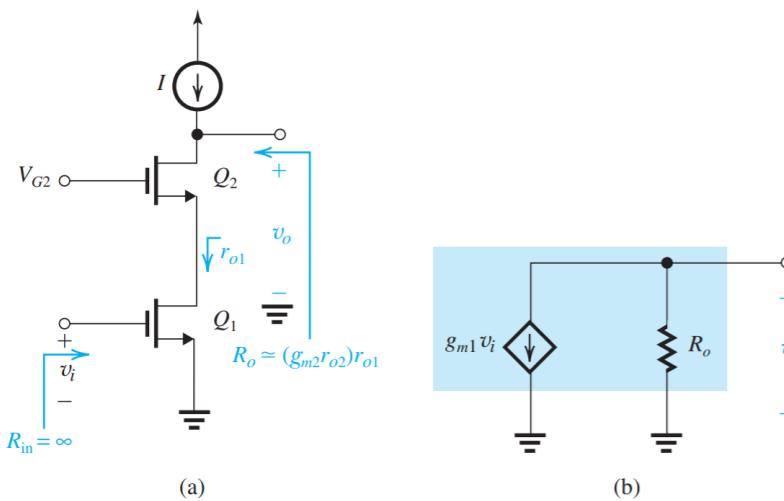


Figure 21: (a) A MOS cascode amplifier with an ideal current-source load; (b) equivalent circuit representation of the cascode output.

$$A_{vo} \equiv \frac{v_o}{v_i} = -g_m R_o \quad (72)$$

Now, since R_s of Q_2 is r_{o1} , the output resistance R_o is given by the approximate

expression

$$R_o \simeq (g_{m2} r_{o2}) r_{o1} \quad (73)$$

Substituting in Eq. 72 results in

$$A_{vo} = -(g_{m1} r_{o1}) (g_{m2} r_{o2}) \quad (74)$$

For the case $g_{m1} = g_{m2} = g_m$ and $r_{o1} = r_{o2} = r_o$,

$$A_{vo} = -(g_m r_o)^2 = -A_0^2 \quad (75)$$

Thus cascoding increases the gain magnitude from A_0 to A_0^2 .

8.1 Implementation of the Constant-Current Source Load

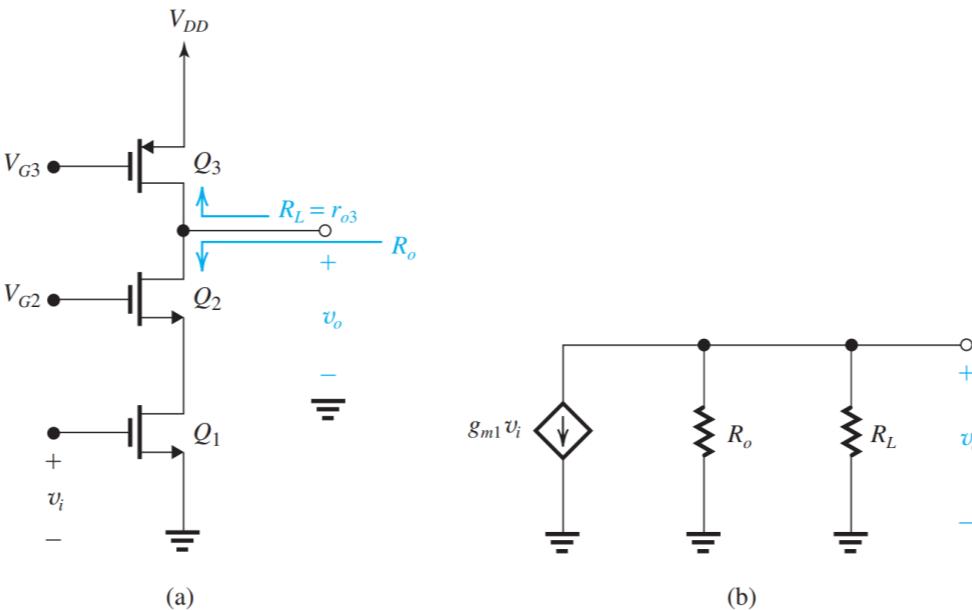


Figure 22: (a) A MOS cascode amplifier loaded in a simple PMOS current source Q_3 . (b) Equivalent circuit at the amplifier output.

and the voltage gain of the cascode amplifier will be

$$R_L = r_{o3} \quad (76)$$

$$A_v = -g_m (R_o \| R_L) \quad (77)$$

$$= -g_m (g_{m2} r_{o2} r_{o1} \| r_{o3}) \quad (78)$$

from which we can readily see that since $R_L \ll R_o$, the total resistance will be approximately equal to r_{o3} and the gain will be

$$A_v \simeq -g_m r_{o3} \quad (79)$$

8.2 The Use of a Cascode Current Source

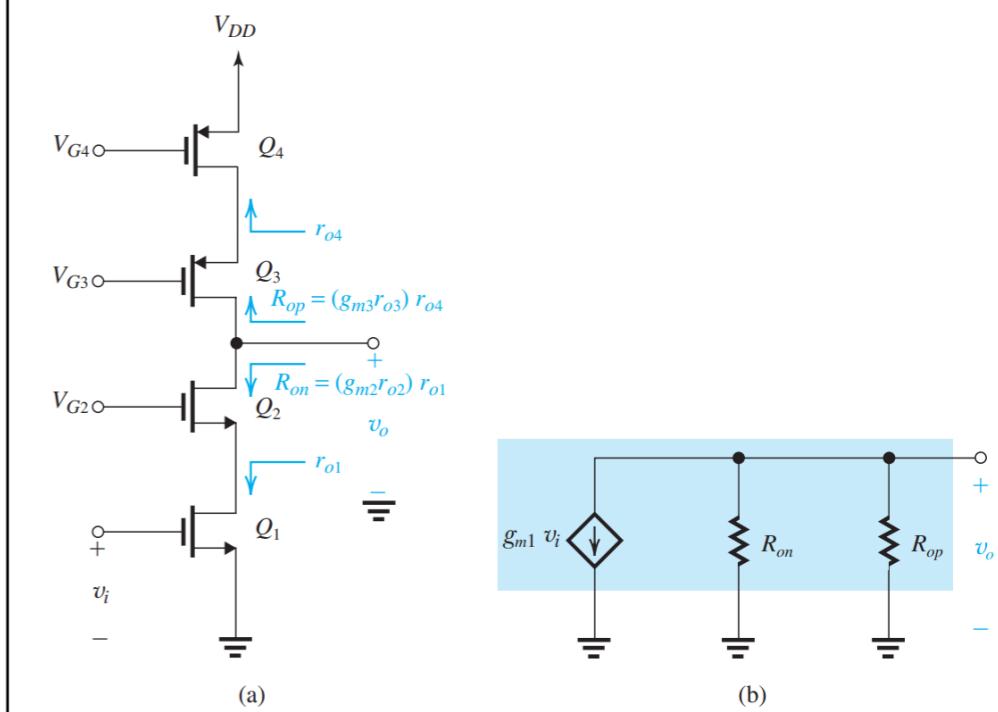


Figure 23: A cascode amplifier with a cascode current-source load.

$$R_o = (g_{m3} r_{o3}) r_{o4} \quad (80)$$

$$A_v = \frac{v_o}{v_i} = -g_m [R_{on} \| R_{op}] \quad (81)$$

Thus,

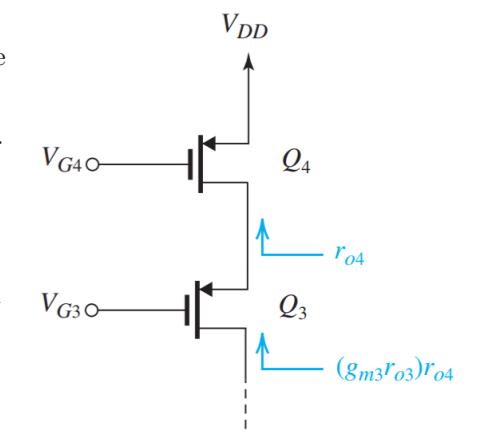
$$A_v = -g_m \{ [(g_{m2} r_{o2}) r_{o1}] \| [(g_{m3} r_{o3}) r_{o4}] \} \quad (82)$$

For the case in which all transistors are identical,

$$A_v = -\frac{1}{2} (g_m r_o)^2 = -\frac{1}{2} A_0^2 \quad (83)$$

11. Q It is required to design the cascode current source of the following figure to provide a current of $100\mu\text{A}$ and an output resistance of $500\text{k}\Omega$. Assume the availability of a $0.18 - \mu\text{m}$ CMOS technology for which $V_{DD} = 1.8 \text{ V}$, $V_{tp} = -0.5 \text{ V}$, $\mu_p C_{ox} = 90\mu\text{A/V}^2$, and $V'_A = -5 \text{ V}/\mu\text{m}$. Use $|V_{OV}| = 0.3 \text{ V}$ and determine L and W/L for each transistor, and the values of the bias voltages V_{G3} and V_{G4} .

11. A



How to solve ?

The output resistance R_o is given by

$$R_o = (g_{m3}r_{o3}) r_{o4}$$

Assuming Q_3 and Q_4 are identical,

$$\begin{aligned} R_o &= (g_m r_o) r_o \\ &= \frac{2I_D}{|V_{OV}|} \times \frac{|V_A|}{I_D} \times \frac{|V_A|}{I_D} \\ &= \frac{|V_A|}{|V_{OV}|/2} \times \frac{|V_A|}{I_D} \end{aligned}$$

Using $|V_{OV}| = 0.3$ V, we write

$$500\text{k}\Omega = \frac{|V_A|}{0.15} \times \frac{|V_A|}{0.1 \text{ mA}}$$

Thus we require

$$|V_A| = 2.74 \text{ V}$$

Now, since $|V_A| = |V'_A| L$ we need to use a channel length of

$$L = \frac{2.74}{5} = 0.55\mu\text{m}$$

which is about three times the minimum channel length. With $|V_t| = 0.5$ V and $|V_{OV}| = 0.3$ V,

$$V_{SG4} = 0.5 + 0.3 = 0.8 \text{ V}$$

and thus,

$$V_{G4} = 1.8 - 0.8 = 1.0 \text{ V}$$

To allow for the largest possible signal swing at the output terminal, we shall use the minimum required voltage across Q_4 , namely, $|V_{OV}|$ or 0.3 V. Thus,

$$V_{D4} = 1.8 - 0.3 = 1.5 \text{ V}$$

Since the two transistors are identical and are carrying equal currents,

$$V_{SG3} = V_{SG4} = 0.8 \text{ V}$$

Thus,

$$V_{G3} = 1.5 - 0.8 = +0.7 \text{ V}$$

We note that the maximum voltage allowed at the output terminal of the current source will be constrained by the need to allow a minimum voltage of $|V_{OV}|$ across Q_3 ; thus;

$$v_{D3 \max} = 1.5 - 0.3 = +1.2 \text{ V}$$

To determine the required W/L ratios of Q_3 and Q_4 , we use

$$\begin{aligned} I_D &= \frac{1}{2} (\mu_p C_{ox}) \left(\frac{W}{L} \right) |V_{OV}|^2 \left(1 + \frac{V_{SD}}{|V_A|} \right) \\ 100 &= \frac{1}{2} \times 90 \times \left(\frac{W}{L} \right) \times 0.3^2 \left(1 + \frac{0.3}{2.74} \right) \end{aligned}$$

which yields

$$\frac{W}{L} = 22.3$$