EEC 332 - Analog Integrated Circuits

Lecture 8
MOSFET Cascode Amplifier

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1 Introduction

Remember from the last lecture, in the common-gate circuit :

$$R_{\text{in}} \simeq \frac{R_L}{g_m r_o}$$

$$R_{\text{out}} \simeq (g_m r_o)\, R_s$$

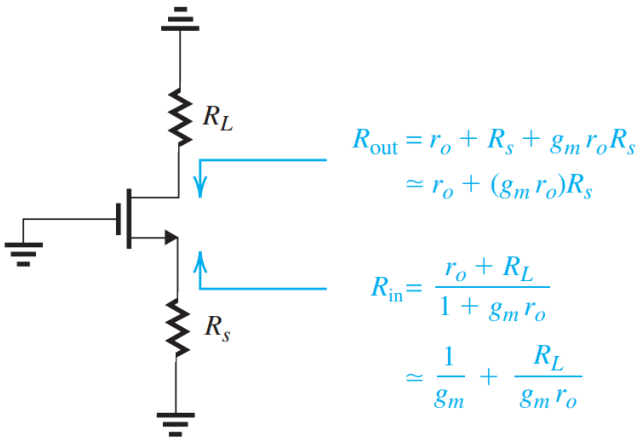


Figure 1: The impedance transformation properties of the common-gate amplifier. Depending on the values of R_s and R_l, we can sometimes write and $R_{in} \approx R_L/(g_m r_o)$ and $R_o \approx R_s(g_m r_o)$. However, such approximations are not always justified

2 MOSFET Cascode Amplifier

Cascoding refers to the use of a transistor connected in the common-gate (or the common-base) configuration to provide current buffering for the output of a common-source (or a common-emitter) amplifying transistor. As we found from our study of the CG and CB circuits in the previous section, their current-buffering action provides a high output resistance, thus enabling the cascode amplifier to have a voltage gain much larger than that possible with the CS or CE gain cells alone

Figure 2(a) shows a MOS cascode amplifier loaded with an ideal constant-current source. The voltage gain realized can be found from the equivalent circuit in Fig. 2(b). Since the load is an ideal constant-current source, the load resistance is infinite. That is, the amplifier is operating with an open-circuit load, and the gain is

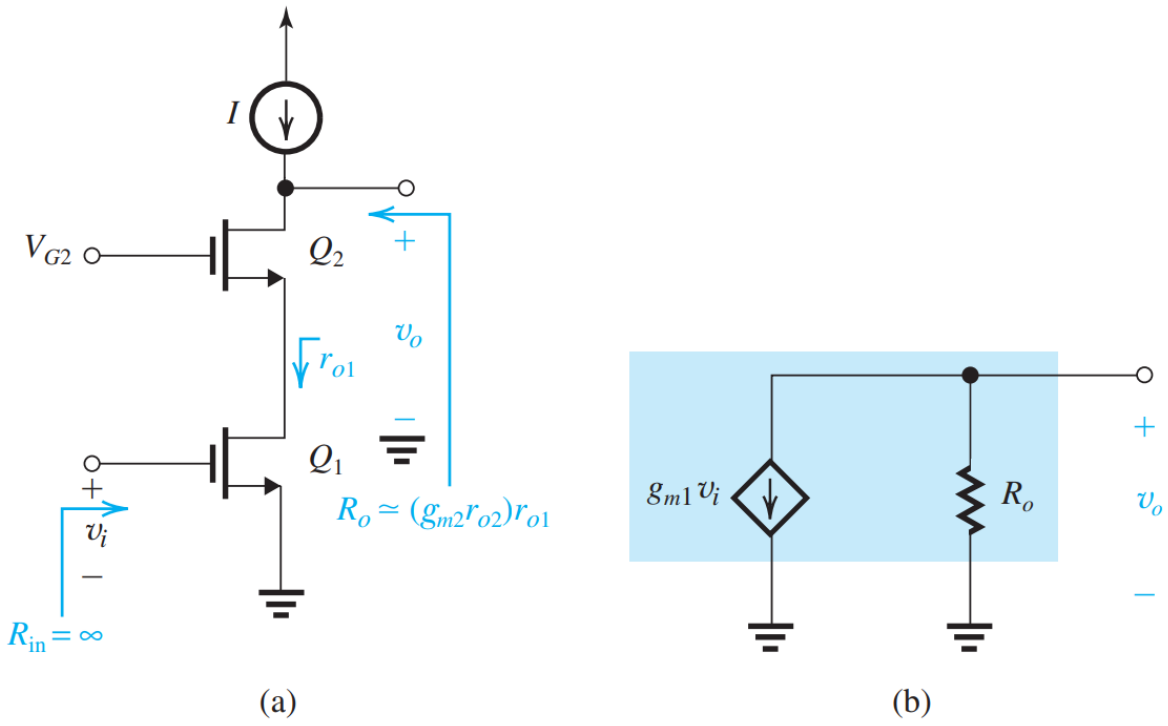


Figure 2: (a) A MOS cascode amplifier with an ideal current-source load; (b) equivalent circuit representation of the cascode output.

$$A_{vo} \equiv \frac{v_o}{v_i} = -g_{m1}R_o \tag{1}$$

Now, since R_s of Q_2 is r_{o1}, the output resistance R_o is given by the approximate expression

$$R_o \simeq (g_{m2}r_{o2})\, r_{o1} \tag{2}$$

Substituting in Eq. 1 results in

$$A_{vo} = -(g_{m1}r_{o1})\,(g_{m2}r_{o2}) \tag{3}$$

For the case $g_{m1} = g_{m2} = g_m$ and $r_{o1} = r_{o2} = r_o$,

$$A_{vo} = -(g_m r_o)^2 \tag{4}$$

$$= -A_0^2 \tag{5}$$

Thus cascoding increases the gain magnitude from A_0 to A_0^2.

2.1 Implementation of the Constant-Current Source Load

If the current source load is implemented with a PMOS transistor (which can be part of a PMOS current mirror) as shown in the following figure, the load resistance R_L will be equal to the output resistance of Q_3, r_{o3},

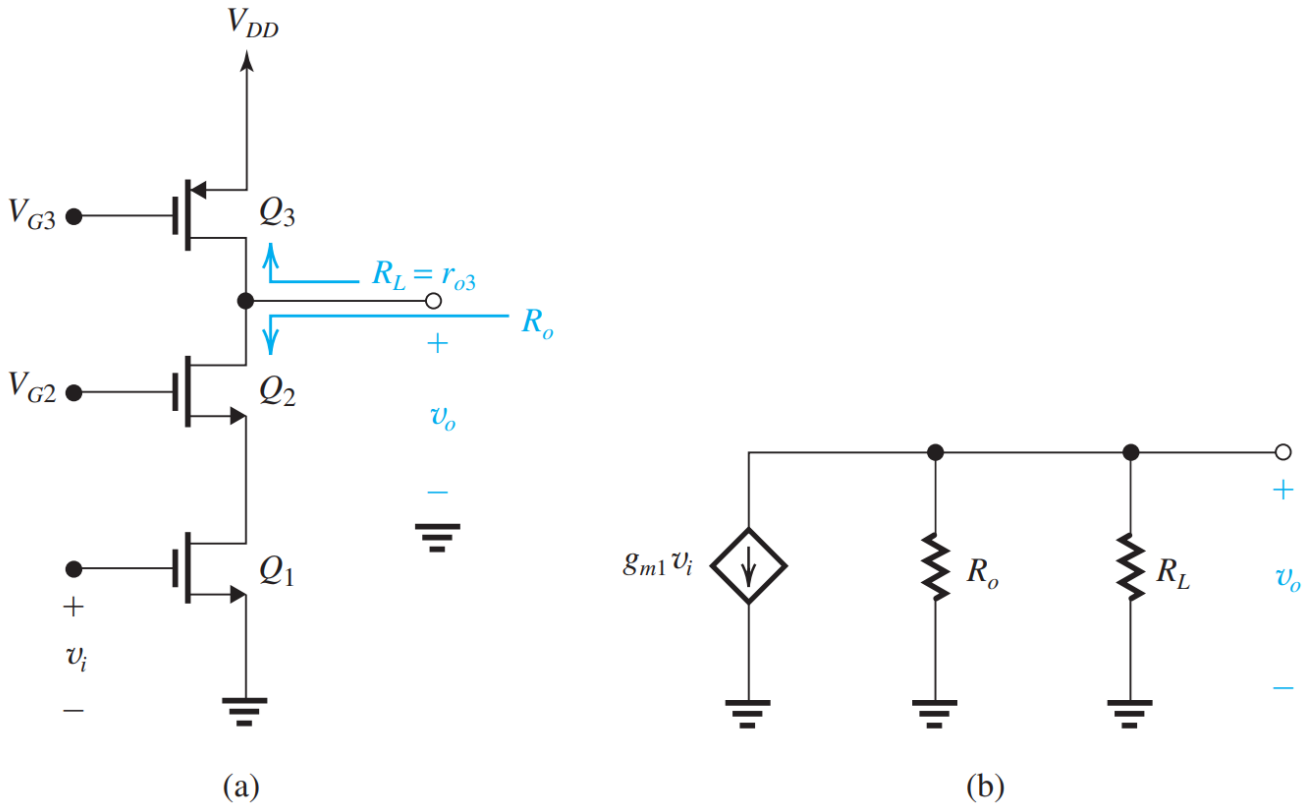


Figure 3: (a) A MOS cascode amplifier loaded in a simple PMOS current source Q3. (b) Equivalent circuit at the amplifier output.

$$R_L = r_{o3} \tag{6}$$

and the voltage gain of the cascode amplifier will be

$$A_v = -g_{m1}\left(R_o \| R_L\right) \tag{7}$$

$$= -g_{m1}\left(g_{m2}r_{o2}r_{o1} \| r_{o3}\right) \tag{8}$$

from which we can readily see that since $R_L \ll R_o$, the total resistance will be approximately equal to r_{o3} and the gain will be

$$A_v \simeq -g_{m1} r_{o3} \tag{9}$$

2.2 The Use of a Cascode Current Source

To realize a gain of the order of A_0^2, the load resistance R_L must be of the same order as R_o of the cascode amplifier. This can be achieved by using a cascode current source such as that shown in Fig. 4. Here Q_4 is the current-source transistor, and Q_3 is the CG cascode transistor. Voltages V_{G3} and V_{G4} are dc bias voltages. The cascode transistor Q_3 multiplies the output resistance of Q_4, r_{o4} by $(g_{m3} r_{o3})$ to provide an output resistance for the cascode current source of Combining a cascode amplifier with a cascode current source results in the circuit of Fig. 5(a). The equivalent circuit at the output side is shown in Fig. 5(b), from which the voltage gain can be easily found as

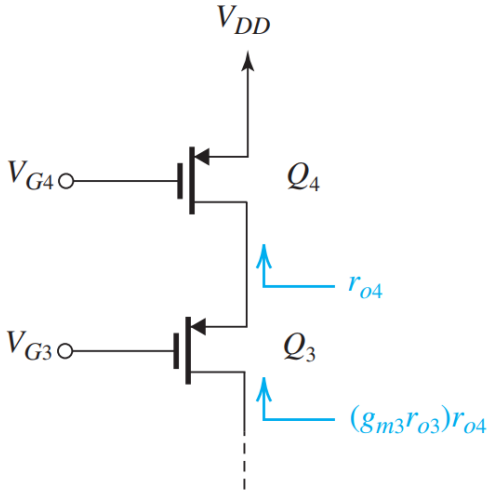


Figure 4: Employing a cascode transistor Q_3 to raise the output resistance of the current source Q_4

$$R_o = (g_{m3} r_{o3})\, r_{o4} \tag{10}$$

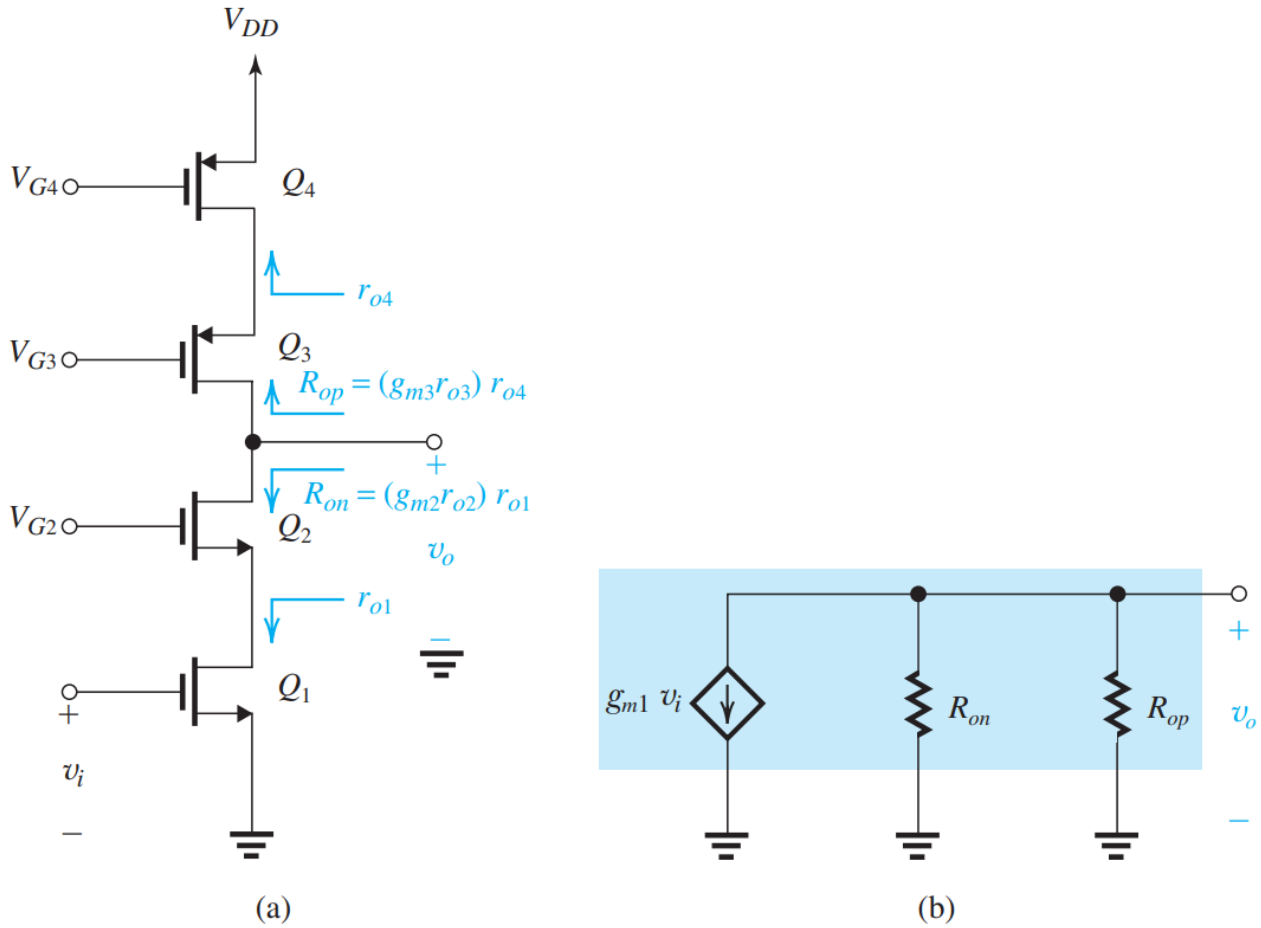


Figure 5: A cascode amplifier with a cascode current-source load.

Combining a cascode amplifier with a cascode current source results in the circuit of Fig. 8.33(a). The equivalent circuit at the output side is shown in Fig. 8.33(b), from which the voltage gain can be easily found as

$$\boldsymbol{A_v = \frac{v_o}{v_i} = -g_{m1}\,[R_{on} \| R_{op}]} \tag{11}$$

Thus,

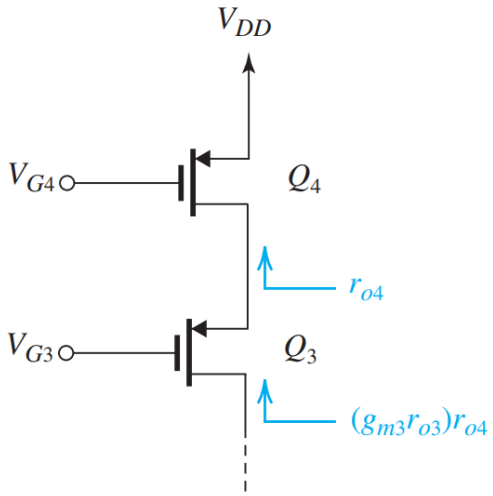
$$\boldsymbol{A_v = -g_{m1}\,\{[(g_{m2}r_{o2})\, r_{o1}] \,\|\, [(g_{m3}r_{o3})\, r_{o4}]\}} \tag{12}$$

For the case in which all transistors are identical,

$$\boldsymbol{A_v = -\frac{1}{2}\,(g_m r_o)^2 = -\frac{1}{2}A_0^2} \tag{13}$$

By comparison to the gain expression , we see that using the cascode configuration for both the amplifying transistor and the current-source load transistor results in an increase in the magnitude of gain by a factor equal to A_0

1. Q It is required to design the cascode current source of the follwing figure to provide a current of 100μA and an output resistance of 500kΩ. Assume the availability of a $0.18-\mu$m CMOS technology for which $V_{DD}=1.8$ V, $V_{tp}=-0.5$ V, $\mu_p C_{ox}=90\mu\text{A/V}^2$, and $V_A'=-5$ V/μm. Use $|V_{OV}|=0.3$ V and determine L and W/L for each transistor, and the values of the bias voltages V_{G3} and V_{G4}.



1. A

The output resistance R_o is given by

$$R_o=(g_{m3}r_{o3})\,r_{o4}$$

Assuming Q_3 and Q_4 are identical,

$$\begin{aligned}R_o&=(g_m r_o)\,r_o\\&=\frac{2I_D}{|V_{OV}|}\times\frac{|V_A|}{I_D}\times\frac{|V_A|}{I_D}\\&=\frac{|V_A|}{|V_{OV}|/2}\times\frac{|V_A|}{I_D}\end{aligned}$$

Using $|V_{OV}|=0.3$ V, we write

$$500\text{k}\Omega=\frac{|V_A|}{0.15}\times\frac{|V_A|}{0.1\text{ mA}}$$

Thus we require

$$|V_A|=2.74\text{ V}$$

Now, since $|V_A|=|V_A'|\,L$ we need to use a channel length of

$$L=\frac{2.74}{5}=0.55\mu\text{m}$$

which is about three times the minimum channel length. With $|V_t|=0.5$ V and

$|V_{OV}| = 0.3$ V,

$$V_{SG4} = 0.5 + 0.3 = 0.8 \text{ V}$$

and thus,

$$V_{G4} = 1.8 - 0.8 = 1.0 \text{ V}$$

To allow for the largest possible signal swing at the output terminal, we shall use the minimum required voltage across Q_4, namely, $|V_{OV}|$ or 0.3 V. Thus,

$$V_{D4} = 1.8 - 0.3 = 1.5 \text{ V}$$

Since the two transistors are identical and are carrying equal currents,

$$V_{SG3} = V_{SG4} = 0.8 \text{ V}$$

Thus,

$$V_{G3} = 1.5 - 0.8 = +0.7 \text{ V}$$

We note that the maximum voltage allowed at the output terminal of the current source will be constrained by the need to allow a minimum voltage of $|V_{OV}|$ across Q_3; thus;

$$v_{D3\,\max} = 1.5 - 0.3 = +1.2 \text{ V}$$

To determine the required W/L ratios of Q_3 and Q_4, we use

$$I_D = \frac{1}{2}(\mu_p C_{ox})\left(\frac{W}{L}\right)|V_{OV}|^2\left(1 + \frac{V_{SD}}{|V_A|}\right)$$

$$100 = \frac{1}{2} \times 90 \times \left(\frac{W}{L}\right) \times 0.3^2\left(1 + \frac{0.3}{2.74}\right)$$

which yields

$$\frac{W}{L} = 22.3$$