EEC 332 - Analog Integrated Circuits

Lecture 3
MOSFET

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MOSFET : Metal Oxide Silicon Field Effect Transistors

Why MOSFET ? MOSFETs are particularly useful in amplifiers due to their input impedance being nearly infinite which allows the amplifier to capture almost all the incoming signal. The main advantage is that it requires almost no input current to control the load current, so the power consumption is nearly zero, that's why we choose MOSFET over BJT.

1 Device Structure

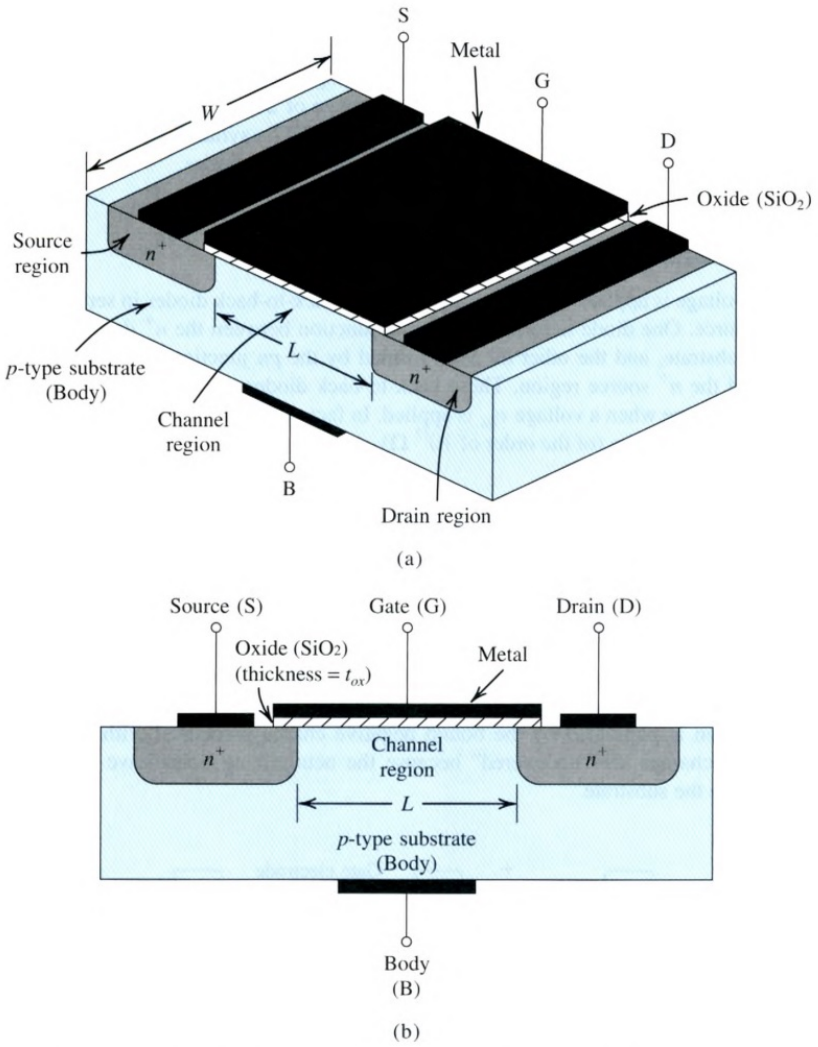

Figure 1: Physical structure of the n-channel enhancement-type MOSFET . Typically, $\boldsymbol{L = 20}$ nm to 1 $\boldsymbol{\mu}$m , $\boldsymbol{W}$ = 30 nm to 100 $\boldsymbol{\mu}$m, and the thickness of the oxide layer ($\boldsymbol{t_{ox}}$) is in the range of 1 to 10 nm.

2 Operation with Zero Gate Voltage

When zero voltage is applied to the gate, the path between drain and source has a very high resistance (of the order of $10^{12}\Omega$). So no current conduction from drain to source when a voltage v_{DS} is applied.

3 Creating a Channel for Current Flow

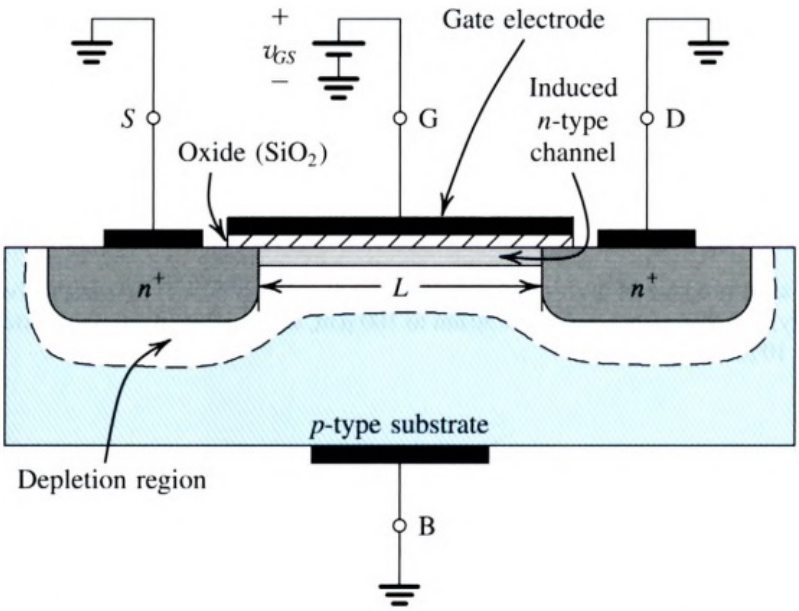

Figure 2: The enhancement-type NMOS transistor with a positive voltage applied to the gate. An n channel is induced at the top of the substrate beneath the gate. (Note that the MOSFET of this figure is called an n-channel MOSFET or, alternatively, an NMOS transistor.)

at $0 \leq v_{GS} < V_t$ an n region starts to appear

when $v_{GS} > V_t$ an n region is created, connecting the source and drain regions to one another

Note that an n-channel MOSFET is formed in a p-type substrate: The channel is created by inverting the substrate surface from p-type to n-type.

threshold voltage (V_t) : The value of v_{GS} at which a sufficient number of mobile electrons accumulate under the gate to form a conducting channel

overdrive voltage (v_{OV}) (aka overdrive voltage) : The excess of v_{GS} over V_t

$$v_{oV} \equiv v_{GS} - V_t$$

We can express the magnitude of the electron charge in the channel by

$$|Q| = C_{ox}(WL)v_{OV}$$

where

C_{ox} : the oxide capacitance, ($\mathrm{F/m^2}$)

W : width of the channel

L : the length of the channel

oxide capacitance (C_{ox}) : capacitance of the parallel-plate capacitor per unit gate area

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

where

ϵ_{ox} : permittivity of the silicon dioxide

t_{ox} : oxide thickness

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1. Q Calculate the oxide capacitance, total capacitance For a MOSFET fabricated in this technology with a channel length $L = 0.18\ \mu$m , width $W = 0.72\ \mu$ and oxide thickness 4 nm, given that the permittivity of the silicon dioxide equals 3.45×10^{-11} F/m

1. A

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

$$C_{ox} = \frac{3.45 \times 10^{-11}}{4 \times 10^{-9}} = 8.6 \times 10^{-3}\ \mathrm{F/m^2}$$

$$C = C_{ox}WL = 8.6 \times 0.18 \times 0.72 = 1.1\mathrm{fF}$$

4 Applying a Small v_{DS}

consider the case where v_{DS} is small (i.e., 50 mV or so). The voltage v_{DS} causes a current i_L) to flow through the induced n channel

To calculate the current i_D :

first find the charge per unit channel length

$$\frac{|Q|}{L} = C_{ox} W v_{OV}$$

The voltage v_{DS} establishes an electric field E across the length of the channel

$$|E| = \frac{v_{DS}}{L}$$

This electric field in turn causes the channel electrons to drift toward the drain with a velocity given by

$$\text{Electron drift velocity } = \mu_n |E| = \mu_n \frac{v_{DS}}{L}$$

where

μ_n **: the mobility of the electrons**

We can now find the value of i_D by multiplying the charge per unit channel length by the electron drift velocity

$$i_D = \left[(\mu_n C_{ox}) \left(\frac{W}{L} \right) v_{OV} \right] v_{DS} \tag{1}$$

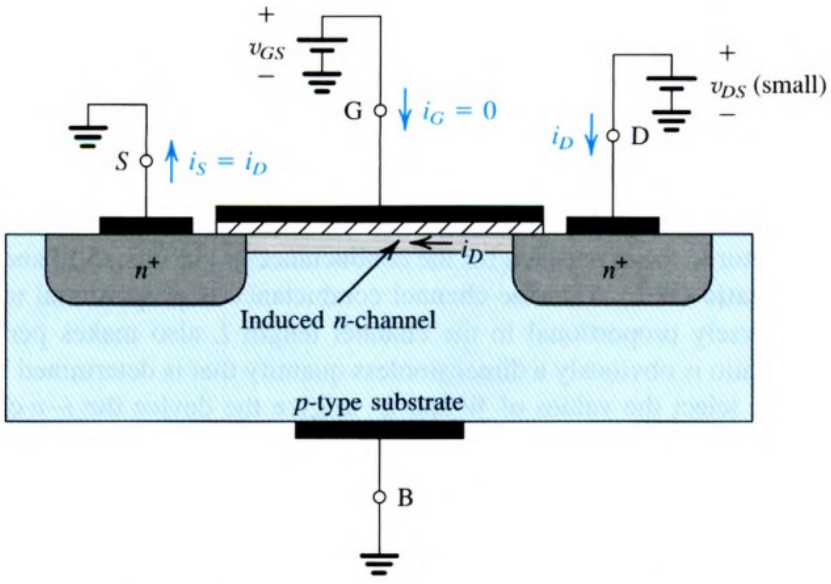

Figure 3: An NMOS transistor with $v_{GS} > V_t$ and with a small v_{DS} applied. The device acts as a resistance whose value is determined by v_{GS}. Specifically, the channel conductance is proportional to $v_{GS} - V_t$, and thus i_D is proportional to $(v_{GS} - V_t)v_{DS}$ Note that the depletion region is not shown (for simplicity).

Thus, for small v_{DS}, the channel behaves as a linear resistance whose value is controlled by the overdrive voltage v_{OV}, which in turn is determined by v_{GS}:

$$i_D = \left[(\mu_n C_{ox})\left(\frac{W}{L}\right)(v_{GS} - V_t)\right] v_{DS}$$

The conductance g_{DS} of the channel can be found from the previous equation

$$g_{DS} = (\mu_n C_{ox})\left(\frac{W}{L}\right) v_{OV}$$

or

$$g_{DS} = (\mu_n C_{ox})\left(\frac{W}{L}\right)(v_{GS} - V_t)$$

process transconductance (k'_n) : The product of each of μ_n and C_{ox} (note the subscript n denotes n channel)

$$k'_n = \mu_n C_{ox}$$

aspect ratio $\left(\frac{W}{L}\right)$: the channel width W divided by the channel length L . It is a dimensionless quantity that is determined by the device design

MOSFET transconductance parameter (k_n) : The product of the process transconductance parameter (k'_n) and the transistor aspect ratio $\left(\frac{W}{L}\right)$

$$k_n = k'_n(W/L) = (\mu_n C_{ox})(W/L)$$

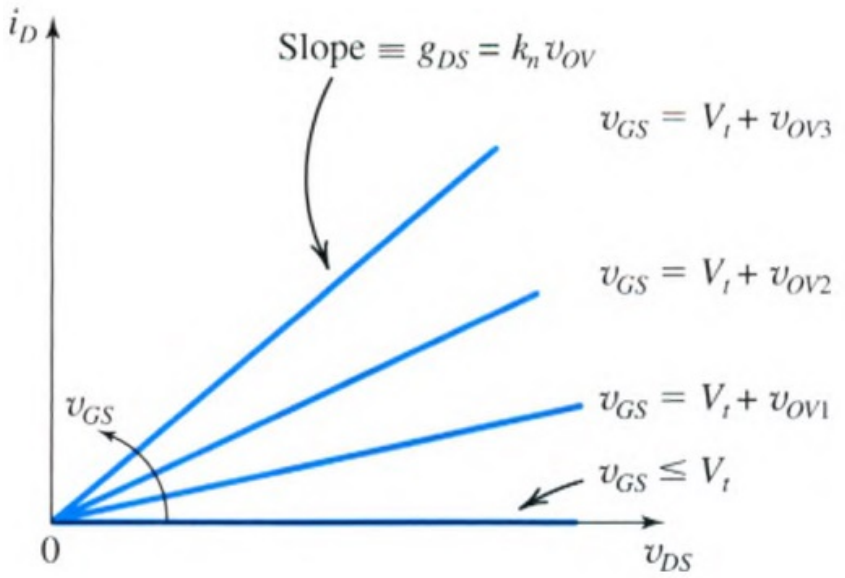

Figure 4: The i_D-v_{DS} characteristics of the MOSFET in when the voltage applied between drain and source, v_{DS}, is kept small. The device operates as a linear resistance whose value is controlled by v_{GS}. Note that the slope is the MOSFET transconductunce (g_m) increases as v_{GS} increases (at small values of v_{DS})

conclusion : The resistance is infinite for $v_{GS} < V_t$ and decreases as v_{GS} is increased above V_t

5 Operation as v_{DS} Is Increased

The voltage between the gate and points along the channel decreases from $v_{GS} = V_t + v_{OV}$ at the source end to $v_{GD} = v_{GS} - v_{DS} = V_t + v_{OV} - v_{DS}$ at the drain end. therefore we find that the channel is no longer of uniform depth; rather, the channel takes the tapered shape shown in the following figure

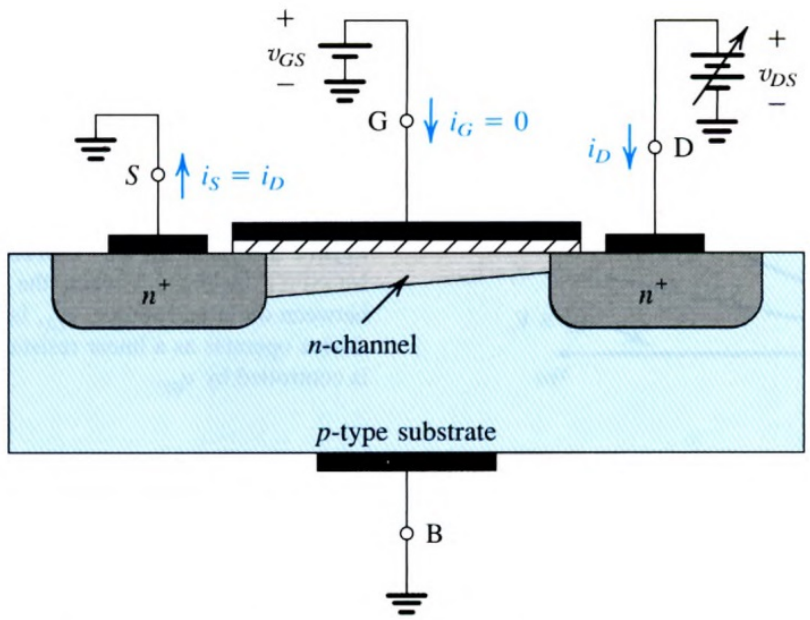

Figure 5: Operation of the MOSFET as v_{DS} is increased. The induced channel acquires a tapered shape, and its resistance increases as v_{DS} is increased. Here, v_{GS} is kept constant at a value $> V_t$; $v_{GS} = V_t + v_{OV}$. It is the widening of the depletion region (not shown) as a result of the increased v_{DS} that makes the channel shallower near the drain.

the relationship between i_D and v_{DS} can be found by replacing v_{OV} in Eq 1

$$i_D = k'_n \left(\frac{W}{L}\right)\left(v_{OV} - \frac{1}{2}v_{DS}\right)v_{DS}$$

This relationship describes the semi-parabolic portion of the $i_D - v_{DS}$ curve in the following curve

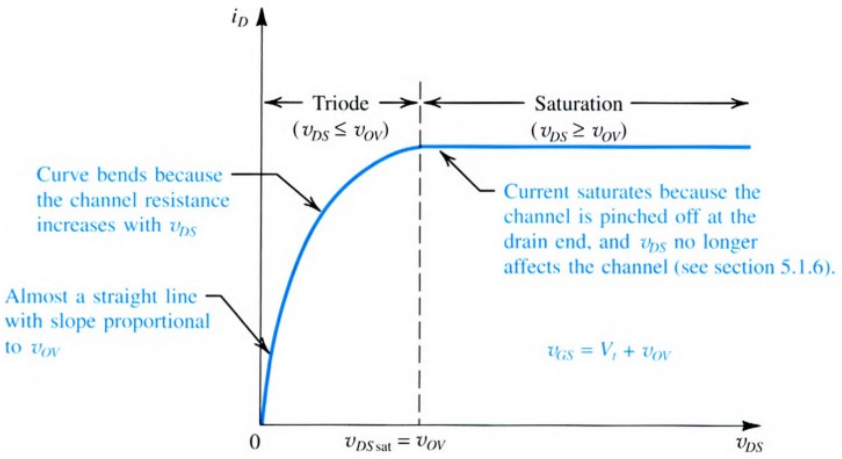

Figure 6: The drain current i_D versus the drain-to-source voltage v_{DS} for an enhancement-type NMOS transistor operated with $v_{GS} = V_t + v_{ov}$

calculating the maximum value

$$\frac{\partial i_D}{\partial V_{DS}} = K_n (v_{OV} - v_{DS}) \qquad \text{let } \frac{\partial i_D}{\partial v_{DS}} = 0$$

$\therefore V_{OS} = V_{OV}$

e.g. i_D reaches the maximum value when $v_{DS} = v_{OV}$, at this point , channel depth at the drain end reduces to zero (pinch-off)

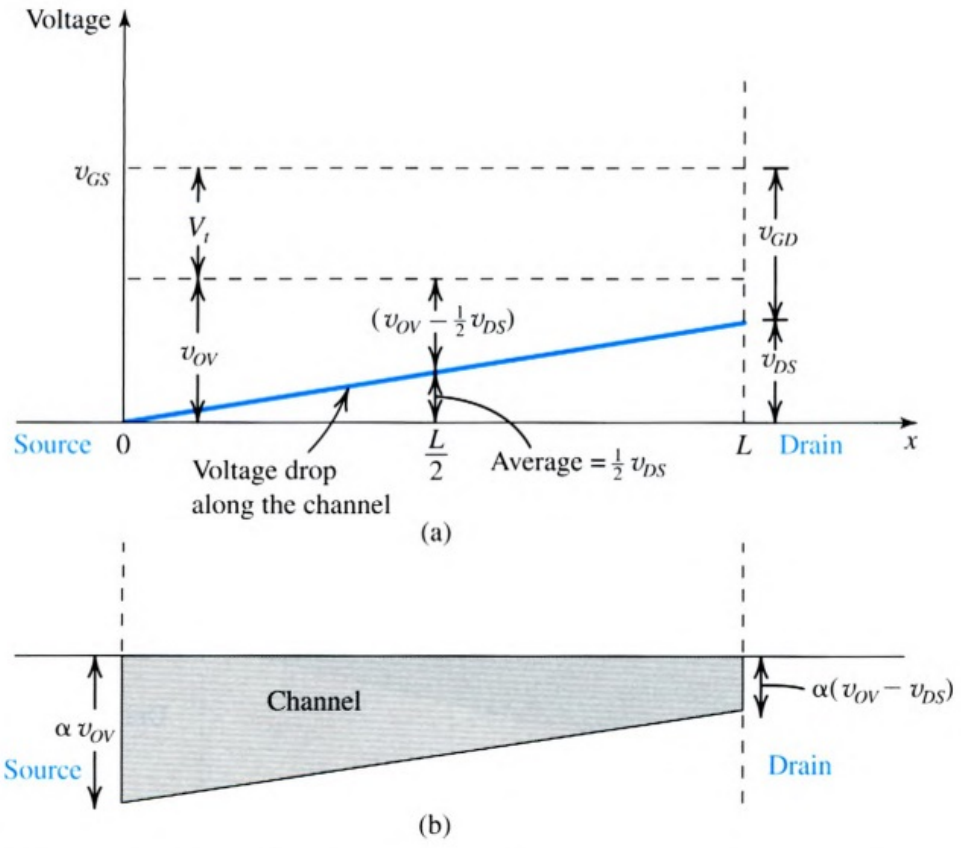

Figure 7: (a) For a MOSFET with $v_{GS} = V_t + v_{OV}$ applying of v_{DS} causes the voltage drop along the channel to vary linearly, with an average value of $\frac{1}{2}v_{DS}$ at the midpoint. Since $v_{GD} > V_t$, the channel still exists at the drain end. (b) The channel shape corresponding to the situation in (a). While the depth of the channel at the source end is still proportional to v_{OV}, that at the drain end is proportional to $(v_{OV} - v_{DS})$.

6 Operation for $v_{DS} > v_{OV}$: Channel Pinch-Off and Current Saturation

for as $v_{DS} = v_{OV}$, $v_{GD} = V_t$, and the channel depth at the drain end reduces to zero

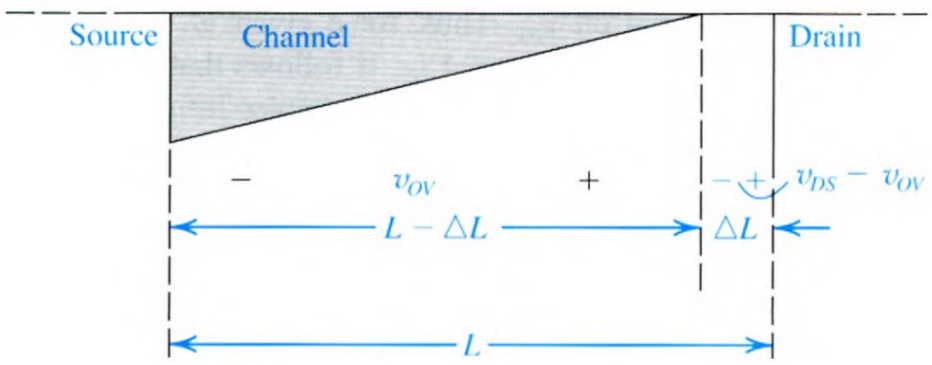

Figure 8: Operation of MOSFET with $v_{GS} = V_t + v_{OV}$, as v_{DS} is increased to v_{OV}. At the drain end, v_{GD} decreases to V_t and the channel depth at the drain end reduces to zero (pinch-off). At this point, the MOSFET enters the saturation mode of operation. Further increasing v_{DS} (beyond $v_{DS\,\text{sat}} = v_{ov}$) has no effect on the channel shape and i_D remains constant

shows v_{DS} reaching v_{OV} and v_{GD} correspondingly reaching V_t. The zero depth of the channel at the drain end gives rise to the term channel pinch-off. Increasing v_{DS} beyond this value (i.e., $v_{DS} > v_{OV}$) has no effect on the channel shape and charge, and the current through the channel remains constant at the value reached for $v_{DS} = v_{OV}$. We say that the drain current saturates at the value found by substituting $v_{DS} = v_{OV}$ or in terms of v_{OV}

$$i_D = \frac{1}{2} k'_n \left(\frac{W}{L}\right) v_{OV}^2$$

we can replace v_{OV} in by $(v_{GS} - V_t)$ to obtain the alternate expression for saturation-mode i_D

$$i_D = \frac{1}{2} k'_n \left(\frac{W}{L}\right) (v_{GS} - V_t)^2$$

7 The $i_D - v_{GS}$ Characteristic

When the MOSFET is used to design an amplifier, it is operated in the saturation region. As the following figure indicates, in saturation the drain current is a constant determined by v_{GS} (or v_{OV}) and is independent of v_{DS}. That is, the MOSFET operates as a constant-current source where the value of the current is determined by v_{GS}. In effect, then, the MOSFET operates as a voltage-controlled current source with the control relationship described by

$$i_D = \frac{1}{2}k'_n\left(\frac{W}{L}\right)(v_{GS} - V_{tn})^2$$

where V_{tn} to denote the threshold voltage of the NMOS transistor

or in terms of v_{OV}

$$i_D = \frac{1}{2}k'_n\left(\frac{W}{L}\right)v_{OV}^2$$

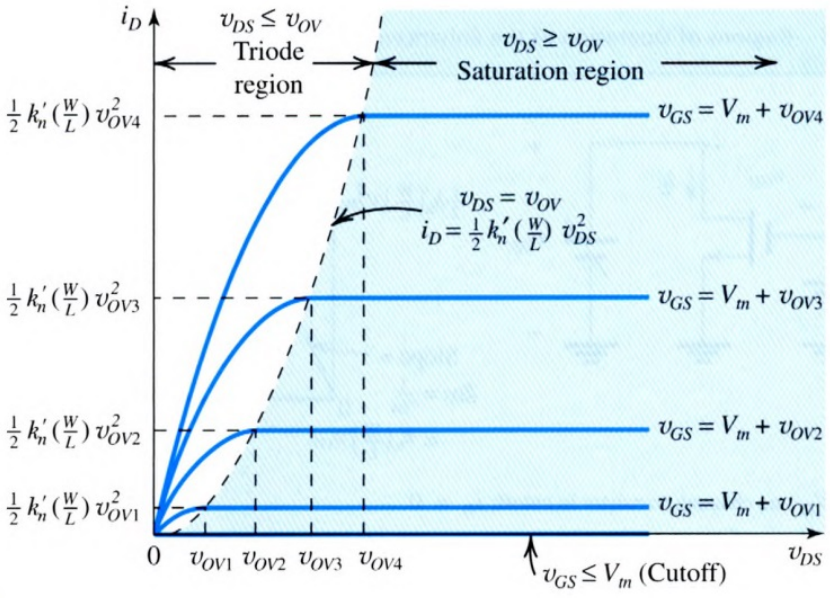

Figure 9: The $i_D - v_{DS}$ characteristics for an enhancement-type NMOS transistor.

8 Finite Output Resistance in Saturation (when v_{DS} reduces so it reduces the channel even more)

in practice, increasing v_{DS} beyond a certain point affects the channel somewhat, causing the channel pinch-off point to move slightly away from the drain. This reduces the channel length, resulting in channel-length modulation, and causes i_D to increase with v_{DS}, We account for this effect in the expression for i_D by including a factor $1 + \lambda(v_{DS} - v_{OV})$ or, for simplicity, $(1 + \lambda v_{DS})$,

$$i_D = \frac{1}{2}k'_n\left(\frac{W}{L}\right)(v_{GS} - V_{tn})^2(1 + \lambda v_{DS})$$

Here λ is a device parameter whose units are reciprocal volts (V^{-1})

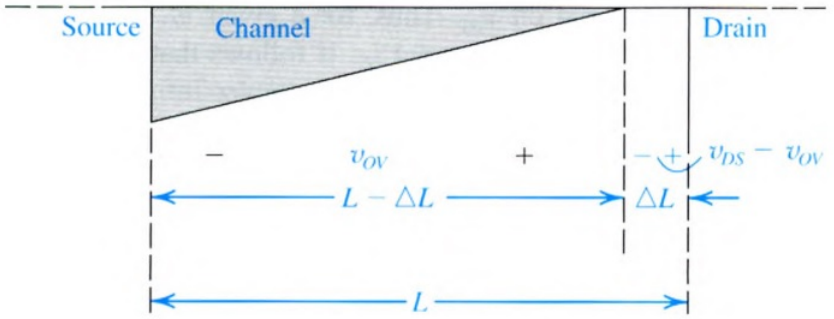

Figure 10: Increasing v_{DS} beyond $v_{DS\,\text{sat}}$ (which is equal to v_{OV}) causes the channel pinch-off point to move slightly away from the drain, thus reducing the effective channel length (by ΔL).

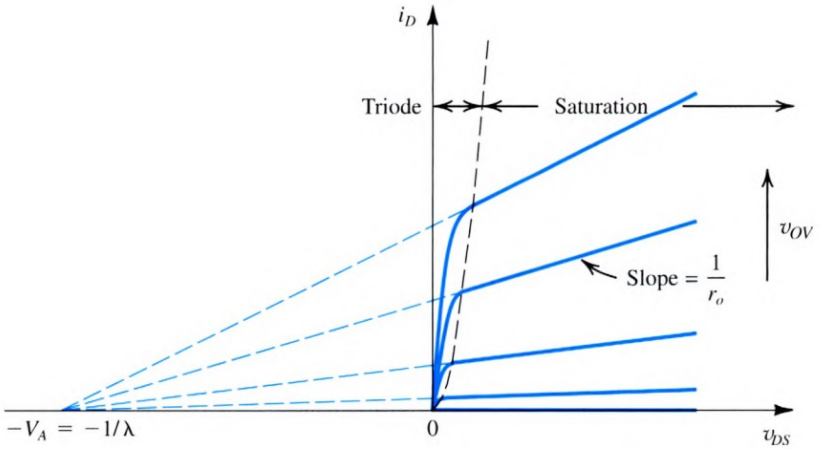

Figure 11: Effect of v_{DS} on i_D in the saturation region. The MOSFET parameter V_A depends on the process technology and, for a given process, is proportional to the channel length L.

from the previous figure:

$$i_D = 0 \qquad \therefore (1 + \lambda v_{DS} = 0)$$

$$\therefore v_{DS} = \frac{-1}{\lambda}$$

$$V_A = V_A' L$$

where

V_A' : process-technology dependent (constant) $\left(\frac{V}{\mu m}\right)$ (range of 5 $\left(\frac{V}{\mu m}\right)$ to 50 $\left(\frac{V}{\mu m}\right)$)

V_A : Early voltage

9 Large-signal, equivalent-circuit model of the n-channel MOSFET

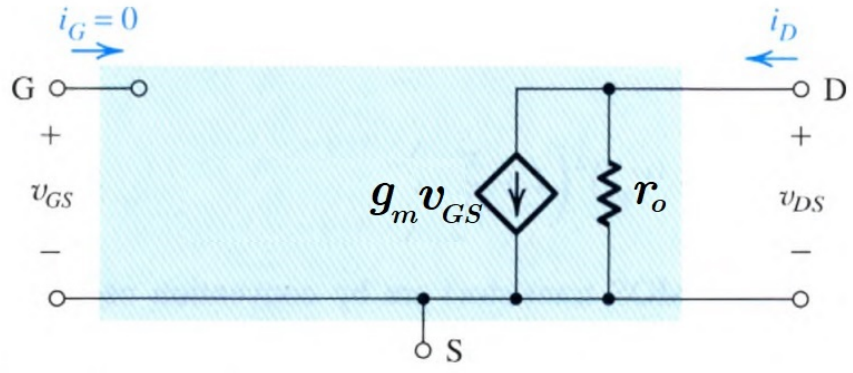

Figure 12: Large-signal, equivalent-circuit model of the n-channel MOSFET in saturation, incorporating the output resistance ro. The output resistance models the linear dependence of iD on vDS and is given by)

the relation between v_{GS} and the current i_D can be models using g_m (transconductance)

$$g_m \equiv \frac{\partial i_D}{\partial v_{GS}} = \frac{\Delta i_D}{\Delta v_{GS}}$$

Defining the output resistance r_o

$$r_o \equiv \left.\frac{\partial v_{DS}}{\partial i_D}\right|_{v_{GS} \text{ constant}} \qquad \therefore r_o = \frac{V_A}{i'_D}$$

where i_D is the drain current without channel-length modulation taken into account; that is:

$$i_D = \frac{1}{2} k'_n \left(\frac{W}{L}\right) (v_{GS} - V_{tn})^2$$