

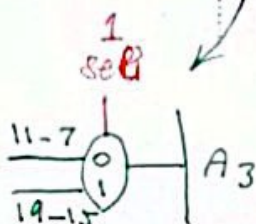
حل تہیں سرے دوں  
مجموعی آکسپریس

For ( $i \leftarrow 0$ ;  $i < 1000$ ;  $i++$ )  
 For ( $j \leftarrow i$ ;  $j < 1000$ ;  $j++$ )  
 if ( $A[i] < A[j]$ ) {  
     tmp = A[i];  
     A[i] = A[j];  
     A[j] = tmp;  
 }

Loop1 :	add \$0, zero, zero	; i = 0
	slti t2, \$0, 4000	{ شرط طے کرنا ہے
	beg t2, zero, END-Loop1	
	add \$1, \$0, zero	; j = i
Loop2 :	slti t2, \$1, 4000	{ شرط طے کرنا ہے
	beg t2, zero, END-Loop2	
	lw t0, A(\$0)	; t0 = A[i]
	lw t1, A(\$1)	; t1 = A[j]
	slt t2, t0, t1	{ if شرط ہے
	beg t2, zero, END-IF	
	sw t1, A(\$0)	{ swap
	sw t0, A(\$1)	
END-IF :	addi \$1, \$1, 4	; j++
	j Loop2	; تکرار
END-Loop2 :	addi \$0, \$0, 4	; i++
	j Loop1	; تکرار
END-Loop1 :	:	

The diagram illustrates a MIPS-like processor architecture with the following components and connections:

- Control Unit:** Receives control signals and outputs:
  - `PCSrc`: 0
  - `ResultSrc`: 11
  - `MemWrite`: 1
  - `ALUControl`: 00001
  - `ALUSrc`: 1
  - `ImmSrc`: 01
  - `RegWrite`: 1
- Instruction Memory:** Receives `PC` and `Instr` (from `PCNext`). It outputs `Inst` to the `Register File`.
- Register File:** Contains registers `A1`, `A2`, and `A3`. `A1` contains 19, `A2` contains 24, and `A3` contains 11. It outputs `SrcA` (19) and `SrcB` (1) to the `ALU`.
- ALU:** Receives `SrcA` and `SrcB`. It outputs `ALUResult` (11) and `Zero` (0).
- Data Memory:** Receives `WriteData` (11) and `ReadData` (11). It outputs `ReadData` (11) to the `Result` register.
- PC (Program Counter):** Receives `PCNext` (0) and `PCPlus4` (4). It outputs `PC` (0) to the `Instruction Memory`.
- Result:** Receives `ReadData` (11) and outputs the final `Result` (11).



swap

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