UNIVERSITY OF TEHRAN

Electrical and Computer Engineering Department

Digital Logic Design, ECE 367 / Digital Systems I, ECE 894

Fall 1402

Homework 4

Karnaugh-Map, Hazards

Name:	**Date:**
Username:	

1. Using Boolean algebra rules minimize the following function and show the NAND realization of the minimized functions.

$$f(a,b,c,d) = a'.b'.c.d' + a'.b.c' + b.c.d + a'.c.d' + b'.c.d' + a.b'.c$$

2. Using Boolean algebra rules minimize the following function and show the NOR realization of the minimized functions.

$$f(a,b,c,d) = a'.b'.c' + a'.b'.c + a.b' + b'.c'.d + b'.c.d'$$

3. Minimize the following function using NOT, 2-input and 3-input NAND gates. the delays of these gates are #6, #5, and #8 NS respectively.
   a. Show all NAND implementation of this circuit resulted from the two-level minimized circuit. Find the worst-case delay value.
   b. Show NAND implementation using only gates listed above. Find the worst-case delay value.
   c. Arrange the gate structure of Part b in such a way to reduce the worst-case delay of the circuit, still using only gates listed above. Find the worst-case delay value.
   d. Write SystemVerilog description of Part c using SystemVerilog primitives.
   e. Using the worst-case delay of Part c, write SystemVerilog description of this circuit using an **assign** statement.
   f. Find input transitions that the circuit of Part a and Part c have different timing behaviors.

$$f(a,b,c,d) = \sum_m (3, 4, 5, 10, 11, 13, 14, 15)$$

4. For the given circuit,
   a. List all potential static hazards
   b. List the logical hazards including their duration, the time they occur and input transition causing them
   c. Of all logical hazards, list those that are also considered as electrical hazards, and
   d. If the output gate drives two gates similar to its own input, then which of the logical hazards also become electrical hazard?

$$f(a,b,c,d) = \sum_m (1, 3, 4, 5, 10, 11, 14, 15)$$

5. Show all minimal two-level SOP minimizations for the following function. Show the circuit using 2-input NAND gates only.

$$f(a,b,c,d) = \sum_m (0, 1, 3, 4, 5, 10, 11, 12, 14), d(13, 15)$$

6. Show all minimal two-level POS minimizations for the following function. Show the circuit using 2-input NOR gates only.

$$f(a,b,c,d) = \sum_m (0, 1, 3, 4, 5, 10, 11, 12, 14), d(13, 15)$$

7. Use tabular QM minimization method to reach the minimal realization of the function shown below. Show all necessary steps and tables.

$$f(a,b,c,d) = \sum_m (0, 1, 3, 4, 5, 10, 11, 12, 14), d(13, 15)$$

8. Show all forms of two-level POS minimizations for the following function.

$$f(a,b,c,d) = \prod_M (0, 1, 3, 4, 5, 10, 11, 12, 14), d(13, 15)$$

9. Show all forms of two-level SOP minimizations for the following function.

$$f(a,b,c,d) = \prod_M (0, 1, 3, 4, 5, 10, 11, 12, 14), d(13, 15)$$