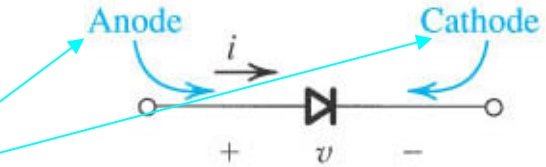
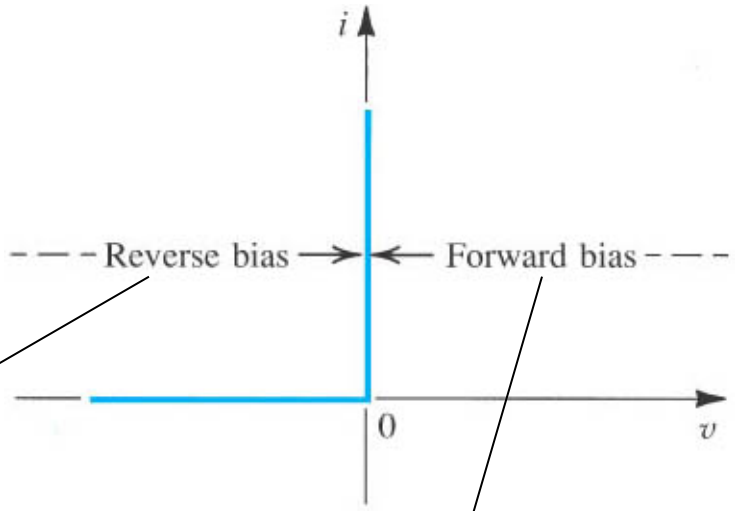
The Ideal Diode

- Most Fundamental non-linear element
- Two terminal device



Terminology from the days of vacuum-tubes

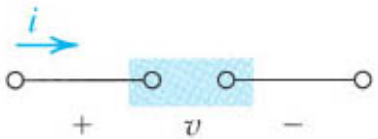
(a)



(b)

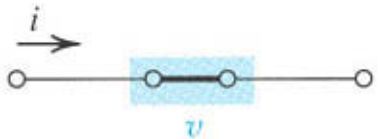
In Cutoff or Simply ‘Off’

Is turned on or Simply ‘On’



$v < 0 \Rightarrow i = 0$

(c)



$i > 0 \Rightarrow v = 0$

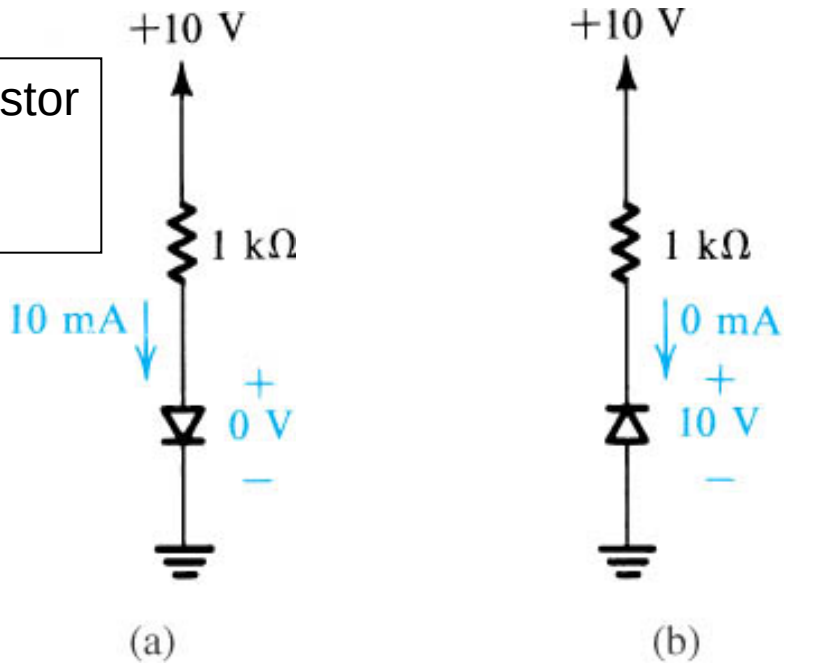
(d)

Figure 3.1 The ideal diode: **(a)** diode circuit symbol; **(b)** *i*–*v* characteristic; **(c)** equivalent circuit in the reverse direction; **(d)** equivalent circuit in the forward direction. Source: Page 140 Sedra and Smith 5th Edition

The Ideal Diode

Example:

1k ohm resistor determines current

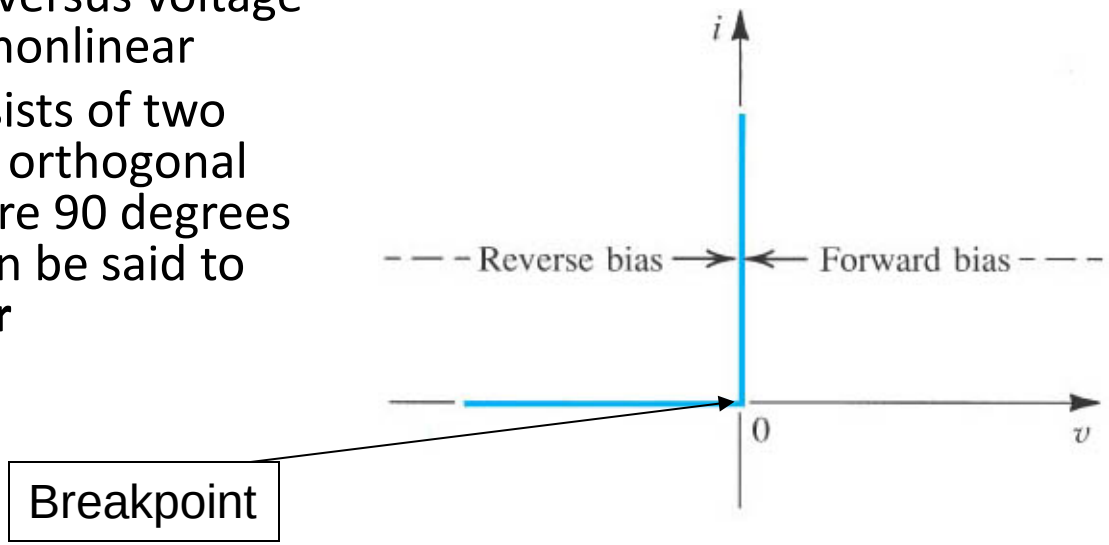


All 10 volts Appears Across the Reverse biased diode

Figure 3.2 The two modes of operation of ideal diodes and the use of an external circuit to limit the forward current **(a)** and the reverse voltage **(b)**. Source: Page 141 Sedra and Smith 5th Edition

The Ideal Diode

- Ideal diode current versus voltage (i-v) curve is highly nonlinear
- But, because it consists of two straight lines, albeit orthogonal (ie operating lines are 90 degrees to each other), it can be said to be **piece-wise linear**



- **Advantage**: If we have a circuit element which exhibits a piece-wise or near piece-wise linear operation and we choose to operate this circuit in the piece-wise linear location / region (eg small signal equivalent circuit models we will see later) then we can treat the circuit as a linear circuit in our analysis – provided we do not allow our design to swing across breakpoints where the circuit switches from one segment of linear operation to another!
- Sometimes a circuit may not be piece-wise linear, like a diode, but if small enough signals are used it can be close enough for analysis.

Circuits with Ideal Diodes

Diode Logic Gates

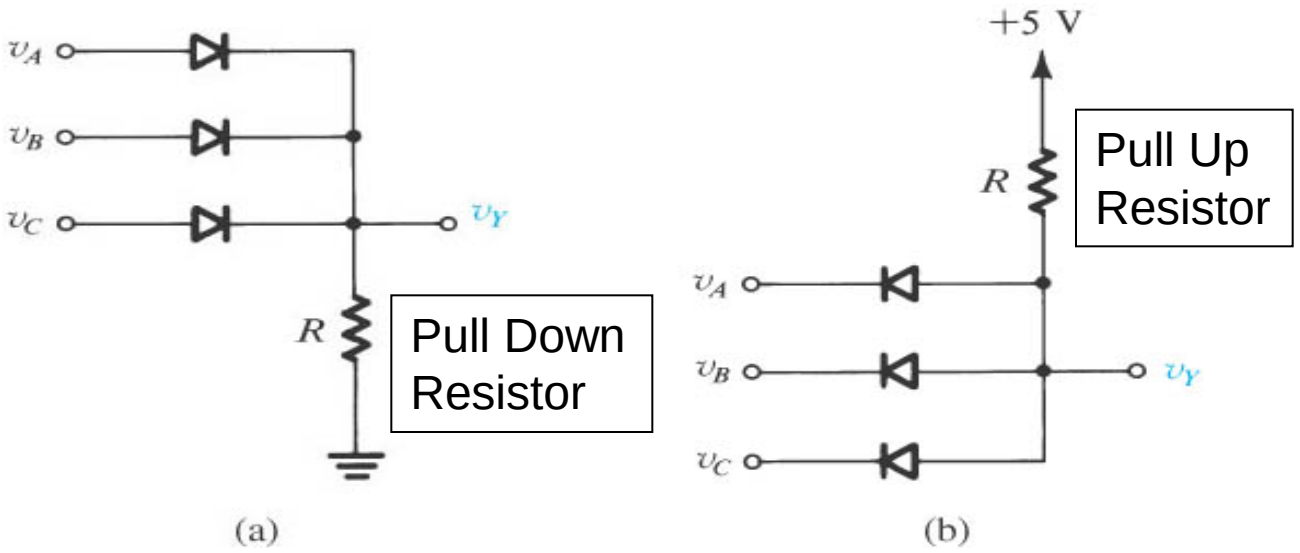
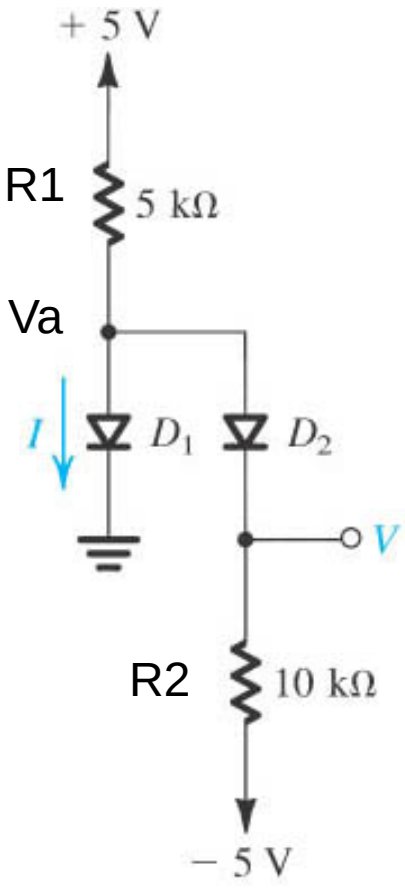


Figure 3.5 Diode logic gates: **(a)** OR gate; **(b)** AND gate (in a positive-logic system). Source: Page 144 Sedra and Smith 5th Edition

If 0V represents 0 and +5V represents 1 (positive logic) then:

- Circuit (a) will have 5V at v_y if any of v_a,v_b, v_c are +5V with any diode or all diodes in the 'on' state; it will be 0V at v_y (pulled down by resistor R) if all inputs are 0V and thus the diodes are all 'off' the logic OR function.
- Circuit (b) will have 0V at v_y if any of v_a,v_b, v_c are 0V with any diode then forward biased ('on' state) but if all of v_a,v_b, v_c are at +5V then the diodes will be 'off' and v_y will be +5V (pulled up by R) thus implementing a logic AND function

Circuits with Ideal Diodes



Q? For the circuit shown find the current I and the Voltage V. (problem 3.9a from Sedra and Smith)

Ans: We need to determine if D_1 , D_2 or both are conducting? So we should make plausible assumptions, proceed and then determine if these assumptions lead to a consistent solution.

So it seems plausible that both D_1 and D_2 are conducting.

If so then all 5V is dropped across the 5kohm resistor R1; resulting in current through R1=5/5k=1mA;

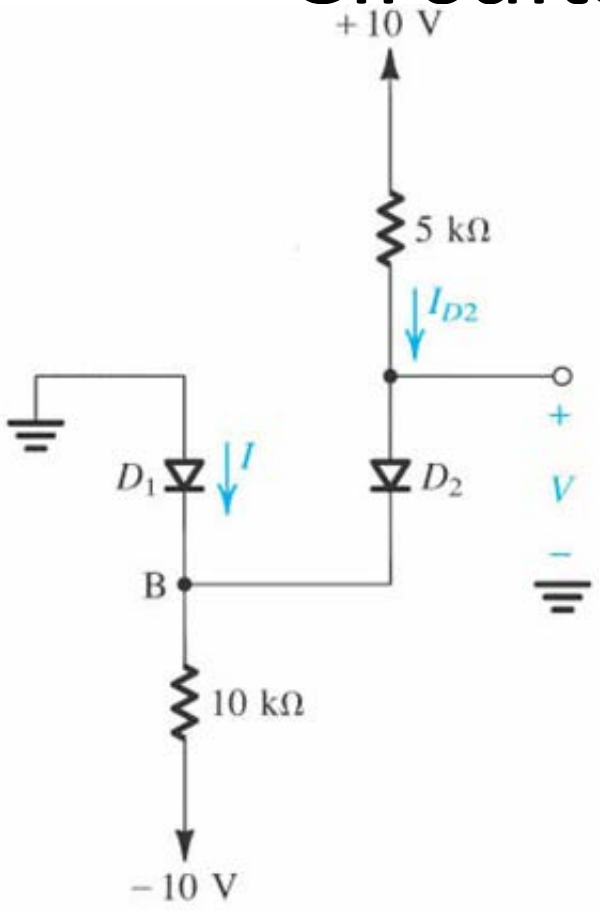
Also if D_2 is conducting V=0 volts and the current through R2 =(0-(-5))/10k=0.5mA

Which means that I=1mA-0.5mA=0.5mA

This seems to be a consistent solution

In fact if D_2 isn't conducting then the voltage Va must be less than -5V and D_1 must be on (for a current flow) but once D_1 is on then Va must be 0 volts (as D_1 is ideal and will have a 0 volt drop across it) so such a solution is not consistent;

Circuits with Ideal Diodes



Now consider this circuit, once again lets assume that D_1 and D_2 are 'on' . If this is so then V_B=0 and V=0

The current in D_2,

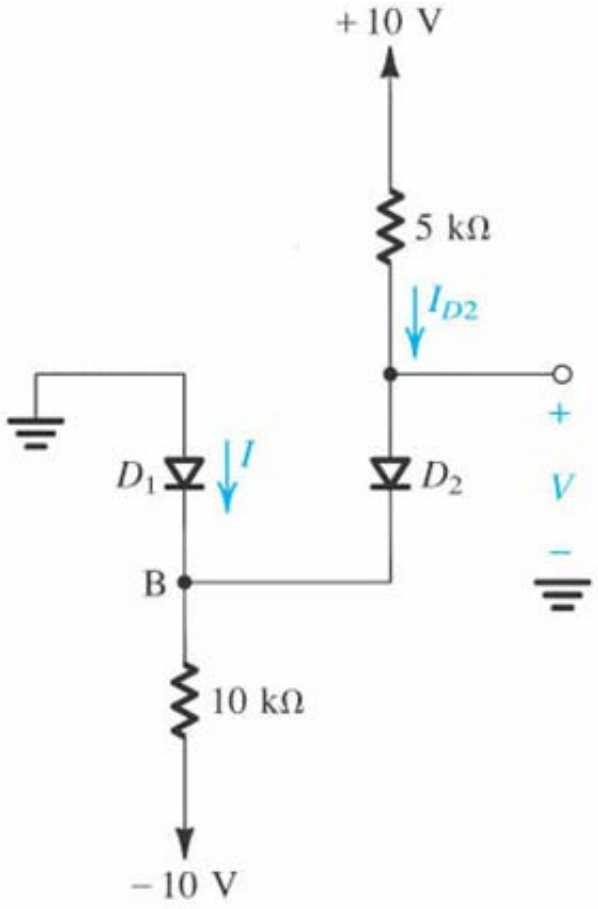
$$I_{D2} = \frac{10-0}{5} = 2mA$$

Forming KCL (Kirchhoff's Current Law) nodal equation at node B gives:

$$I + 2 = \frac{0-(-10)}{10}$$

which results is an inconsistent current for I of -1mA!! So D_1 and D_2 cannot be both on!

Circuits with Ideal Diodes



Now assume D_1 is 'off' and D_2 is 'on'
The current in D_2 is then:

$$I_{D2} = \frac{10-(-10)}{(10+5)} = 1.33mA$$

and the voltage at node B is:

$$V_B = -10 + (10 * 1.33) = +3.3V$$

Which is consistent with D_1 being off and D_2 being on; hence V_B=3.3V and I=0 for this circuit

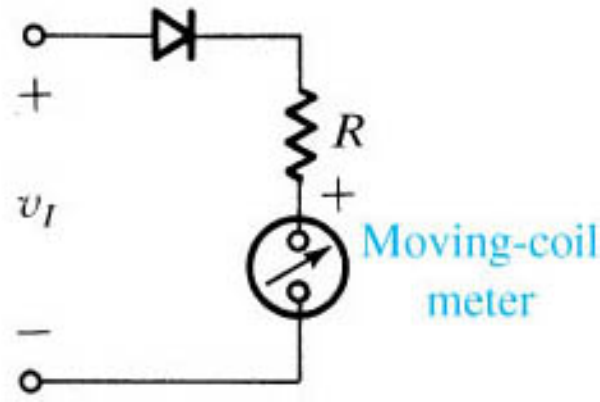
Circuits with Ideal Diodes

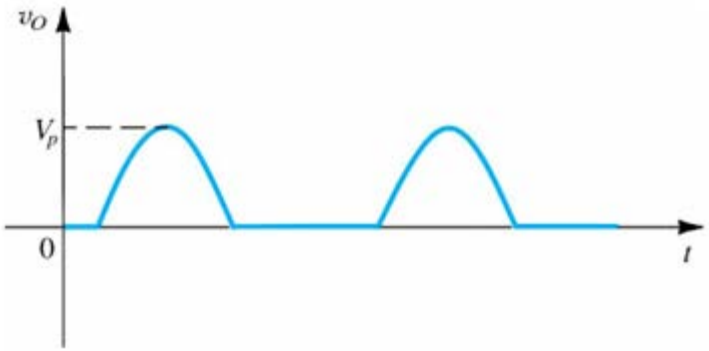
Q?: The figure shows a circuit for an ac voltmeter. It utilizes a moving coil meter that gives a full scale reading when the average current flowing through it is 1mA. The moving coil meter has a resistance of 50 ohms. Find the value of R that results in the meter indicating full scale reading when the input sine wave voltage v_I is 20 Volts peak to peak. Given that the average of a half sine wave (result of half wave rectification with ideal diode) is peak value divided by π.

Ans: Peak current = (10 Volts peak) / (R+50Ω)

Thus average current = $\frac{1}{\pi} \cdot \frac{10}{R+50}$

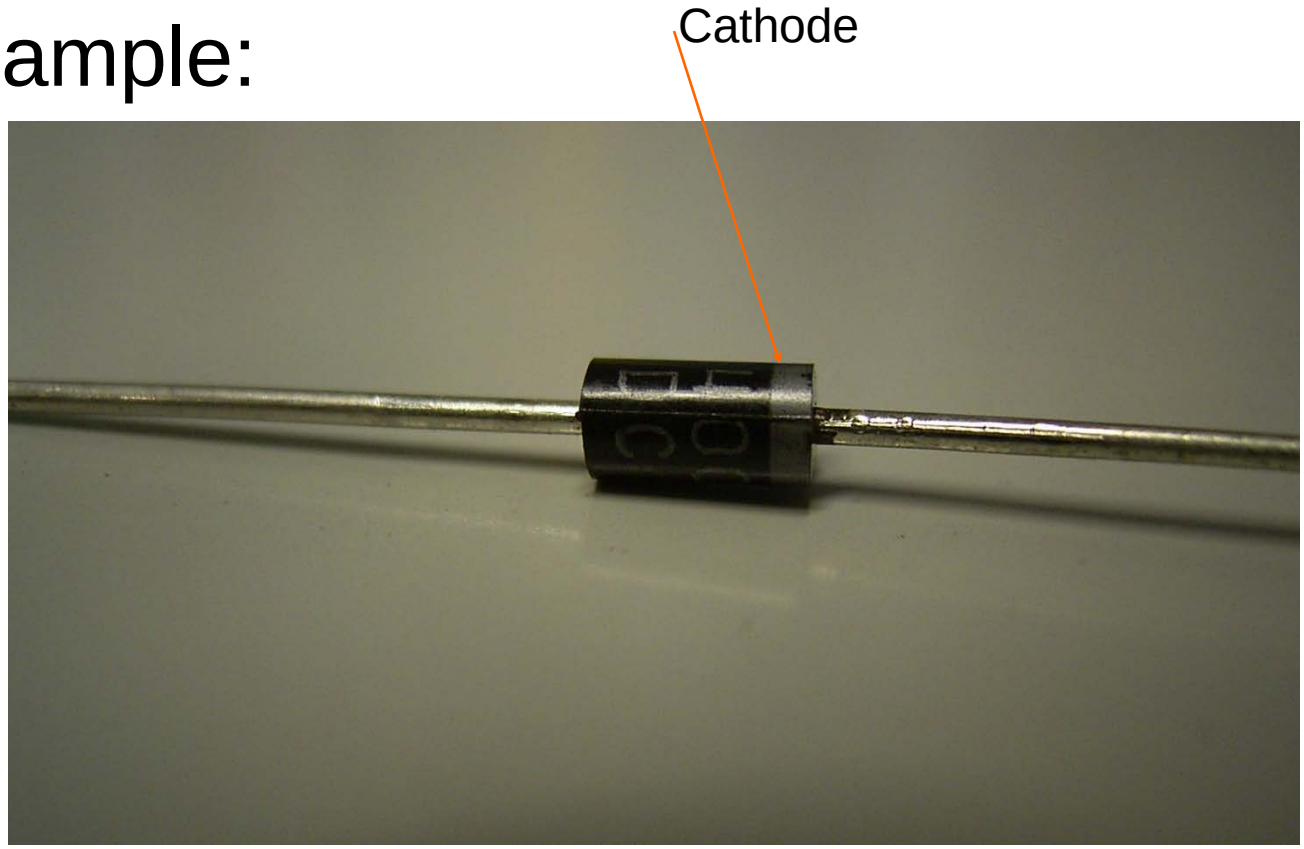
Equate this to 1mA (for full scale deflection) and re-arranging results in an R =3133Ω





Real Diodes: Diode Markings

- The Cathode (K) is usually marked with a silver bar
- Example:



Real Diodes

Silicon Junction Diode

The current-voltage relationship of a typical silicon junction diode appears like this:

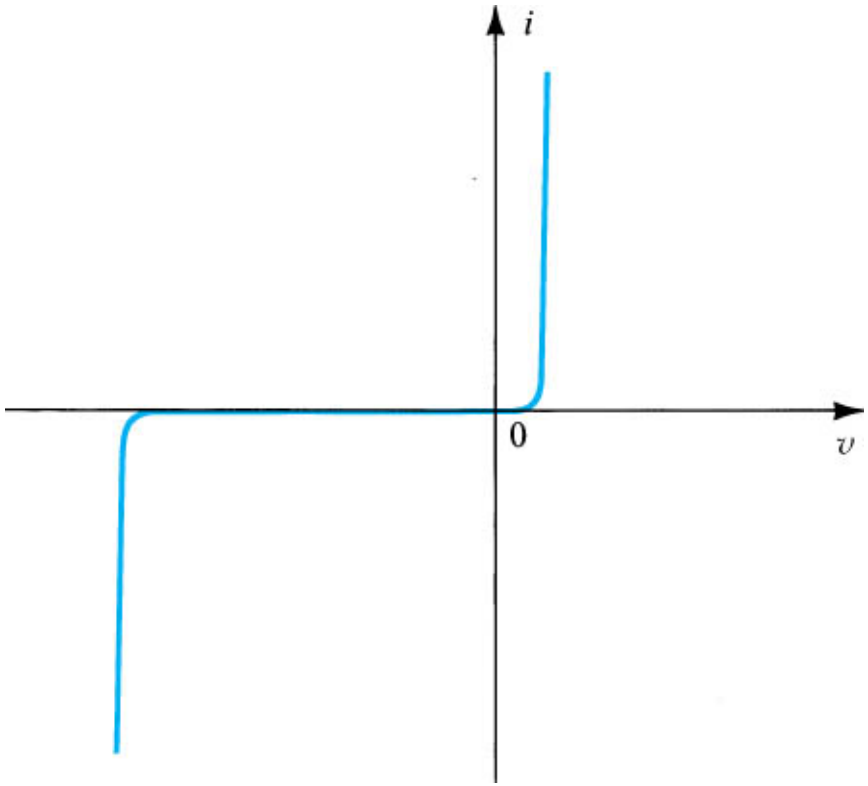


Figure 3.7 The *i–v* characteristic of a silicon junction diode.

Real Diodes

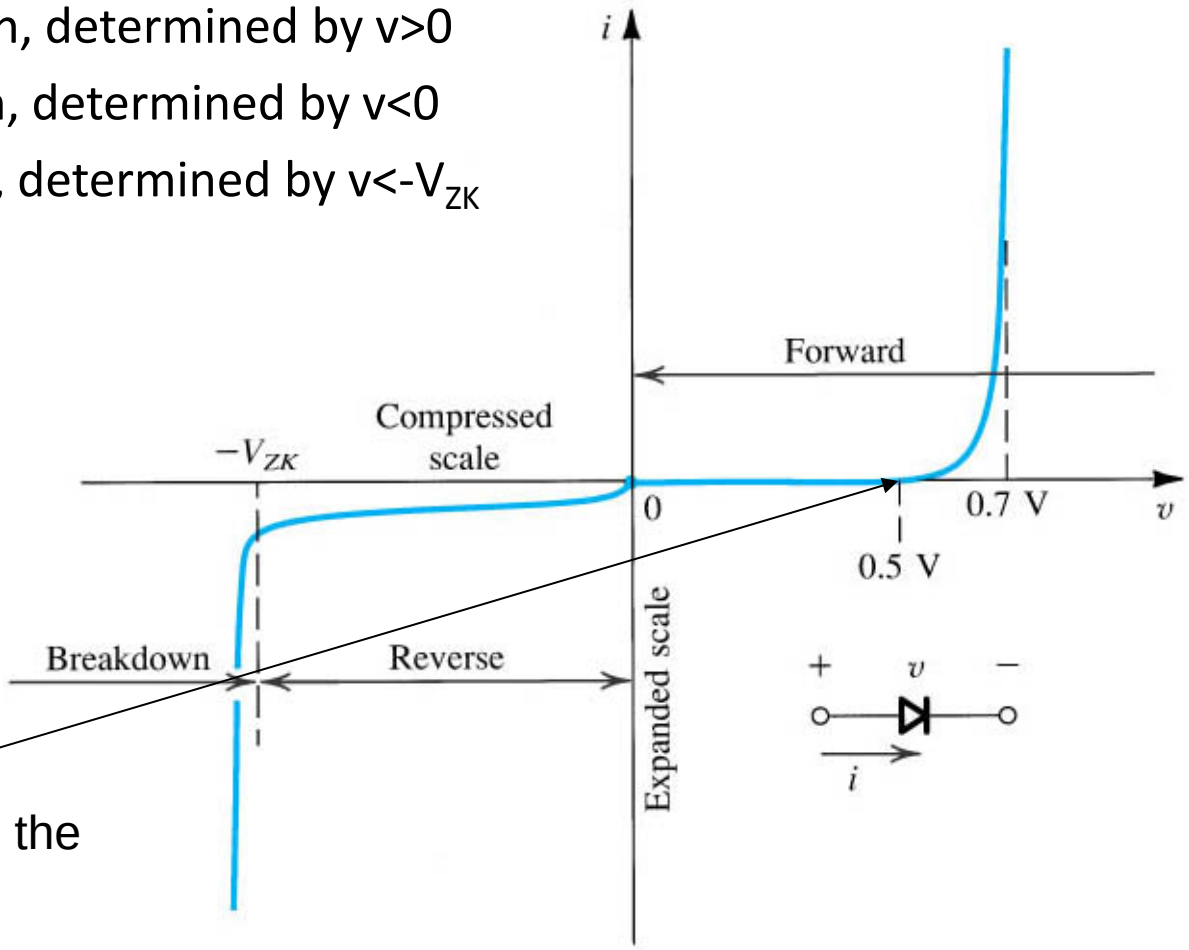
Silicon Junction Diode

Three distinct regions are:

i) The **forward bias** region, determined by v>0

ii) The **reverse bias** region, determined by v<0

iii) The **breakdown** region, determined by $v<-V_{ZK}$



Note: below 0.5V
the current is negligibly small
The voltage 0.5V is referred to as the
cut-in voltage

Figure 3.8 The diode *i–v* relationship with some scales expanded and others compressed in order to reveal details.

Real Diodes: Silicon Junction Diode

Forward Bias Region

When v>0 we have:

- i-v relationship closely approx. by→

$$i = I_S\left(e^{v/nV_T} - 1\right)$$

  - I_s is usually called the **Saturation Current** (sometimes called the **Scale Current**)
  - For small signal diodes (low power) it has a value in the order of 10^{-15} Amps
  - Rule of thumb: for every 5 degrees of temperature I_s doubles in value
- V_T is called the thermal voltage
  - given by:
  - k= Boltzmann's constant = 1.38×10^{-23} joules / kelvin
  - T=the absolute temperature in kelvins = 273+temp in celsius
  - q= the magnitude of charge of an electron = 1.60×10^{-19} coulomb

$$V_T = \frac{kT}{q}$$

Real Diodes: Silicon Junction Diode

Forward Bias Region

$$i = I_S\left(e^{v/nV_T} - 1\right)$$

- For V_T:
  - At room temperature (20 degrees C) the value of V_T is 25.2mV
  - At 25 degrees (often assumed for electronic equipment stored in a cabinet) it is 25.8mV
  - For simplicity we will use 25mV
- The constant n in equation:
  - Has a value between 1 and 2 (function of material used and physical structure of diode)
  - Normally assume n=1 (unless stated otherwise)

Real Diodes: Silicon Junction Diode
Forward Bias Region

For the case where the current $i >> I_s$ the approximation that can be used is:

$$i \cong I_S e^{v/nV_T}$$

Alternatively we can express this in logarithmic (natural-base e) form:

$$v \cong nV_T \ln\left(\frac{i}{I_S}\right)$$

Exponential i-v relationship holds over many decades of current – can be as much as a span of 7 decades ie a factor of 10^7 ===> This also applies to BJT's

Real Diodes: Silicon Junction Diode

Forward Bias Region

Using $$i \cong I_S e^{v/nV_T}$$

And evaluating the current I_1 which related to a diode voltage V_1 we have:

$$I_1 = I_S e^{V_1/nV_T}$$

And evaluating the current I_2 which related to a diode voltage V_2 we have:

$$I_2 = I_S e^{V_2/nV_T}$$

Dividing the second equation by the first gives:

$$\frac{I_2}{I_1} = e^{(V_2 - V_1)/nV_T}$$

Real Diodes: Silicon Junction Diode

Forward Bias Region

Taking natural logarithms of both sides gives:

$$\ln\left(\frac{I_2}{I_1}\right) = \ln\left(e^{(V_2-V_1)/nV_T}\right)$$

$$\ln\left(\frac{I_2}{I_1}\right) = (V_2-V_1)/nV_T$$

which means that:

$$V_2 - V_1 = nV_T \ln\left(\frac{I_2}{I_1}\right)$$

Or we can get the results in terms of log10 by changing the base:

Since,

$$\log_a N = \frac{\log_b N}{\log_b a}$$

$$\therefore \ln\left(\frac{I_2}{I_1}\right) = \frac{\log_{10}\left(\frac{I_2}{I_1}\right)}{\log_{10} e} \quad \text{where} \quad \frac{1}{\log_{10}(e)} \cong 2.3$$

Which gives:

$$V_2 - V_1 = 2.3nV_T \log_{10}\left(\frac{I_2}{I_1}\right)$$

Real Diodes: Silicon Junction Diode

Forward Bias Region

$$V_2 - V_1 = 2.3nV_T \log_{10}\left(\frac{I_2}{I_1}\right)$$

Simply stated, for a decade of change in current the diode voltage drop changes by $2.3nV_T$:

- About 60mV for n=1
- About 120mV for n=2

This suggests that diode *i-v* characteristics are best plotted on semi-log paper or scales--- using *v* as vertical & linear axis, and *i* as the horizontal and log scaled axis one will obtain a straight line with a slope of $2.3nV_T$ per decade of current

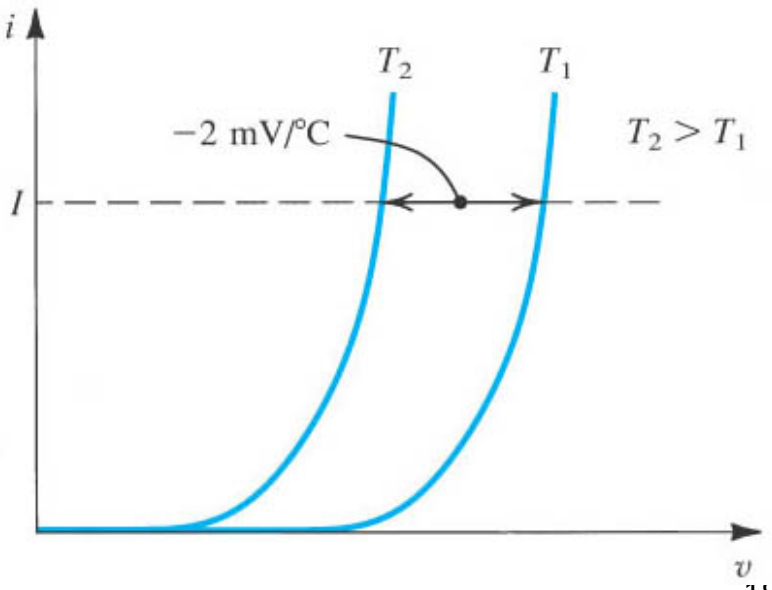
Not knowing 'n' circuit designers use the rule of $2.3nV_T$ being equal to 0.1 V ie a 0.1V/decade change

Real Diodes: Silicon Junction Diode

Forward Bias Region

- Note that diodes with different current ratings will experience a 0.7 V drop (used as a rule of thumb for a fully conducting diode which will be typically in the range of 0.5-0.8V drop- and the basis of the model we will most often employ for diodes) at different currents (see assignment)
- Also, I_S and V_T are both temperature dependent which means forward i-v characteristic is also a function of temperature:

Figure 3.9 Illustrating the temperature dependence of the diode forward characteristic. At a constant current, the voltage drop decreases by approximately 2 mV for every 1°C increase in temperature. (pg 151 Sedra&Smith) This characteristic has been exploited to produce electronic thermometers!



Real Diodes: Silicon Junction Diode

Reverse Bias Region

From $i = I_S\left(e^{v/nV_T} - 1\right)$ (in theory), if v is negative and a few times larger than V_T then we can say that:

$$i \cong -I_S$$

That is the current in the reverse direction is constant and equal in magnitude to the saturation current (this constancy is the origin of its name!)

Real diodes exhibit currents that are still small but larger than I_S would indicate

- eg a small signal diode has I_S about 10^{-14} to 10^{-15} Amps but the reverse current could be of the order of 1nA(10^{-9})

There is also a tendency for the reverse current to increase in magnitude with the reverse voltage

The reverse current is less sensitive to temperature changes doubling (rule of thumb) every 10 °C rise in temperature (see slide 17)

We normally don't need to consider this in an analysis as currents are small compared to a forward biased current

Real Diodes: Silicon Junction Diode

Break down Region

- Used in Zener diodes (diodes designed to be operated in the breakdown region)
- Once the reverse voltage exceeds a voltage called the breakdown voltage the diode will conduct in the reverse direction
- Provided power dissipation is limited by the surrounding circuit topology to a safe level (refer to devices data sheet) the diode can be operated in the breakdown region – normally we only do this to zener diodes in our designs
- One application of the breakdown region is that of a voltage regulator as its i-v characteristic is almost vertical

Diode Models

Forward Bias

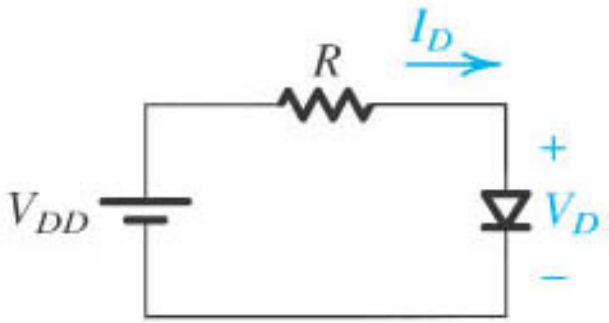
The Exponential Model

- Most accurate model
- Severely non-linear so difficult to use
- A **graphical technique** is employed with a load line or an **iterative technique** is employed

Diode Models Forward Bias

Exponential Model

Consider the circuit:



We have:

$$I_D = I_S e^{V_D/nV_T}$$

And using KVL:

$$I_D = \frac{V_{DD} - V_D}{R}$$

We will assume that n and I_S are known

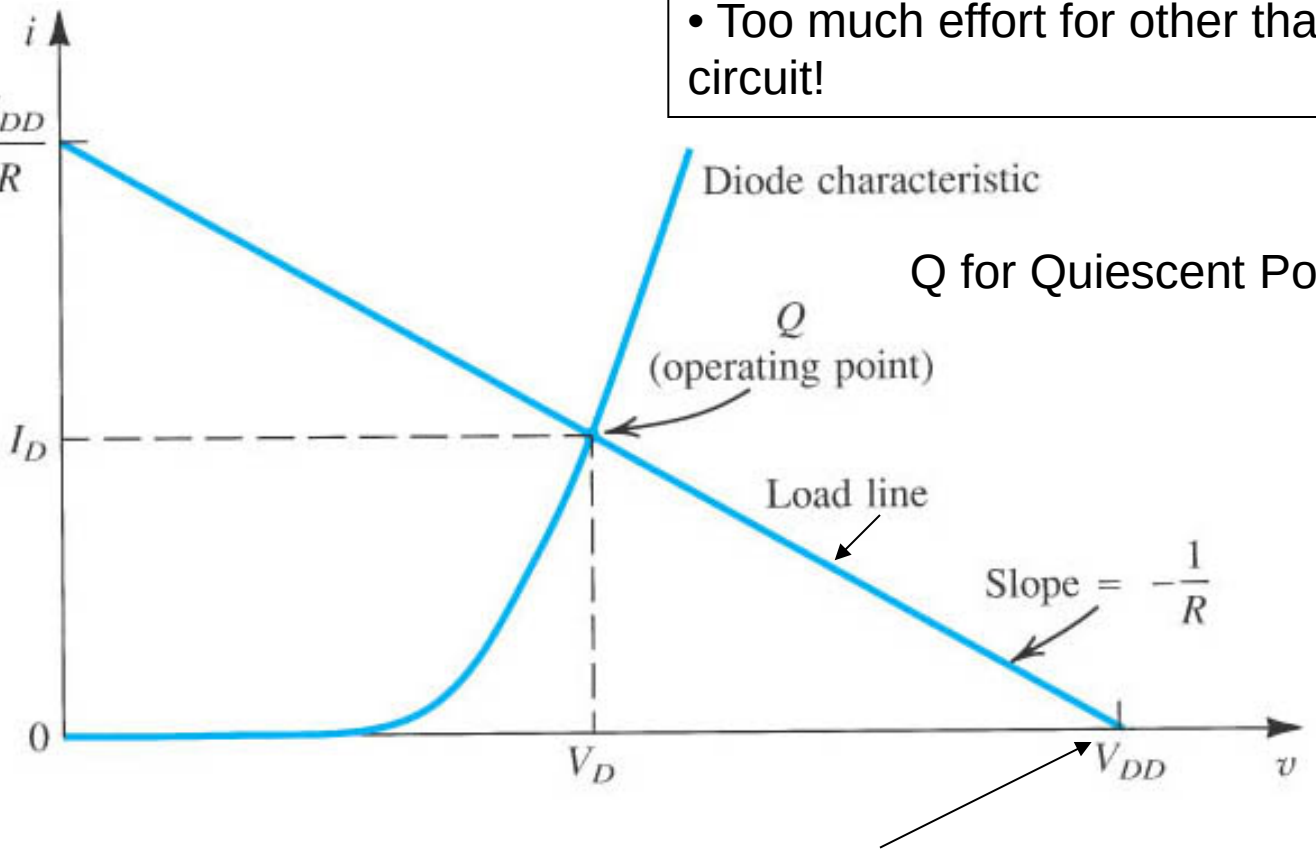
Diode Models Forward Bias

Exponential Model

Graphical Analysis

- Intersection of load line and i-v gives values for I_D and V_D
- Too much effort for other than simple circuit!

For i-axes let Diode voltage drop, v, be zero and calculate i – gives v=0 crossing



For v-axes let the current be 0 (i=0, open circuited diode) and then work out the voltage which would just be the supply voltage I – gives v=0 crossing

Diode Models Forward Bias

Exponential Model

Iterative Analysis

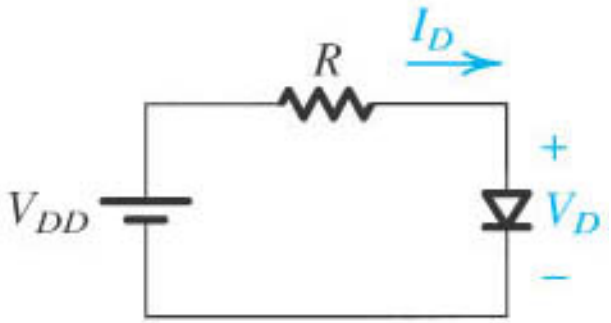
Let R=1 kΩ and V_{DD}=5 V. Assume V_D=0.7 V,

and a voltage drop changes by

0.1V/decade then:

$$I_D = \frac{V_{DD} - V_D}{R}$$

$$= \frac{5 - 0.7}{1} = 4.3mA$$



Now use the diode equation to get a better estimate for V_D:

$$V_2 - V_1 = 2.3nV_T \log_{10}\left(\frac{I_2}{I_1}\right)$$

Using $2.3nV_T$ = 0.1 V (ie a 0.1V/decade change)

solving with V_1=0.7;I_1=1mA;

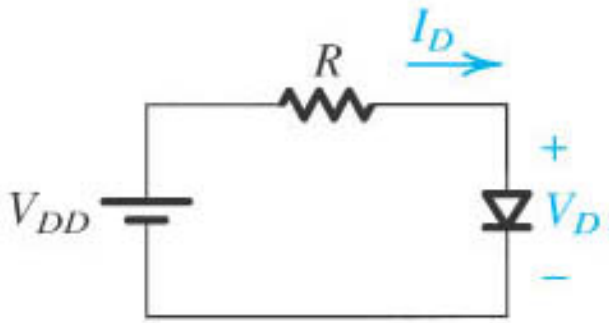
$$V_2 = V_1 + 0.1 * \log_{10}\left(\frac{I_2}{I_1}\right)$$

I_2=4.3mA leads to V_2=0.763V

Diode Models Forward Bias

Exponential Model

Iterative Analysis



The result of the first iteration is then:

I_D=4.3mA and V_D=0.763 V

Now use these values in a second iteration:

$$I_D = \frac{V_{DD} - V_D}{R}$$

$$= \frac{5 - 0.763}{1} = 4.237mA$$

and:

$$V_2 = V_1 + 0.1 * \log_{10}\left(\frac{I_2}{I_1}\right)$$

$$= 0.763 + 0.1 * \log_{10}\left(\frac{4.237}{4.3}\right)$$

$$= 0.762 \quad V$$

The result of the second iteration is then:

I_D=4.237mA and V_D=0.762 V

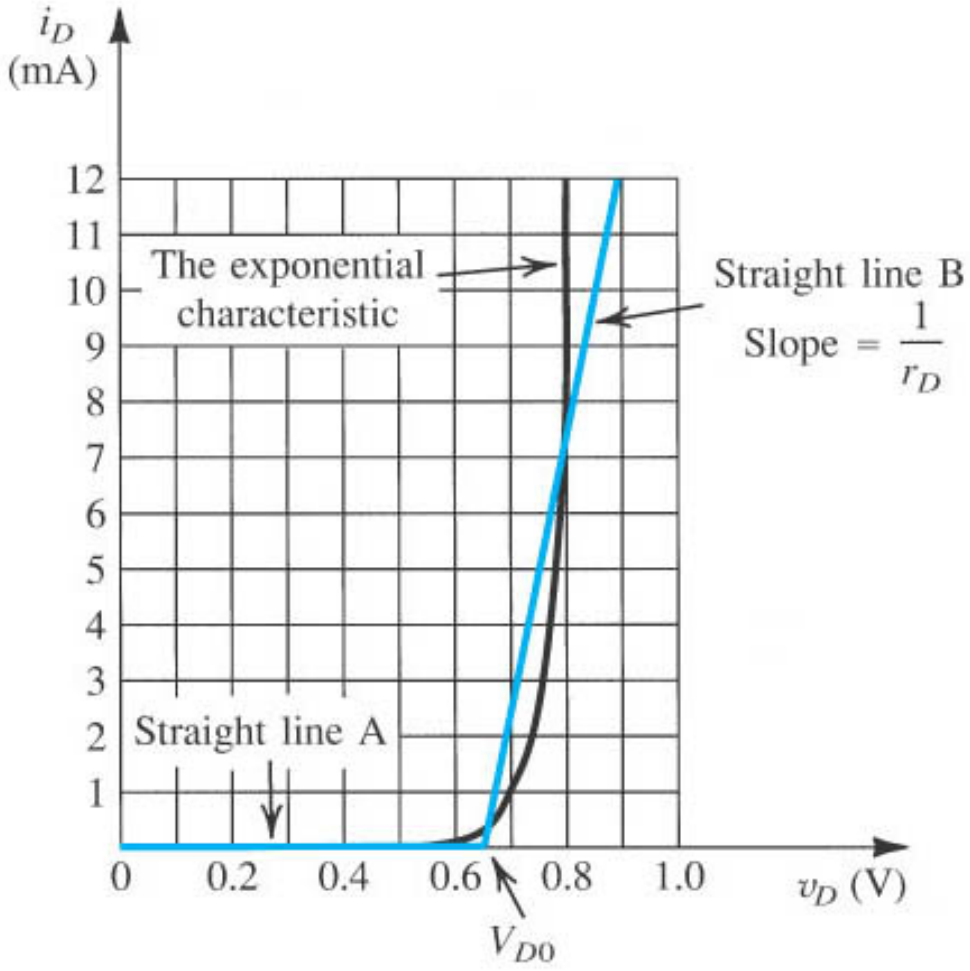
Which is the solution since the change was very small from first iteration

Diode Models Forward Bias

Piecewise-Linear Model

- Approximates the curve by two straight lines, line A with 0 slope and line B with non zero slope
- Difference between actual and real is less than 50mV
- Could refine to restrict to current ranges and get more lines but closer match to real curve

Figure 3.12 Approximating the diode forward characteristic with two straight lines: the piecewise-linear model. Pg 156 Sedra and Smith



Mathematically:

$$i_D = 0, \quad v_D \le V_{D0}$$
$$i_D = (v_D - V_{D0})/r_D, \quad v_D \ge V_{D0}$$

Where V_{D0} is the intercept of line B on V-axes and r_D is the inverse slope of line B

Diode Models Forward Bias

Piecewise-Linear Model

The models equivalent circuit is:

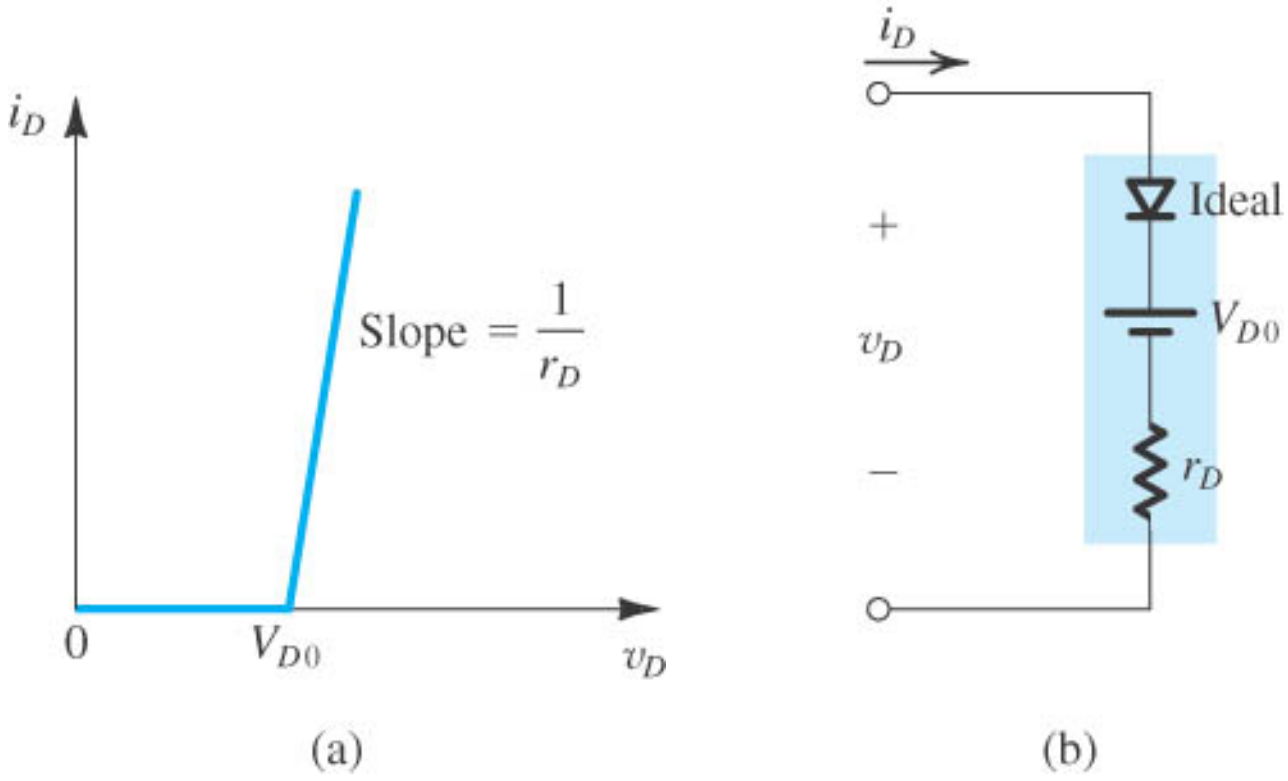
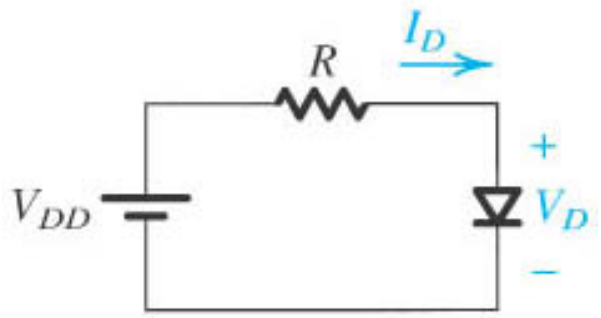


Figure 3.13 Piecewise-linear model of the diode forward characteristic and its equivalent circuit representation.
Pg 156 Sedra and Smith

Also known as battery-plus resistance model

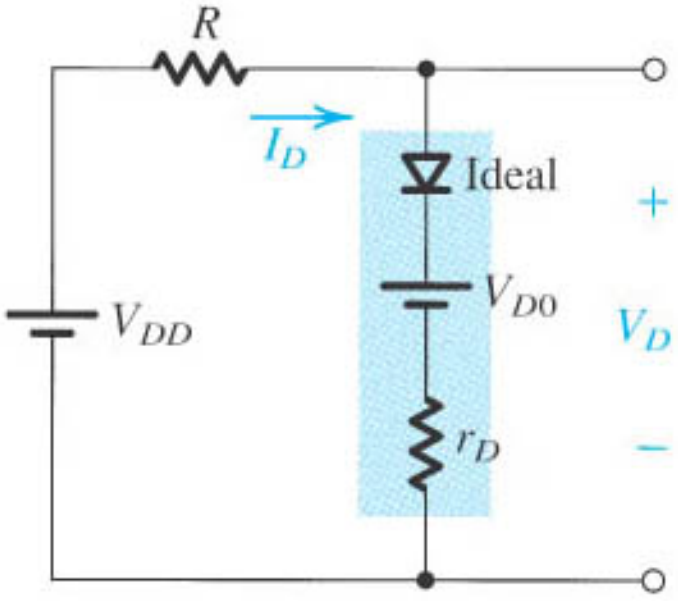
Diode Models Forward Bias

Piecewise-Linear Model



Using the same example as for the exponential model with parameters (from graph) of V_{D0}=0.65 V and r_D=20Ω we will re-solve using the Piecewise linear model:

The circuit becomes:



Then for I_D we have:

$$I_D = \frac{V_{DD} - V_{D0}}{R + r_D} = \frac{5 - 0.65}{1 + 0.02} = 4.26mA$$

The Diode voltage is then:

$$V_D = V_{D0} + I_D r_D = 0.65 + 4.26 \times 0.02 = 0.735 \quad V$$

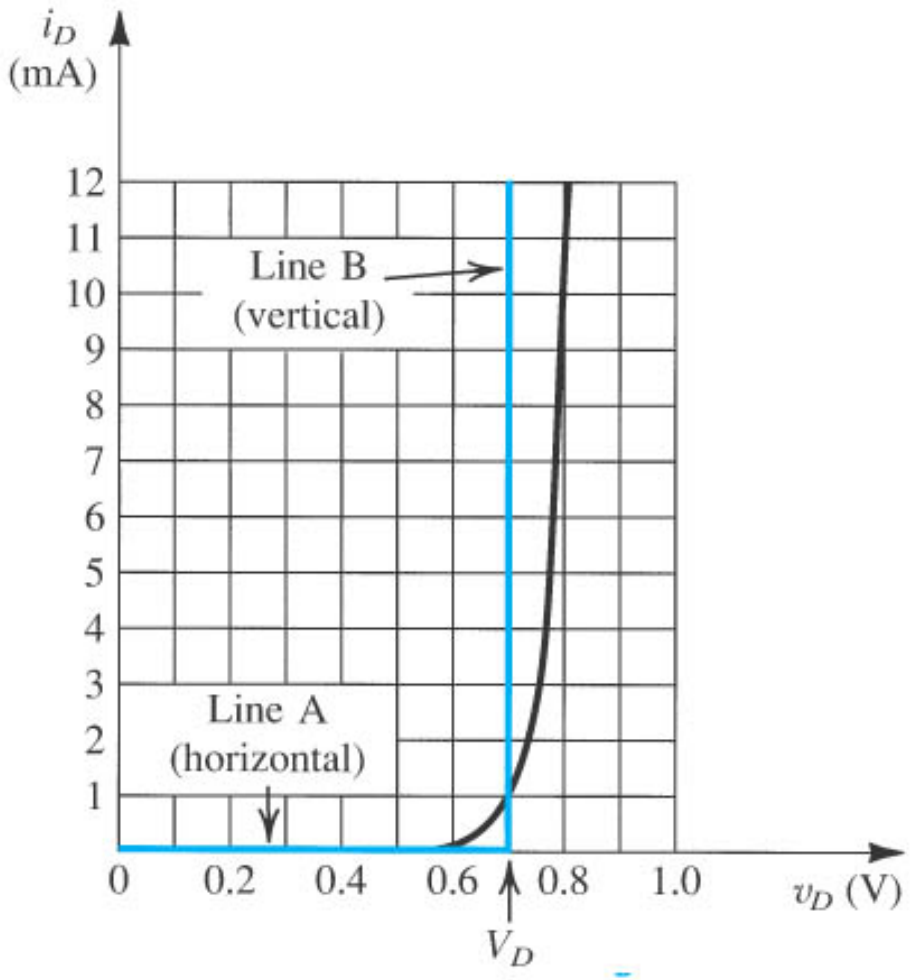
Compared to 4.237mA and 0.762V for exponential model

Diode Models Forward Bias

Constant Voltage Drop Model

- Simplest diode model
- Most often employed in quick calculations and at the initial phases of electronic design
- Uses a fixed forward bias diode drop of 0.7 V (usually) for silicon diodes
- The i-v curve for this model (compared to exponential) is:

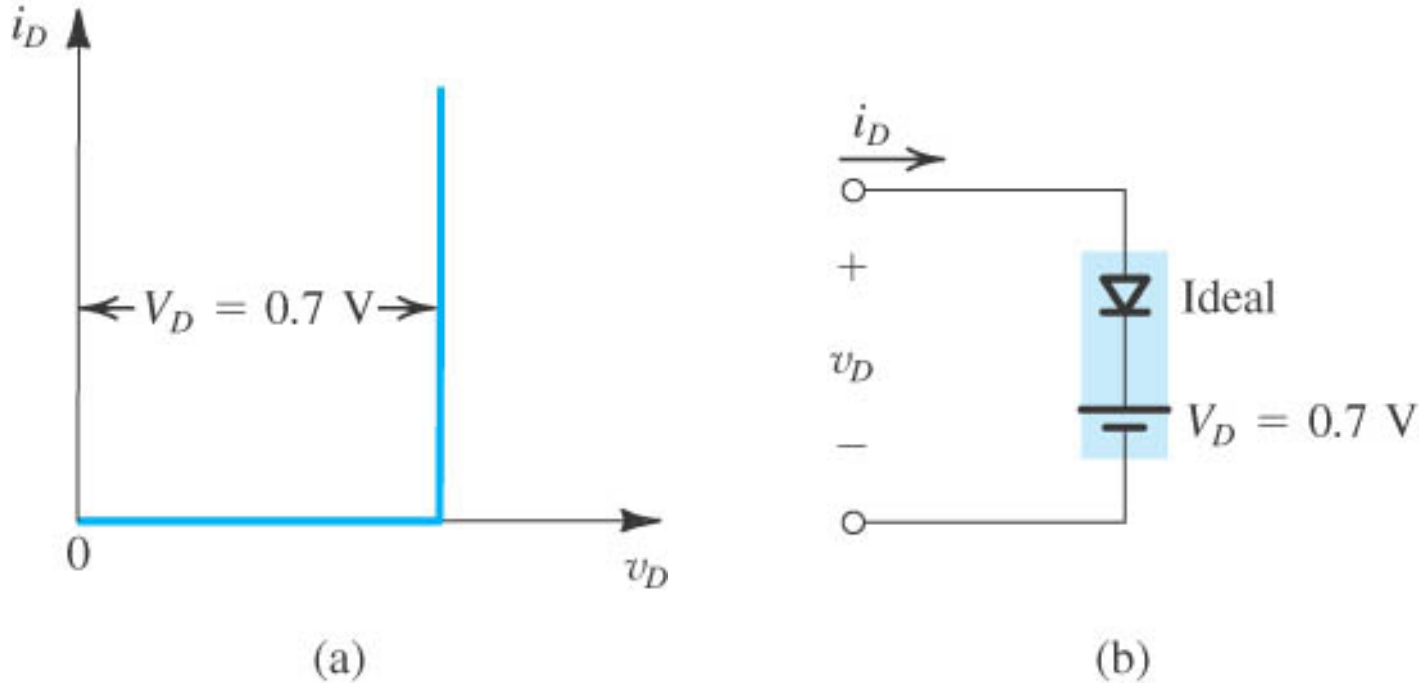
- It is clearly a form of the piecewise linear model where line B has infinite slope! (r_D=0Ω) And V_{D0}=0.7 V



Diode Models Forward Bias

Constant Voltage Drop Model

The equivalent circuit of this model is:



To solve our earlier problem here V_D=0.7 V and I_D is given by:

$$I_D = \frac{V_{DD} - V_D}{R} = \frac{5 - 0.7}{1} = 4.3 \quad mA$$

Compared to 4.237mA and 0.762V for exponential model

Diode Models Forward Bias

Ideal Diode Model

- Already seen this model
- Used as a gross estimate of circuit performance
- For little extra effort the assumption of a fixed 0.7 V gives more realistic results
- Ideal diode model most often used to decide which diodes are ‘on’ and which ‘off’ in a circuit topology

Break

Diode Models Forward Bias

Small Signal Diode Model

- Some circuit applications will require a diode to operate at a certain voltage and current and have a small signal superimposed on it
- In such circumstances we use one of the previous models (most likely the constant voltage model) to calculate the DC biasing point and then we need to calculate the effect of a small AC signal superimposed on the DC bias point
- To do this we can use the small signal diode model
- It is based on taking the slope of a tangent to the exponential curve at the calculated Q point (the DC bias point)

Diode Models Forward Bias

Small signal Approximation:

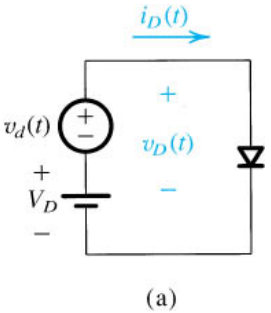
Small Signal Diode Model

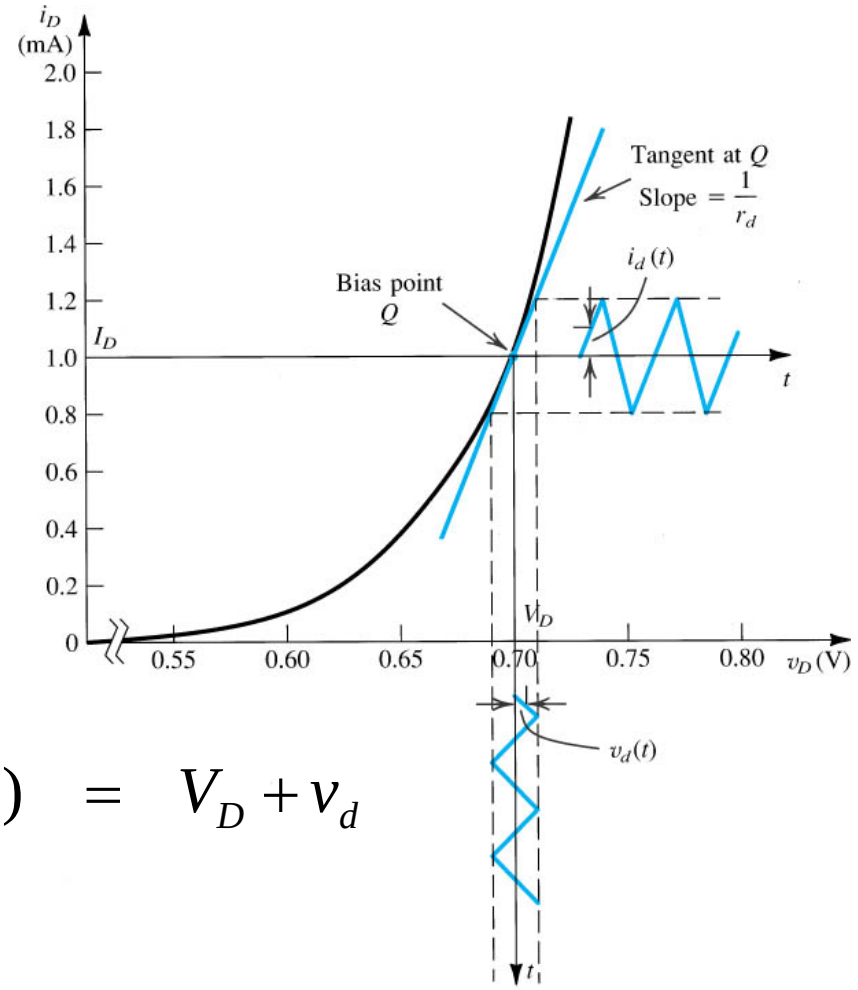
$$i_D(t) \cong I_D\left(1+\frac{v_d}{nV_T}\right) \longrightarrow i_D(t) = I_D + i_d \longrightarrow i_d = \frac{I_D}{nV_T}v_d$$

Provided: $\dfrac{v_d}{nV_T} << 1$

Where v_d and i_d are time dependent small signal variations as shown

Note: This approx. is valid for signals whose amplitudes at 20 °C (V_T=25mV) is 10mV if n=2
and 5mV if n=1





$$v_D(t) = V_D + v_d$$

Diode Models Forward Bias

Small Signal Diode Model

The relationship between small signal current, i_d, and small signal voltage, v_d, is:

$$\frac{i_d}{v_d} = \frac{I_D}{nV_T}$$

It has the dimensions of conductance, mhos ( ) ℧

It is called the **diode small-signal conductance**

The inverse of this parameter is the diode **small-signal resistance** or **incremental resistance**, r_d

Note: r_d is inversely proportional to bias (DC) current I_D

Diode Models Forward Bias

Small Signal Diode Model

Point to note:

Using the principle of superimposition, and provided the small signal Superimposed is small such that:

$$\frac{v_d}{nV_T} << 1$$

then we can calculate the DC bias point first then do the AC analysis by eliminating ALL DC sources by:

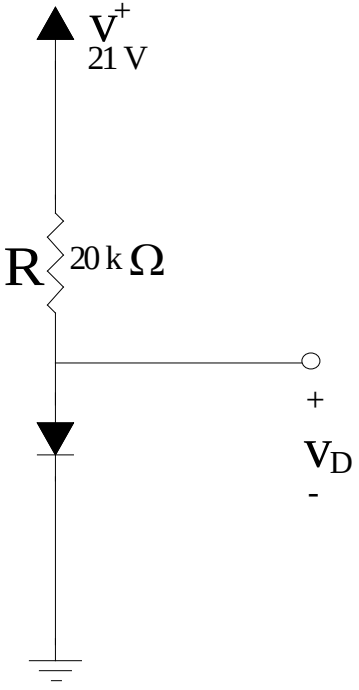
- Short circuiting DC voltage sources
- Open circuiting DC current sources

Then replace the diode with its small signal resistance

Diode Models Forward Bias

Small Signal Diode Model

Example: Consider the circuit shown



The V+ terminal is providing a 21 V DC supply with a superimposed sinusoidal **ripple voltage** with frequency 50Hz and peak amplitude of $2\sqrt{2}$ volts. Calculate the DC voltage of the diode and the amplitude of the sine wave appearing across it. Justify the use of the small signal model. Assume the diode has a 0.7 Volt drop at 1mA current and the value of 'n' is 2.

Diode Models Forward Bias

Small Signal Diode Model

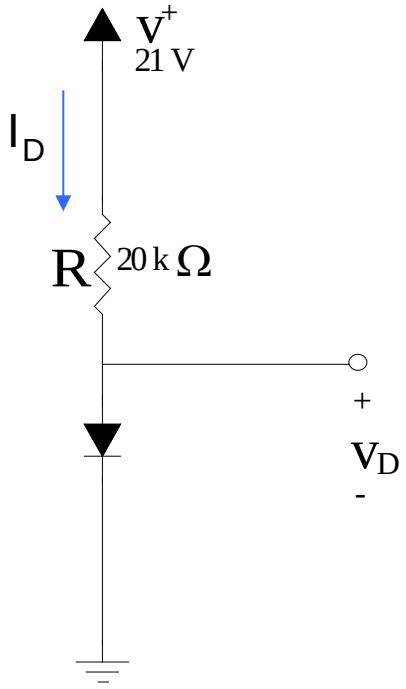
Example

DC calculation:

Assume $V_D \cong 0.7V$ and calculate the diode current (ie use constant voltage drop model):

$$I_D = \frac{V^+ - V_D}{R} = \frac{21 - 0.7}{20} = 1.015mA$$

as this is very close to 1mA we can be reasonably certain that the voltage drop will be 0.7V



Diode Models Forward Bias

Small Signal Diode Model

Example

Small Signal Model:

At the DC operating point we can calculate the diode incremental resistance, r_d:

$$r_d = \frac{nV_T}{I_D} = \frac{2 \times 25mV}{1.015mA} = 49.26\Omega$$

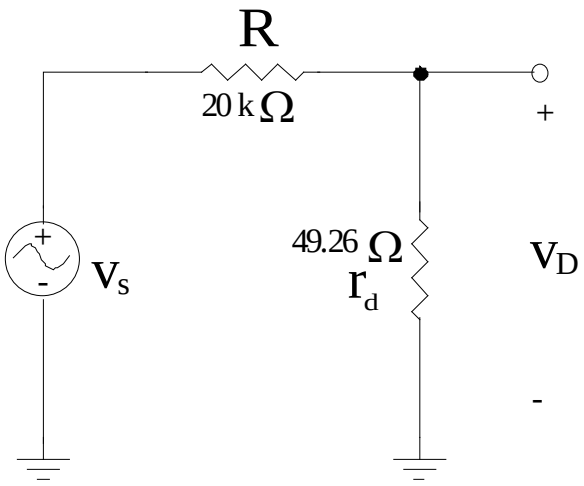
For this example n=2; normally we will assume n=1 unless told otherwise!

Diode Models Forward Bias

Small Signal Diode Model

Example

The small signal equivalent circuit with suppressed DC sources is then→



Using the voltage divider rule the peak amplitude v_d can be found as:

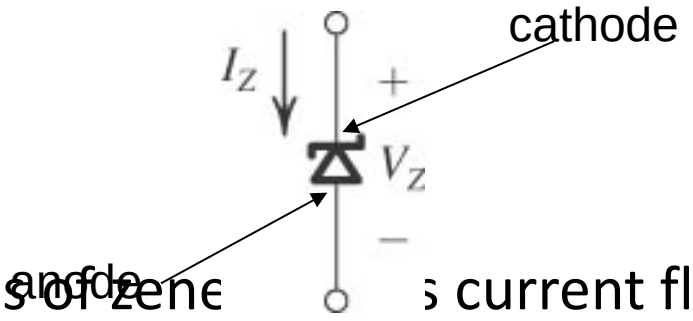
$$v_d(peak) = v_s \cdot \frac{r_d}{R + r_d}$$

$$= \sqrt{2} \cdot \frac{0.04926}{20 + 0.04926} = 3.475mV$$

Since this is quite small (since n=2 we use <10mV ;see slide 41) it satisfies the small signal criteria and justifies our use of the model!

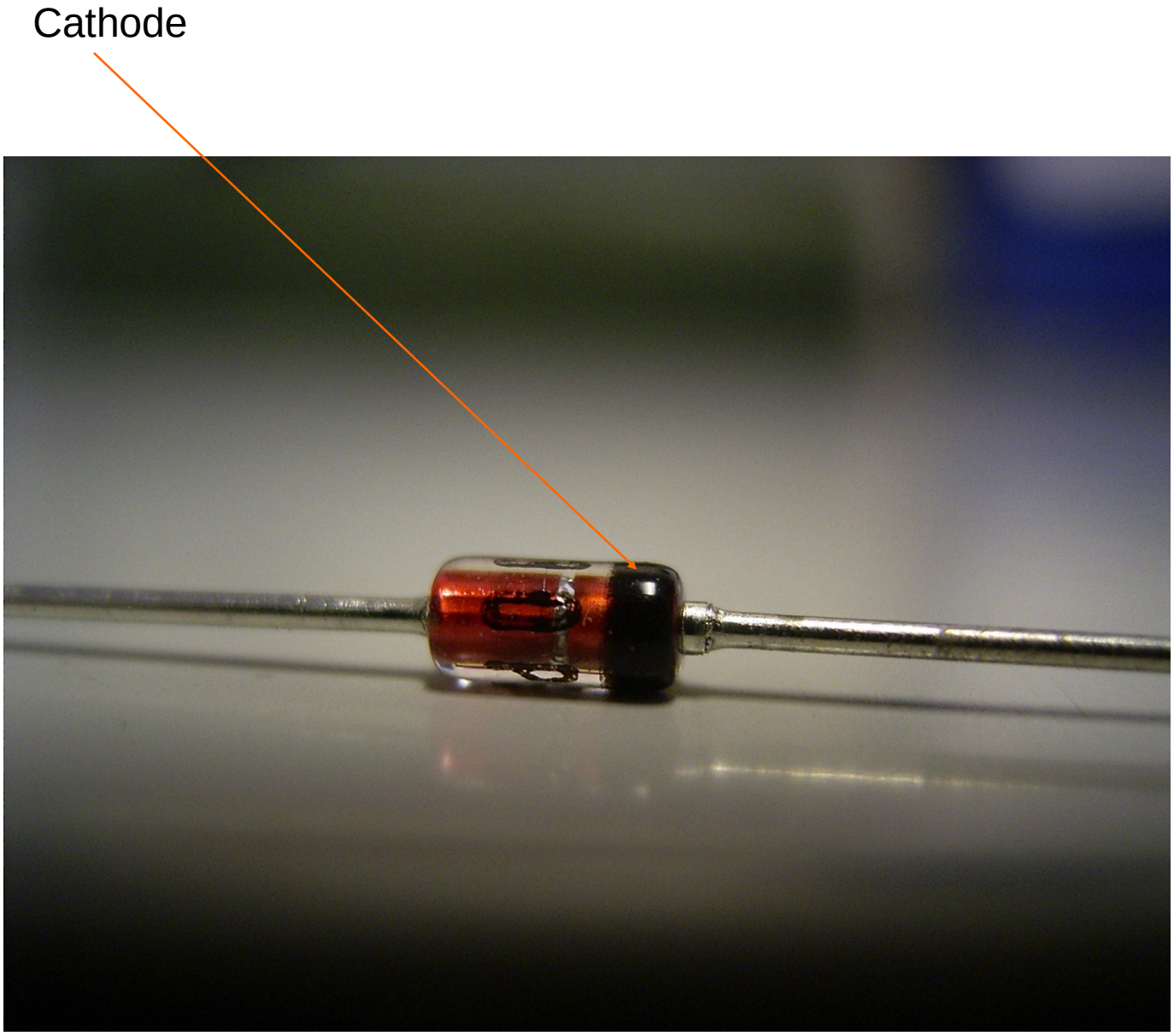
Zener Diodes

- Diodes designed to operate in the breakdown region
- Have application in voltage regulators but now these have special purpose devices that do this (not as important as they once were)
- Can also be called breakdown diodes
- The circuit diagram of a zener is:



- Normal applications of zene s current flows into the cathode, and the cathode is +ve with respect to the anode which means that I_z and V_z have +ve values in this diagram

Zener Diodes



Zener Diodes

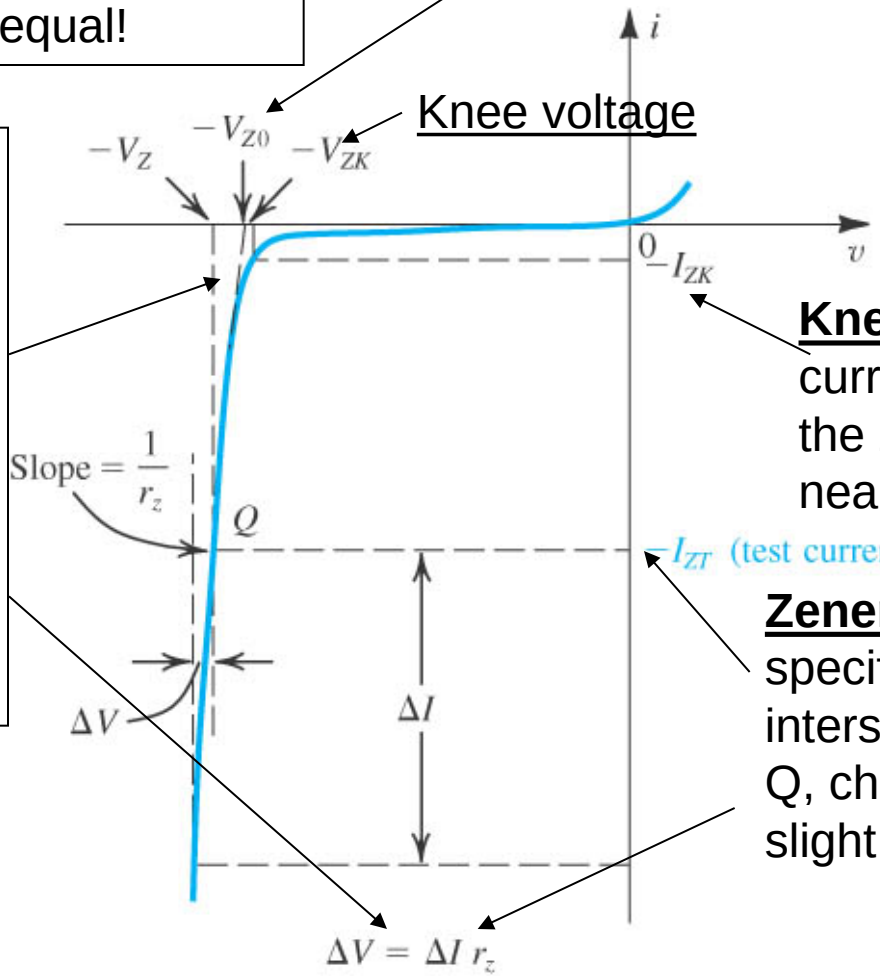
i-v characteristics of zener breakdown region:

Note that for V_{Z0} and V_{ZK} In practice their values Are almost equal!

Point at which the line with slope $1/r_z$ intersects the voltage axes

Knee voltage

Good idea to avoid Operation around Knee as here the Slope varies widely and hence the **Incremental** (dynamic) resistance r_z (this is also Specified in data sheets) will also vary widely



Knee current: for currents above this the zener current is nearly a straight line

Zener test current, specified in data sheet intersects with curve at Q, changes in i will cause slight changes in v

Zener Diodes
Model

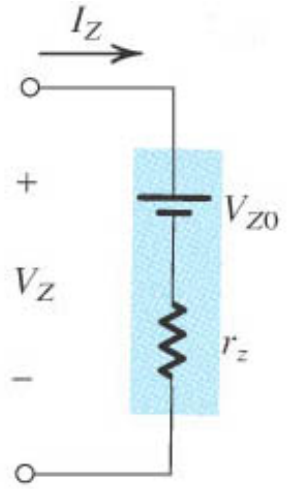
Using the values from the breakdown curve as labeled, the Zener Voltage , V_Z, can be given as:

$$V_Z = V_{Z0} + r_z I_z$$

which applies for $I_Z > I_{Zk}$ and $V_Z > V_{Z0}$ (the breakdown region where curve conducts nearly linearly); with r_z given by the inverse of the slope in the breakdown region at the operating point , Q and we know that:

$$\Delta V = r_z \Delta I$$

So the equivalent circuit model is:

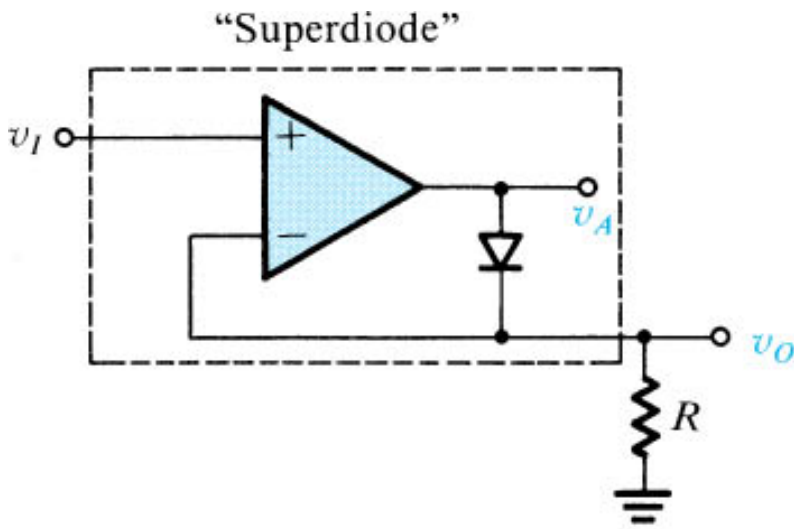


Special purpose Diode
Schottky Barrier Diode (SBD)

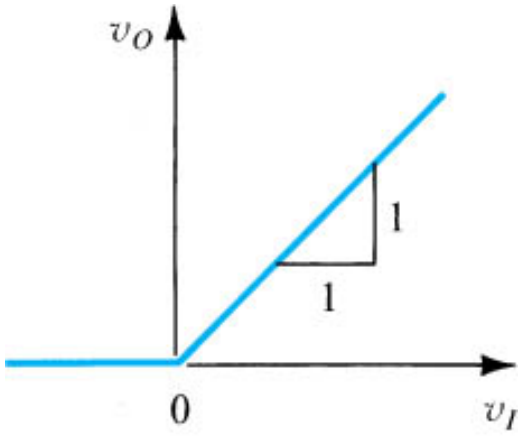
- Schottky Barrier Diode is formed by bringing metal into contact with a moderately doped n-type semiconductor material
- Also called hot carrier diodes
- Similar to Silicon Diode characteristic but
  - Current is conducted by electrons (major carriers) without a minority carrier charge storage effect at forward biased pn junction which means a faster on-off and off-on switching characteristic
  - Slightly higher currents flow when diode is reverse biased compared to silicon
  - Typically forward voltage drop of 0.3V to 0.5V are achieved compared to 0.6V to 0.8V of silicon
- Applications in design of GaAs circuits (very specialised) and in design of special purpose Bipolar transistor logic circuits called Schottky-TTL (transistor to transistor logic)

Super Diode

Consider this op-amp circuit and its output voltage vs input voltage transfer characteristic:



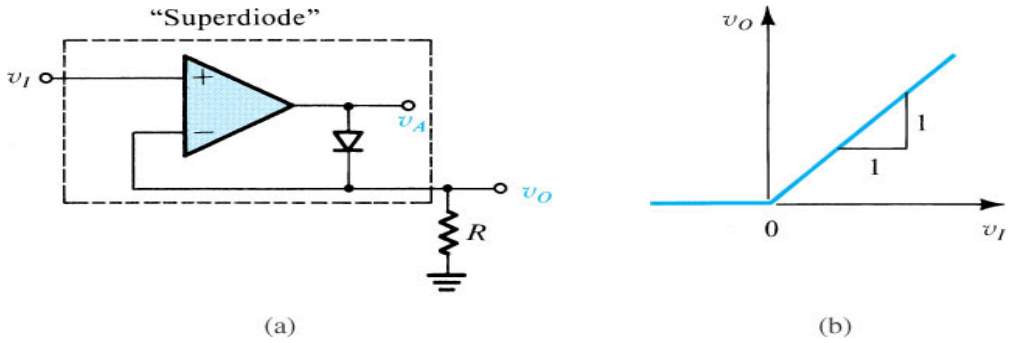
(a)



(b)

Super Diode

When the input voltage, v_i, is +ve then the output voltage v_A goes +ve and the diode will conduct



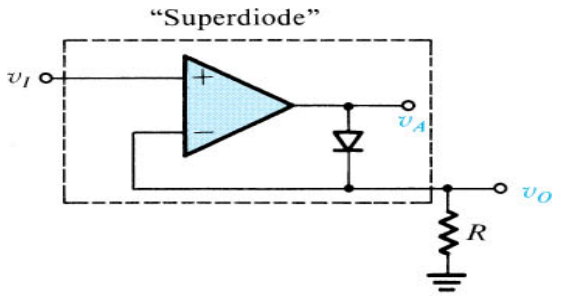
Which establishes a closed feedback path between the op-amps Output and its negative input, this results in a voltage follower type Situation with the virtual short occurring so the voltage at the Positive input will equal the voltage at the negative input ie

$$v_o = v_i \qquad v_i \geq 0$$

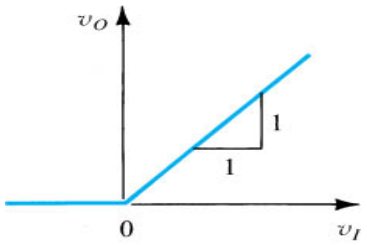
For this op-amp to start operation the input voltage needs to exceed 0.7/(open loop gain of Op-Amp,A) ➔as the op-amp gain is typically very large, this voltage will be very small!

Super Diode

<u>Example</u> if Open Loop Gain, A=100,000 then this voltage is 7μV



(a)



(b)

What about v_i negative?

When negative the diode will become reverse biased, ie it will open circuit. This will force the op-amp into open loop mode and the output v_a will swing to the negative voltage rail, as no current can pass through the op-amps –ve terminal or diode (in real devices insignificant currents) then no current flows through the load resistor R and the output v_o is also 0V's as shown ie:

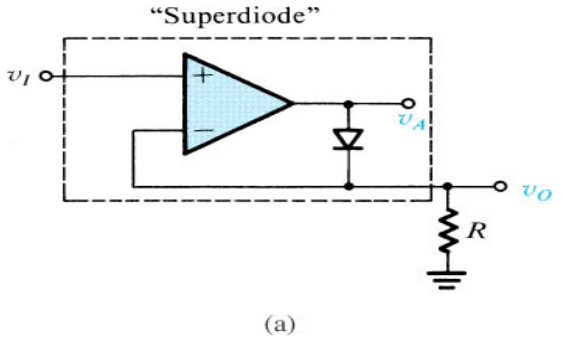
$$v_o = 0 \qquad v_i < 0$$

This circuit is suitable for low frequency and small voltages

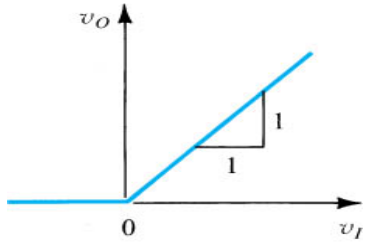
eg rectification of 100 mV sinusoidal/AC signal

Super Diode

see pg1208 Sedra and Smith



(a)



(b)

Disadvantages:

- When input voltage is negative and output voltage is zero all of the input voltage's magnitude appears across the two input terminals of the op-amp --- if this is greater than a few volts the op-amp will need **overvoltage protection** (most modern op-amps have this) or it could be damaged
- When the input voltage is negative the op-amp will be saturated and to return to the op-amps linear operation will take time (hence the low frequency requirement)

An improved circuit is possible!

Super Diode with 2 Diodes!

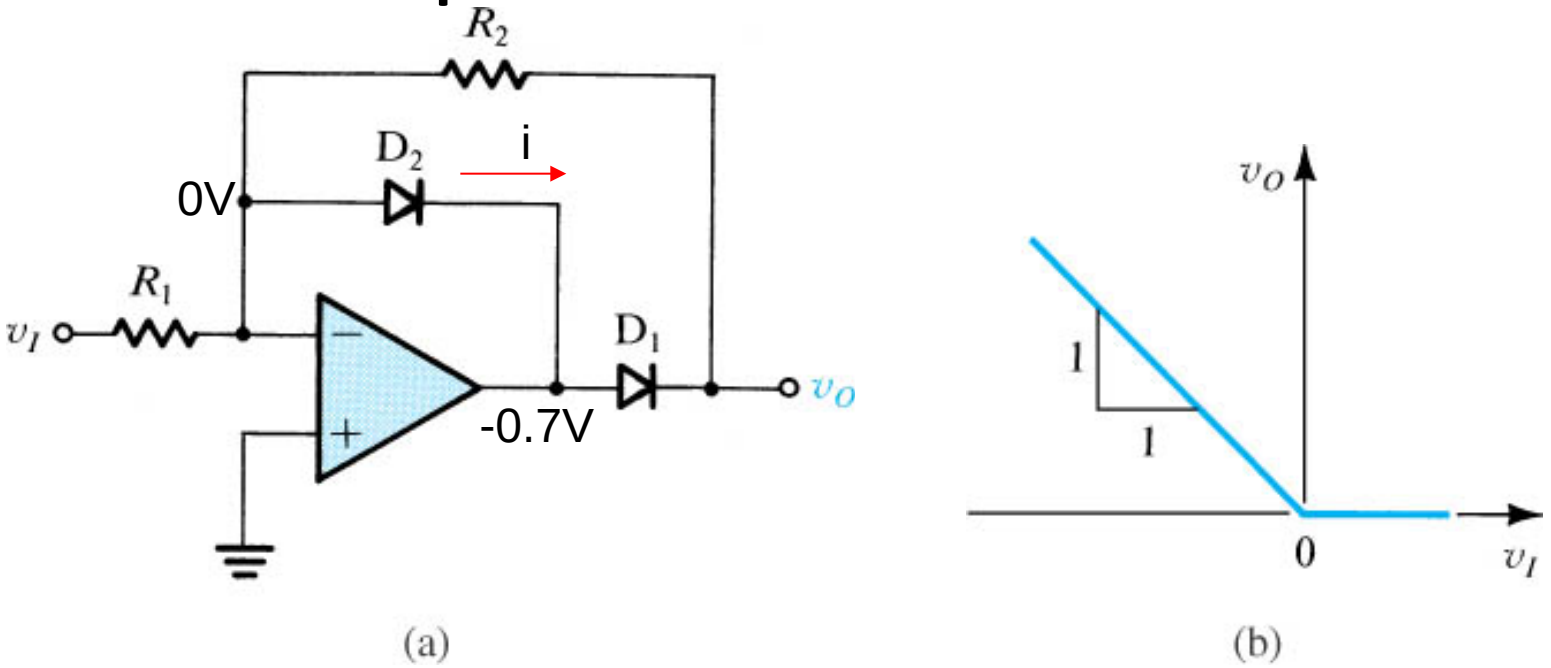


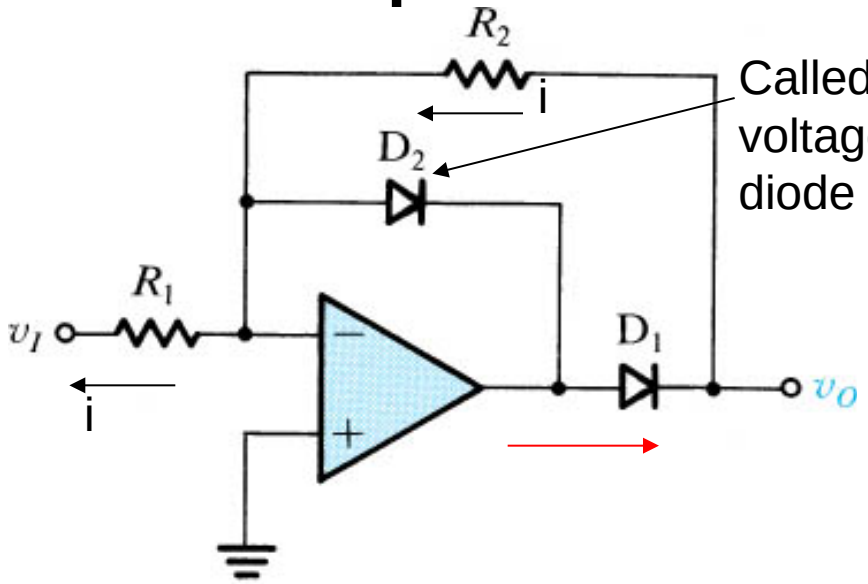
Figure 13.34 **(a)** An improved version of the precision half-wave rectifier: Diode D_2 is included to keep the feedback loop closed around the op amp during the off times of the rectifier diode D_1, thus preventing the op amp from saturating. **(b)** The transfer characteristic for $R_2 = R_1$.
pp.1208 Sedra and Smith

This circuit does not suffer from the problems of the original circuit – delay and need for over-voltage protection

Operation:

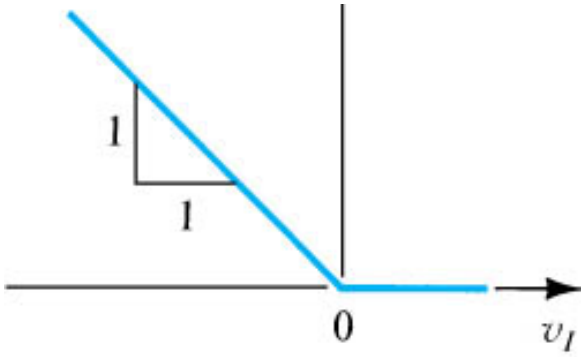
- D_2 , for *positive input* voltage, closes the –ve feedback loop around the op-amp resulting in a virtual ground appearing across the inverting input and the op-amp output is clamped at one diode forward bias voltage drop below ground; this means that D_1 is reverse biased and thus no current flows through R_2 (since there is no current return path) so then v_o is zero!

Super Diode with 2 Diodes!



(a)

Called Catching diode: since it "catches" the op-amp voltage as it goes negative and clamps it to a diode drop below ground!

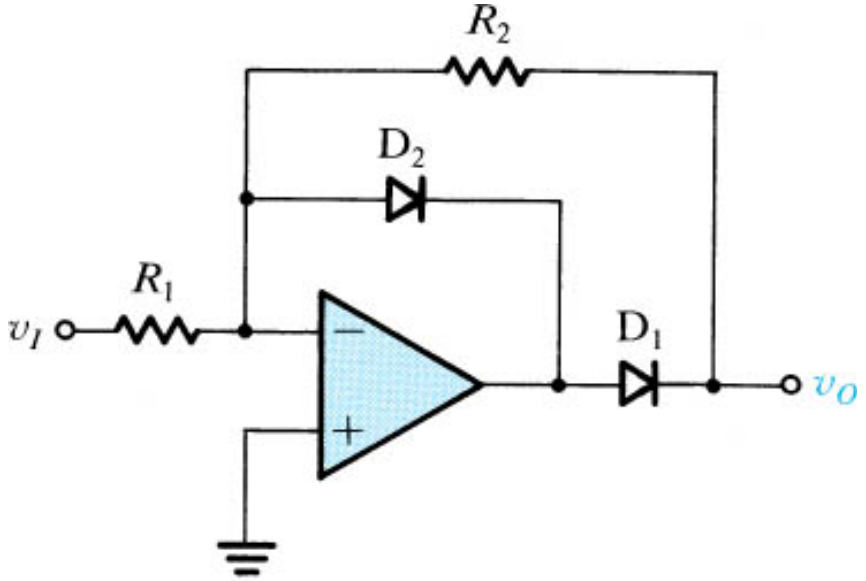


(b)

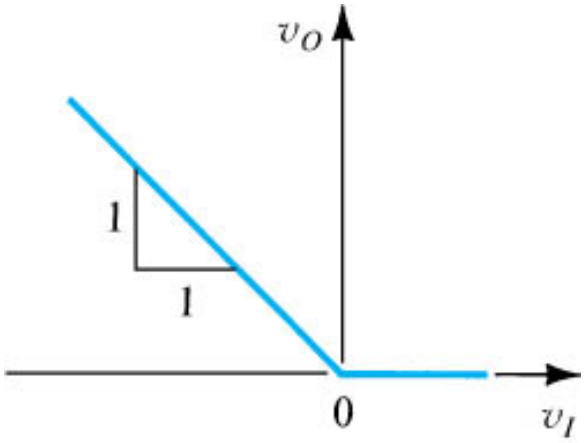
Operation:

- D_2 , for *negative input* voltage, is reverse biased as the the –ve input will now tend to go negative, with the output voltage going positive BUT now D_1 will be able to conduct (and will since its forward biased) via R_2 which results in a closed negative feedback path around the op-amp ; forcing a virtual ground to appear at the –ve input – as no current passes into the op-amp (ideal) or very little (real) - then all the current passes through R_1 and R_2 and this current is equal

Super Diode with 2 Diodes!



(a)



(b)

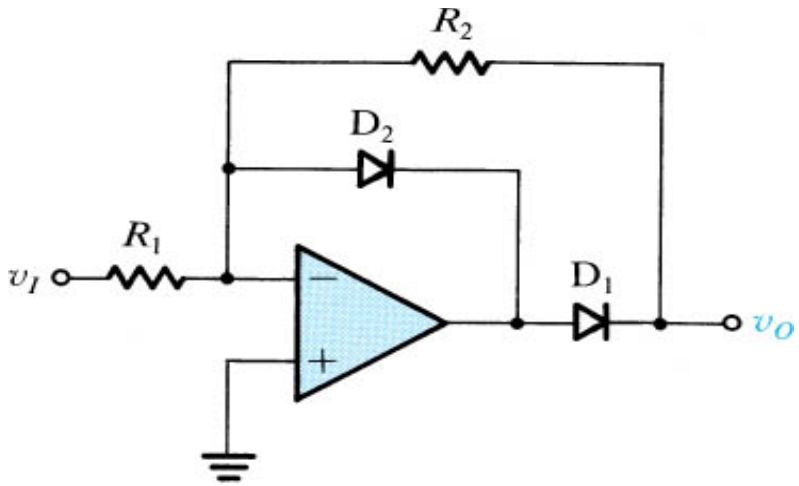
- The output voltage is then given by:

$$v_o = -\frac{R_2}{R_1} v_i \quad for \quad v_i \leq 0$$

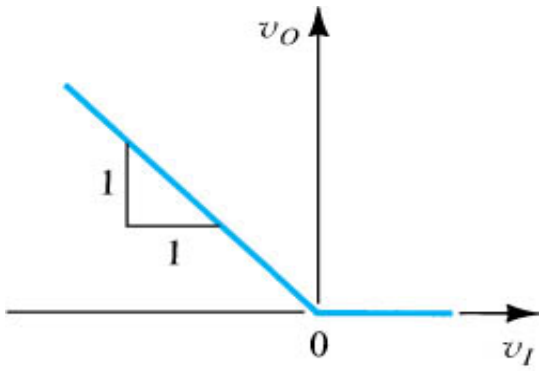
- If R_1=R_2 the output voltage will be:

$$v_o = -v_i \quad for \quad v_i \leq 0$$

Super Diode with 2 Diodes!



(a)



(b)

<u>Advantages</u>:

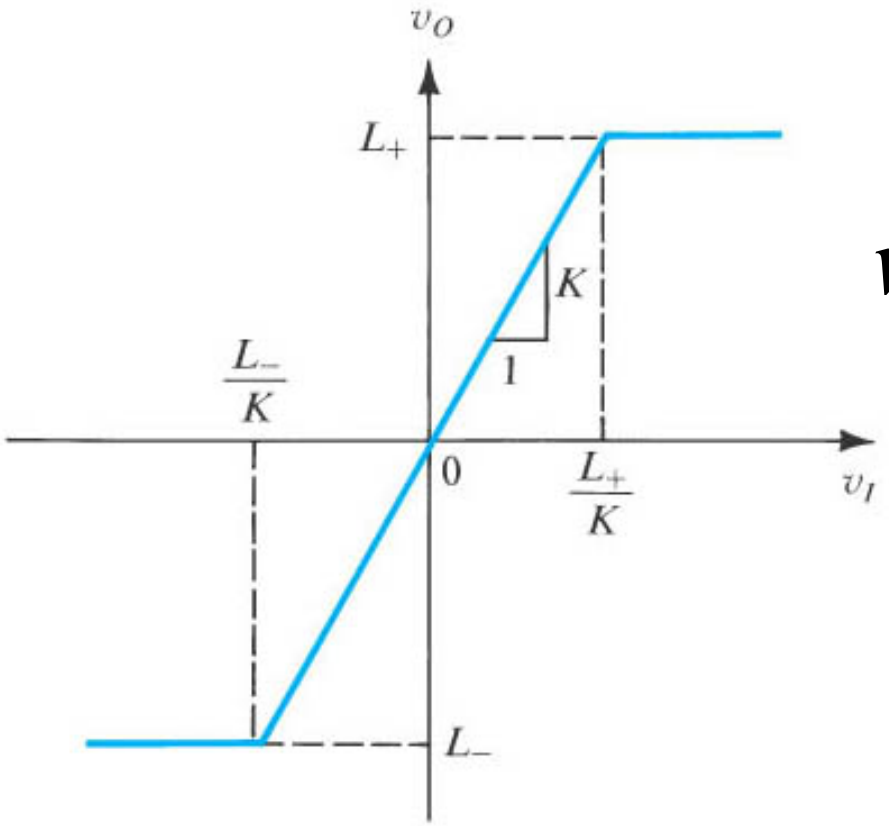
- feedback loop remains closed at all times and thus the op-amp remains in its linear region avoiding the possibility of saturation and the associated time delay to get out of saturation.
- It also now can be used without worrying too much about over-voltage protection required for the original super-diode (we have a virtual ground in operation)

Limiting and Clamping Circuits

Limiting Circuits

Diodes can be used in a limiting circuit

A generic transfer function for a limiting circuit is:



$$v_o = Kv_i$$

Circuits we will look at have $K \leq 1$ And are known as passive limiters

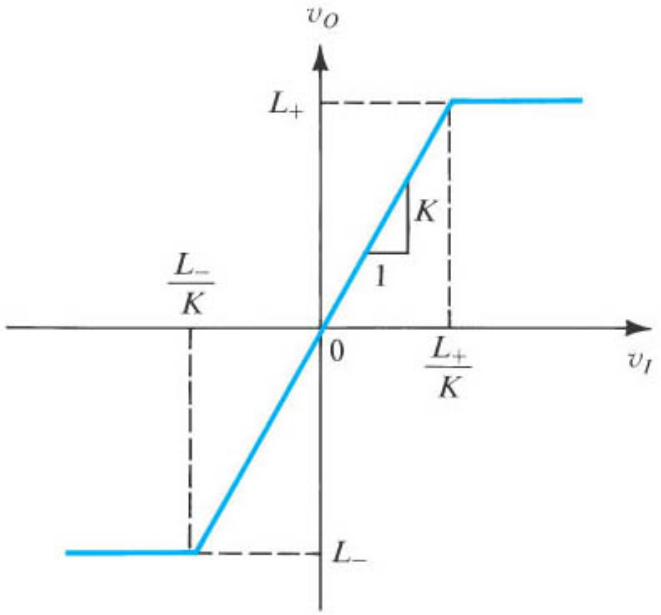
Figure 3.32 General transfer characteristic for a limiter circuit.pp. 185 Sedra & Smith

Limiting and Clamping Circuits

Limiting Circuits

The transfer function depicted in Fig 3.32 describes a **double limiter** – where both positive and negative peaks are limited

A **single limiter** only work on one side of the peaks (either negative or positive but not both)



$$v_o = Kv_i$$

Figure 3.32 General transfer characteristic for a limiter circuit.pp. 185 Sedra & Smith

Limiting and Clamping Circuits

Limiting Circuits

Fig 3.33 shows the effect on a sinusoidal waveform passed into a double limiter – the peaks have been clipped (a non-linear function) and hence sometimes these circuits are called **clippers**

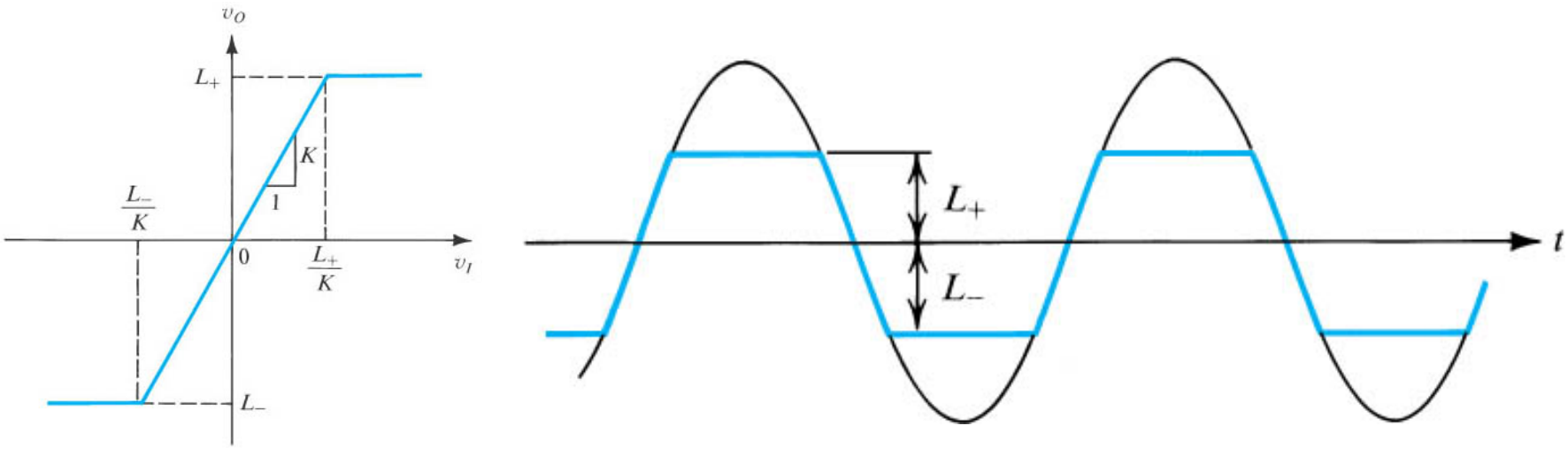
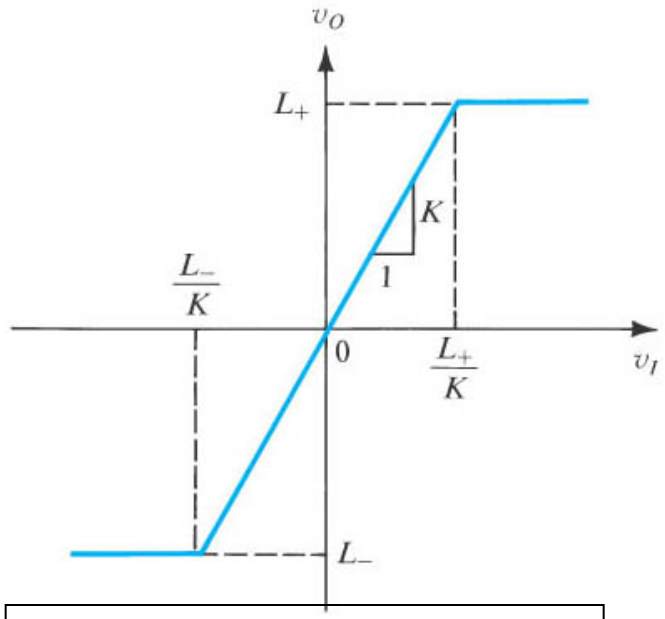


Figure 3.33 Applying a sine wave to a limiter can result in clipping off its two peaks.

Limiting and Clamping Circuits

Limiting Circuits



Hard Limiter characteristic

Smoother transition
between linear and saturated region

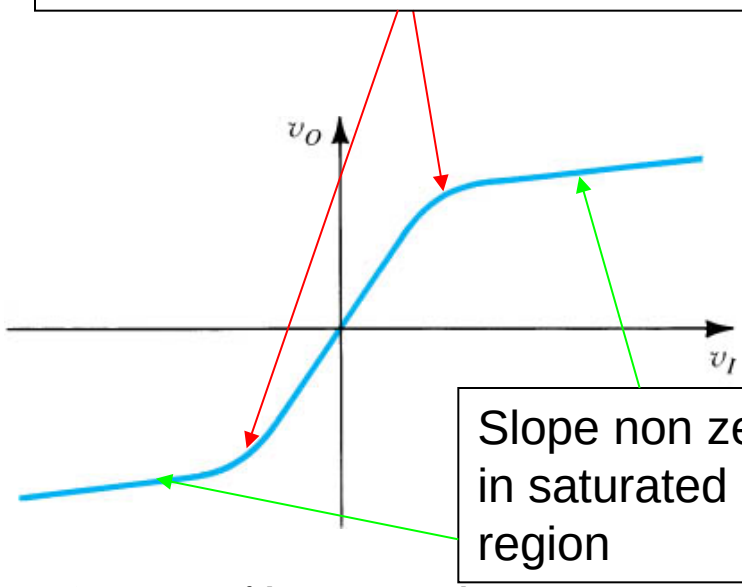


Figure 3.34 Soft limiting.S&Smith pg185

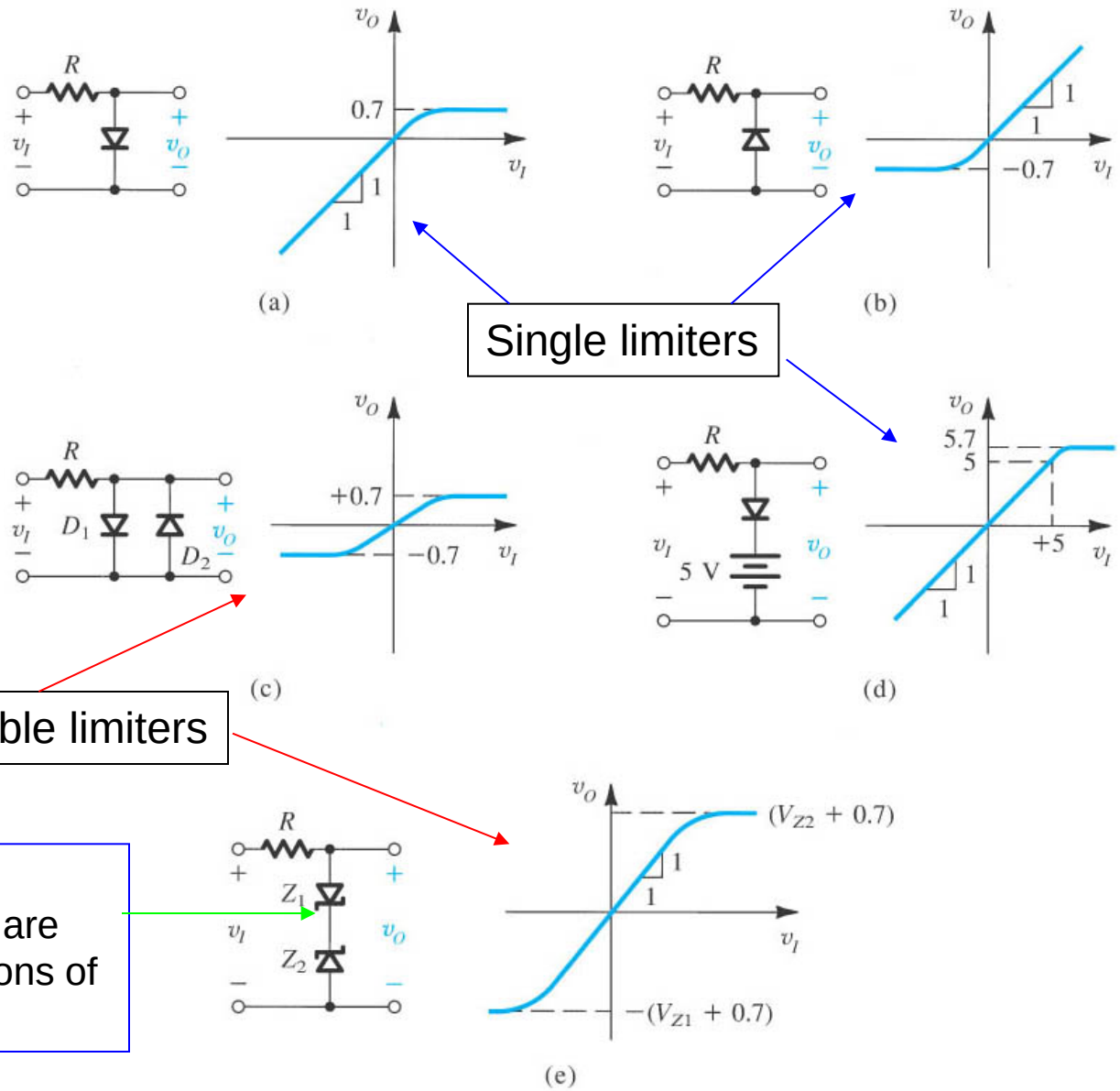
Soft Limiter characteristic

Limiters find applications in signal processing applications such as a situation where Voltages can damage electronic components if exceeded: an example is used in The schools DSP C3x boxes where a circuit using diodes ensures students can't Exceed the specified limits of 0 to 5V DC – a fuse is used to limit current.

Limiting and Clamping Circuits

Limiting Circuits

(Modeling diodes using the constant 0.7V diode model) some examples of limiting circuits are:



Single limiters

Double limiters

Figure 3.35 A variety of basic limiting circuits.
Pg. 186 S&Smith

Special pairs of zener diodes called **double-anode zener** diodes are Available commercially for applications of This type

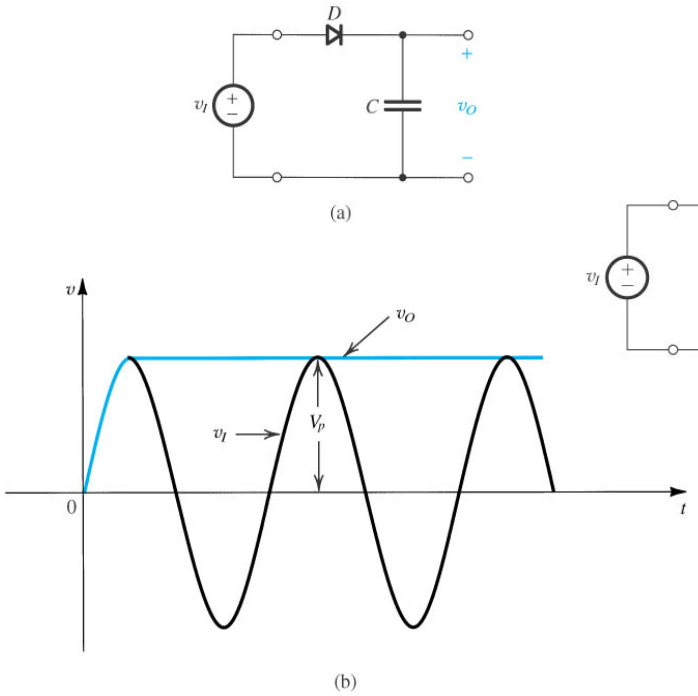
Limiting and Clamping Circuits

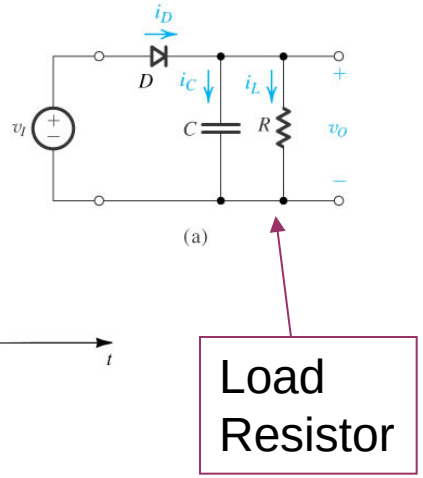
The Clamped Capacitor or DC Restorer

A circuit (covered in detail in on pg 177-182) is the peak detector (or peak rectifier):

Ripple voltage

$$V_r = \frac{V_p}{fCR}$$





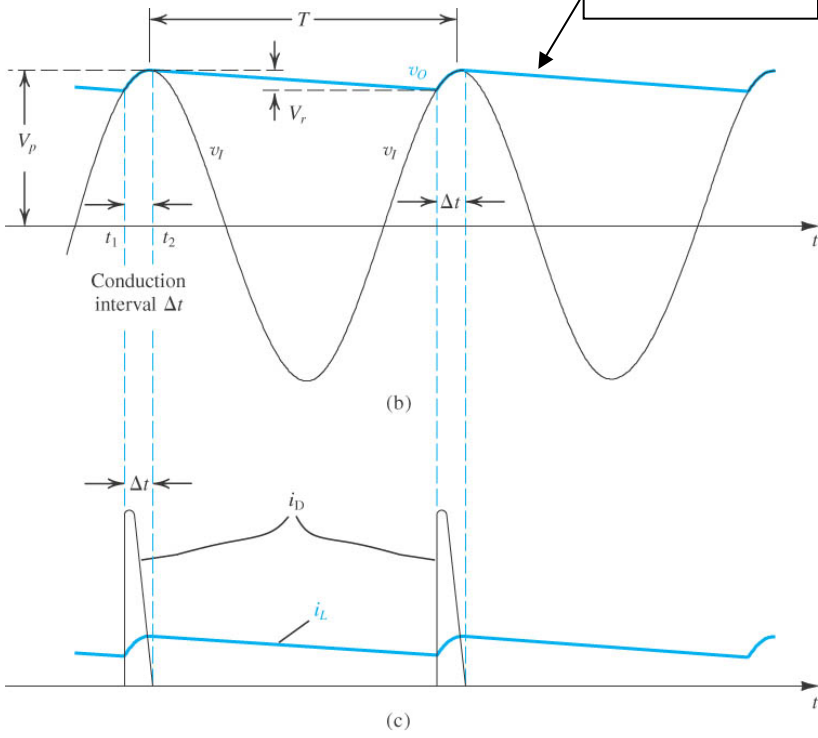


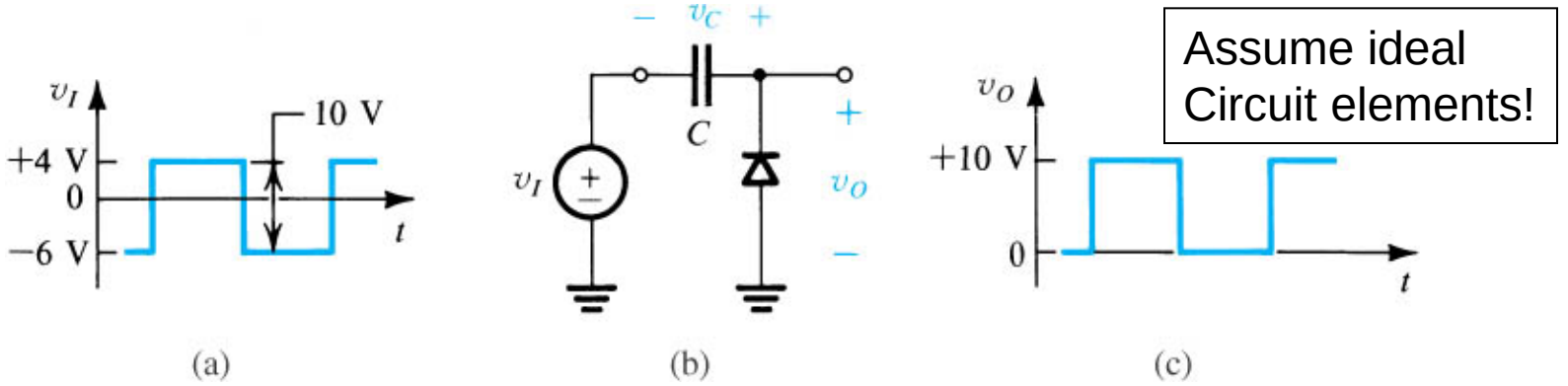
Figure 3.28 **(a)** A simple circuit used to illustrate the effect of a filter capacitor. **(b)** Input and output waveforms assuming an ideal diode. Note that the circuit provides a dc voltage equal to the peak of the input sine wave. The circuit is therefore known as a peak rectifier or a peak detector.

Figure 3.29 Voltage and current waveforms in the peak rectifier circuit with CR @ T. The diode is assumed ideal.

Limiting and Clamping Circuits

The Clamped Capacitor or DC Restorer

Now if we take the peak detector circuit and look at the voltage across the diode instead of the capacitor we have a DC restorer:



Assume ideal Circuit elements!

Figure 3.36 The clamped capacitor or dc restorer with a square-wave input and no load. Pg. 188 S&Smith

Due to the polarity connection of the diode the capacitor in fig. (b) will charge to A voltage v_c with the polarity shown on the diagram (output pin positive) This voltage will have the magnitude of the <u>most negative peak</u> of the input Waveform – eventually the diode turns off and the capacitor retains the charge Indefinitely.

<u>Example</u>: in fig.(a) the most negative voltage of the square wave input is -6V, while The voltage range is 10V, then v_c will charge to 6V; the output voltage (using KVL) Is then the input voltage (v_i) plus the capacitor voltage (v_c) which gives the waveform At the output indicated by fig.(c) – the output has been shifted by v_c volts compared To the input waveform

Limiting and Clamping Circuits

The Clamped Capacitor or DC Restorer

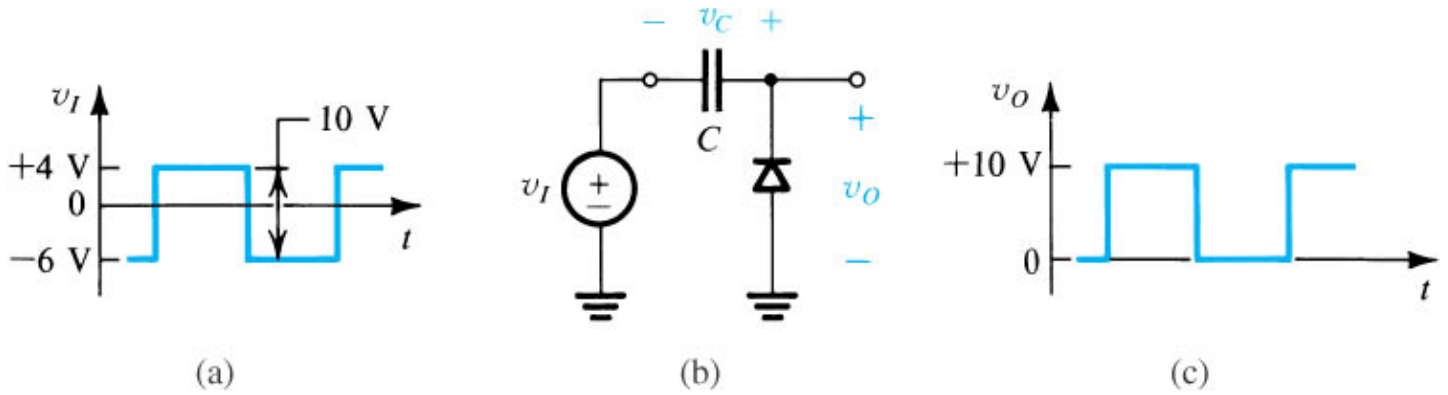


Figure 3.36 The clamped capacitor or dc restorer with a square-wave input and no load. Pg. 188 S&Smith

- The diode (with shown polarity) prevents the output voltage from going below 0 V (ground) – done by conducting and charging up the capacitor –however the diode does not constrain the positive swing of v_o hence the circuit has the effect of *clamping the lowest peak* to 0V hence its alternate name the clamped capacitor!
- If we reverse the polarity then the highest peak will be clamped to 0V
- If we pass a pulse or AC signal with a DC component through a capacitor coupling (or ac coupled system) then that signal will lose its DC component – we can use this circuit to restore a known DC component; a process known as *DC restoration*→hence the other name DC restorer

Limiting and Clamping Circuits

The Clamped Capacitor or DC Restorer

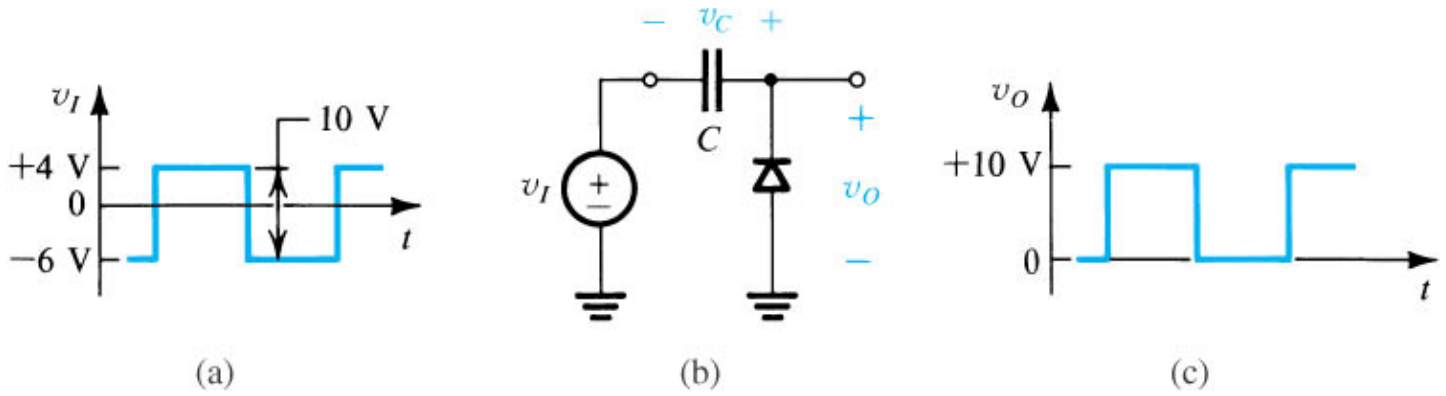


Figure 3.36 The clamped capacitor or dc restorer with a square-wave input and no load. Pg. 188 S&Smith

Application?

- DC component or average value of a pulse waveform is a measure of duty cycle (which is the proportion of each cycle occupied by the pulse)
- Duty cycle can be modulated (with information) in a process called Pulse Width Modulation (PWM) ie pulse width is changed to convey different signal (data) conditions eg speed control using H-bridge (special IC packages available –used in SoccerBot u/g thesis project 2004-6) for a small DC permanent magnet motor
- The DC Restorer followed by a Single Time Constant (RC) low pass filter could be used to find the average value of the pulse train (or superimposed pulses)

Limiting and Clamping Circuits

If we now connect a load resistance , R, shunted across the diode the situation is different (alternatively, we could have used an op-amp voltage follower so its not loaded):

Diode conducts heavily and Capacitor charges

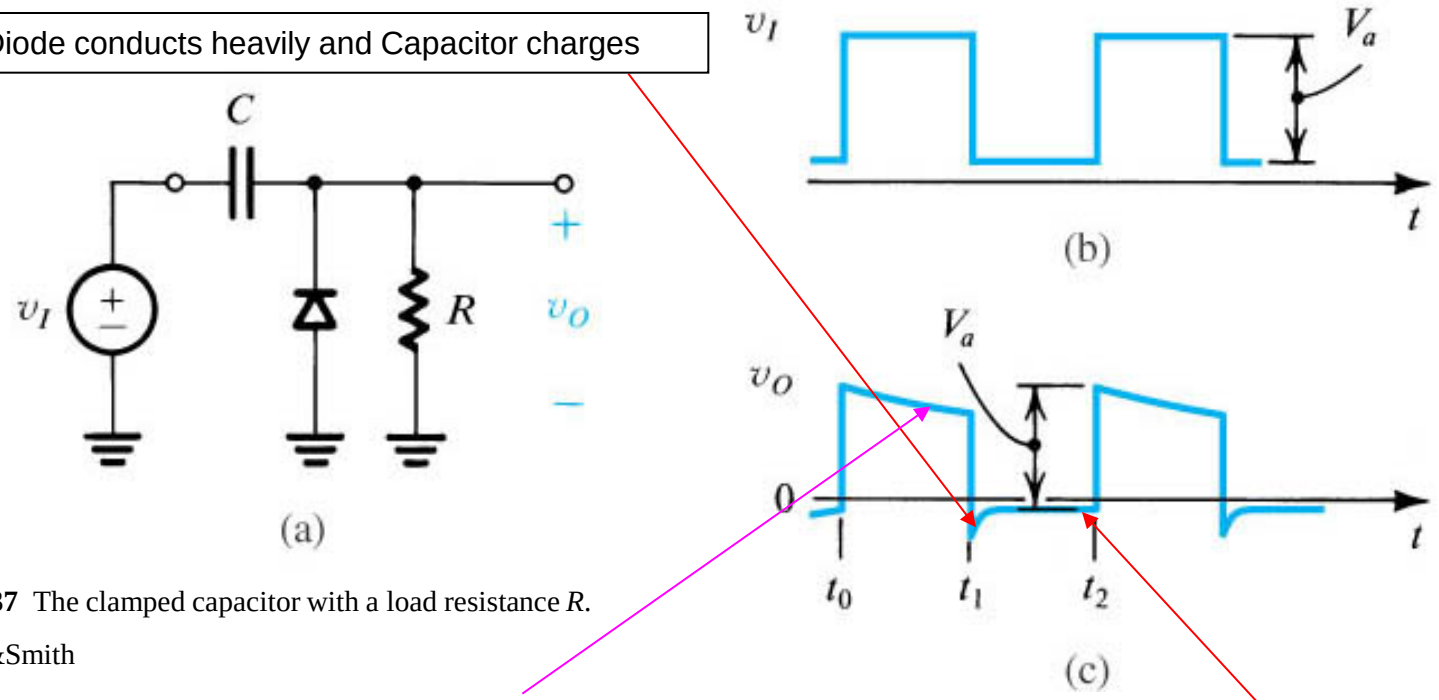


Figure 3.37 The clamped capacitor with a load resistance *R*.

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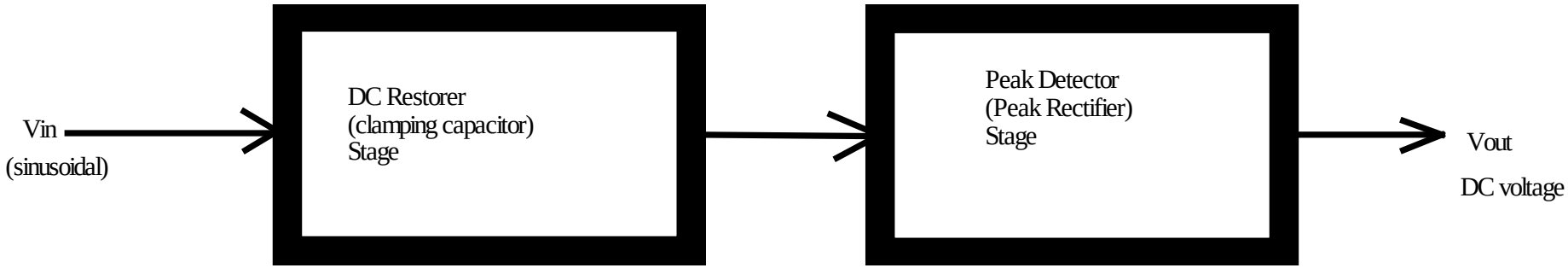
The capacitor can now be discharged through R, through t_0 to t_1 the capacitor discharges exponentially with time constant CR but during t_1 to t_2 the capacitor recovers its lost charge as the input voltage rises by V_a volts (diode conducts)

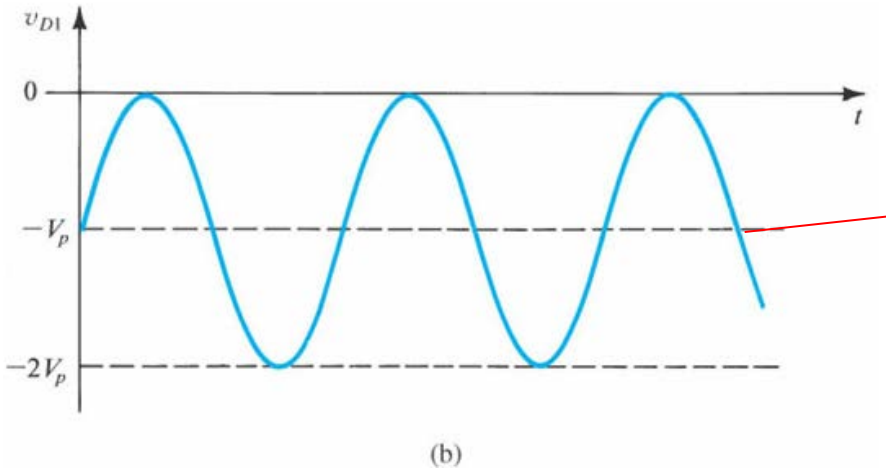
Just before t_2 the output voltage is typically A few tenths of a volt negative say -0.5 V

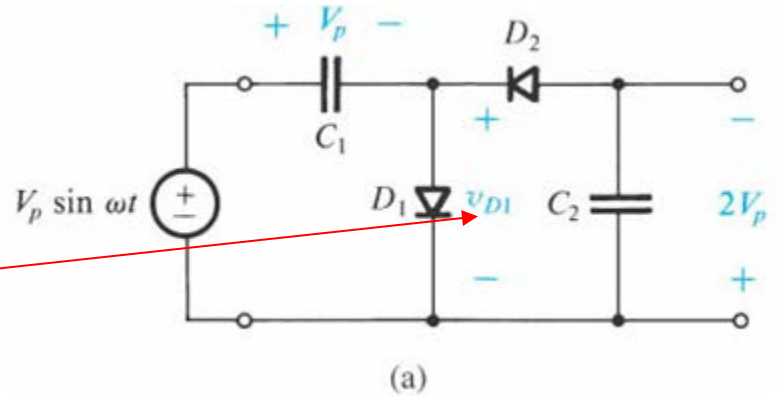
We can use the charge equilibrium to Calculate the average diode current And the detail of the output voltage

The Voltage Doubler

If we have a clamped capacitor (DC restorer) stage followed (cascaded) by a peak detector (peak rectifier) stage we can provide a DC output voltage that is twice the input voltages peak value:







The Diode Ring Modulator

For the Lab in weeks 8-13 as alternative!

- We can use diodes to do rectification (half-wave and full wave) and also to produce a Balanced modulator
- We will now briefly look at the Balanced modulator called a diode ring modulator (can get CA3039 IC for this purpose)

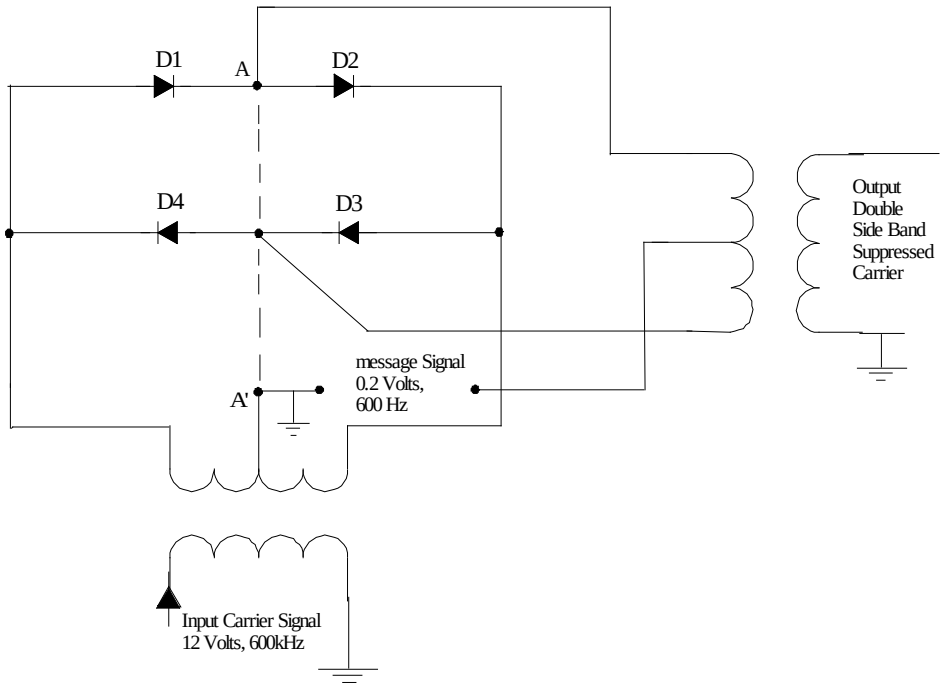
The Diode Ring Modulator

For the Lab in weeks 8-13 as alternative!

- The diode ring circuit for a Balanced Modulator capable of providing Double Side Band Suppressed Carrier (or signal multiplication) is:

When message Signal is zero, Output Is zero (balanced) ie A and A' have the same voltage value (here 0)

When message is non zero then provided Diode forward biases are not Exceeded by amplitude of message signal the points A and A' are unbalanced and DSB-SC results With D1 and D2 conducting on one cycle and D4 and D3 on opposite Cycle – being modulated in unbalance by the message signal!



Mathematically:

$$A_c \cos(\omega_c t) \times A_m \cos(\omega_m t) = \frac{A_c A_m}{2} \cos((\omega_c - \omega_m)t) + \frac{A_c A_m}{2} \cos((\omega_c + \omega_m)t)$$

EWB Simulation – Available on WebCT