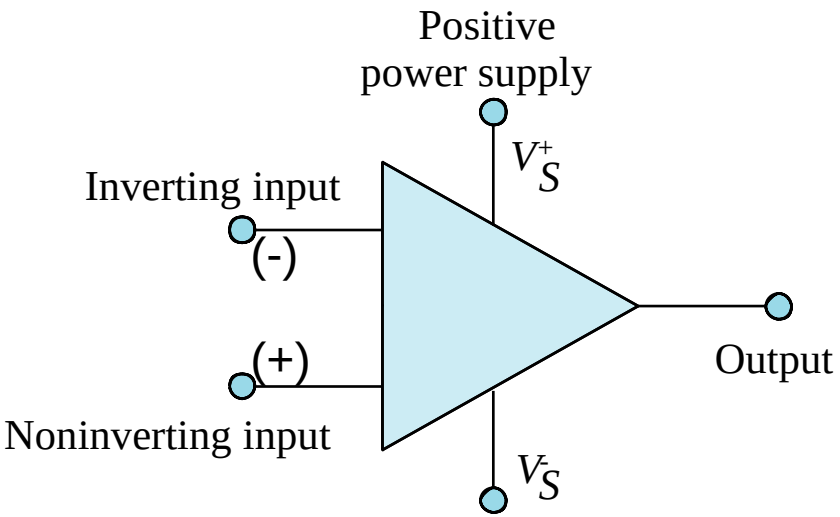
The Operational Amplifier



Simplified circuit symbol

$$V_S^- < V_{out} < V_S^+$$

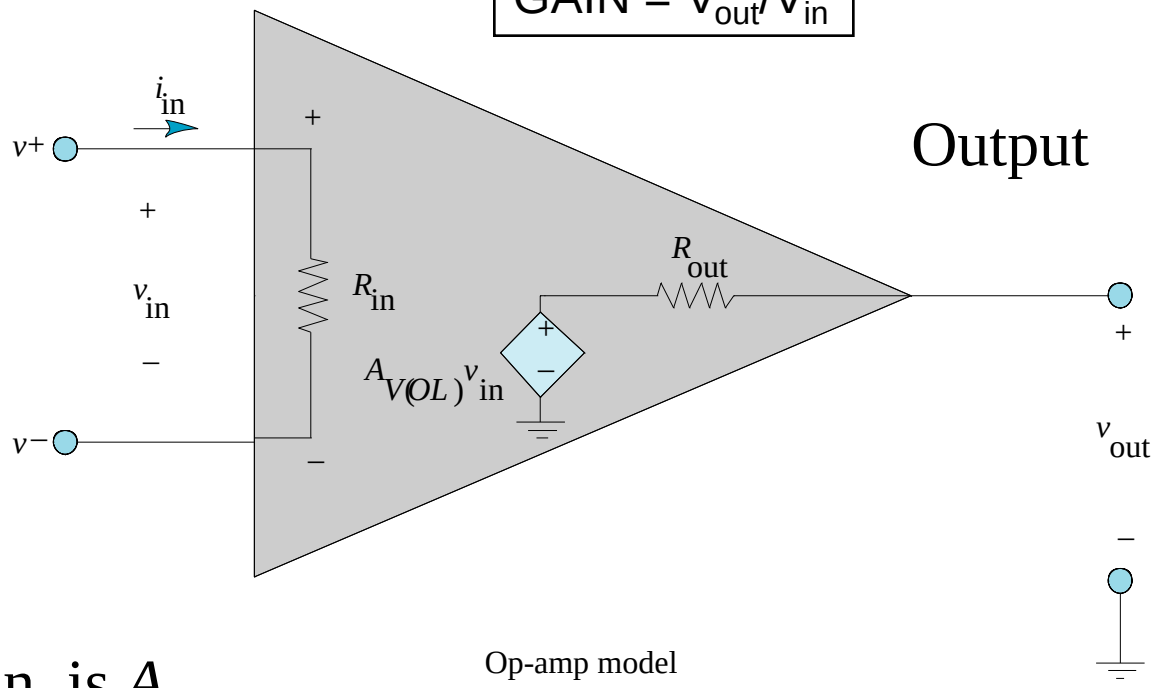
Example: $+V_S$ is +15 volts,
$-V_S$ is -15 volts
Then V_{out} is somewhere
Between the power
Supply extremes!

The Operational Amplifier

GAIN = V_{out}/V_{in}

Noninverting input

Inverting input



Op-amp model

The Open Loop Gain is $A_{V(OL)}$

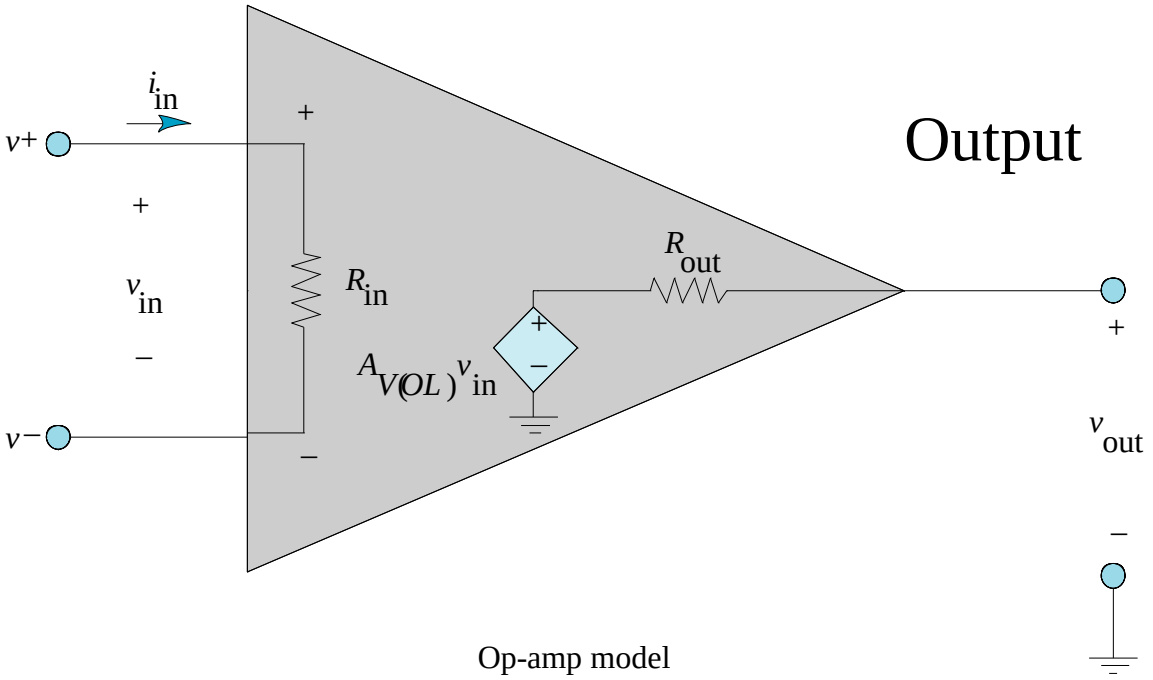
For an IDEAL operational amplifier we have $A_{V(OL)} = \infty$

For a practical operational amplifier we have finite but large (typically 100000) value for the open loop gain, $A_{V(OL)}$

The Operational Amplifier

Noninverting input

Inverting input



Op-amp model

We have a differential input Voltage, v_{in}, *given by:* $v_{in} = v^+ - v^-$

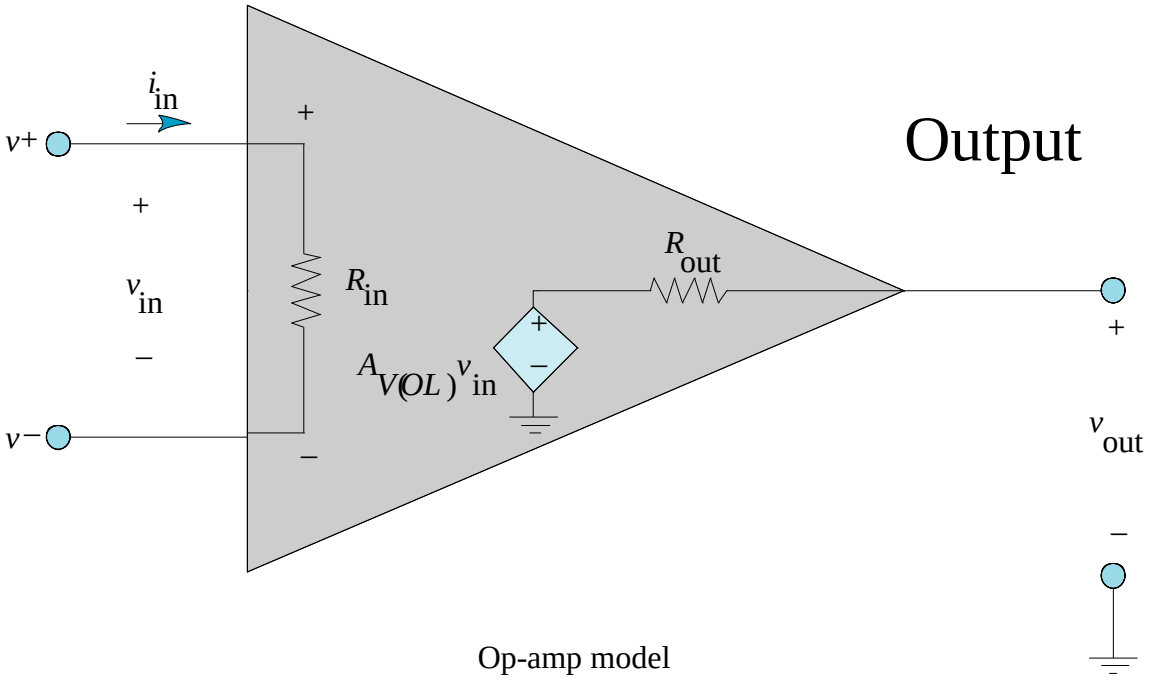
We can then have the relationship between the output and differential input, v_{in}, as:

$$v_{out} = A_{V(OL)}(v_{in}) = A_{V(OL)}(v^+ - v^-)$$

The Operational Amplifier

Noninverting input

Inverting input



Op-amp model

Ideal operational amplifier
Has infinite input resistance:

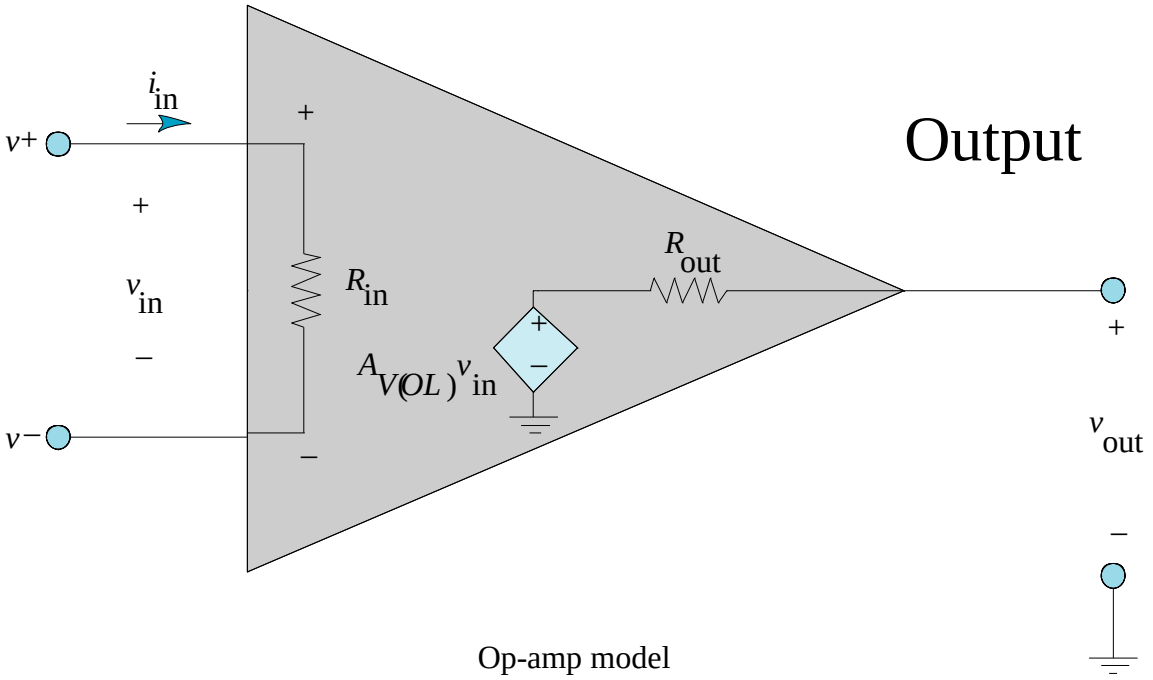
$$R_{in} = \infty$$

Non-Ideal operational amplifiers
Have very large input resistance
In the order of $10^6\ \Omega$'s

The Operational Amplifier

Noninverting input

Inverting input



Op-amp model

Since Ideal operational amplifier Have infinite input resistance:

$$R_{in} = \infty$$

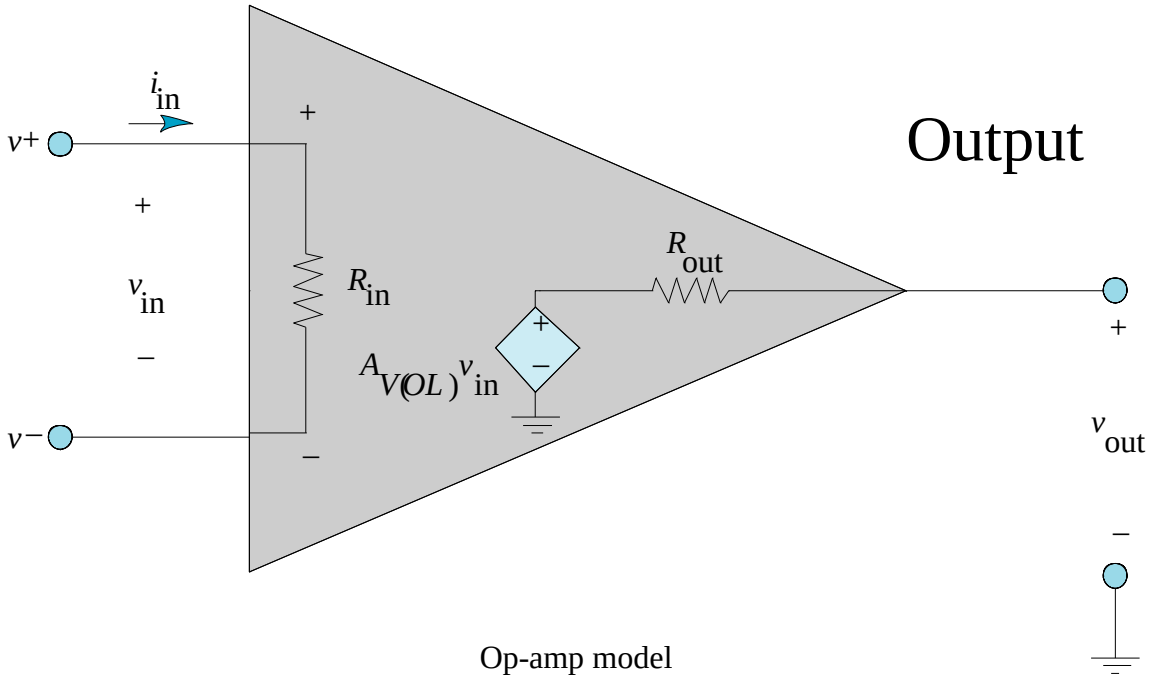
Then the current into an ideal Op-amps terminals (+ve or –ve) Is zero! $i_{in}^{+} = i_{in}^{-} = 0$

Since Non-Ideal operational amplifiers Have very large input resistances of the order of $10^6\,\Omega$'s so the current Into the Op-amps terminals is Negligibly small!

The Operational Amplifier

Noninverting input

Inverting input



Op-amp model

Ideal operational amplifier

Have zero output resistance:

$R_{out} = 0$

Non-Ideal operational amplifiers

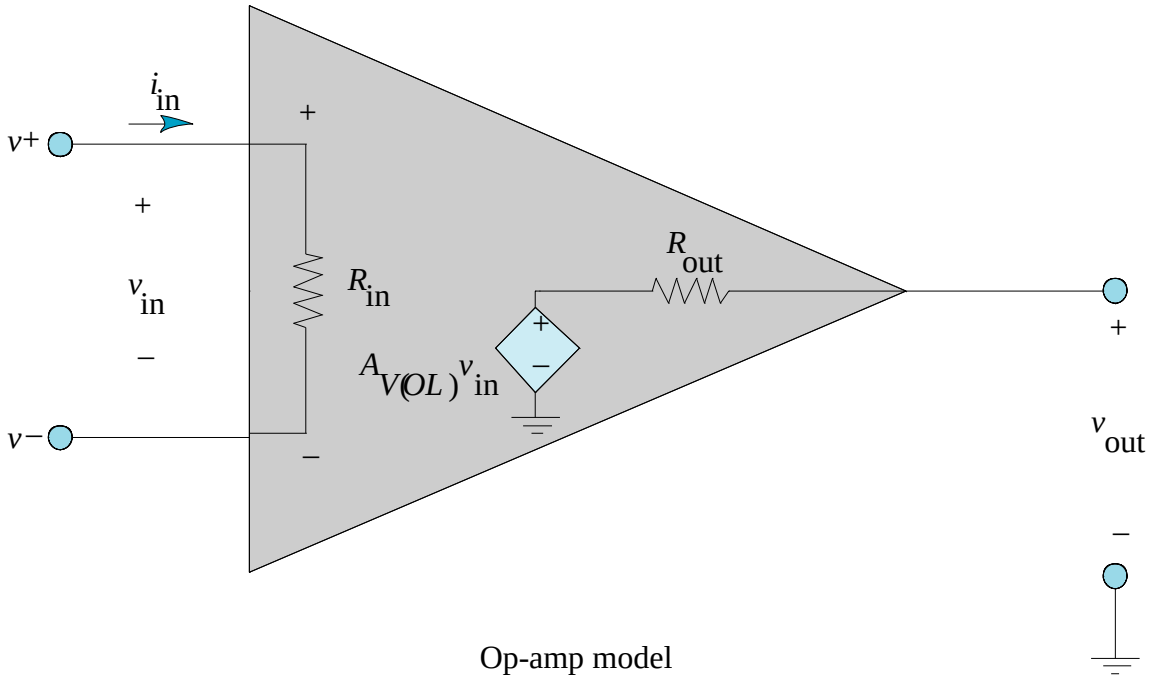
Have very low Output Resistances

of the order of a few hundred ohms

Or less!

The Operational Amplifier

Noninverting input



Op-amp model

Inverting input

SUMMARY

An IDEAL op-amp has:

- Infinite Input Resistance
- Zero Output Resistance
- Infinite Open Loop Gain
- Infinite Bandwidth

This is not true of non-ideal op-amps
See ECTE212!

The Operational Amplifier

The Virtual Short Circuit

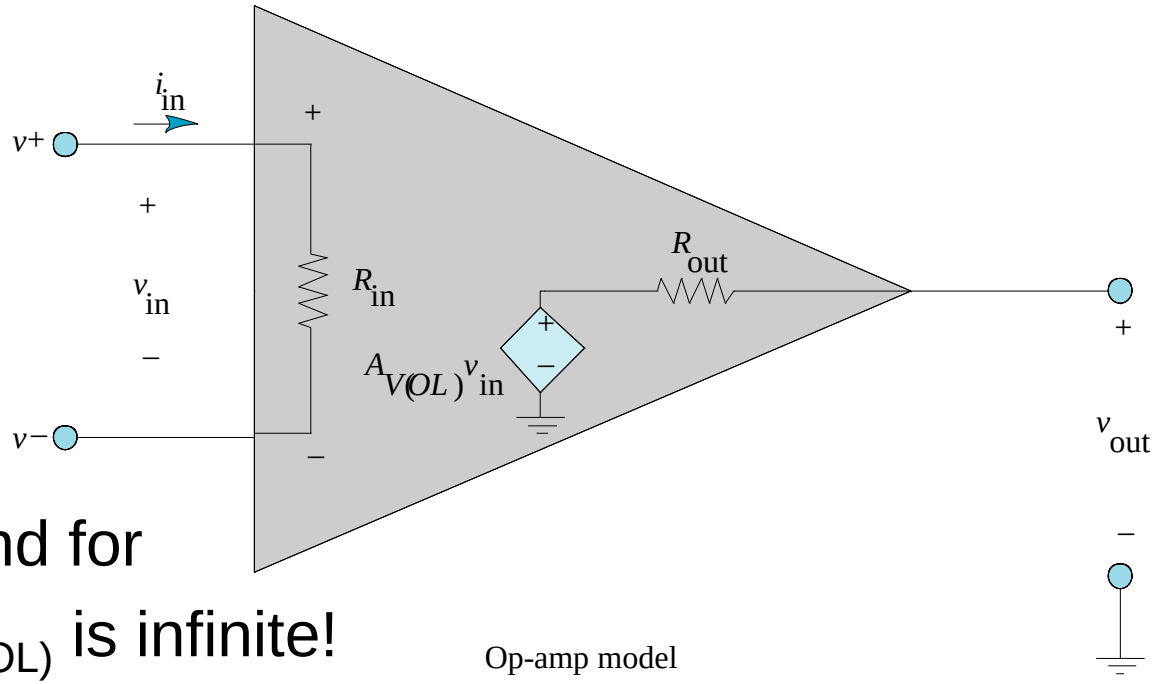
Consider an IDEAL Op-amp:

In this case $R_{out}=0$

Then we have:

$$v_{out} = A_{V(OL)} v_{in}$$

If $A_{V(OL)} >> v_{out}$ And for IDEAL it is because $A_{V(OL)}$ is infinite!



Op-amp model

Then we can write:

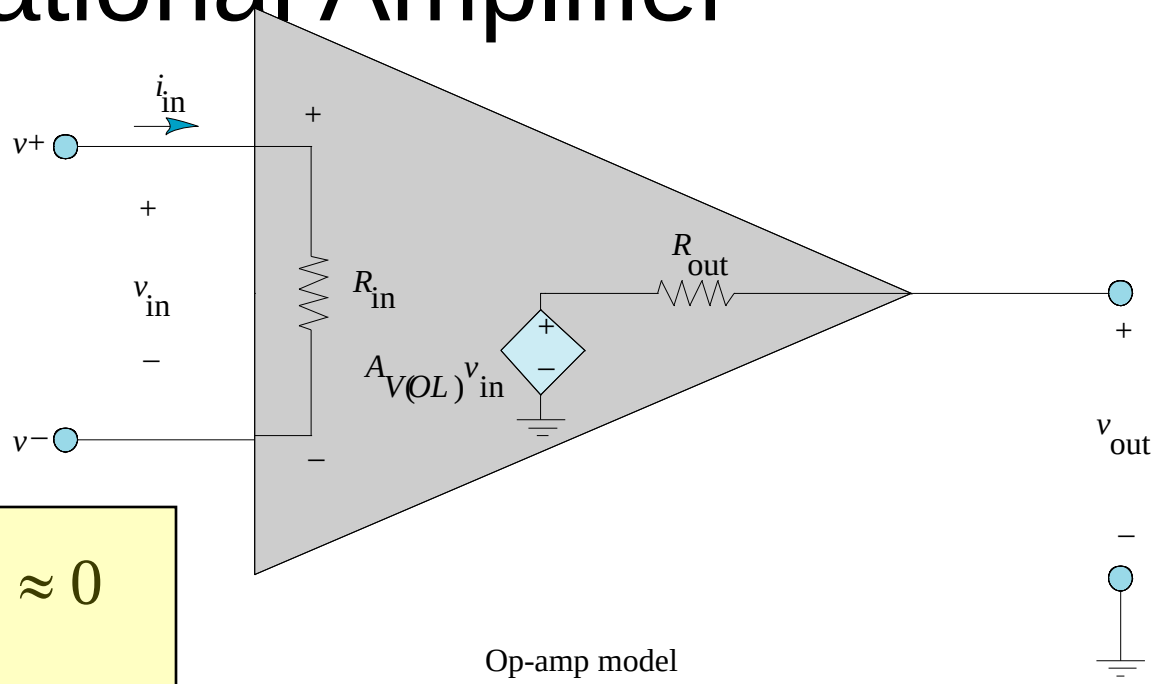
$$v_{in} = \frac{v_{out}}{A_{V(OL)}} = v^+ - v^- \approx 0$$

or $v^+ \approx v^-$ Which also means that

$$i_{in} = \frac{v^+ - v^-}{R_{in}\big|_{R_{in}=\infty}} \approx \frac{0}{\infty} = 0$$

The Operational Amplifier

The Virtual Short Circuit



Op-amp model

Thus we have a Virtual short Circuit such That:

$$v_{in} = \frac{v_{out}}{A_{V(OL)}} = v^+ - v^- \approx 0$$

and

$$i_{in} = \frac{v^+ - v^-}{R_{in}\big|_{R_{in}=\infty}} \approx \frac{0}{\infty} = 0$$

and

$$v^+ \approx v^-$$

The Operational Amplifier

The Virtual Ground

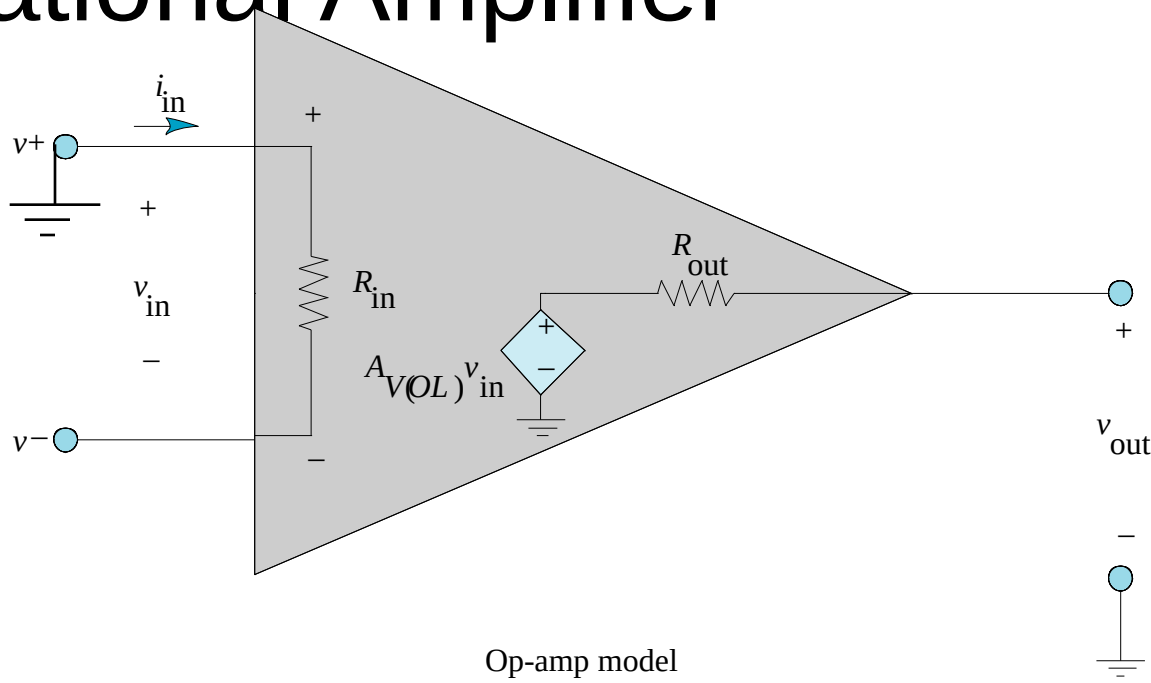
If we set: $v^+ = 0$

Then we have a Virtual ground Since for an ideal Op-amp:

$$v^- \approx v^+ = 0$$

Implies that:

$$v^- = 0$$



Op-amp model

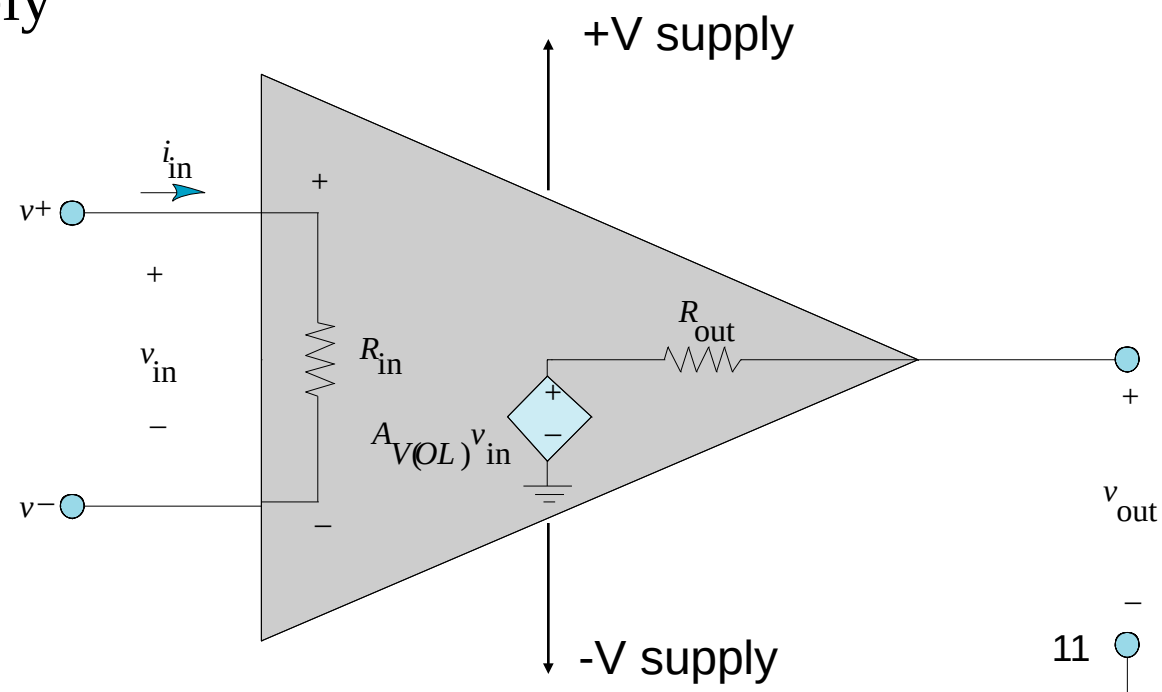
The Operational Amplifier

Consider the relationship between the output and differential input, v_{in}, :

$$v_{out} = A_{V(OL)}(v_{in}) = A_{V(OL)}(v^{+} - v^{-})$$

If the difference between the +ve and –ve terminals is not close to zero, the infinite (or large) gain will drive the output to either A very large +ve or very large –ve value. Real op-amps will Saturate at the +ve supply Rail or –ve supply rail

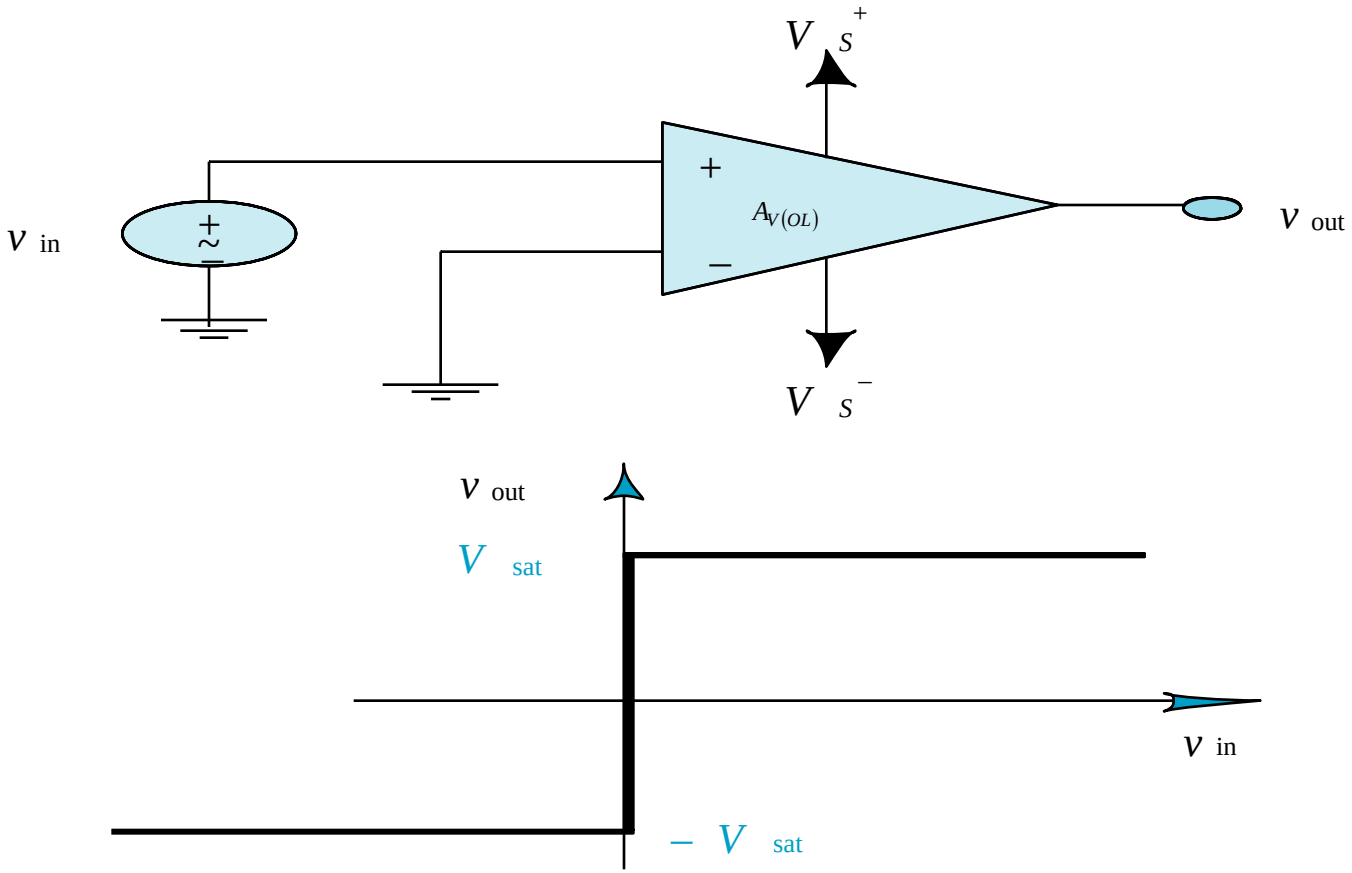
This allows the development of a Zero crossing circuit…



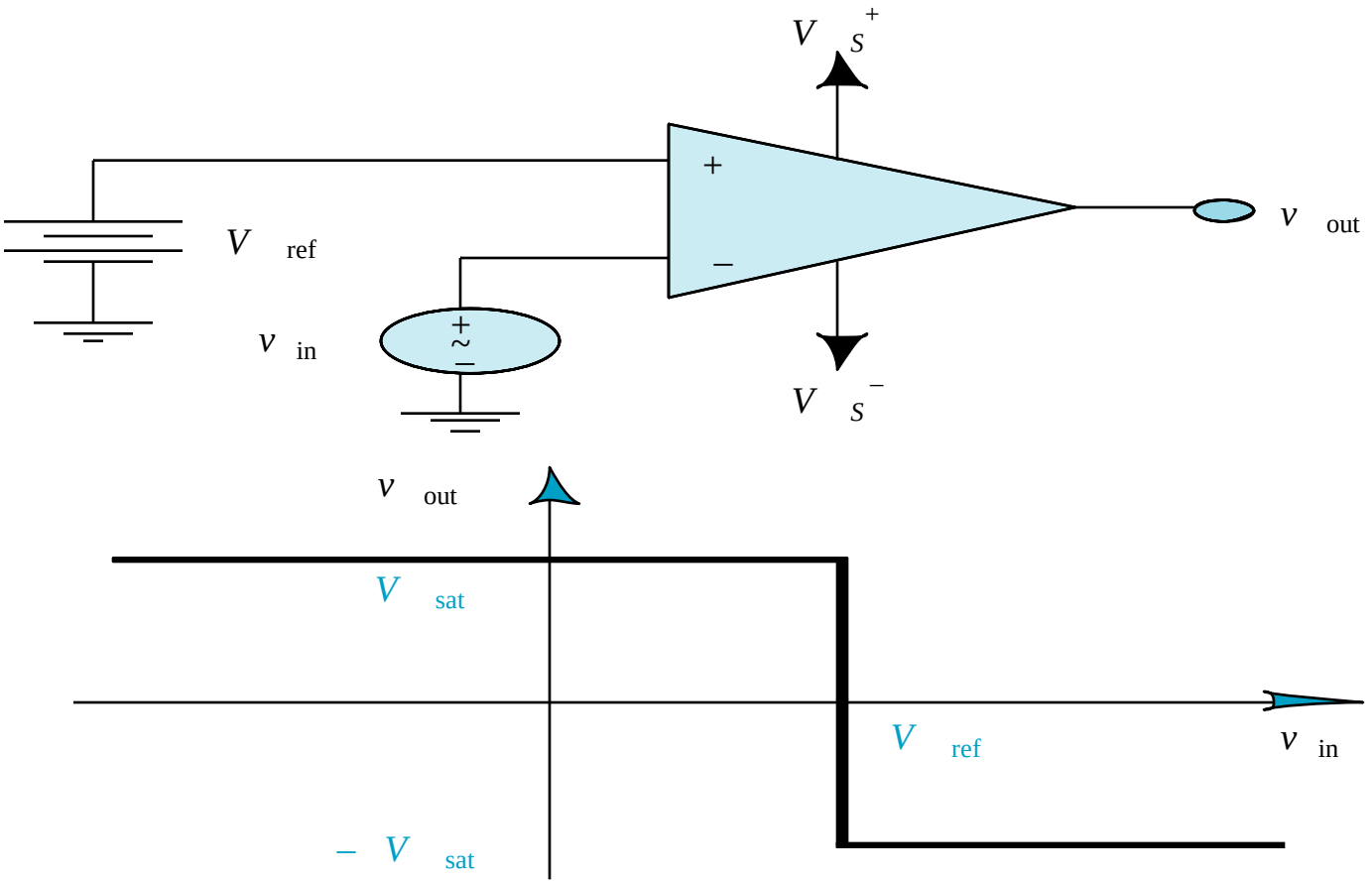
Op-amp model

The Operational Amplifier

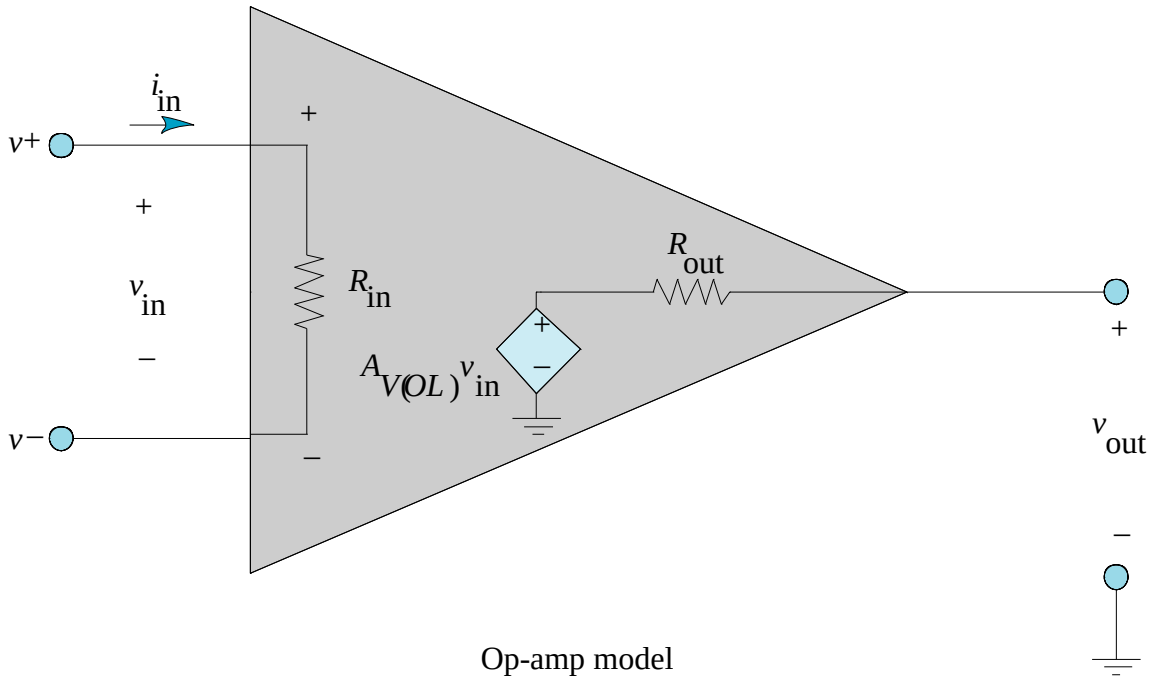
Zero-crossing comparator



The Operational Amplifier
Inverting comparator with offset



The Operational Amplifier



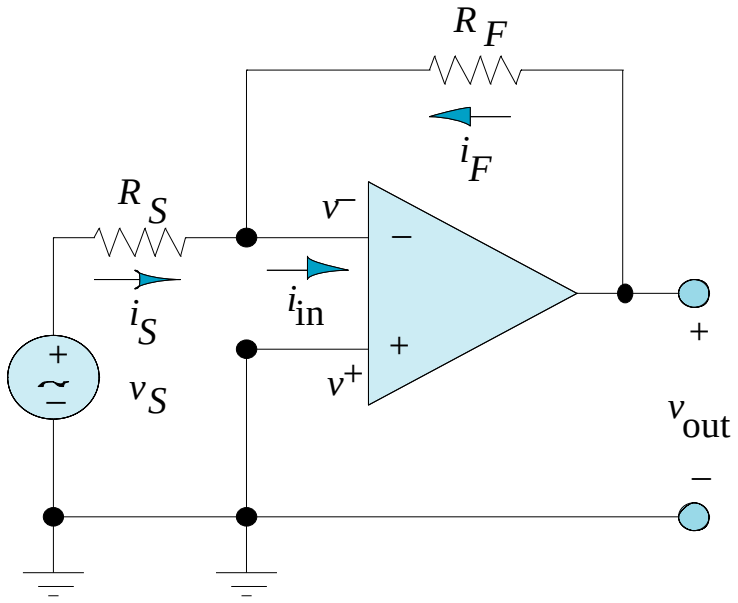
Op-amp model

Operational amplifiers are almost always used with negative feedback, in which part of the output signal is returned to the input in opposition to the source signal.

The Operational Amplifier

In a negative feedback system, the ideal op-amp output voltage attains the value needed to force the differential input voltage and input current to zero.

- Part of the output is returned to the input
- The feedback signal opposes the input source



Comment

When the fed back signal opposes the
Input we call this negative feedback

Note we will find that by providing
Negative feedback from the output to the input
That the infinite gain is changed to some
Finite gain – this is one of the typical
Consequences of negative feedback

The Operational Amplifier

Analysis of Ideal Op-Amp

- Verify that negative feedback is present
- Assume that the differential input voltage and the input current of the op-amp are zero
- Apply standard circuit analysis principles

The Operational Amplifier

The Inverting Amplifier

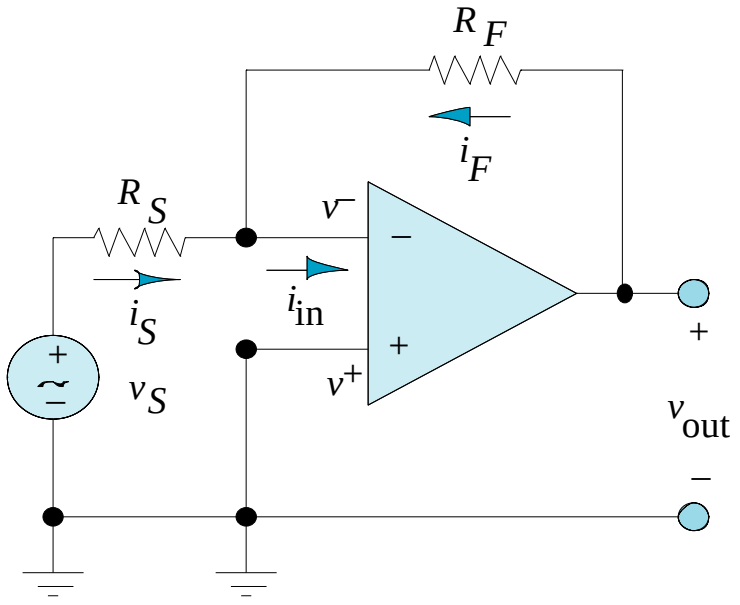
Consider the situation where we connect the +ve terminal
To ground and the -ve terminal is connected via
A feedback (R_F) resistor to the output and then the input is
Connected to another resistor (R_S) to the –ve terminal:

The currents are shown, where i_F is the
Current from the output to the –ve terminal
Through the feedback resistor R_F and
i_s is the current from the input voltage source
v_s into the the input resistor R_S

i_{in} is the current into the –ve terminal
Of the op-amp

Now if we assume that the op-amp
Is ideal then the current into the –ve
Terminal is zero , that is:

$$i_{in} = 0$$ IDEAL OP-AMP



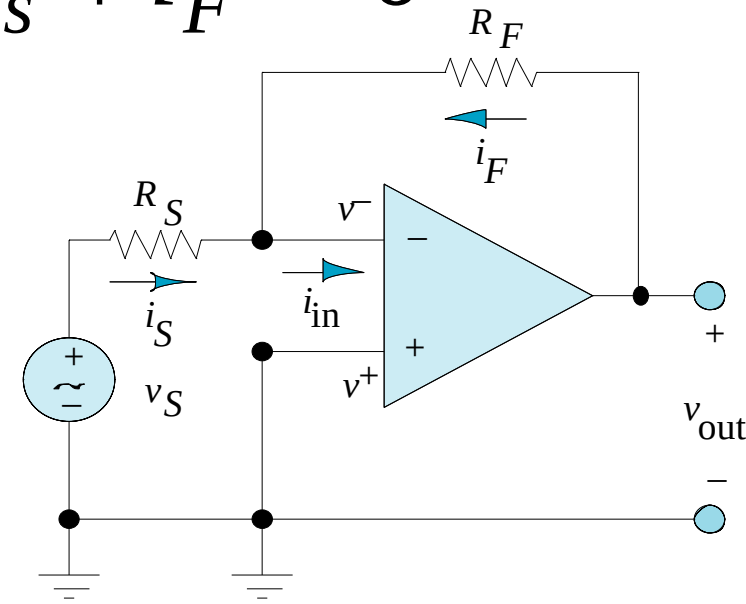
The Operational Amplifier

The Inverting Amplifier

Given that i_{in} is zero we can apply KCL at the –ve terminal:

$$i_s + i_F - i_{in} = 0 \Rightarrow i_s + i_F = 0$$

Now we know that by grounding the +ve input
Due to the infinite gain of the Ideal Op-Amp
That the –ve terminal will also have the same
Voltage (virtual short circuit property), so
This means the –ve terminal has a voltage of
Zero (0) volts! Which means that:



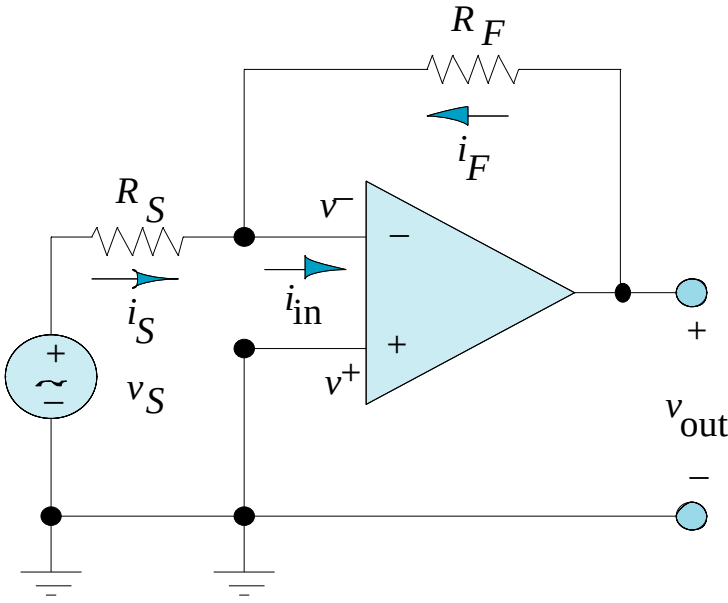
$$i_S = \frac{v_S - v^-}{R_S} = \frac{v_S - 0}{R_S} = \frac{v_S}{R_S}$$

The Operational Amplifier

The Inverting Amplifier

We can also calculate i_F using:

$$i_F = \frac{v_{out} - v^-}{R_F} = \frac{v_{out} - 0}{R_F} = \frac{v_{out}}{R_F}$$



Now we apply our equation for KCL at The –ve node to get:

$$i_S + i_F = 0 = \frac{v_S}{R_S} + \frac{v_{out}}{R_F}$$

Which after rearranging gives:

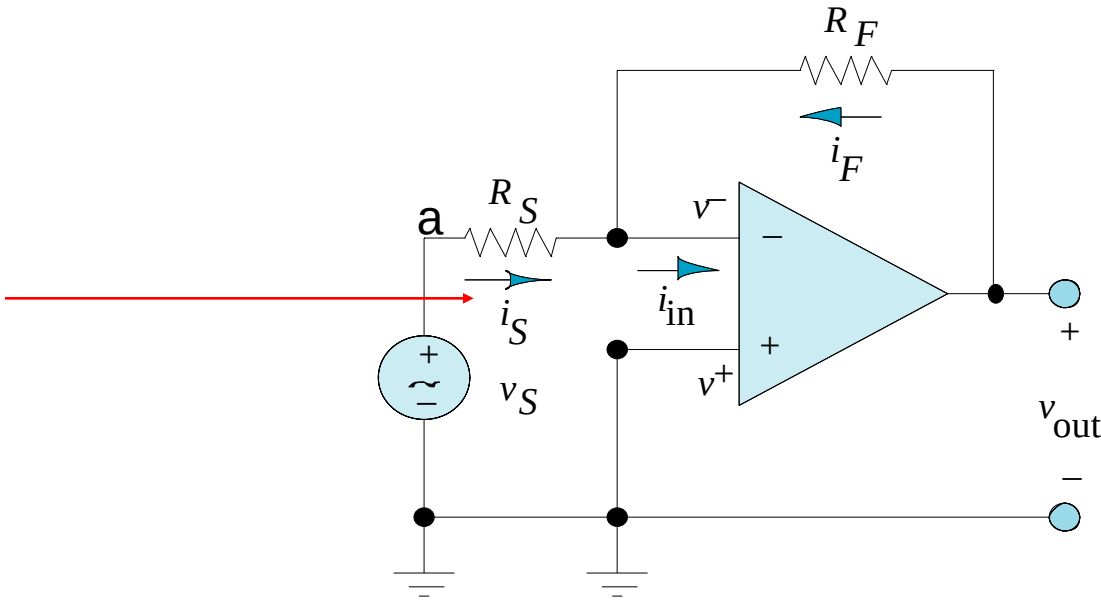
$$\frac{v_{out}}{v_S} = -\frac{R_F}{R_S} = Gain = A_v$$

The Operational Amplifier

The Inverting Amplifier

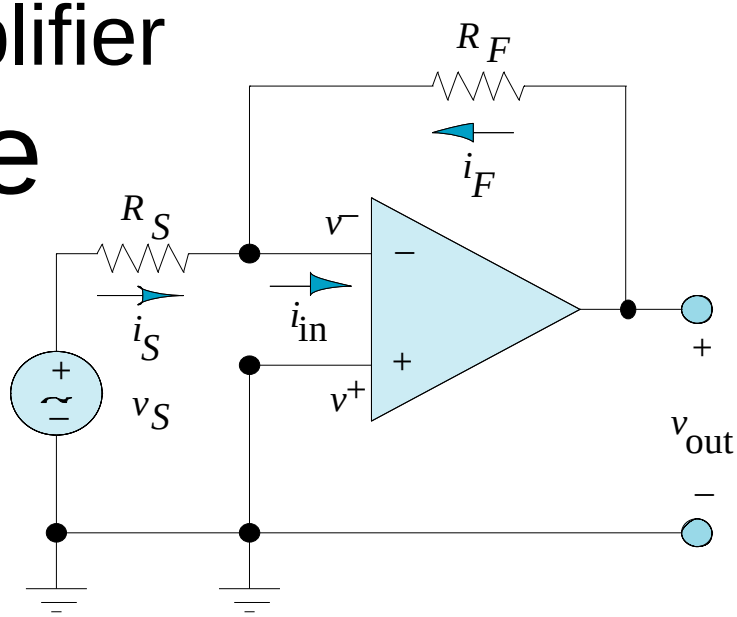
The input resistance looking In from the terminal (a) to Ground for the inverting amplifier is in fact the Value of the resistor R_S:

$$R_{in} = R_S \equiv \frac{v_S}{i_S}$$



The Inverting Amplifier

Example



If the input voltage, v_S, is 2 volts DC and the supply rails are +15 volts and -15 volts respectively (not Shown) what is the output Voltage v_{out} equal to when R_S=10 kΩ and R_F=20 kΩ?

Answer:

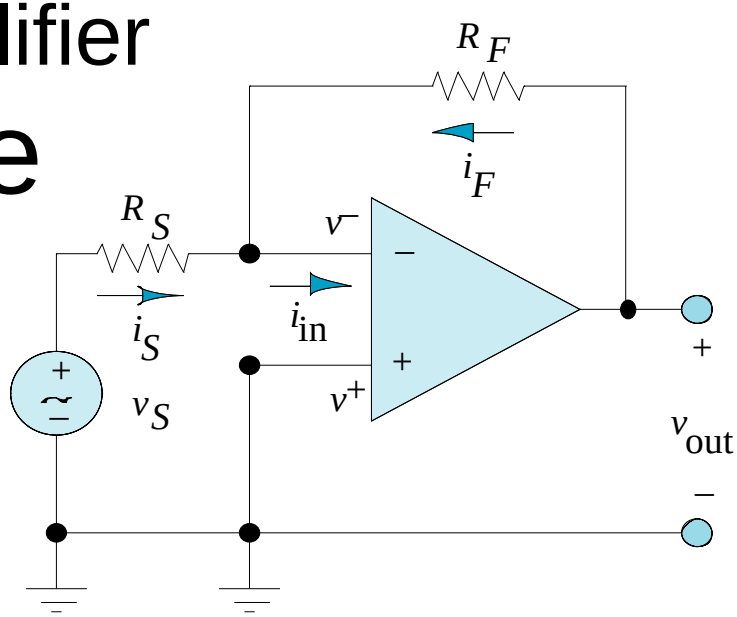
$$\frac{v_{out}}{v_S} = -\frac{R_F}{R_S} = Gain = A_v = -\frac{20000\ \Omega}{10000\ \Omega} = -2$$

$$\therefore v_{out} = -2v_S = -2 \times 2 = -4 \quad volts$$

Notice that this voltage is still between the voltage supply rails of the op-amp And is inverted (opposite polarity) to the input voltage

The Inverting Amplifier

Example



If the input voltage, v_S, is -3.333 volts DC and the supply rails are +15 volts and -15 volts respectively (not Shown) what is the output Voltage v_{out} equal to when R_S=1 kΩ and R_F=3 kΩ?

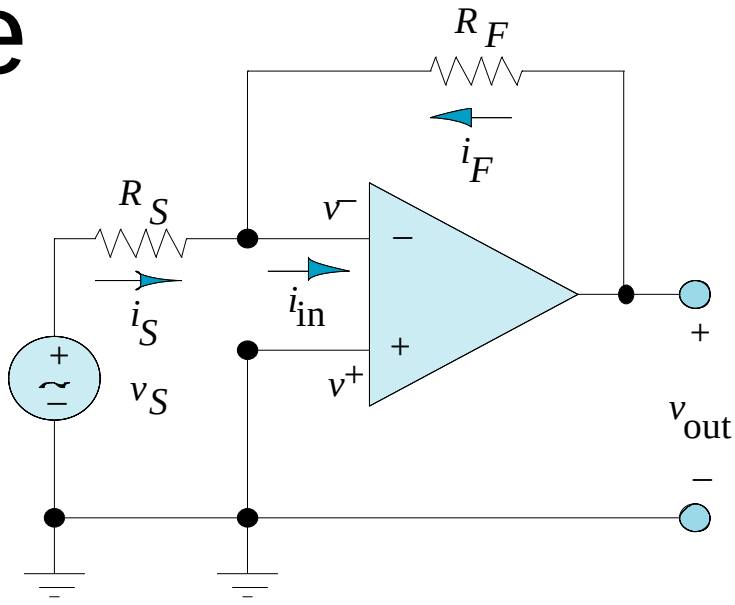
Answer:

$$\frac{v_{out}}{v_S} = -\frac{R_F}{R_S} = Gain = A_v = -\frac{3000\ \Omega}{1000\ \Omega} = -3$$

$$\therefore v_{out} = -3v_S = -3\times\left(\frac{-10}{3}\right) = +10 \quad volts$$

Example

If the input voltage, v_S, is $\left(3\sqrt{2}\right)\sin\left(2000\times\pi\times t\right)$ volts and the supply rails are +15 volts and -15 volts DC respectively (not shown) what is the output Voltage v_{out} equal to when R_S=10 kΩ and R_F=15 kΩ?



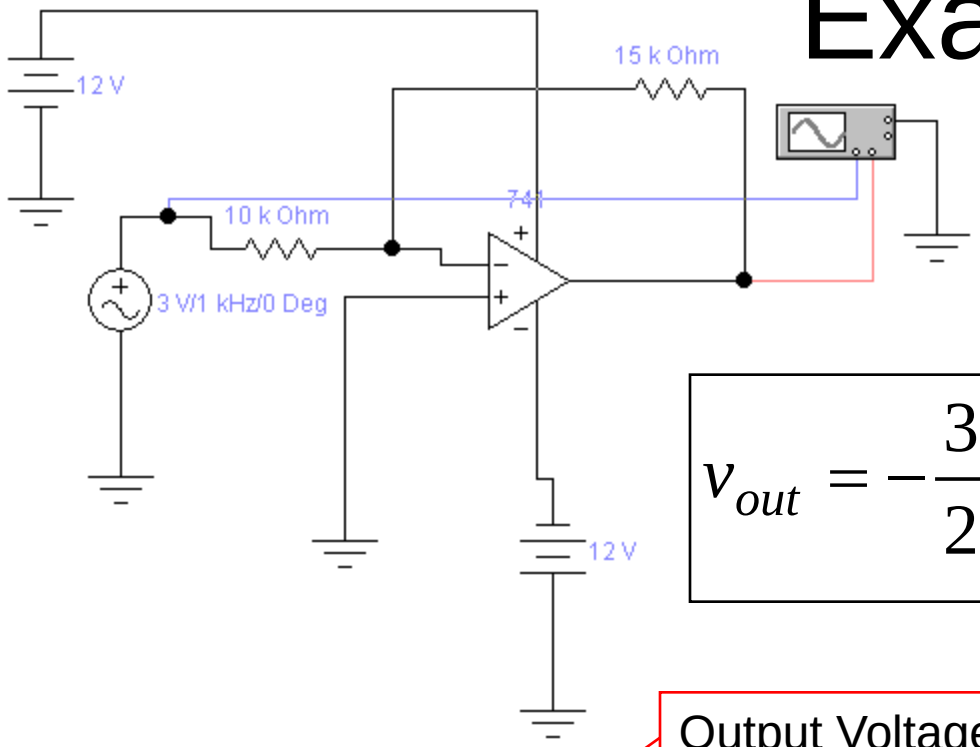
Answer:

$$\frac{v_{out}}{v_S} = -\frac{R_F}{R_S} = Gain = A_v = -\frac{15000\ \ \Omega}{10000\ \ \Omega} = -1.5$$

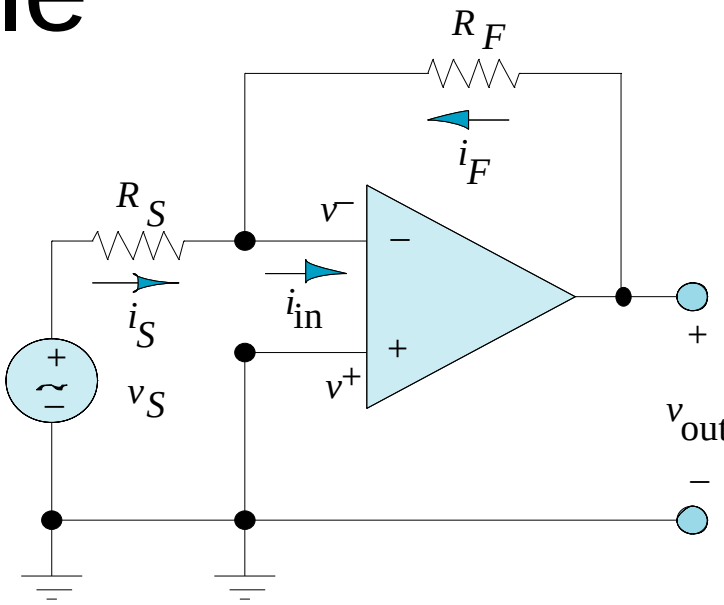
$$\therefore v_{out} = -\frac{3}{2}v_S = -\frac{3}{2}\times\left(3\sqrt{2}\sin\left(2000\times\pi\times t\right)\right)$$

$$= -\frac{9}{\sqrt{2}}\sin\left(2000\times\pi\times t\right)\quad volts$$

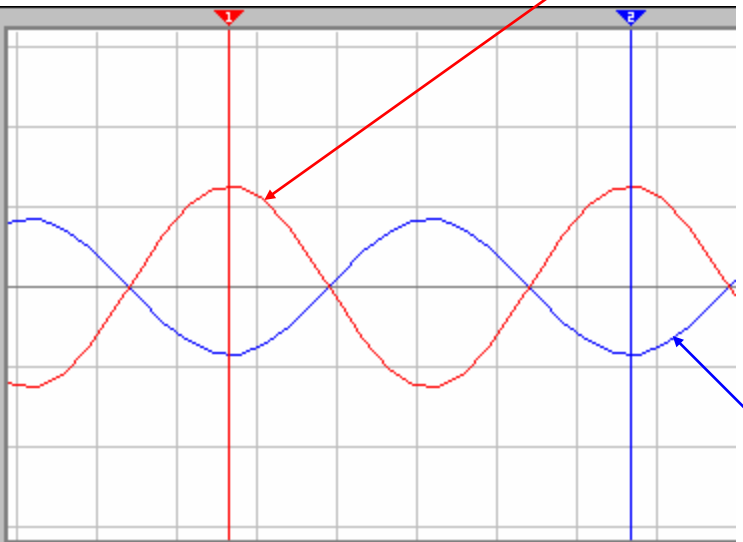
Example



$$v_{out} = -\frac{3}{2} v_S$$



Output Voltage

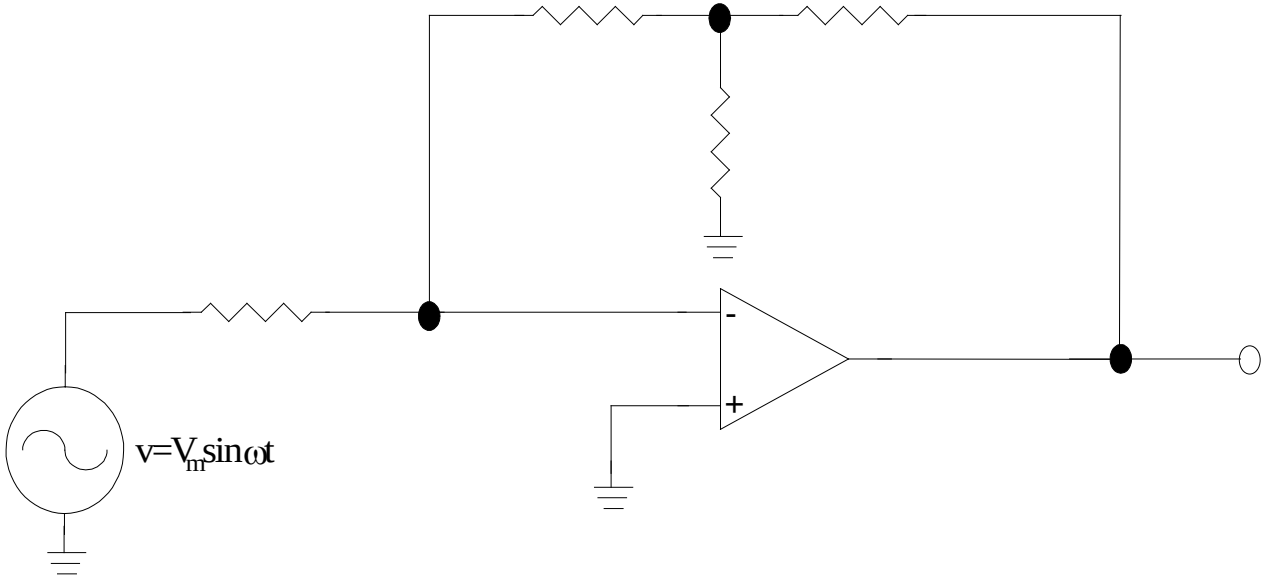


Input Voltage

We say that the inverter results in the Output sinusoid being 100% out of Phase with the input sinusoid (that is the inversion of the input signal)

The Operational Amplifier

The Inverting Amplifier

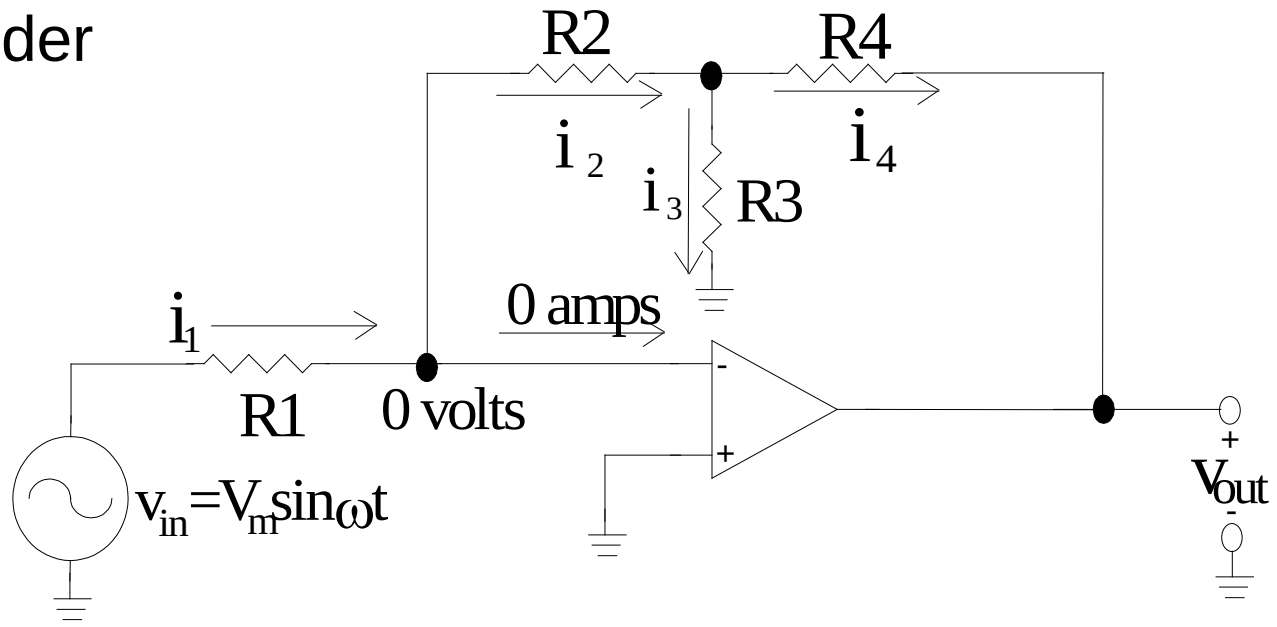


We can use the same technique to analyse this circuit (which is still an inverting amplifier!)

The Operational Amplifier

The Inverting Amplifier

Consider



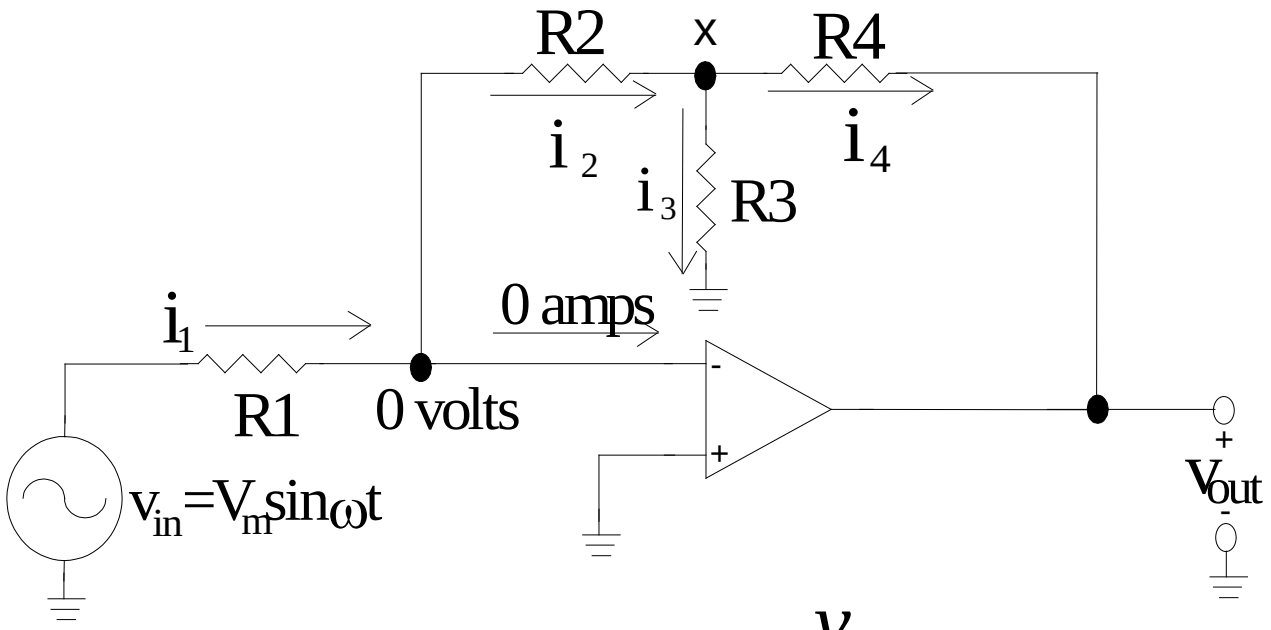
As before we apply KCL at the –ve terminal to get:

$$i_1 - 0 - i_2 = 0$$ Or $$i_1 = i_2$$

We can calculate i_1 using Ohms law: $$i_1 = \frac{v_{in} - 0}{R1} = \frac{v_{in}}{R1}$$

The Operational Amplifier

The Inverting Amplifier



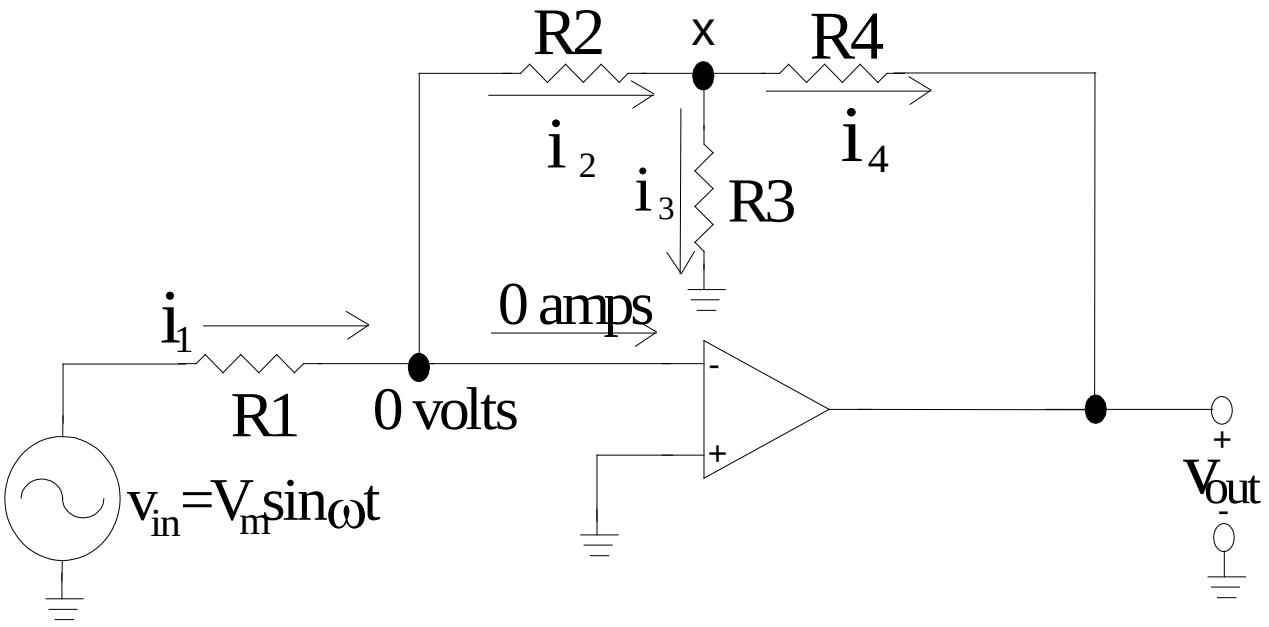
Thus we can see that $i_1 = i_2 = \frac{v_{in}}{R1}$

We can now determine the voltage
At node ‘x’ above:

$$v_x = 0 - i_2 R2 = -i_1 R2 = -\frac{v_{in}}{R1} \cdot R2 = -\frac{R2}{R1} \cdot v_{in}$$

The Operational Amplifier

The Inverting Amplifier

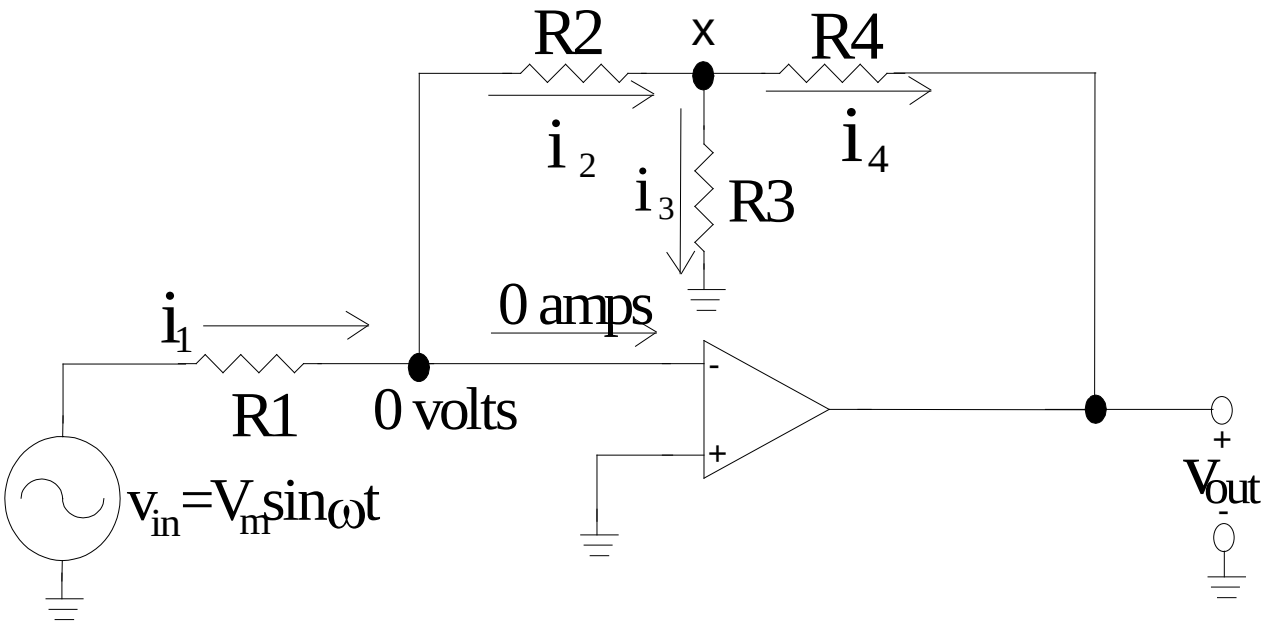


Now we can find the current through R3, i_3:

$$i_3 = \frac{v_x - 0}{R3} = \frac{v_x}{R3} \qquad = \left(\frac{-\left(\left(R2/R1 \right) \cdot v_{in} \right)}{R3} \right) = -\left(\frac{R2}{R1 \times R3} \right) \cdot v_{in}$$

The Operational Amplifier

The Inverting Amplifier



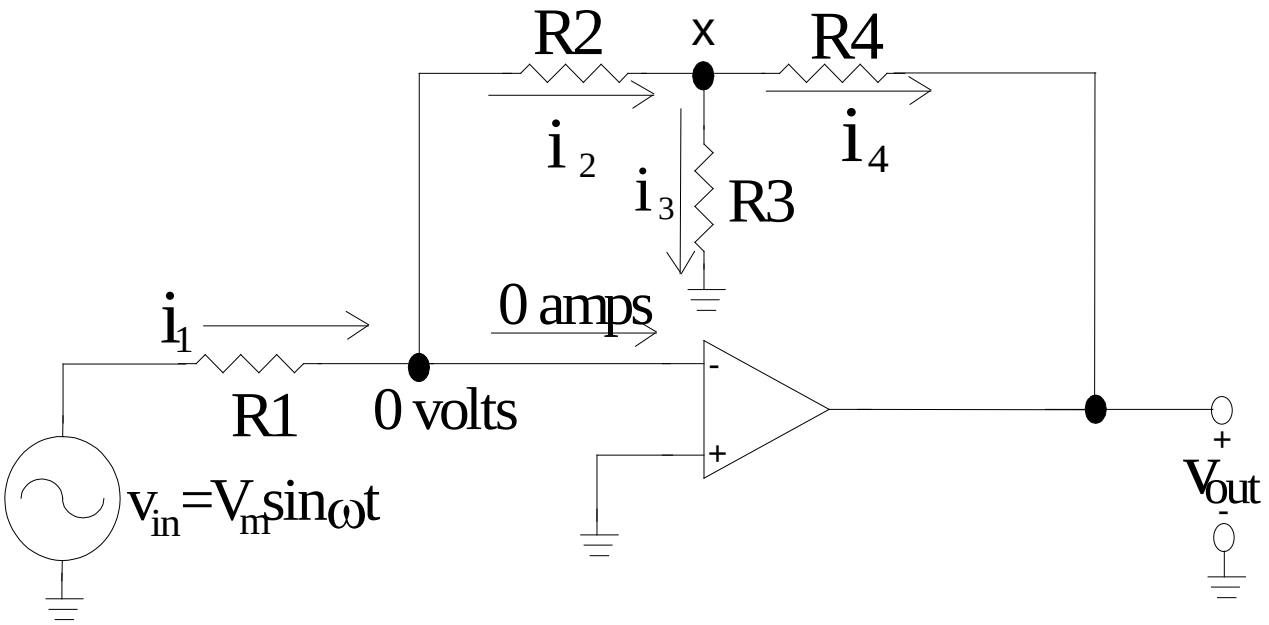
To find i_4 we use KCL at 'x': $i_2 - i_3 - i_4 = 0$

$$\therefore i_4 = i_2 - i_3$$

Thus: $$i_4 = \left(\frac{v_{in}}{R1}\right) - \left(\left(\frac{-R2}{R1 \times R3}\right) \cdot v_{in}\right) = \frac{v_{in}}{R1} + \frac{R2 \cdot v_{in}}{R1 \cdot R3}$$

The Operational Amplifier

The Inverting Amplifier



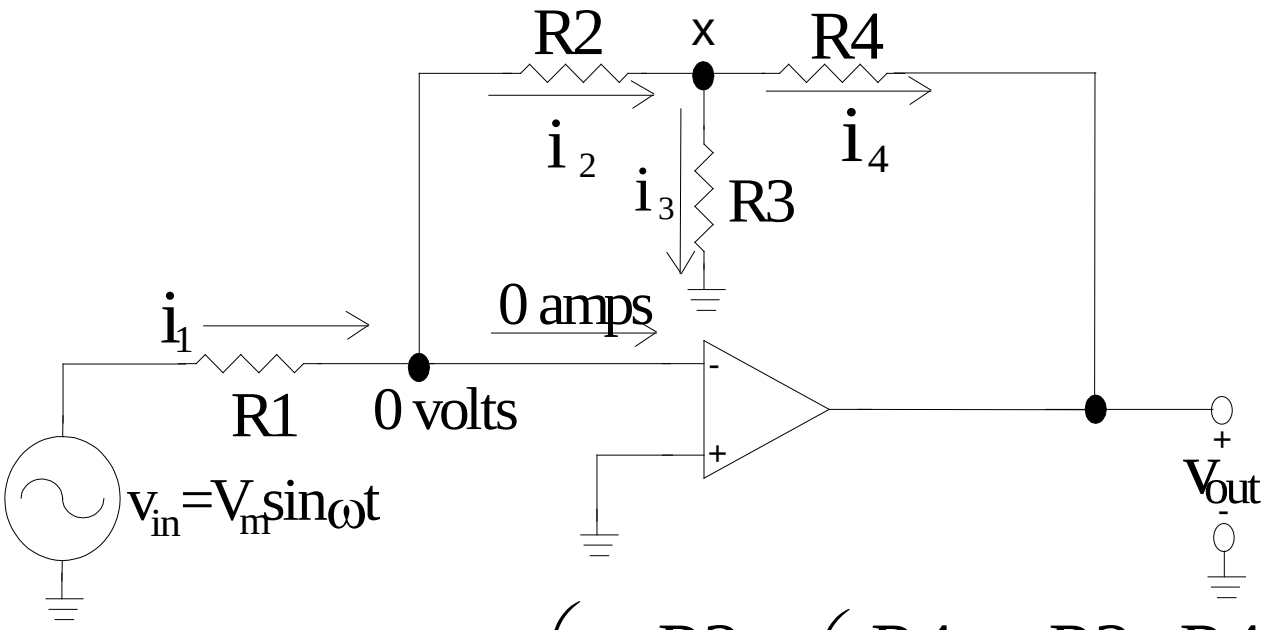
Now we can include v_{out} in our expressions:

$$v_{out} = v_x - i_4 \cdot R4$$

$$= -\frac{R2}{R1} \cdot v_{in} - \left(\frac{v_{in}}{R1} + \frac{R2 \cdot v_{in}}{R1 \cdot R3} \right) \cdot R4$$

The Operational Amplifier

The Inverting Amplifier



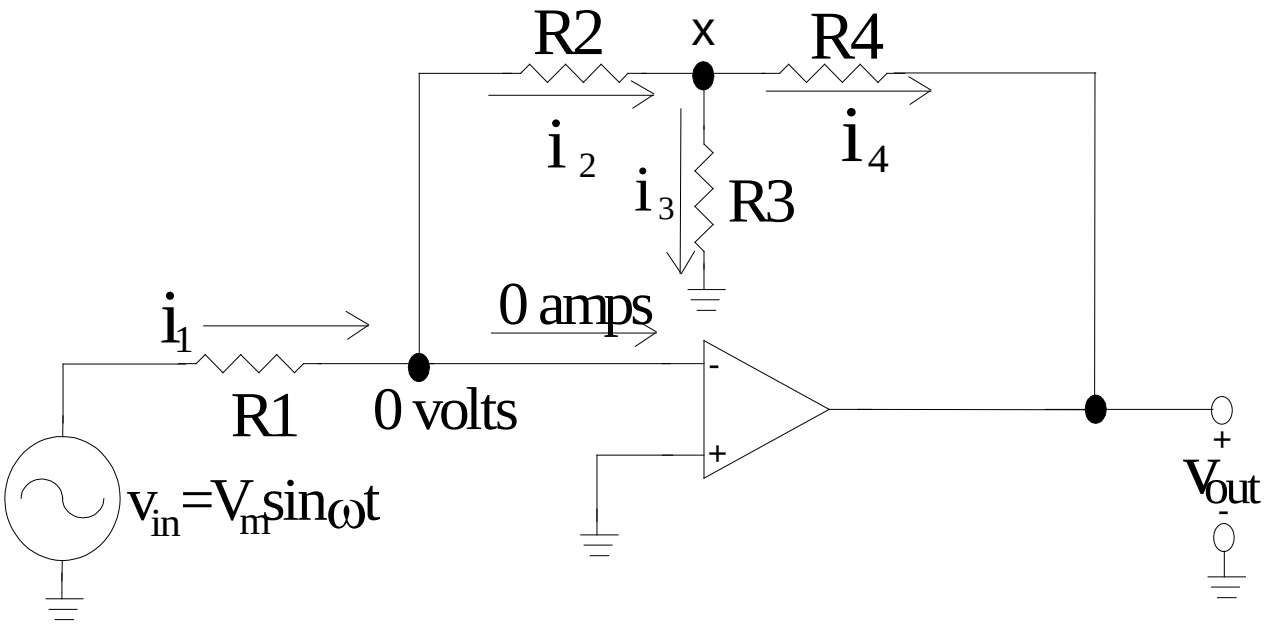
Rearranging:

$$v_{out} = v_{in} \cdot \left(-\frac{R2}{R1} - \left(\frac{R4}{R1} + \frac{R2 \cdot R4}{R1 \cdot R3} \right) \right)$$

$$\therefore \frac{v_{out}}{v_{in}} = -\left(\frac{R2}{R1} + \frac{R4}{R1}\left(1 + \frac{R2}{R3} \right) \right) = A_v$$

The Operational Amplifier

The Inverting Amplifier

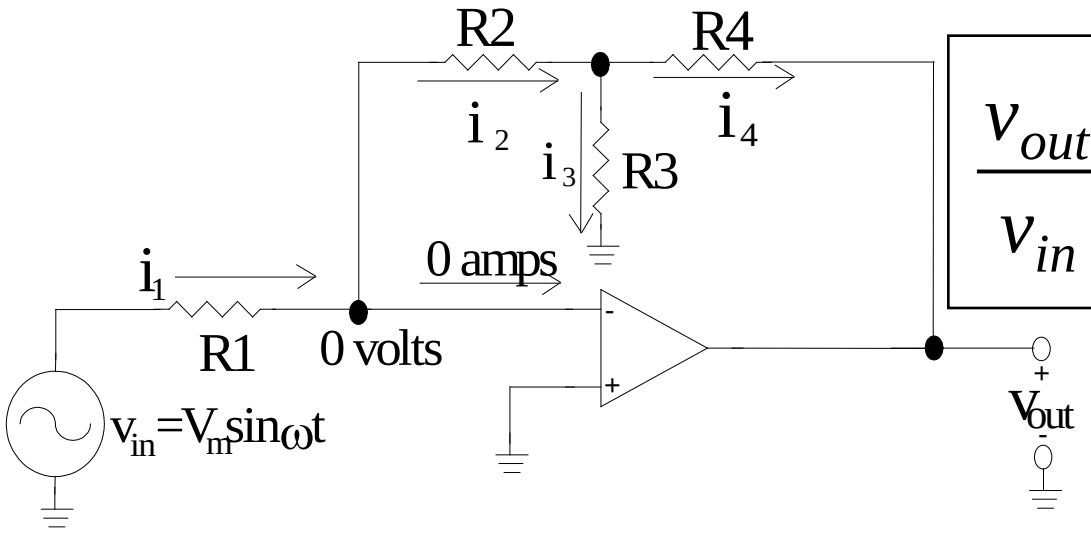


Which can also be expressed as:

$$\frac{v_{out}}{v_{in}} = -\frac{R2}{R1}\left(1+\frac{R4}{R2}+\frac{R4}{R3}\right)$$

The Operational Amplifier

The Inverting Amplifier

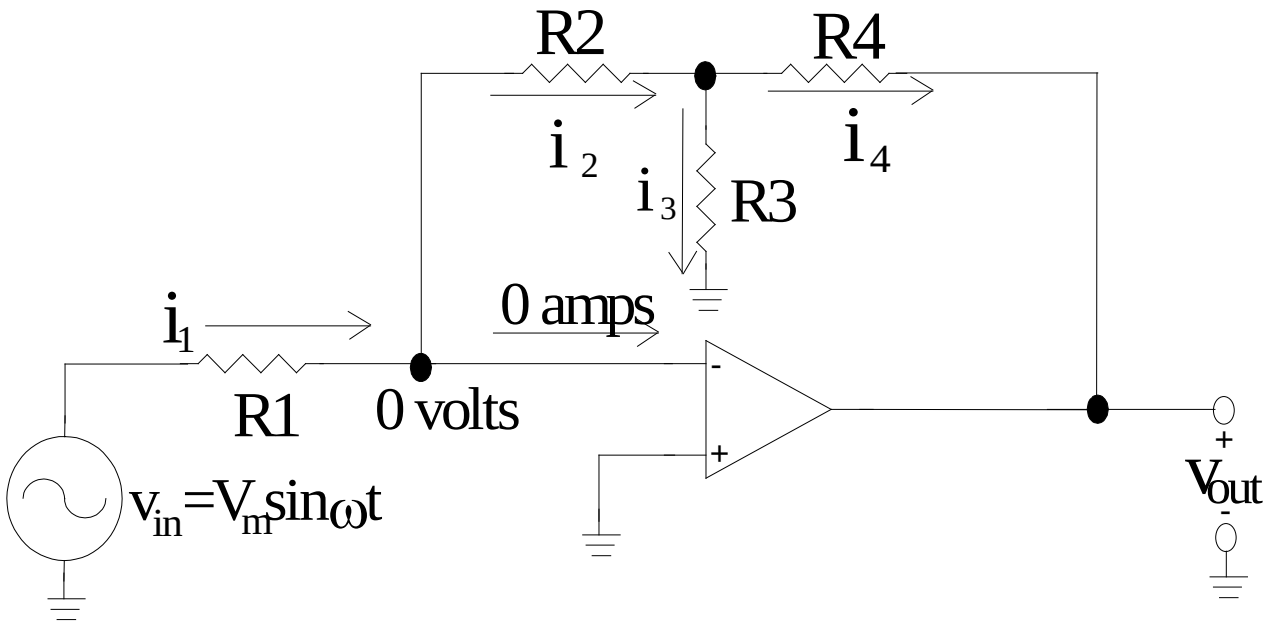


$$\frac{v_{out}}{v_{in}} = -\frac{R2}{R1}\left(1+\frac{R4}{R2}+\frac{R4}{R3}\right)$$

This circuit has the advantage that it can have a large Input resistance and large gain, Consider this next example…

The Operational Amplifier

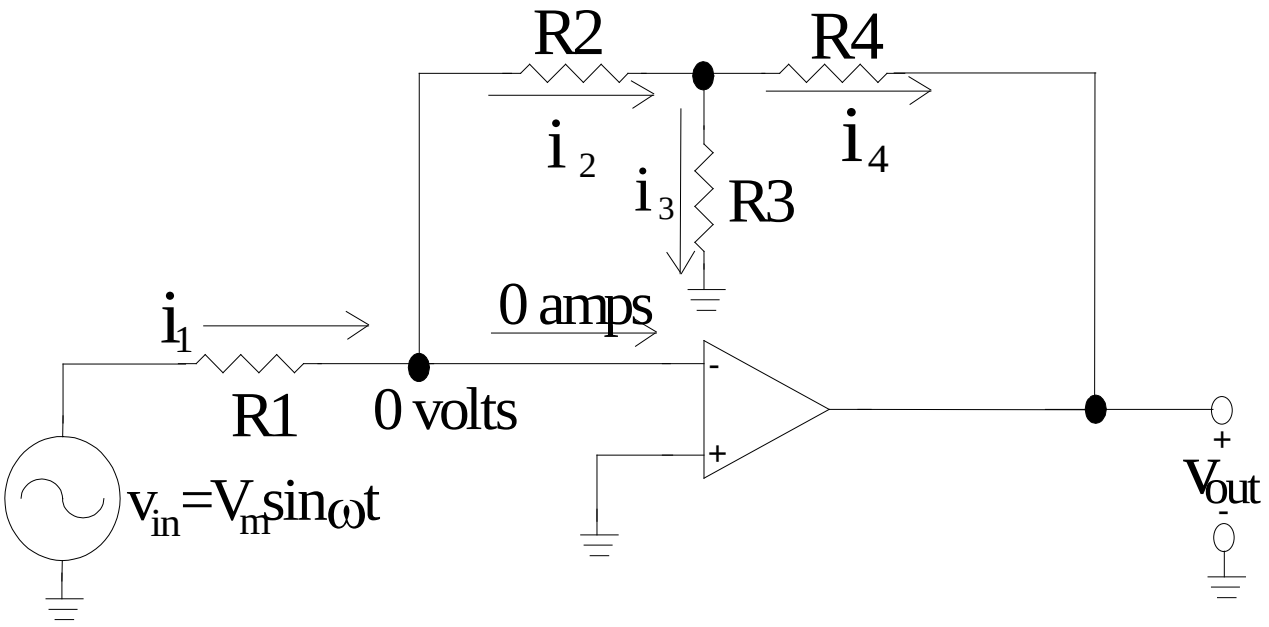
The Inverting Amplifier



It is specified that we need an amplifier with an Input resistance of 1 MΩ and a gain of approximately -100 Volt / Volt to within 10%. The maximum value of resistance values available is 1MΩ. Choose values for R1, R2, R3 & R4 in the op-amp circuit above to achieve this specification.

The Operational Amplifier

The Inverting Amplifier



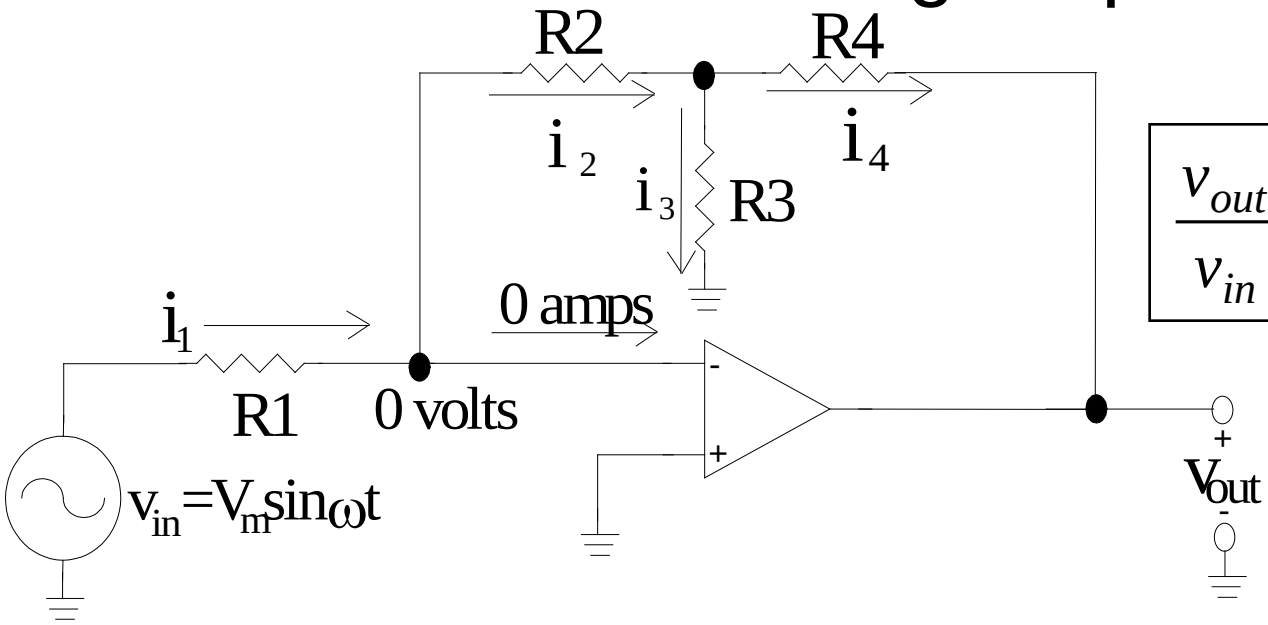
Given that the input resistance is 1MΩ we then select R1 to Be 1 MΩ ie: $R1 = 1M\Omega$

Since: $\frac{v_{out}}{v_{in}} = -\frac{R2}{R1}\left(1 + \frac{R4}{R2} + \frac{R4}{R3}\right)$

Then let R2=R1=1MΩ
Ie Ratio R2/R1 = 1

The Operational Amplifier

The Inverting Amplifier



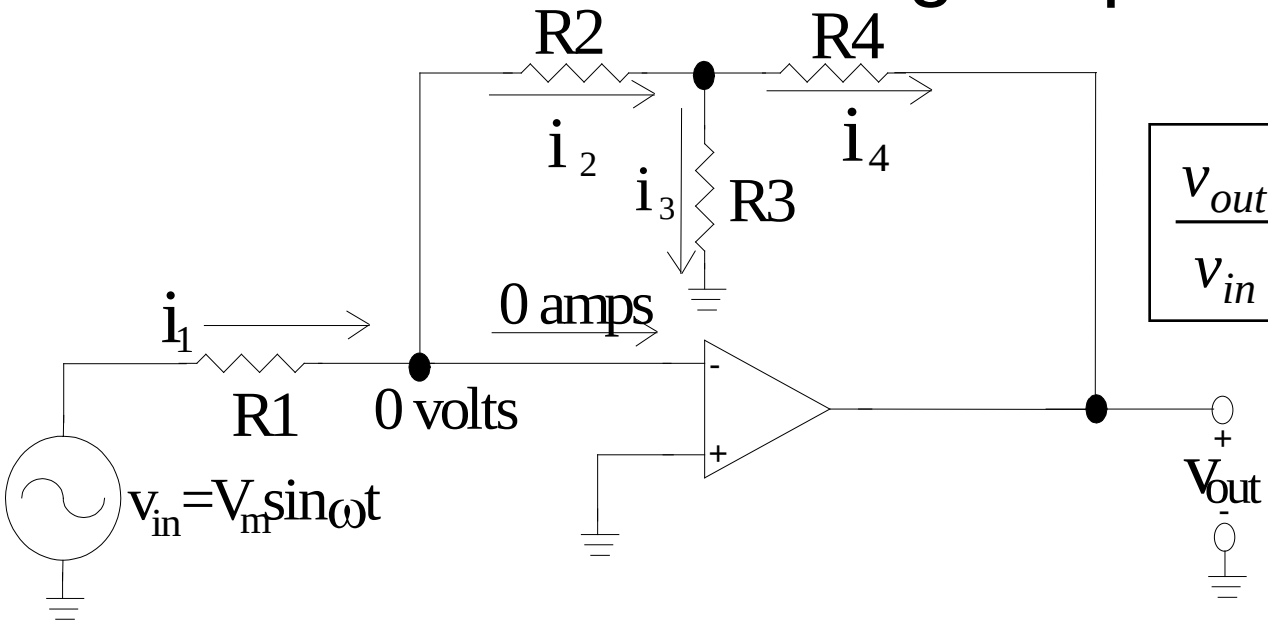
$$\frac{v_{out}}{v_{in}} = -\frac{R2}{R1}\left(1+\frac{R4}{R2}+\frac{R4}{R3}\right)$$

Now this means that R4/R2 will contribute little to the gain since R2 is 1MΩ and this is the largest possible resistor value

We must get our gain from the ratio of R4/R3.

The Operational Amplifier

The Inverting Amplifier

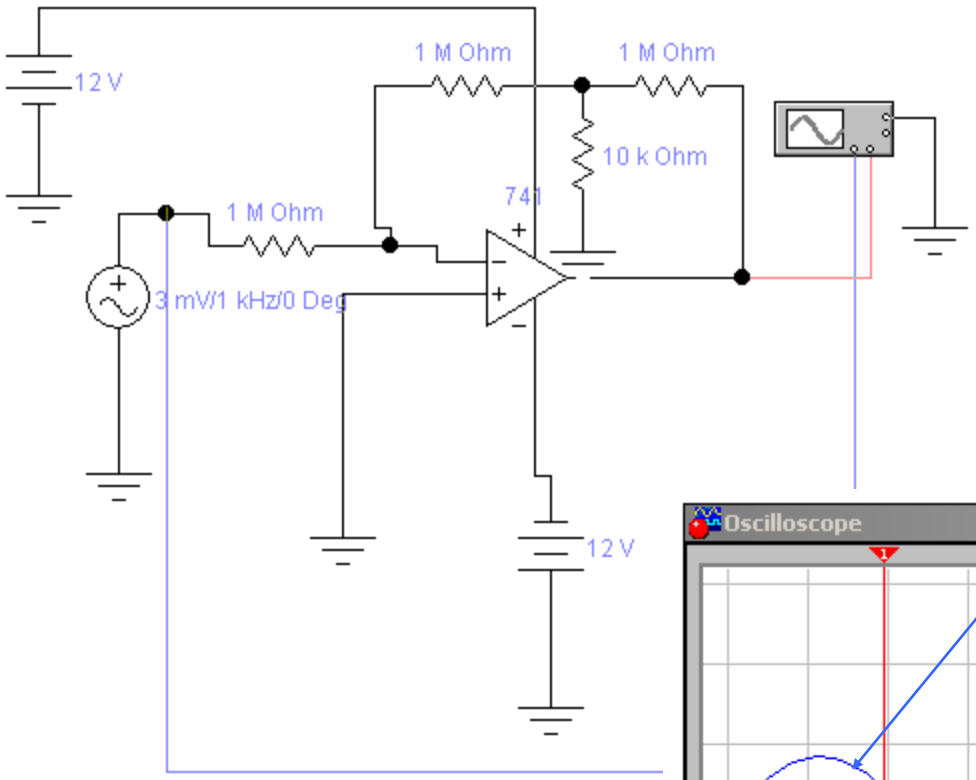


$$\frac{v_{out}}{v_{in}} = -\frac{R2}{R1}\left(1+\frac{R4}{R2}+\frac{R4}{R3}\right)$$

If we choose R4 to be 1MΩ and choose R3 to be 10 kΩ , then:

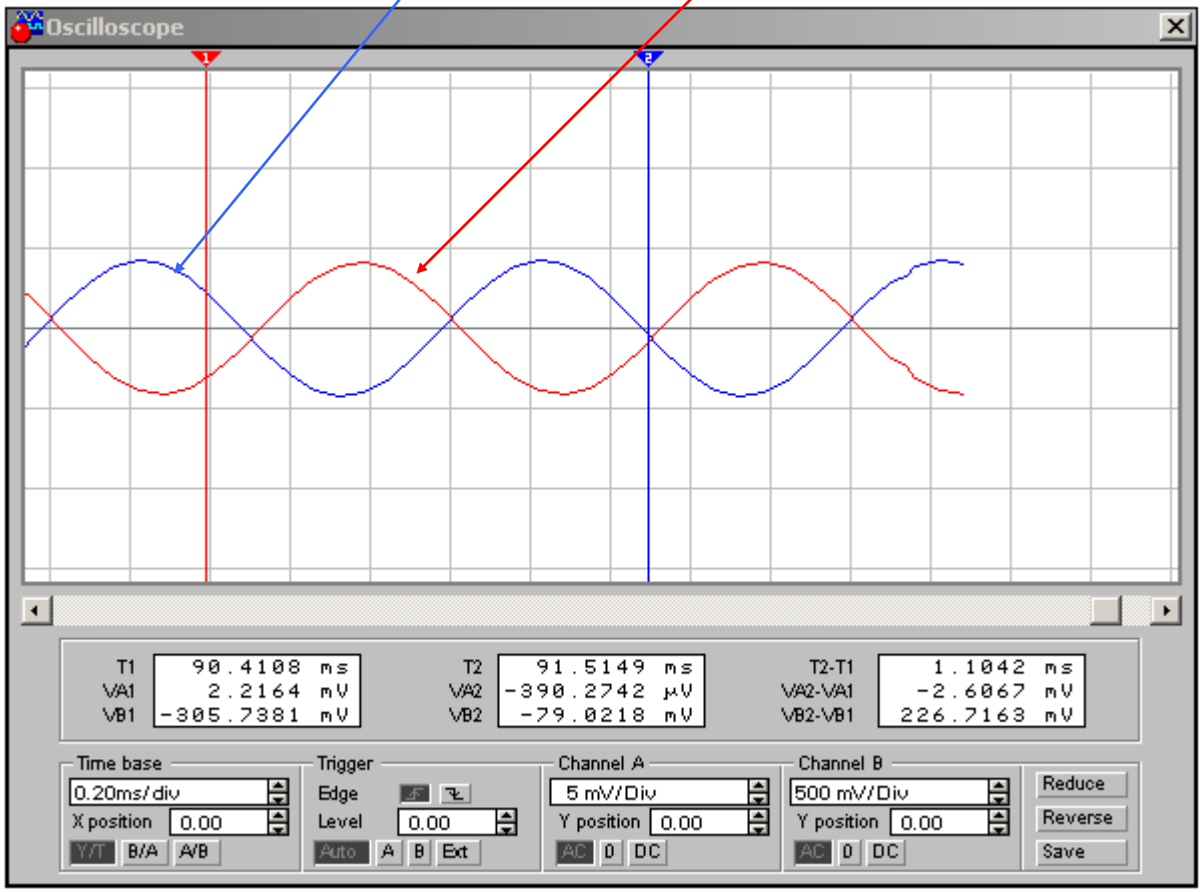
$$\frac{v_{out}}{v_{in}} = -\frac{R2}{R1}\left(1+\frac{R4}{R2}+\frac{R4}{R3}\right) = -\frac{1}{1}\left(1+\frac{1}{1}+\frac{1}{0.01}\right) = -1(1+1+100) = -102$$

This satisfies the required gain to within 10%



Input, channel A

Output, channel B



Output is on 500mV/div
Scale whereas
Input is on 5mV/div
Scale so amplification
Is by a factor -100 V/V
As we can still see
The sinusoids
Are 180 degrees out of phase

The Operational Amplifier

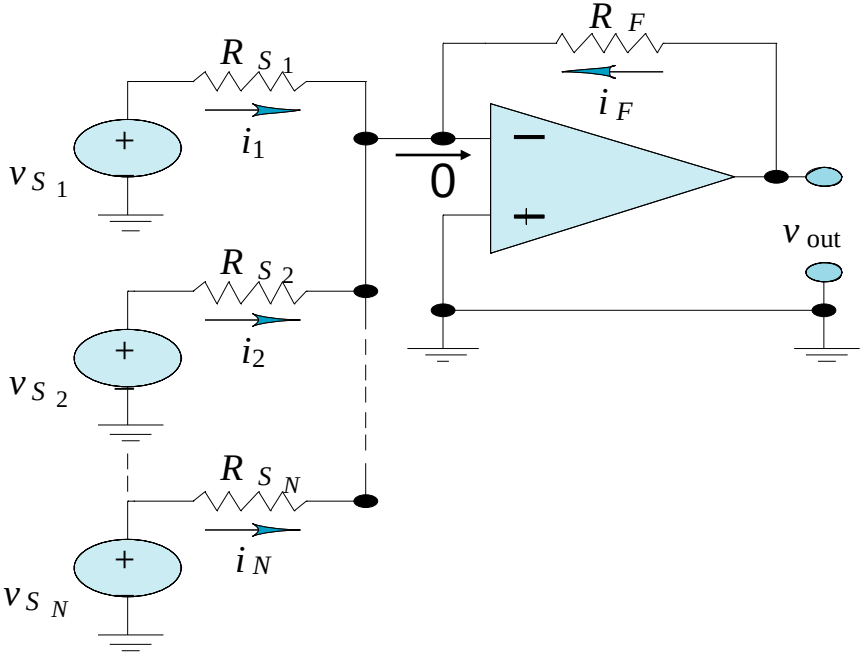
The Summing Amplifier

Consider this circuit where we
Have multiple input signals
With multiple input resistors

Each voltage source 'sees'
An input resistance equal to
The value of the input resistor
For that 'leg'

That is v_{s1} sees an input resistance R_{S1}

and v_{s2} sees an input resistance R_{S2}



We want to find an expression for the output
Voltage in terms of the individual input voltages!

To do this we will apply KCL at the –ve terminal of the op-amp, ie:

$$i_1 + i_2 + \ldots + i_N - 0 + i_F = 0$$

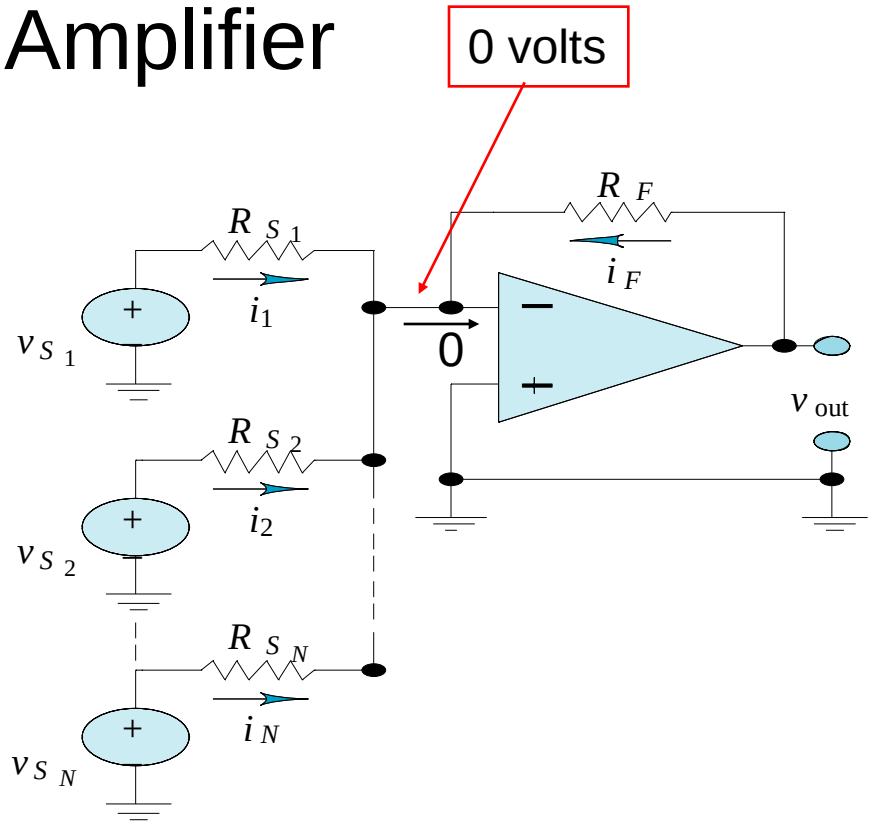
Since Ideal, zero current into –ve terminal

The Operational Amplifier

The Summing Amplifier

Now the virtual ground forces the –ve Terminal to a 0 V potential.

We use Ohms Law to find the Input currents:



$$i_1 = \frac{v_{S1} - 0}{R_{S1}} = \frac{v_{S1}}{R_{S1}}$$

$$i_2 = \frac{v_{S2} - 0}{R_{S2}} = \frac{v_{S2}}{R_{S2}}$$

$$\vdots$$

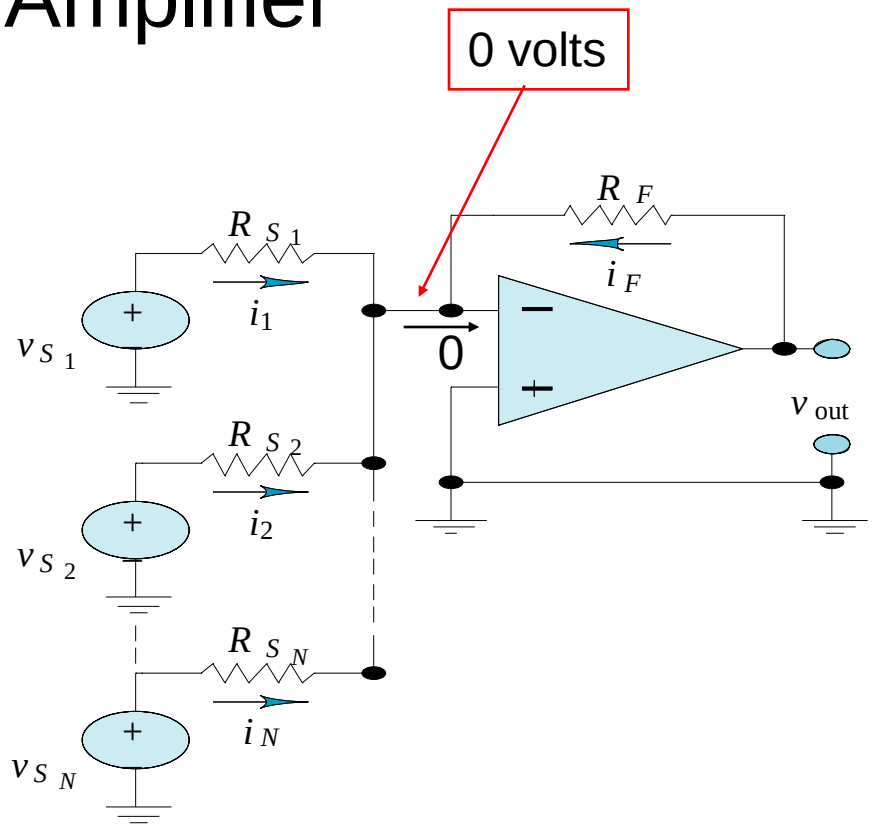
$$i_N = \frac{v_{SN} - 0}{R_{SN}} = \frac{v_{SN}}{R_{SN}}$$

KCL ⇒ $$\frac{v_{S1}}{R_{S1}} + \frac{v_{S2}}{R_{S2}} + \cdots + \frac{v_{SN}}{R_{SN}} + i_F = 0$$

The Operational Amplifier
The Summing Amplifier

We can use the same principle
To calculate the current in R_F:

$$i_F = \frac{v_{out} - 0}{R_F} = \frac{v_{out}}{R_F}$$



So subbing into KCL equation:

$$\frac{v_{S1}}{R_{S1}} + \frac{v_{S2}}{R_{S2}} + \cdots + \frac{v_{SN}}{R_{SN}} + \frac{v_{out}}{R_F} = 0$$

Rearranging:

$$v_{out} = -R_F \cdot \left(\frac{v_{S1}}{R_{S1}} + \frac{v_{S2}}{R_{S2}} + \cdots + \frac{v_{SN}}{R_{SN}} \right)$$

If we allow all the input resistors to be the same ie: $R_{S1} = R_{S2} = \cdots = R_{SN} = R_S$

Then:

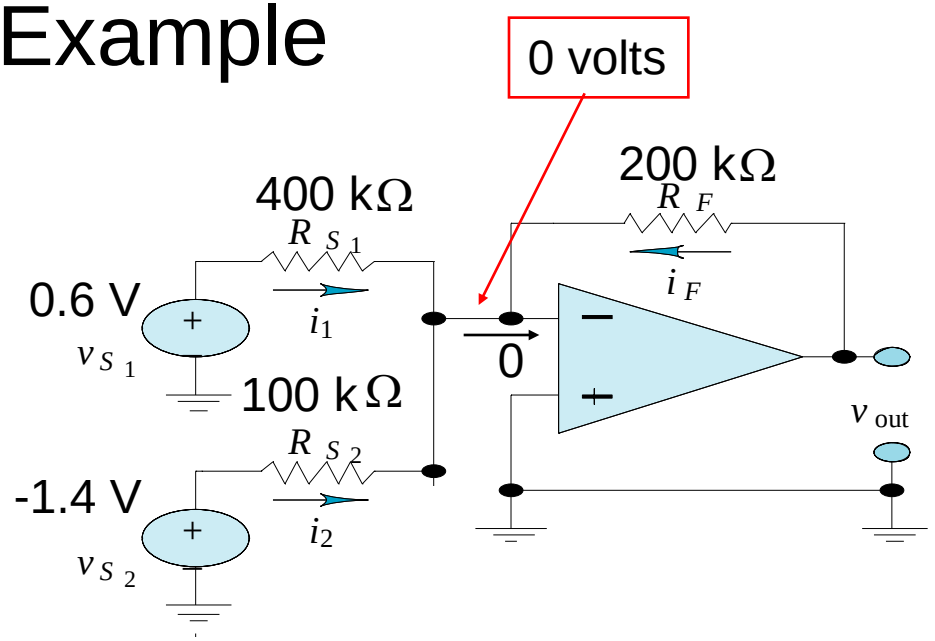
$$v_{out} = -\frac{R_F}{R_S}\left(v_{S1} + v_{S2} + \cdots + v_{SN}\right)$$

That is the SUM!

The Operational Amplifier

The Summing Amplifier: Example

If v_{s1}=+0.6 volts and v_{s2} = -1.4 volts, With R_{S1} = 400kΩ and R_{S2}= 100kΩ, And R_F=200kΩ, determine the output Voltage.



Answer:

$$v_{out} = -R_F \cdot \left(\frac{v_{S1}}{R_{S1}} + \frac{v_{S2}}{R_{S2}} \right)$$

Subbing values:

$$v_{out} = -(200 \quad k\Omega) \cdot \left(\frac{0.6 \quad volts}{400 \quad k\Omega} + \frac{-1.4 \quad volts}{100 \quad k\Omega} \right)$$

$$= -\left(\frac{200}{100} \right) \cdot \left(\frac{6}{40} - \frac{7 \times 8}{5 \times 8} \right) = -2 \cdot \left(-\frac{50}{40} \right) = +2.5 \quad volts$$

The Operational Amplifier

The Non-Inverting Amplifier

We can also put the op-amp in an non-inverting configuration which has Infinite input resistance looking into the +ve terminal and the input will be Inphase with the output

We want to find an expression for v_{out}:

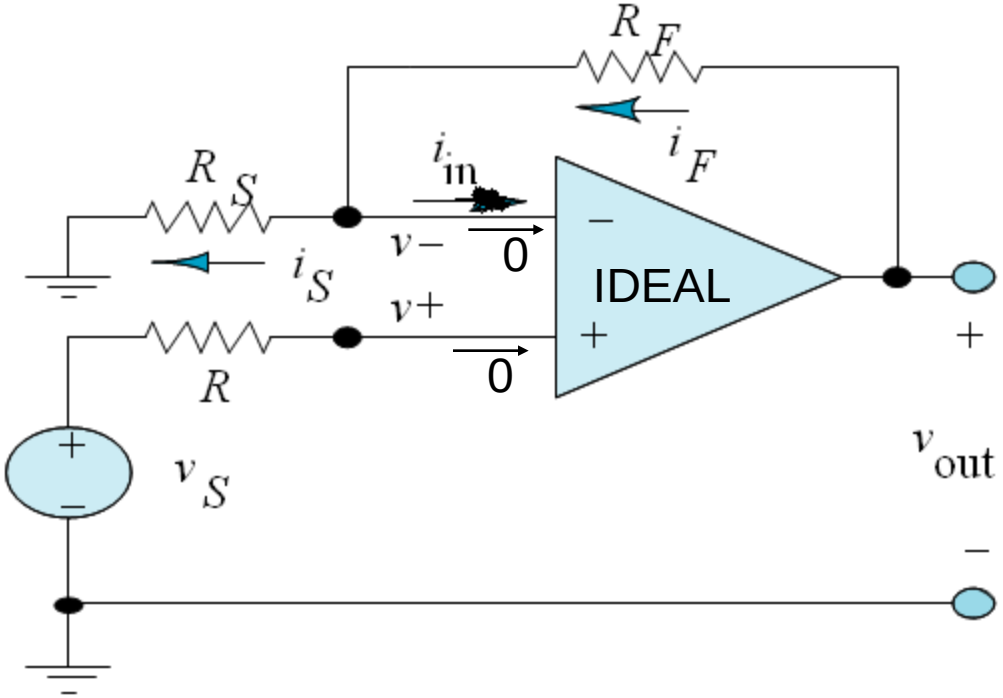
Since zero current flows into the –ve terminal
We can write:

$$i_S = i_F$$

And the virtual short circuit
Means that: $v_S = v^+ = v^-$

So we can use Ohms Law:

$$i_S = \frac{v_S}{R_S}$$



The Operational Amplifier

The Non-Inverting Amplifier

Thus we can write using KVL: $v_{out} - i_F R_F - i_S R_S = 0$

Subbing for i_s and rearranging:

$$v_{out} = i_S \left(R_F + R_S \right) \quad \text{Since} \quad i_S = i_F$$

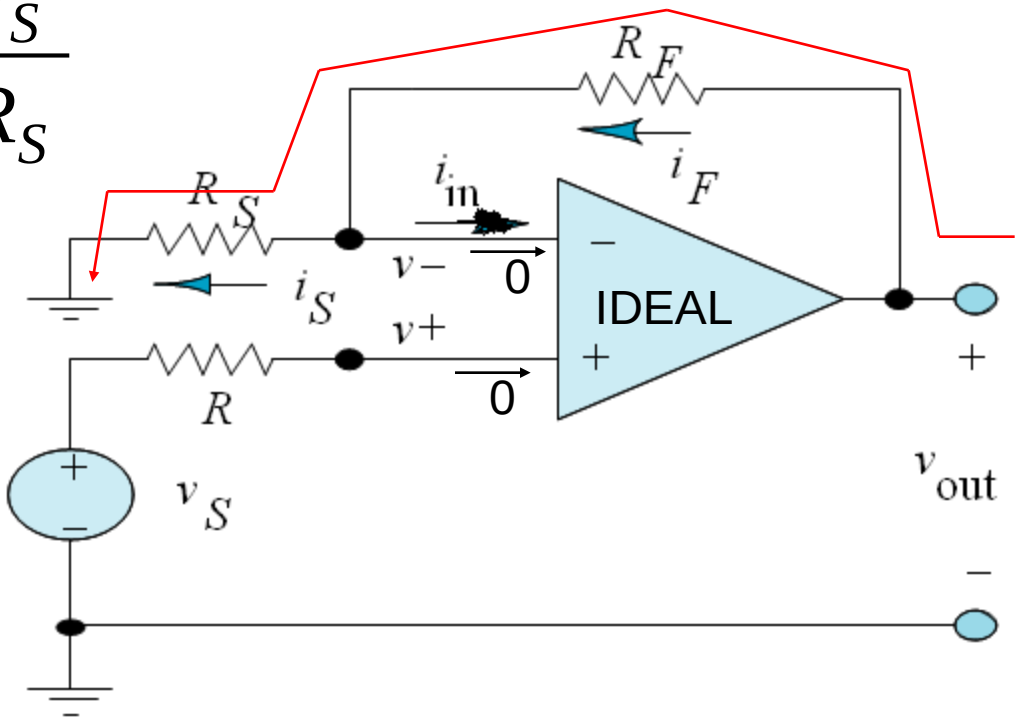
Which means that:

$$i_S = \frac{v_{out}}{\left(R_F + R_S \right)} = \frac{v_S}{R_S}$$

Thus:

$$v_{out} = \frac{v_S}{R_S}\left(R_F + R_S \right)$$

$$= \left(1 + \frac{R_F}{R_S} \right) \cdot v_S$$



The Operational Amplifier Example

If the input voltage, v_S, is 2 volts DC and the supply rails are +15 volts and -15 volts respectively (not Shown) what is the output Voltage v_{out} equal to when R_S=10 kΩ and R_F=20 kΩ?

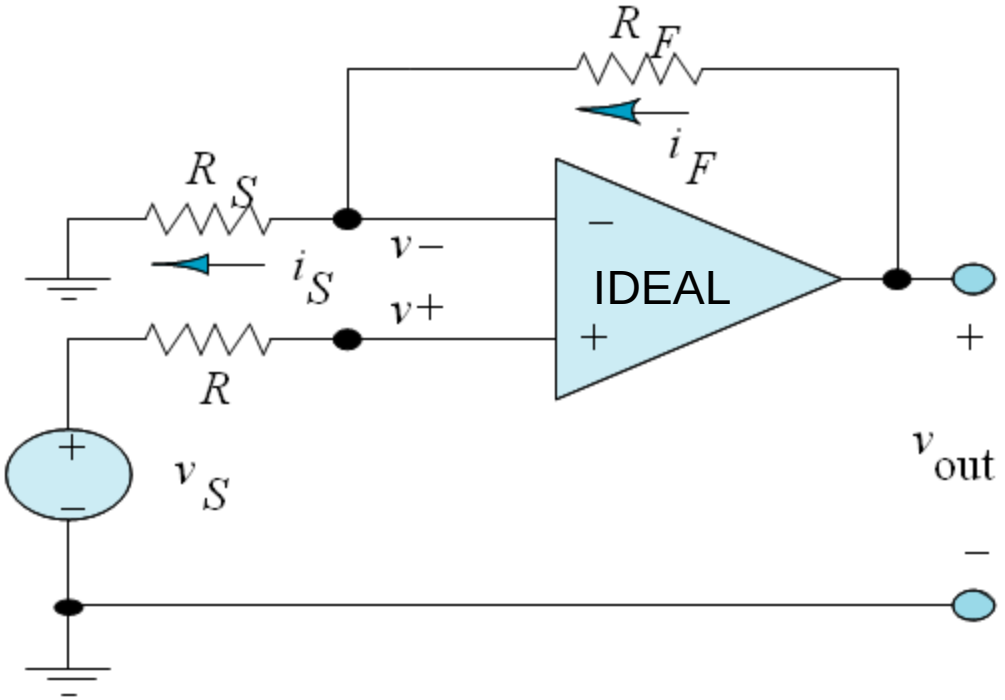
Answer:

$$v_{out} = \left(1 + \frac{R_F}{R_S}\right) \cdot v_S$$

$$= \left(1 + \frac{20}{10}\right) \cdot (2)$$

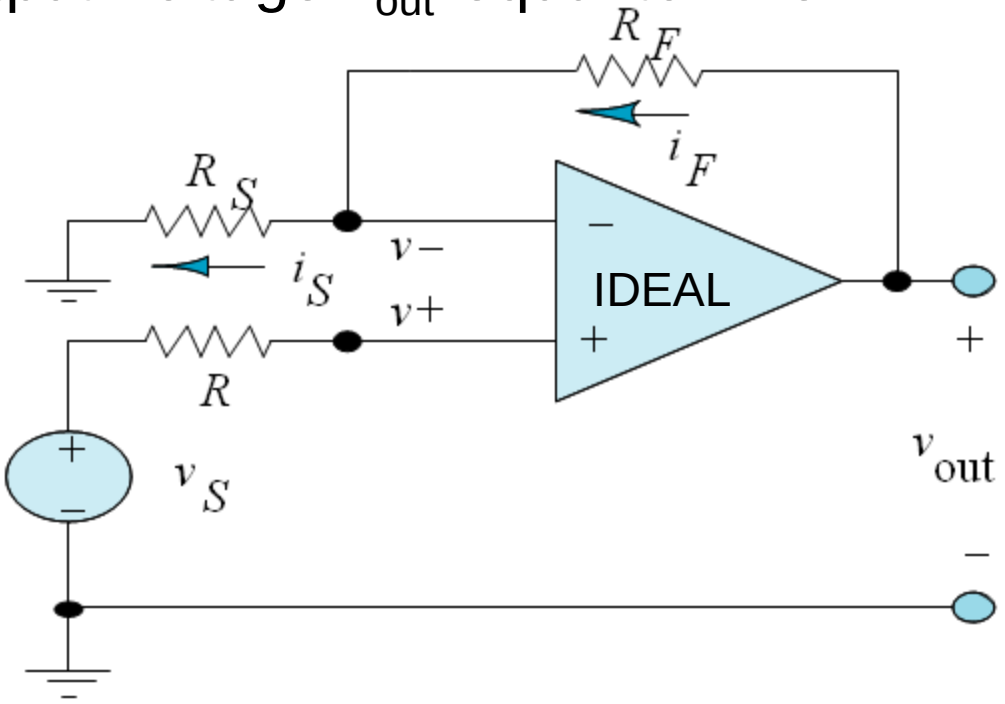
$$= (3) \cdot (2)$$

$$= +6 \quad volts$$



The Operational Amplifier Example

If the input voltage, v_S, is $\left(3\sqrt{2}\right)\sin\left(2000\times\pi\times t\right)$ volts and the supply rails are +15 volts and -15 volts DC respectively (not shown) what is the output Voltage v_{out} equal to when R_S=10 kΩ and R_F=15 kΩ?



Answer:

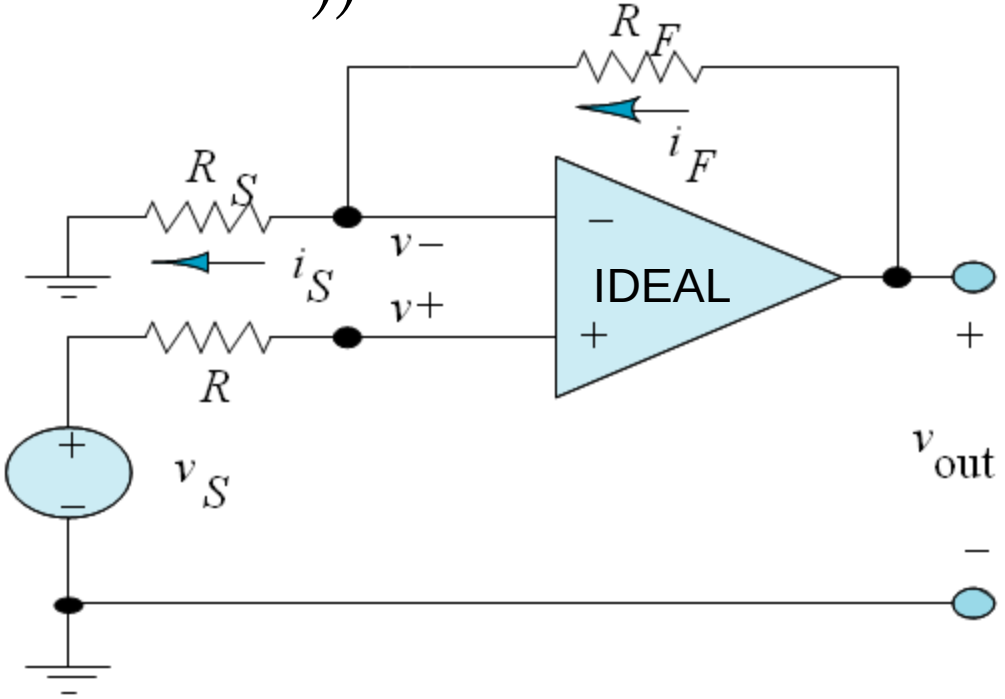
$$v_{out} = \left(1+\frac{R_F}{R_S}\right)\cdot v_S$$

$$= \left(1+\frac{15}{10}\right)\cdot\left(3\sqrt{2}\sin\left(2000\times\pi\times t\right)\right)$$

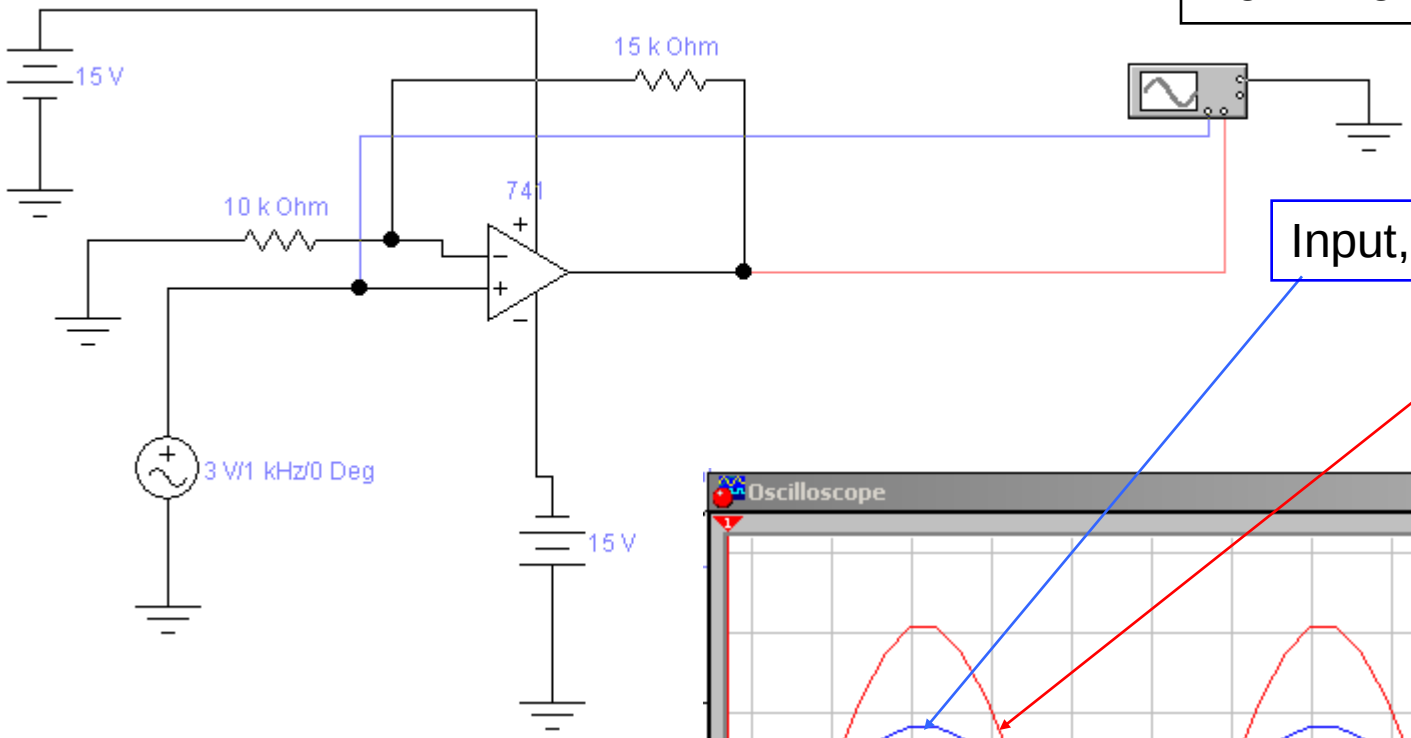
The Operational Amplifier Example

$$v_{out} = \left(\frac{5}{2}\right) \cdot \left(3\sqrt{2}\sin\left(2000 \times \pi \times t\right)\right)$$

$$= \left(\frac{15}{\sqrt{2}}\right) \cdot \left(\sin\left(2000 \times \pi \times t\right)\right)$$

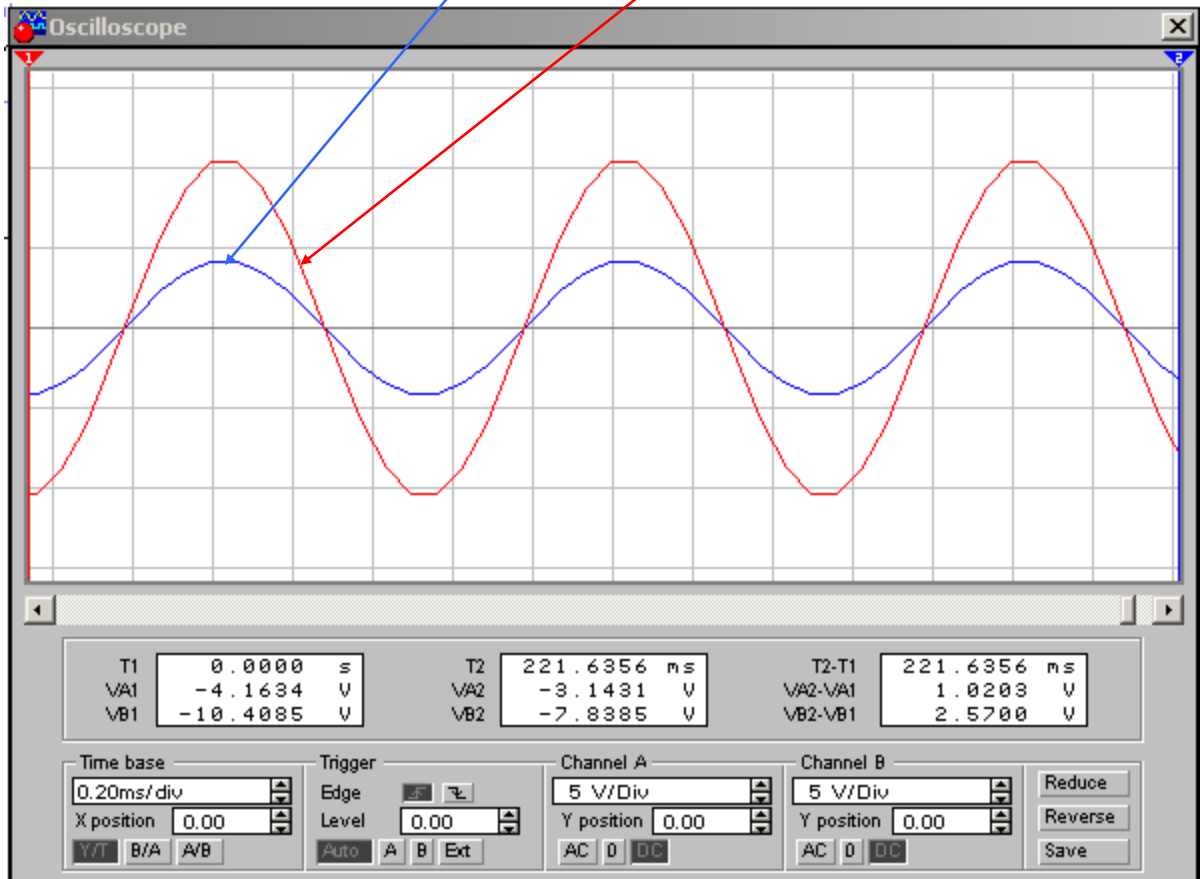


Non-Inverting Op-Amp



Input, channel A

Output, channel B



Clearly, input and
Output are in-phase
And the output
Is 2.5 times the input

The Operational Amplifier

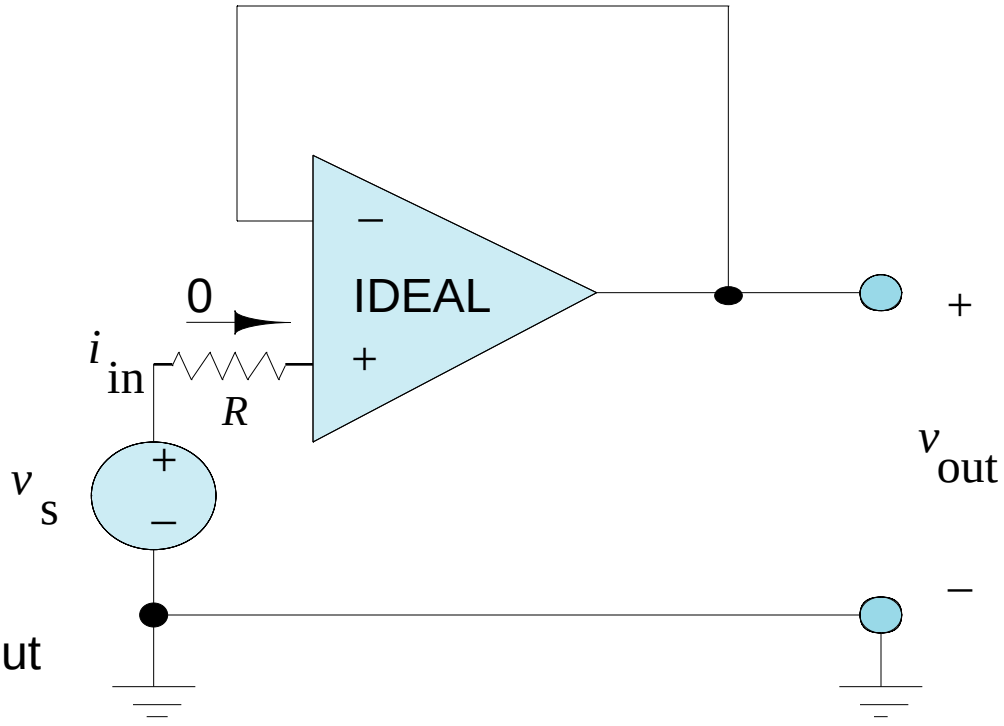
The Voltage Follower or Buffer

Another configuration close to the non-inverting configuration is the Voltage follower:

Since the op-amp is ideal
There is zero current into
The +ve terminal and no
Need for R, which can be
Modeled as the internal
Resistance of the source, v_s

The virtual short
Circuit between the
+ve and –ve terminals
Means that:

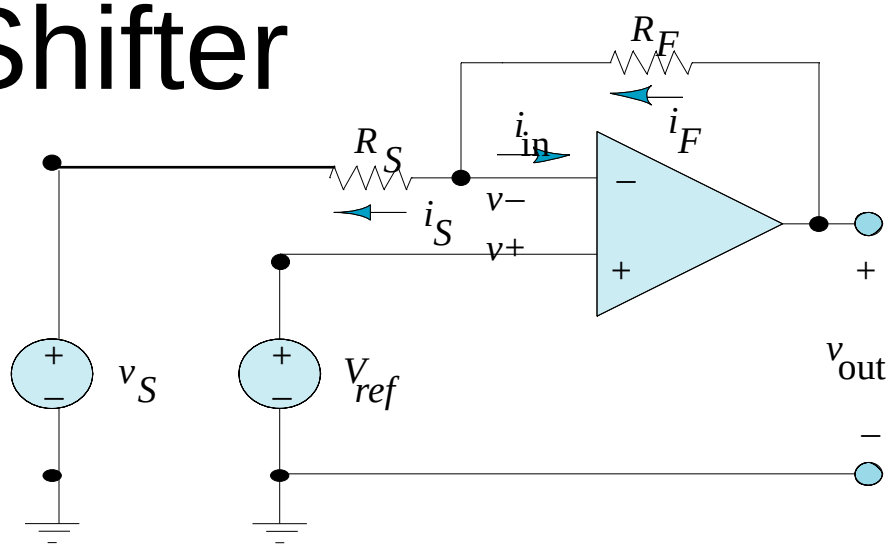
$$v_{out} = v_S$$



And we have a high resistance
Input with low resistance output
With the same voltage at the output
as the source
- Hence the term voltage follower!

Level Shifter

This provides a method to
Shift the DC level of a circuit
Needed , for example, to remove DC!



We want to find v_{out}:

First suppress v_s:

$$v_S = 0 \Rightarrow v_{out} = \left(1 + \frac{R_F}{R_S}\right) V_{ref}$$

Then suppress V_{ref}:

$$V_{ref} = 0 \Rightarrow v_{out} = -\frac{R_F}{R_S} v_S$$

Now using Superposition we add them together to get:

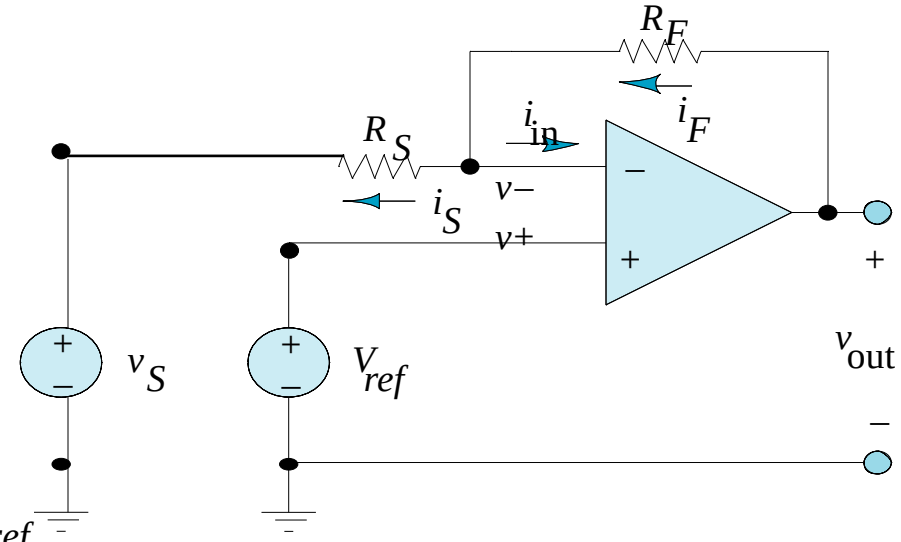
$$v_{out} = -\frac{R_F}{R_S} v_S + \left(1 + \frac{R_F}{R_S}\right) V_{ref}$$

Example

Given: $v_S = 1.8 + 0.1\cos(\omega t); \quad R_F = 220k \quad \Omega; \; R_S = 10k \quad \Omega;$

Find: V_{ref} to remove the DC bias

Solution:



$$v_{out} = -\frac{R_F}{R_S}\left[1.8 + 0.1\cos(\omega t)\right] + \left(1 + \frac{R_F}{R_S}\right)V_{ref}$$

$$= -\frac{R_F}{R_S}0.1\cos(\omega t) - \frac{R_F}{R_S}(1.8) + \left(1 + \frac{R_F}{R_S}\right)V_{ref}$$

Removing the sinusoid and setting the DC component to equal zero:

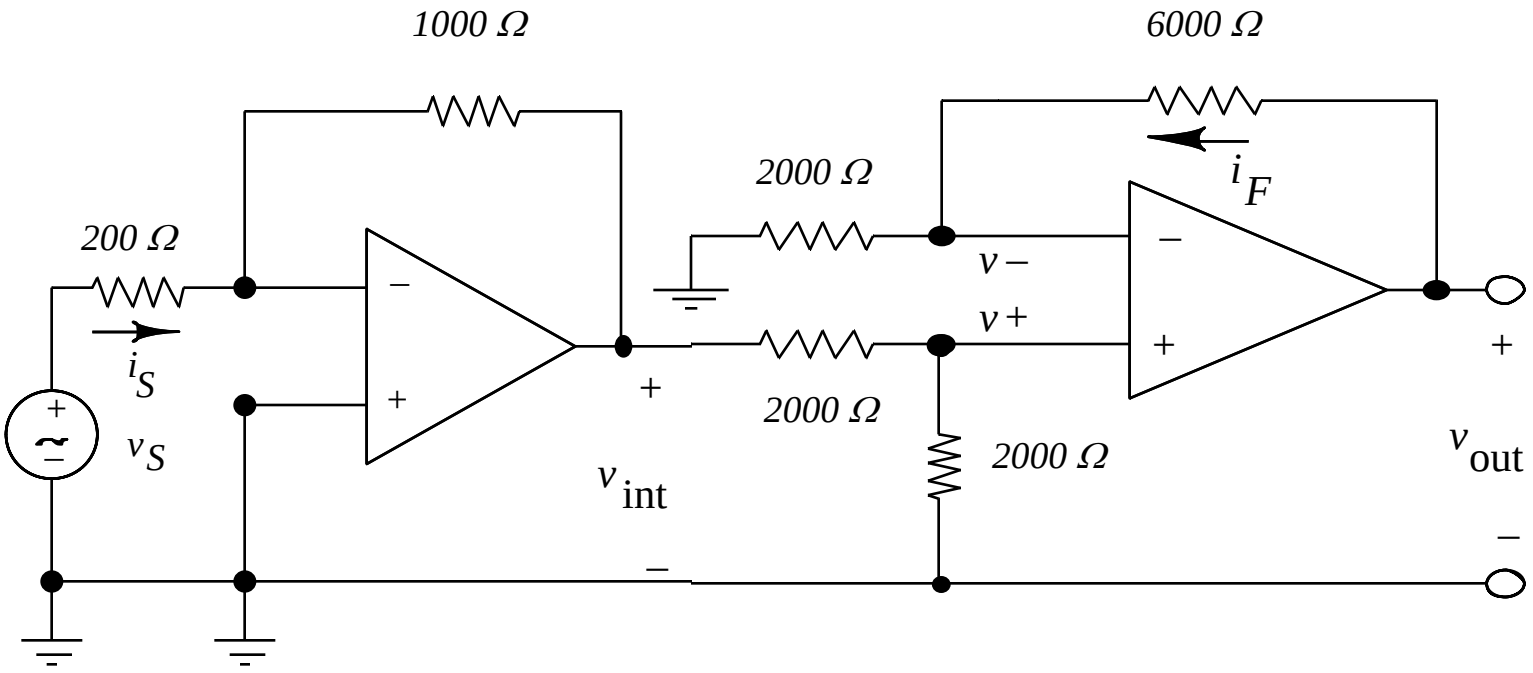
$$-\frac{R_F}{R_S}(1.8) + \left(1 + \frac{R_F}{R_S}\right)V_{ref} = 0 \quad \Rightarrow \quad V_{ref} = 1.72 \quad V$$

Example

$v_s = 100\sin 100t$

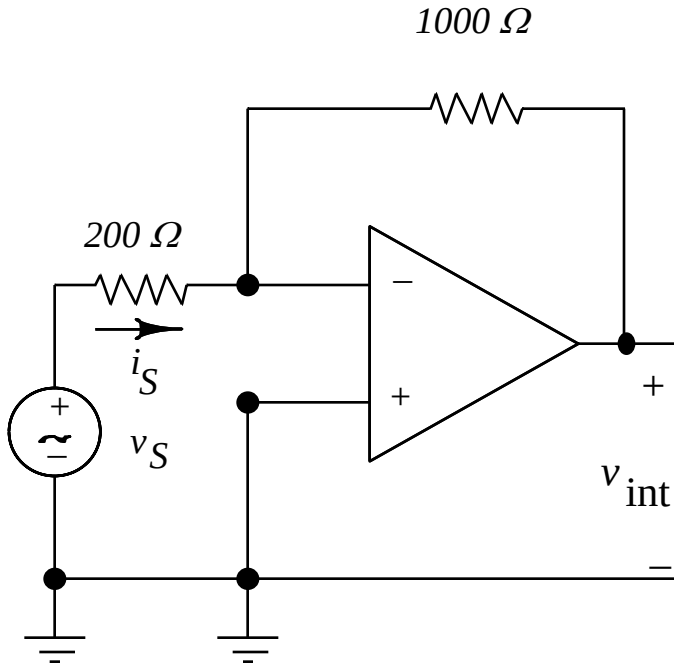
Determine the voltage v_{int} and v_{out}.

Determine the current i_s and i_F.



Solution

- Since this is a cascaded amplifier circuit, treat each stage as individual (just as we did with the Voltage follower used as a BUFFER)
- The first stage is an inverting amplifier:



Thus: $v_{\text{int}} = -\frac{R_F}{R_S} v_S = -\frac{1000}{200} v_S$

$= -5 v_S = -5 \times 100 \sin(100t)$

$= -500 \sin(100t)$

The current i_S is then:

$$i_S = \frac{v_S}{R_S} = \frac{100 \sin(100t)}{200} = 0.5 \sin(100t)$$

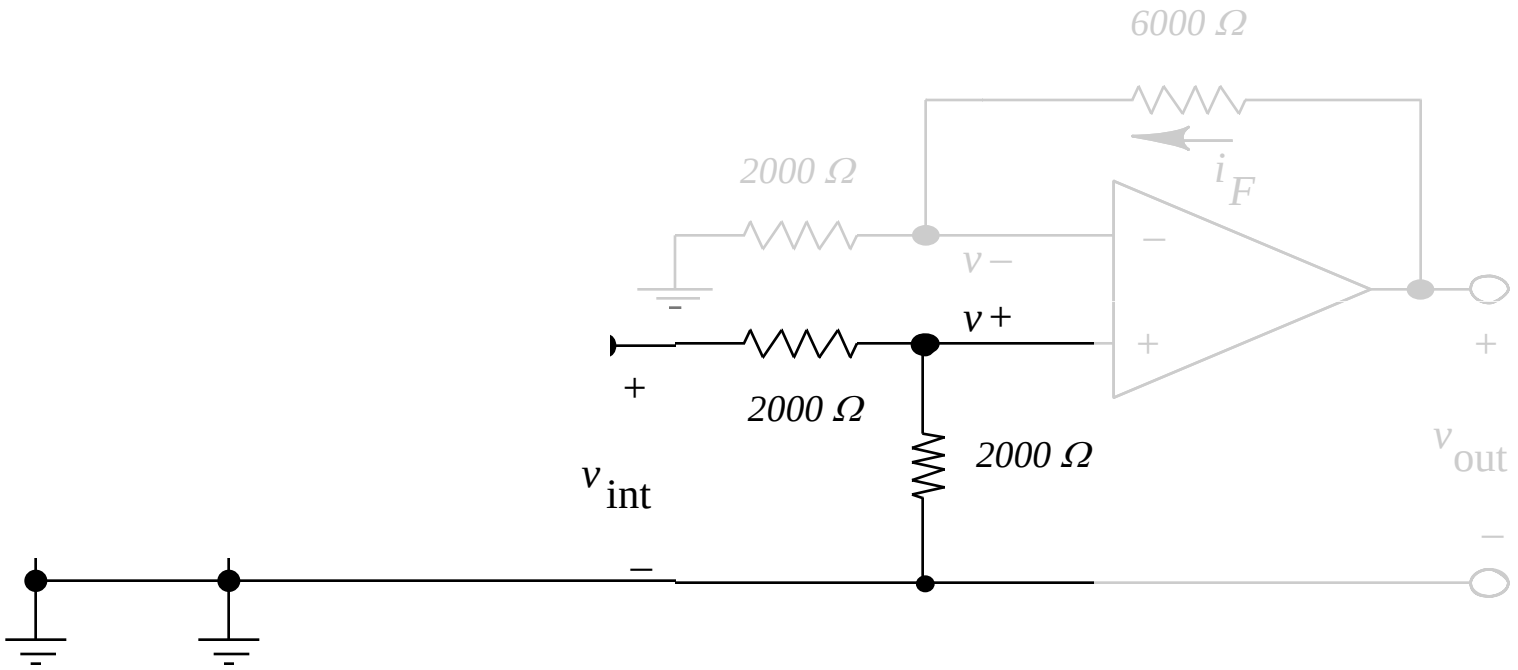
Due to the virtual ground

Solution

The next stage is a resistor network, basically dividing the output of the Inverting amplifier by 2 and presenting it to the non-inverting amplifier:

Here we have:

$$v^+ = \left(\frac{2000}{4000}\right) v_{\text{int}} = 0.5 \times v_{\text{int}} = -250 \sin(100t)$$

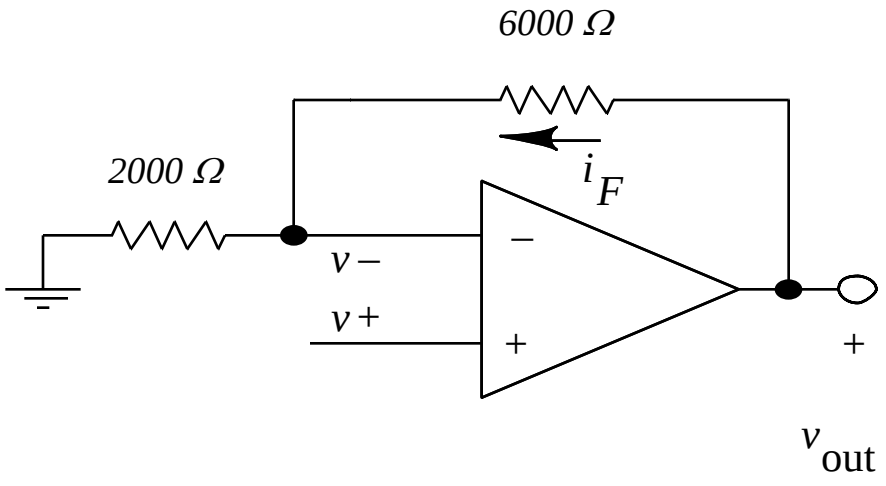


Solution

The next stage is the non-inverting amplifier where:

$$v_{out} = \left(1 + \frac{R_F}{R_S}\right) v^+ = \left(1 + \frac{6000}{2000}\right) v^+ = 4v^+$$

$$= -1000 \sin(100t)$$

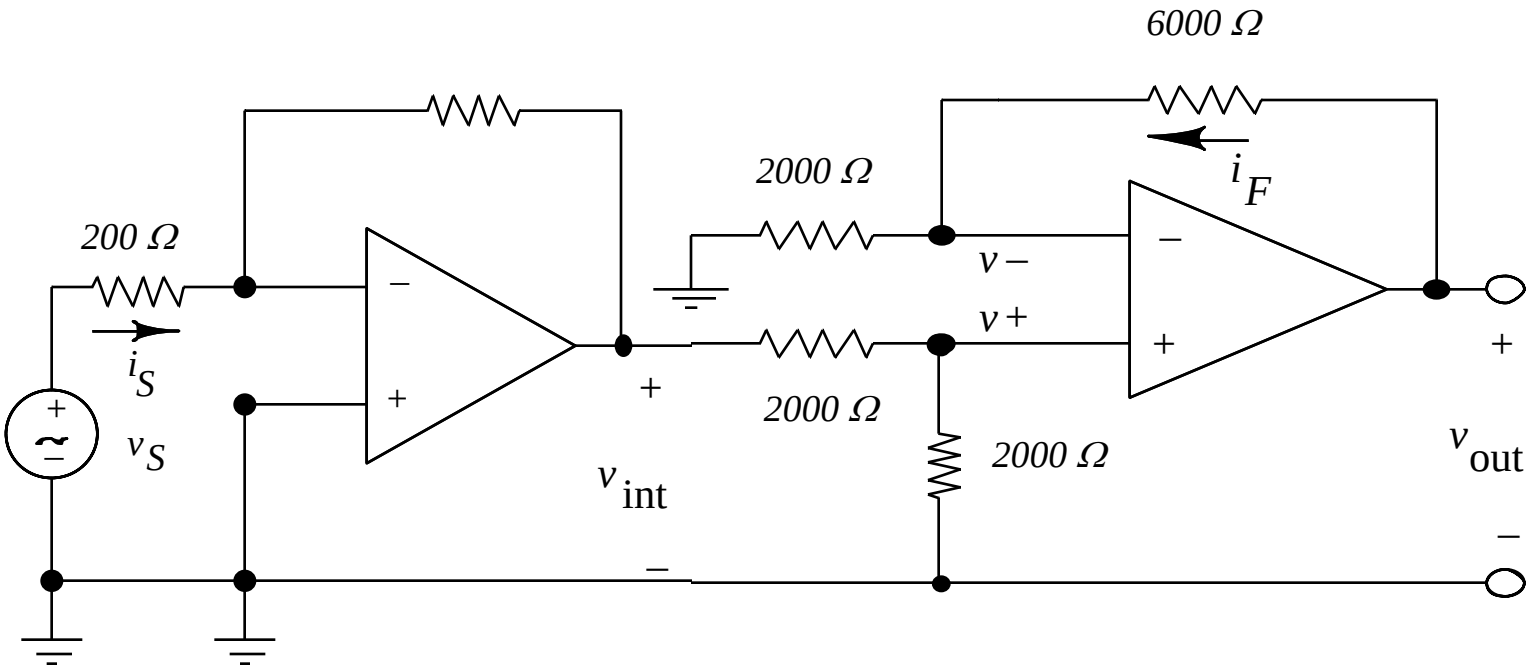


Solution

And we can then calculate i_F as:

$$i_F = \frac{v_{out} - v^-}{R_F} = \frac{v_{out} - v^+}{R_F} = \frac{-1000\sin(100t) - (-250\sin(100t))}{6000} = \frac{-750\sin(100t)}{6000}$$

$$= -0.125\sin(100t)$$

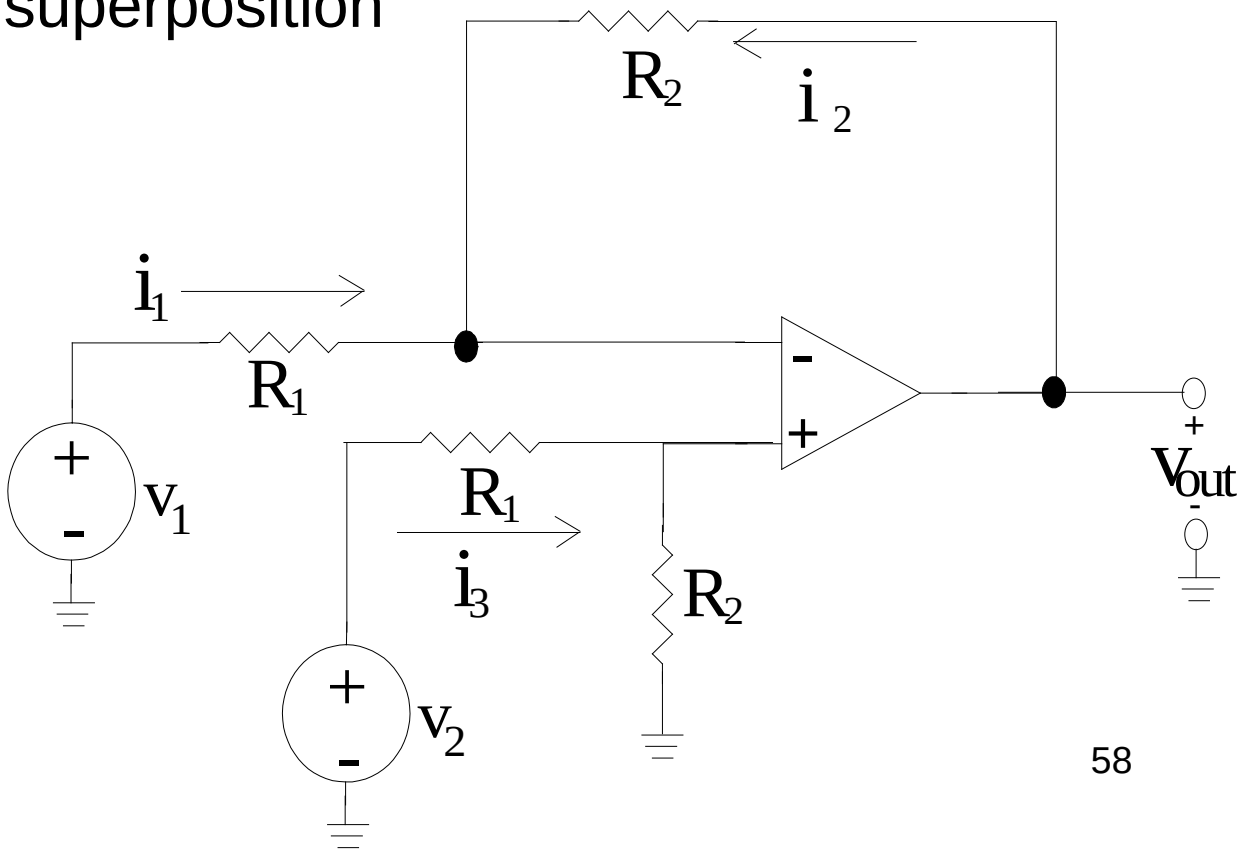


Differential Amplifier

This is a difference amplifier, it will amplify the difference between two voltage signals

We want to get an expression for v_{out}:

To do this we will use superposition

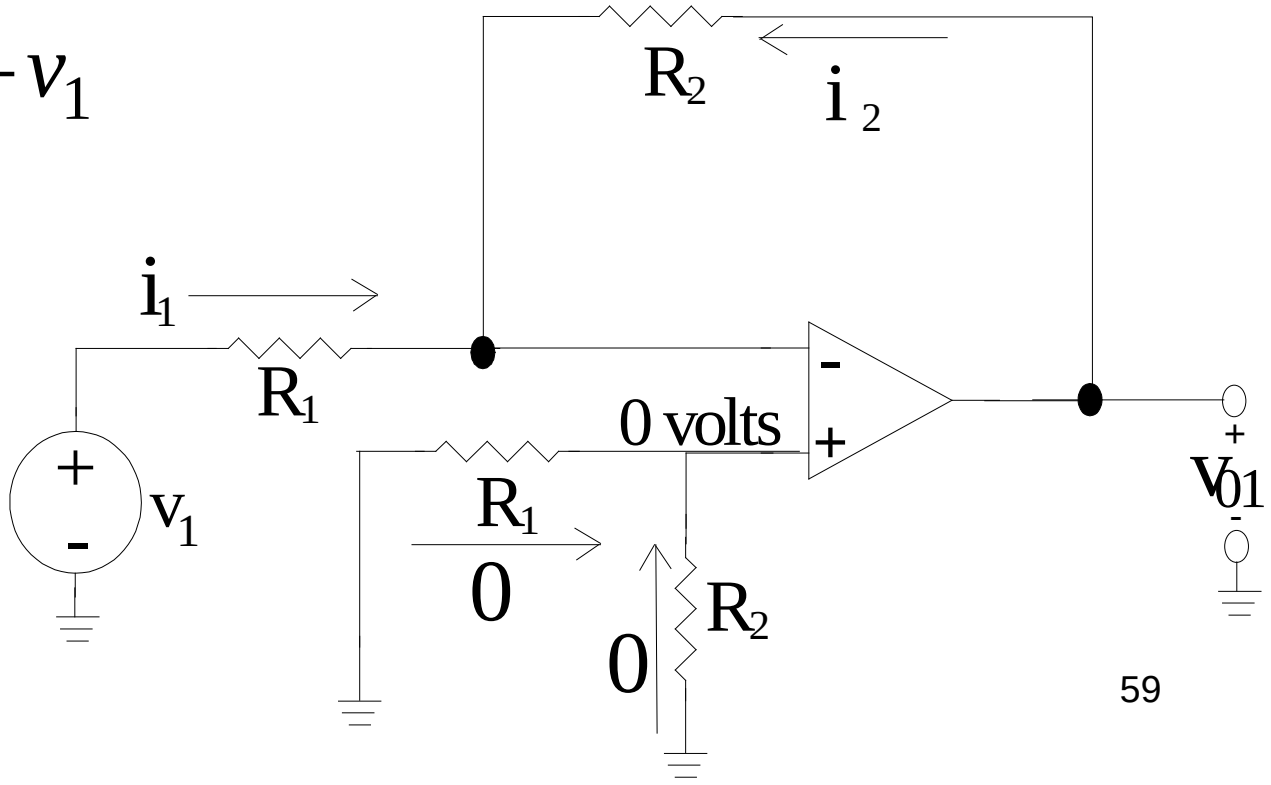


Differential Amplifier

First we suppress v_2 and calculate the output voltage v_{o1}:

This circuit is simply an inverting amplifier as no Current flows in the bottom two resistors so we Have a virtual ground, ie:

$$v_{o1} = -\frac{R_2}{R_1} v_1$$

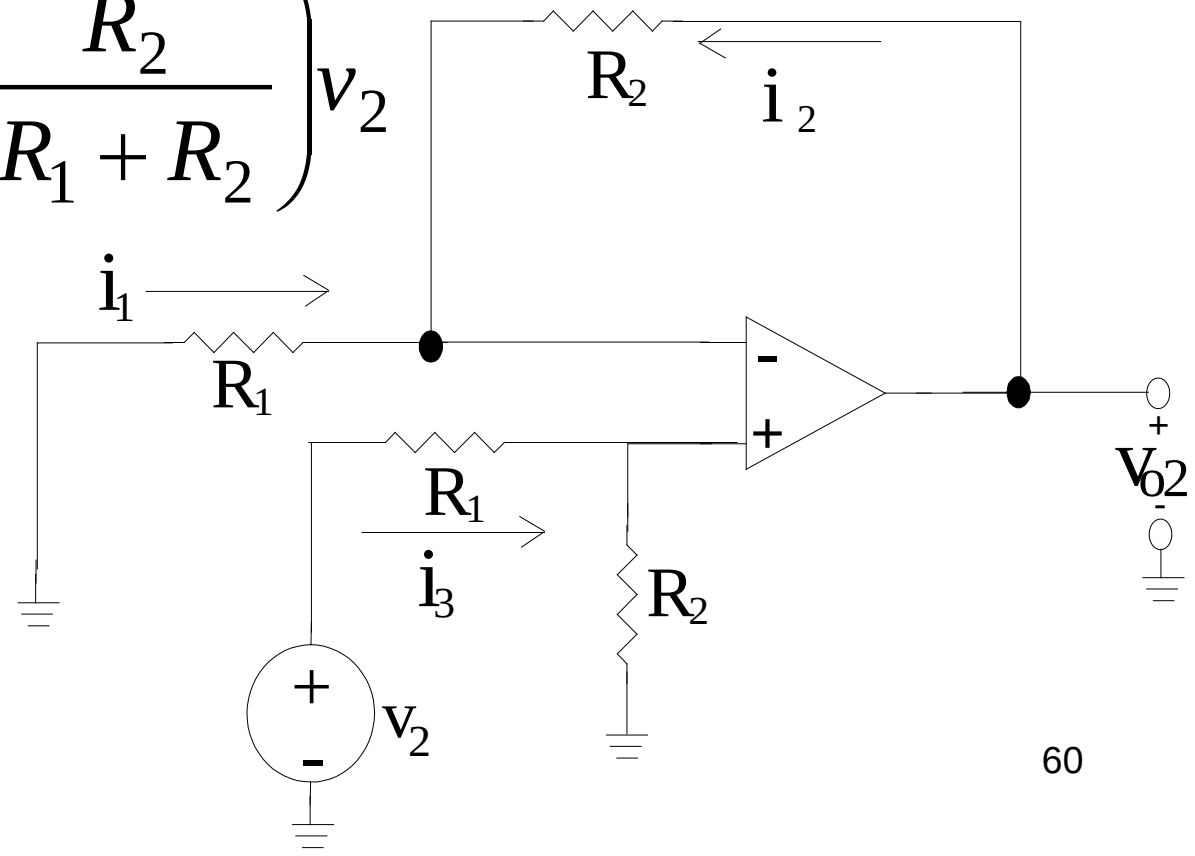


Differential Amplifier

Now we suppress v_1 and calculate the output voltage v_{o2}:

This circuit is simply an non-inverting amplifier with a Voltage divider on the input signal:

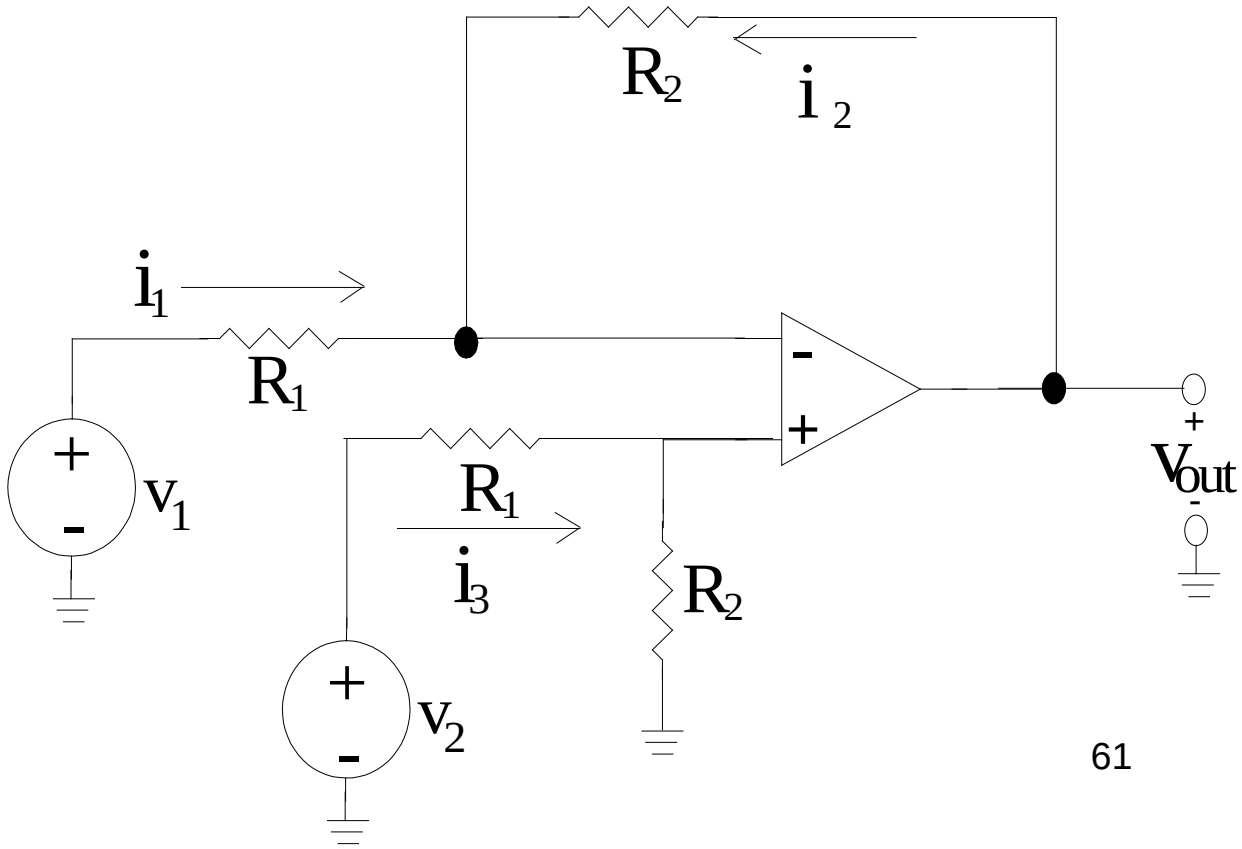
$$v_{o2} = \left(1 + \frac{R_2}{R_1}\right) \cdot \left(\frac{R_2}{R_1 + R_2}\right) v_2$$



Differential Amplifier

Adding v_{01} and v_{02} to get v_{out}:

$$v_{out} = v_{01} + v_{02} = -\frac{R_2}{R_1} v_1 + \left(1 + \frac{R_2}{R_1}\right) \cdot \left(\frac{R_2}{R_1 + R_2}\right) v_2$$



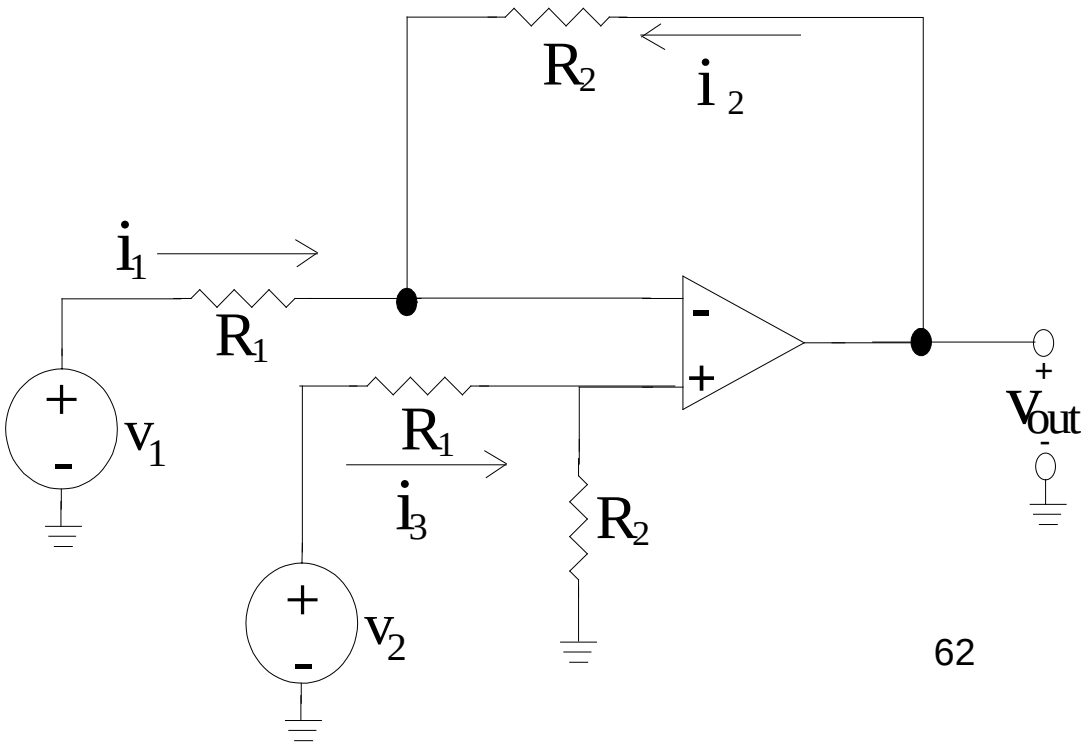
Differential Amplifier

Rearranging gives:

$$v_{out} = -\frac{R_2}{R_1}v_1 + \left(\frac{R_1 + R_2}{R_1}\right)\cdot\left(\frac{R_2}{R_1 + R_2}\right)v_2$$

$$= -\frac{R_2}{R_1}v_1 + \frac{R_2}{R_1}v_2$$

$$\therefore v_{out} = \frac{R_2}{R_1}(v_2 - v_1)$$

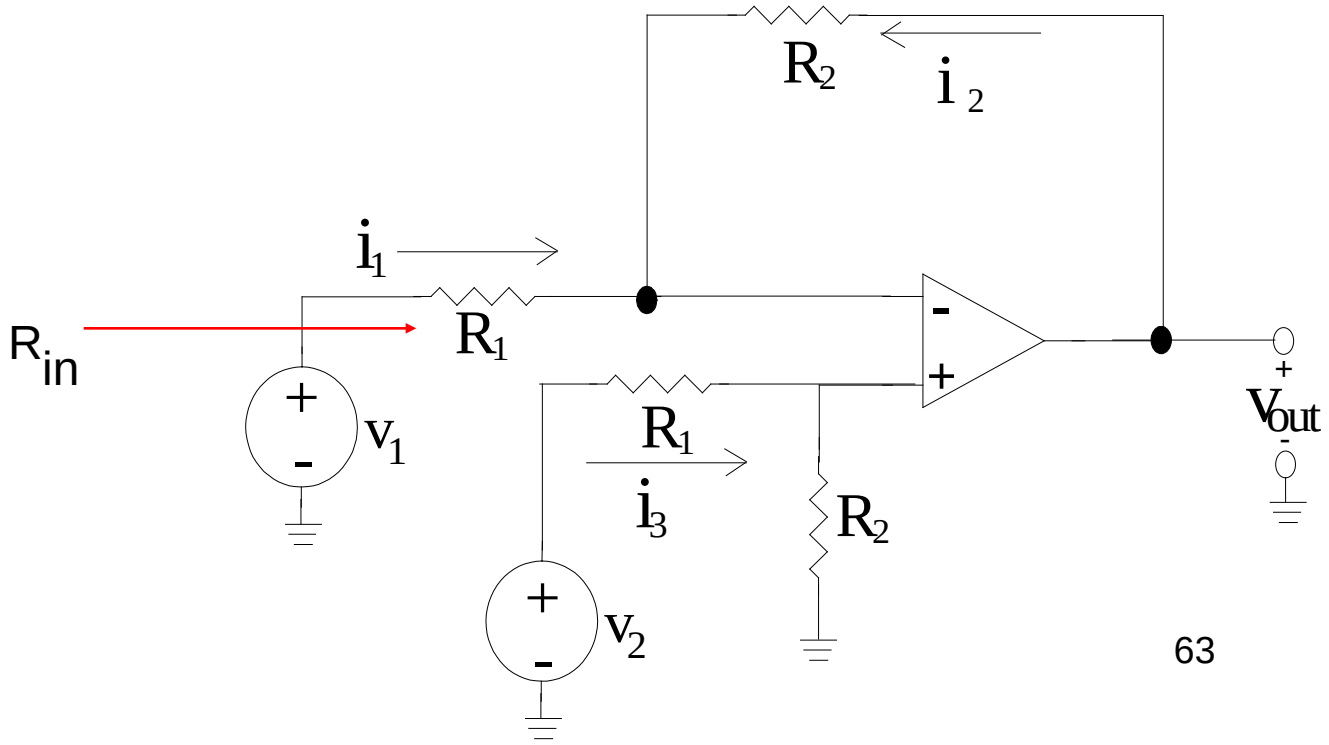


Which amplifiers the Difference voltage between v_2 and v_1!

Differential Amplifier

Input Differential Resistance

If we want to calculate the input resistance seen from a Differential signal connected between the difference Inputs v_1 and v_2, then we can draw an equivalent circuit And calculate the input differential resistance



Differential Amplifier

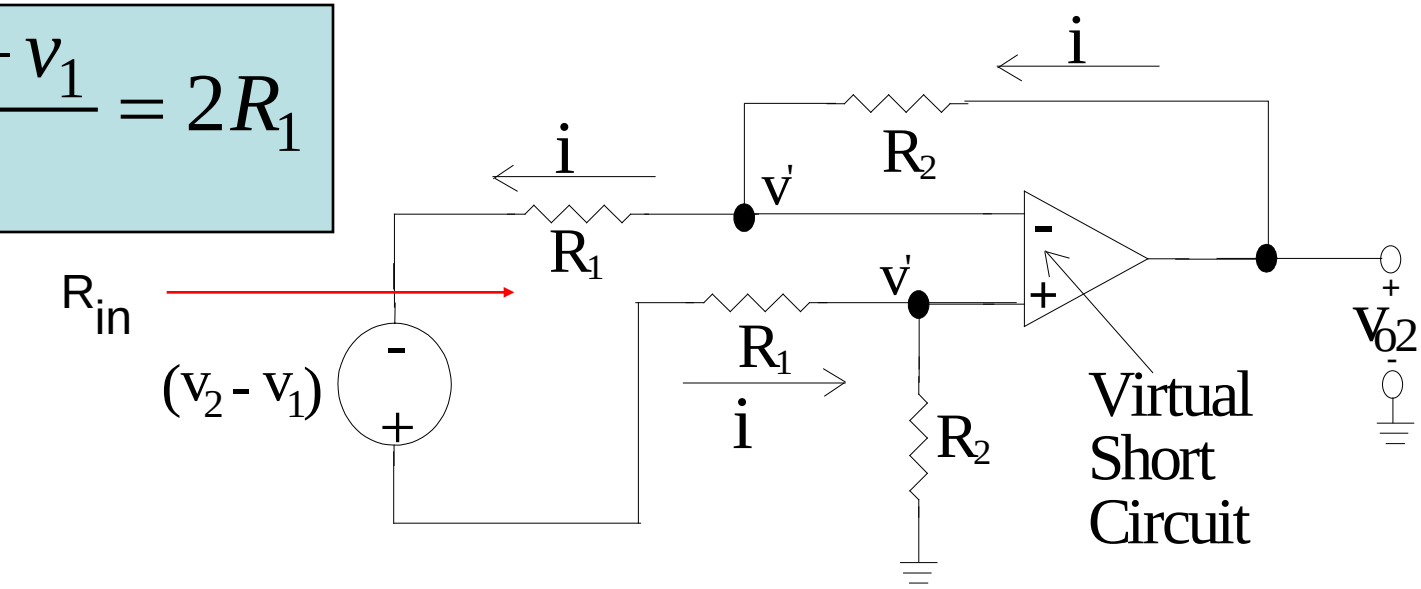
Input Differential Resistance

Using KVL on the input loop and noting that the Virtual short circuit causes the +ve and –ve Terminals to have the same voltage v':

$$v_2 - v_1 = iR_1 + 0 + iR_1$$

$$= 2iR_1$$

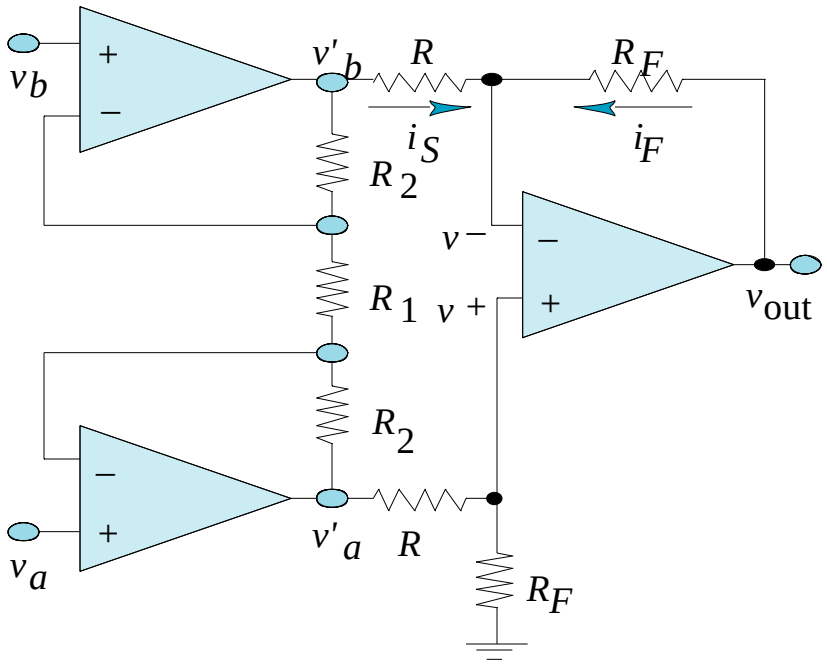
$$\therefore R_{in} \equiv \frac{v_2 - v_1}{i} = 2R_1$$



Instrumentation Amplifier

A alternate differential
Amplifier is called an
Instrumentation amplifier
And its advantage is
That it has infinite
Differential input resistance

Thus it does not ‘load’ the
Signal sources its connected
Too (draws no current)

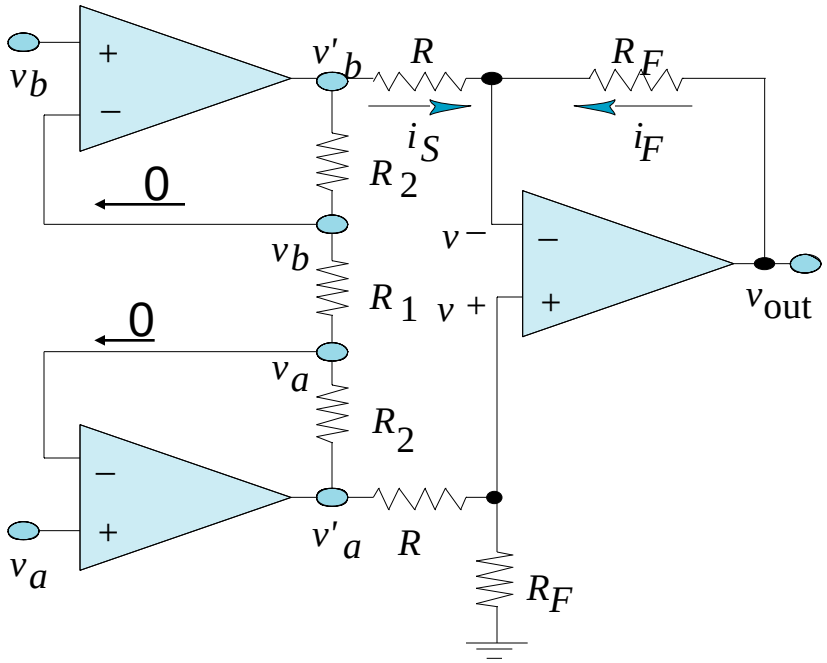


Instrumentation Amplifier

An analysis of the circuit
Would reveal that:

$$v_{out} = \frac{R_F}{R}\left(v_a^{'} - v_b^{'}\right)$$

Since output Stage is simply The Difference Amplifier we just Analysed!



also $$v_a^{'} = \left(1 + \frac{R_2}{R_1/2}\right)v_a$$

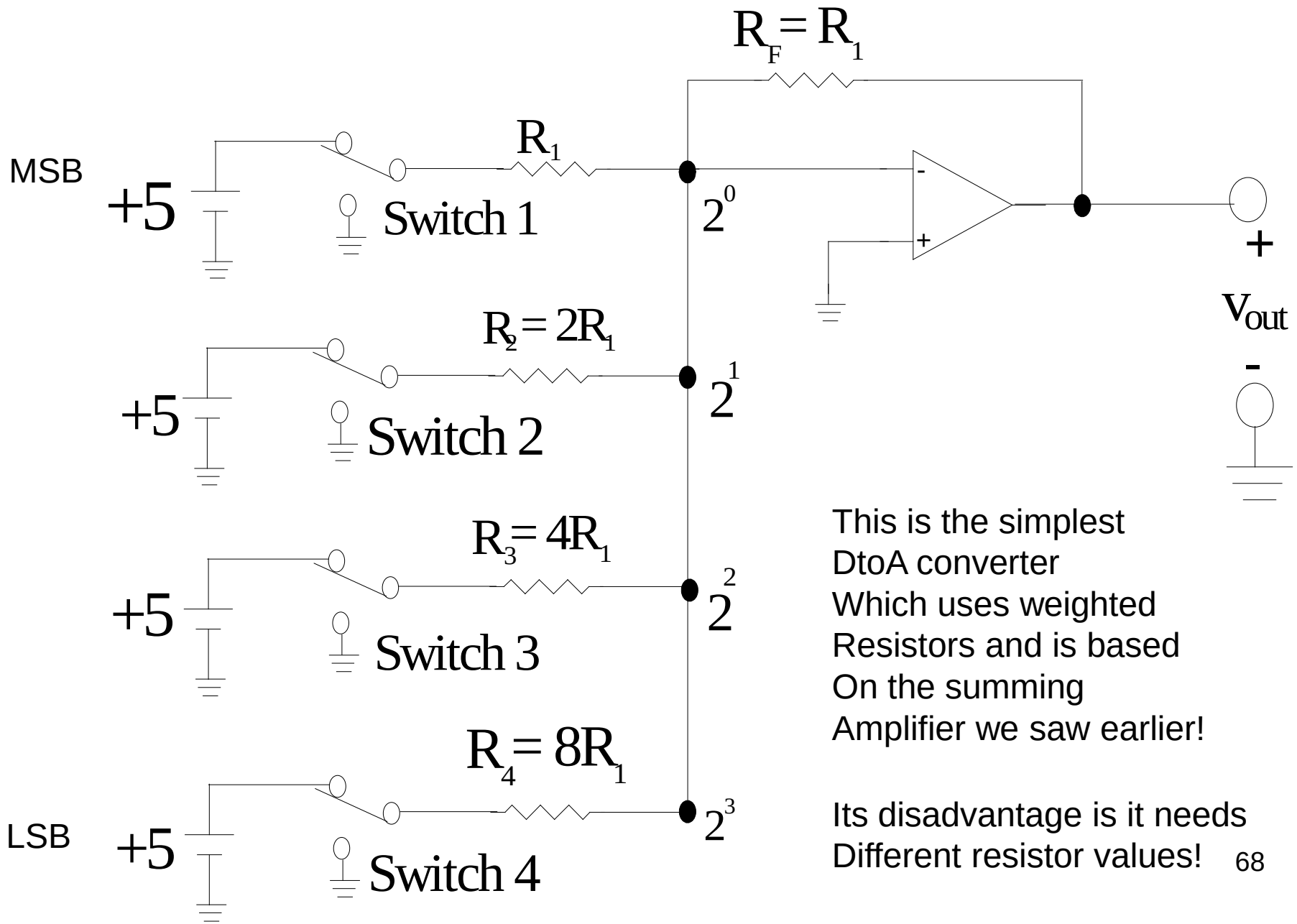
and $$v_b^{'} = \left(1 + \frac{R_2}{R_1/2}\right)v_b$$

$$\therefore v_{out} = \frac{R_F}{R}\left(1 + \frac{R_2}{R_1/2}\right)\left(v_a - v_b\right) = \frac{R_F}{R}\left(1 + \frac{2R_2}{R_1}\right)\left(v_a - v_b\right)$$

Digital to Analog Converters

- Our next topic will be digital circuits
- It should be of interest how we convert a digital signal to analog and vice-a-versa
- First we will consider some simple Digital to analog structures!
- We use D/A or DAC as abbreviations for these devices
- They are available in specialised ‘chips’ and also can be built in to DSP boards as well (eg Systems on a Chip (SOC))!

Digital to Analog Converters



This is the simplest
DtoA converter
Which uses weighted
Resistors and is based
On the summing
Amplifier we saw earlier!

Its disadvantage is it needs
Different resistor values!

Digital to Analog Converters

Here the switches are digital providing either 0V for ‘0’ and +5V for ‘1’

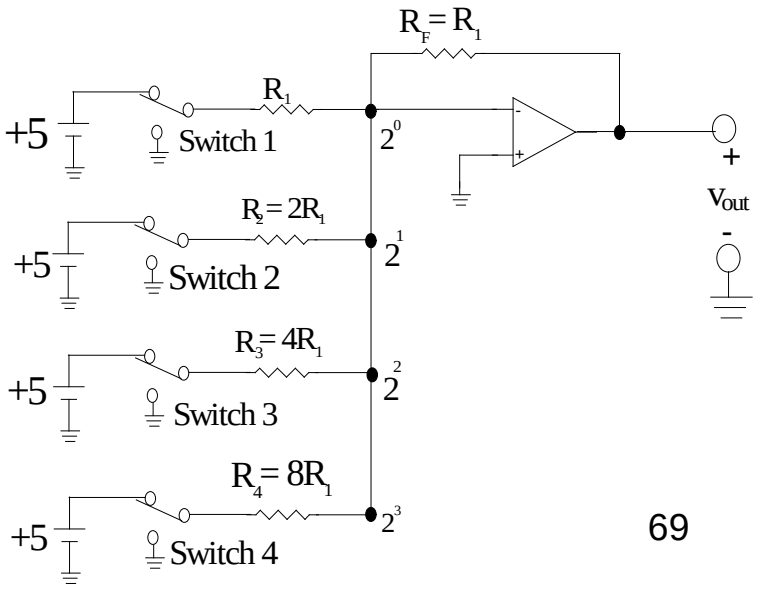
The output voltage is given by:

$$v_{out} = -R_F \cdot \left(\frac{v_{S0}}{R_{S0}} + \frac{v_{S1}}{R_{S1}} + \frac{v_{S2}}{R_{S2}} + \frac{v_{S3}}{R_{S3}} \right)$$

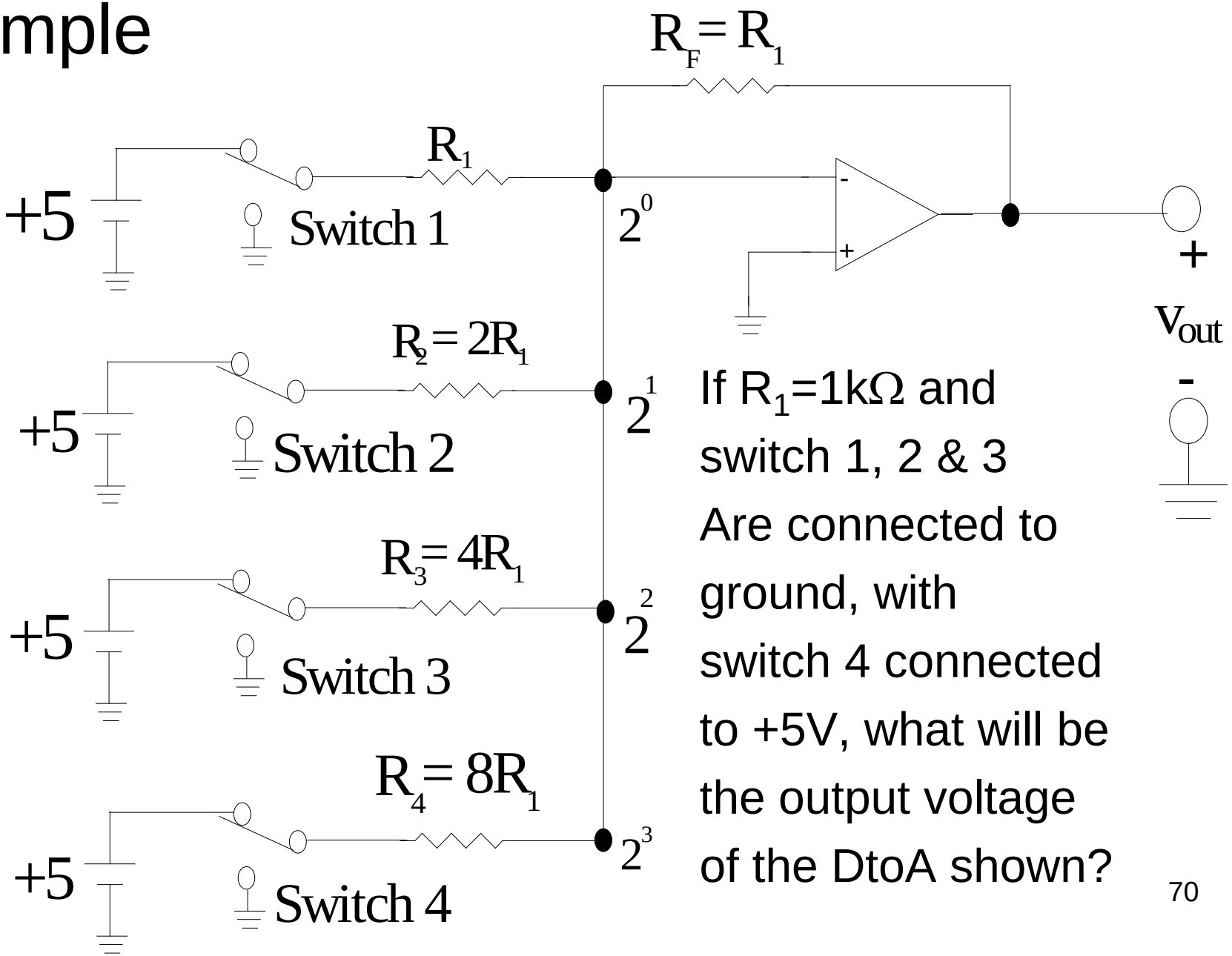
Where v_{S0} is the first digital input, v_{S1} is 2nd etc…

$$\therefore v_{out} = -R_1 \cdot \left(\frac{v_{S0}}{R_1} + \frac{v_{S1}}{2R_1} + \frac{v_{S2}}{4R_1} + \frac{v_{S3}}{8R_1} \right)$$

$$= -\left(v_{S0} + \frac{v_{S1}}{2} + \frac{v_{S2}}{4} + \frac{v_{S3}}{8} \right)$$



Digital to Analog Converters Example



If R_1=1kΩ and switch 1, 2 & 3 Are connected to ground, with switch 4 connected to +5V, what will be the output voltage of the DtoA shown?

Digital to Analog Converters Example

$$v_{out} = -\left(v_{S0} + \frac{v_{S1}}{2} + \frac{v_{S2}}{4} + \frac{v_{S3}}{8} \right)$$

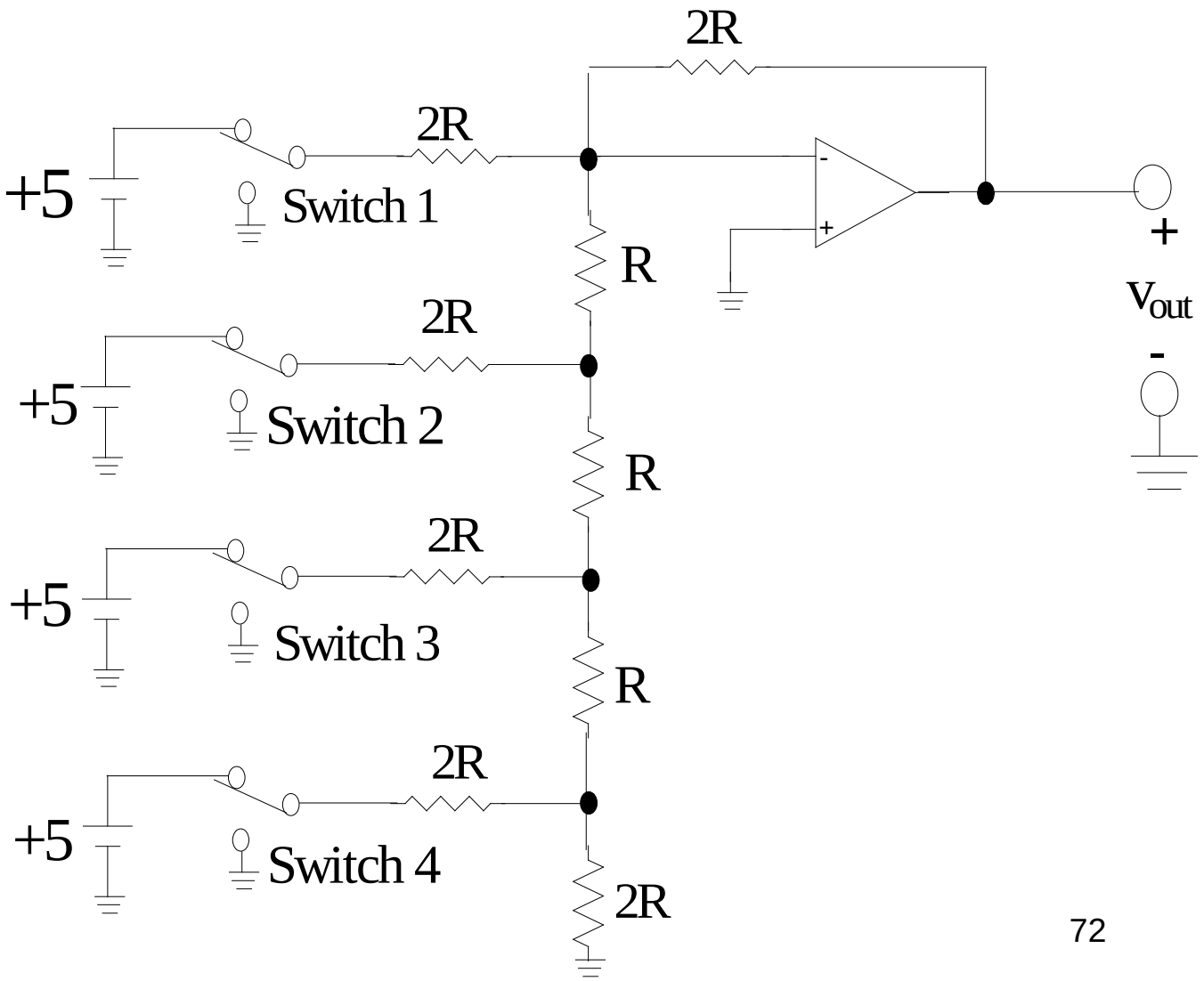
$$= -\left(0 + \frac{0}{2} + \frac{0}{4} + \frac{5}{8} \right)$$

$$= -0.625 \quad volts$$

This would correspond to the binary number ‘0001’
And also shows the resolution of the Converter
(it changes in steps of 0.625 volts!)

Digital to Analog Converters
R/2R ladder D/A

Has the
Advantage
Of only
Needing
Two resistor
Values,
2R and R

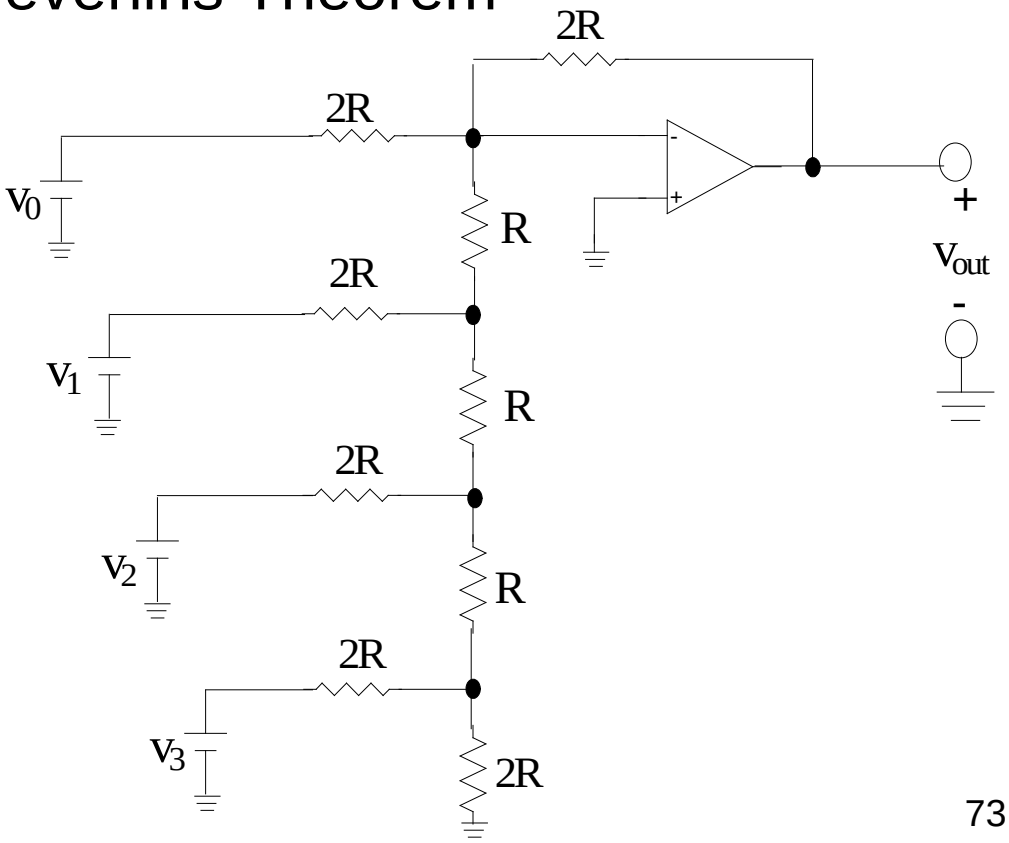


Digital to Analog Converters
R/2R ladder D/A

Analysis:

We use the principle of superposition once again to solve This and we will need Thevenins Theorem

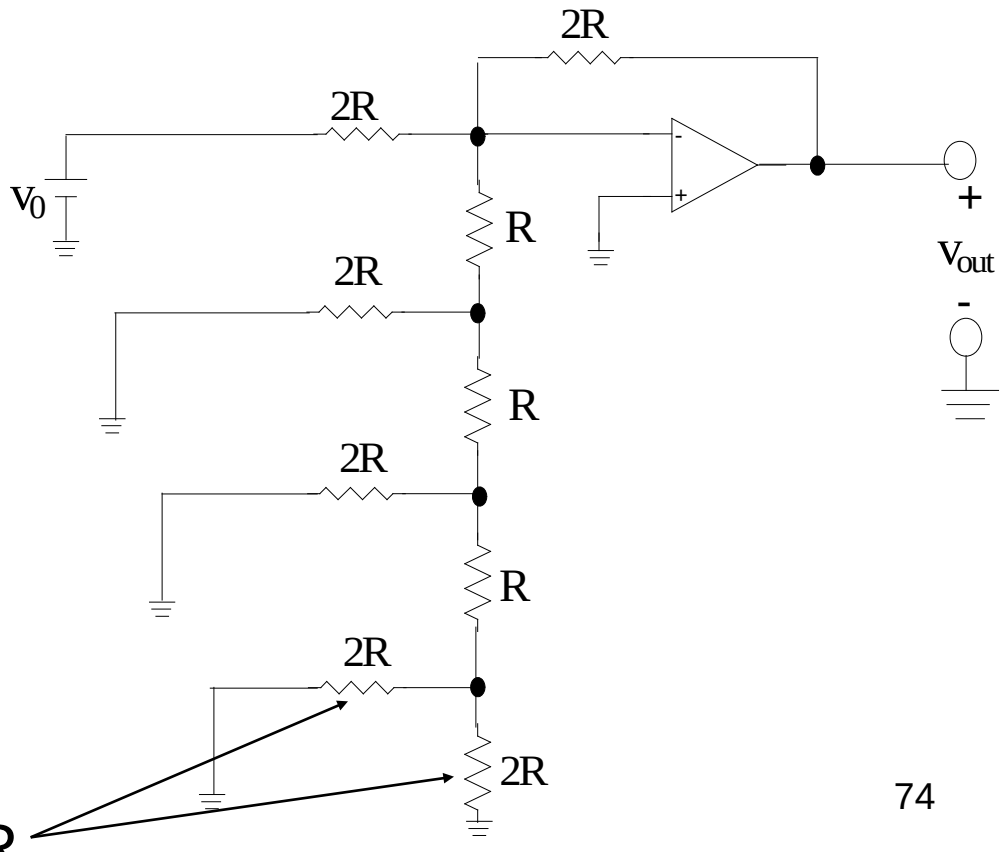
Redrawing the circuit but now changing the switches to voltage Sources we get:



Digital to Analog Converters
R/2R ladder D/A

With v_1, v_2 & v_3 suppressed:

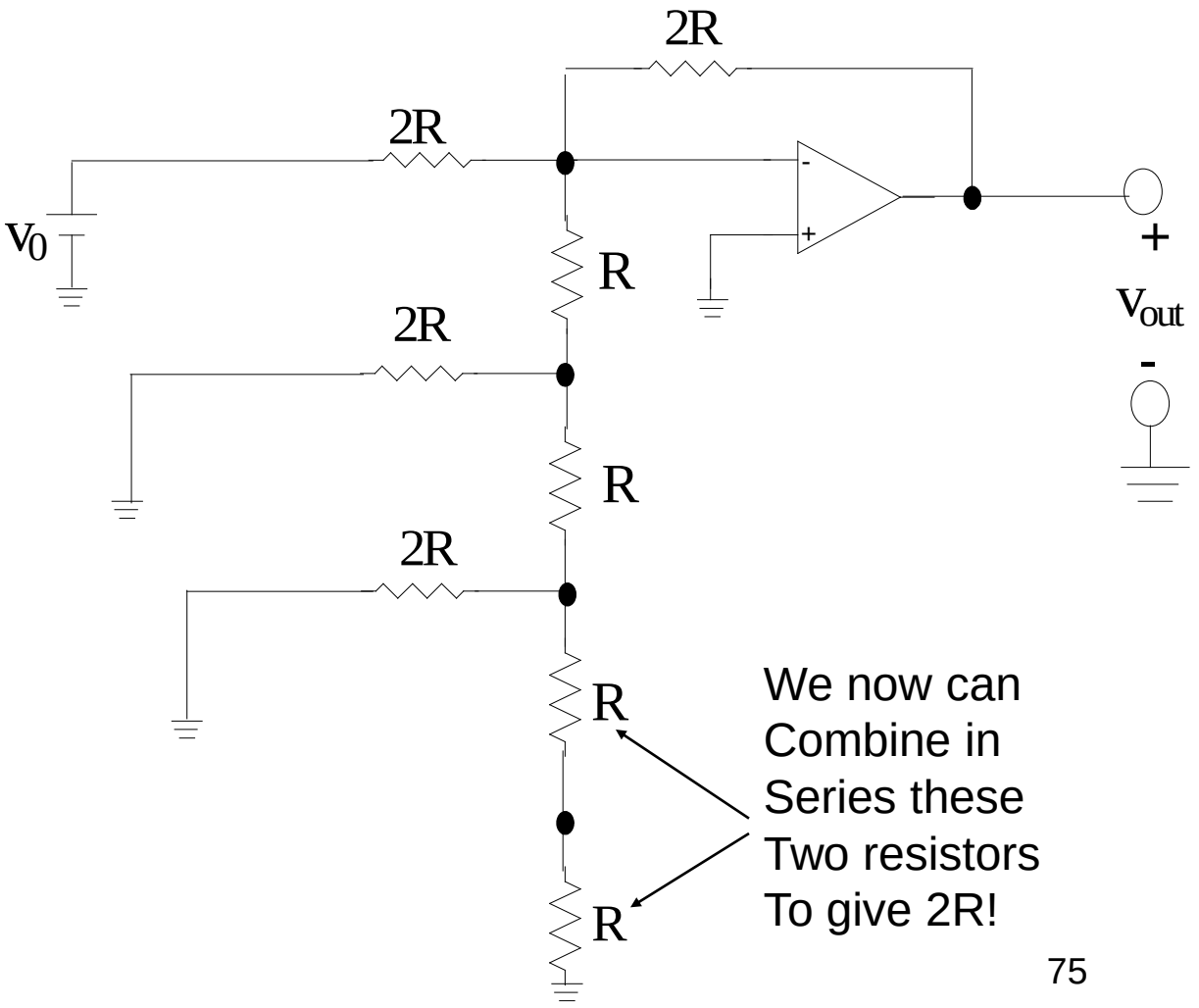
We could stop here and
Note that whatever the
Resistance of the ladder
Network is the virtual
Ground makes this
Resistance irrelevant,
But for the next stage we
Need to do this, so…



We now note that
These two resistors
Are in parallel ie 2R || 2R

Digital to Analog Converters
R/2R ladder D/A

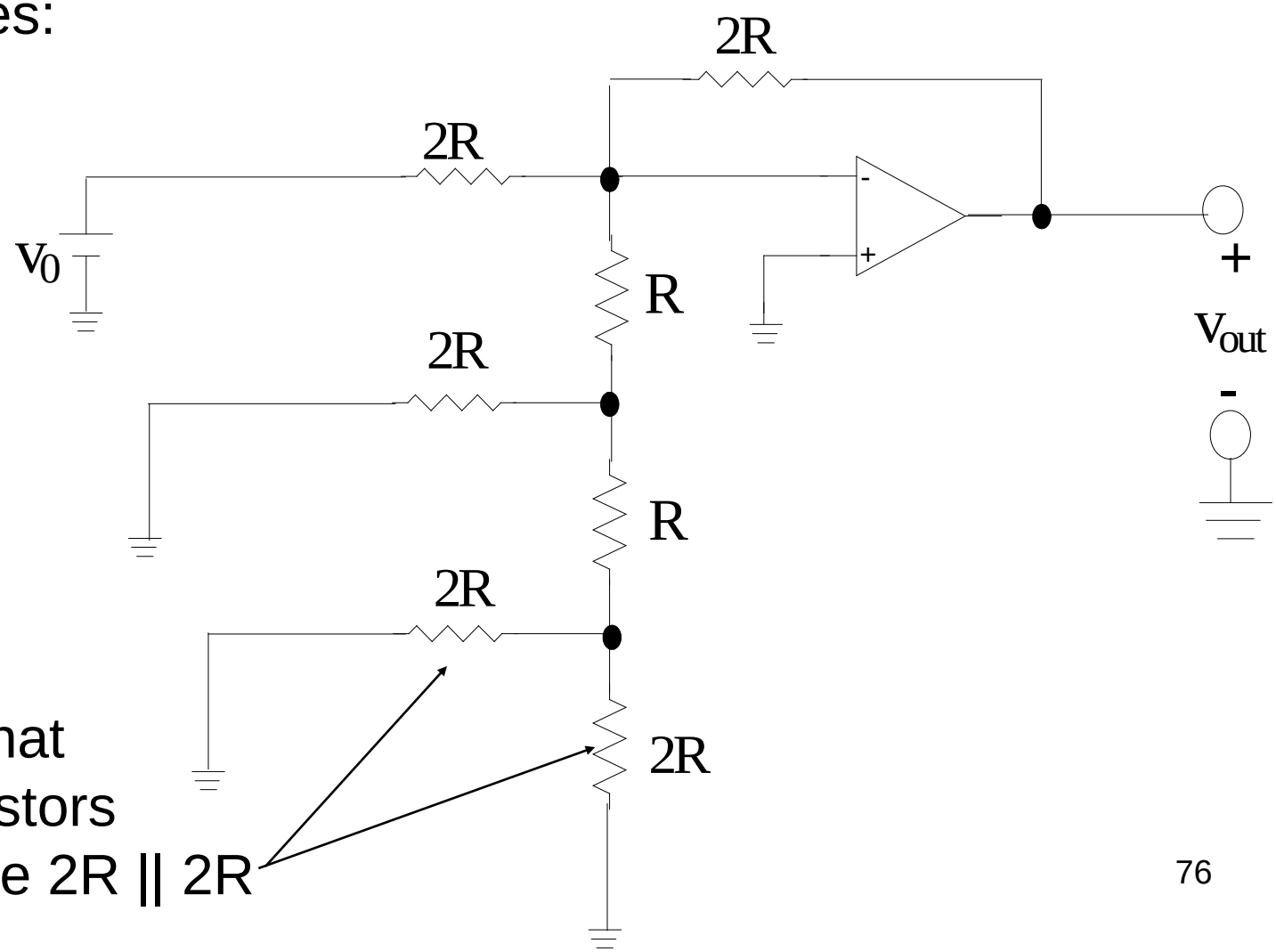
Which gives:



We now can Combine in Series these Two resistors To give 2R!

Digital to Analog Converters
R/2R ladder D/A

Which gives:



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Digital to Analog Converters
R/2R ladder D/A

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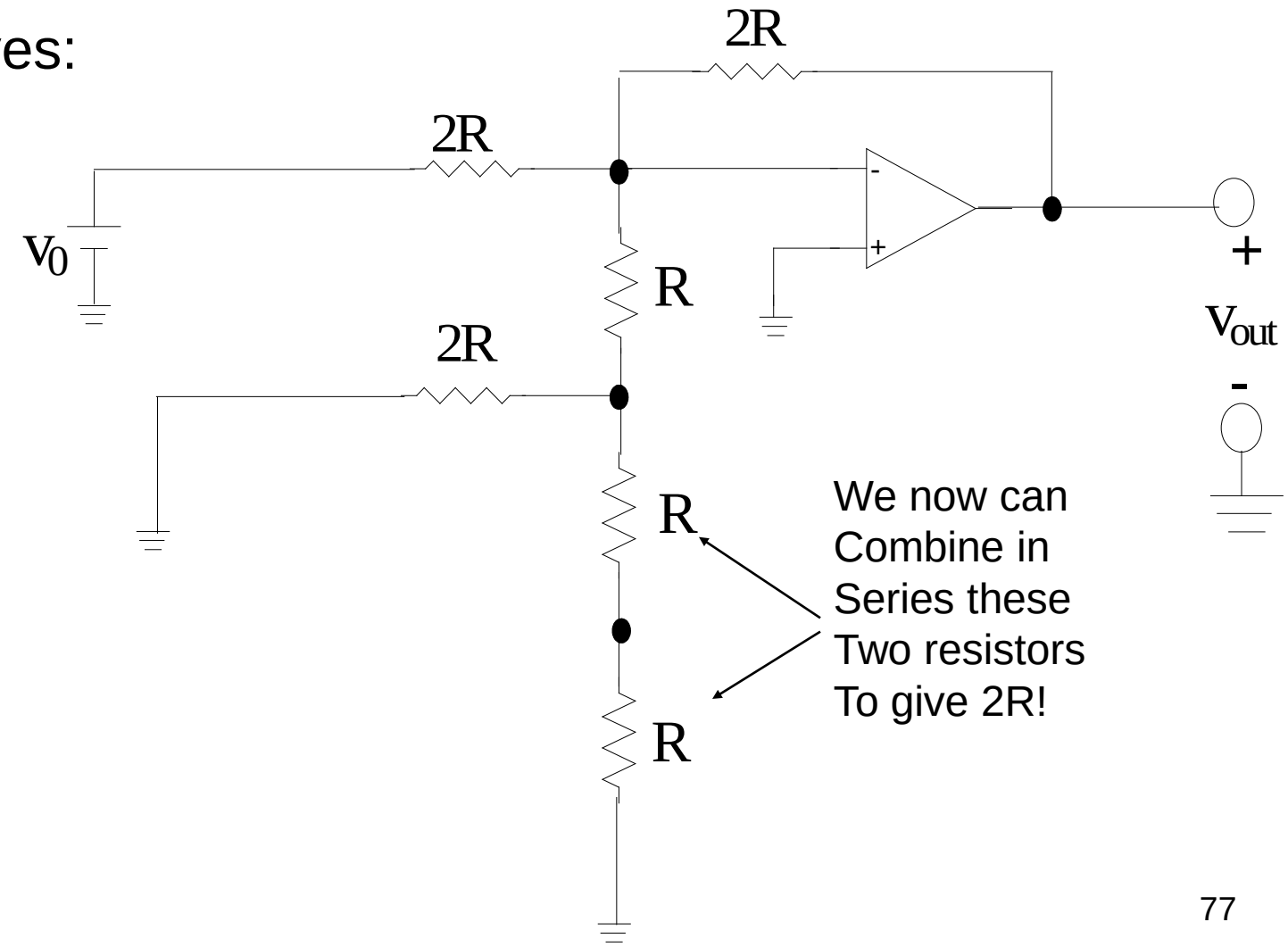
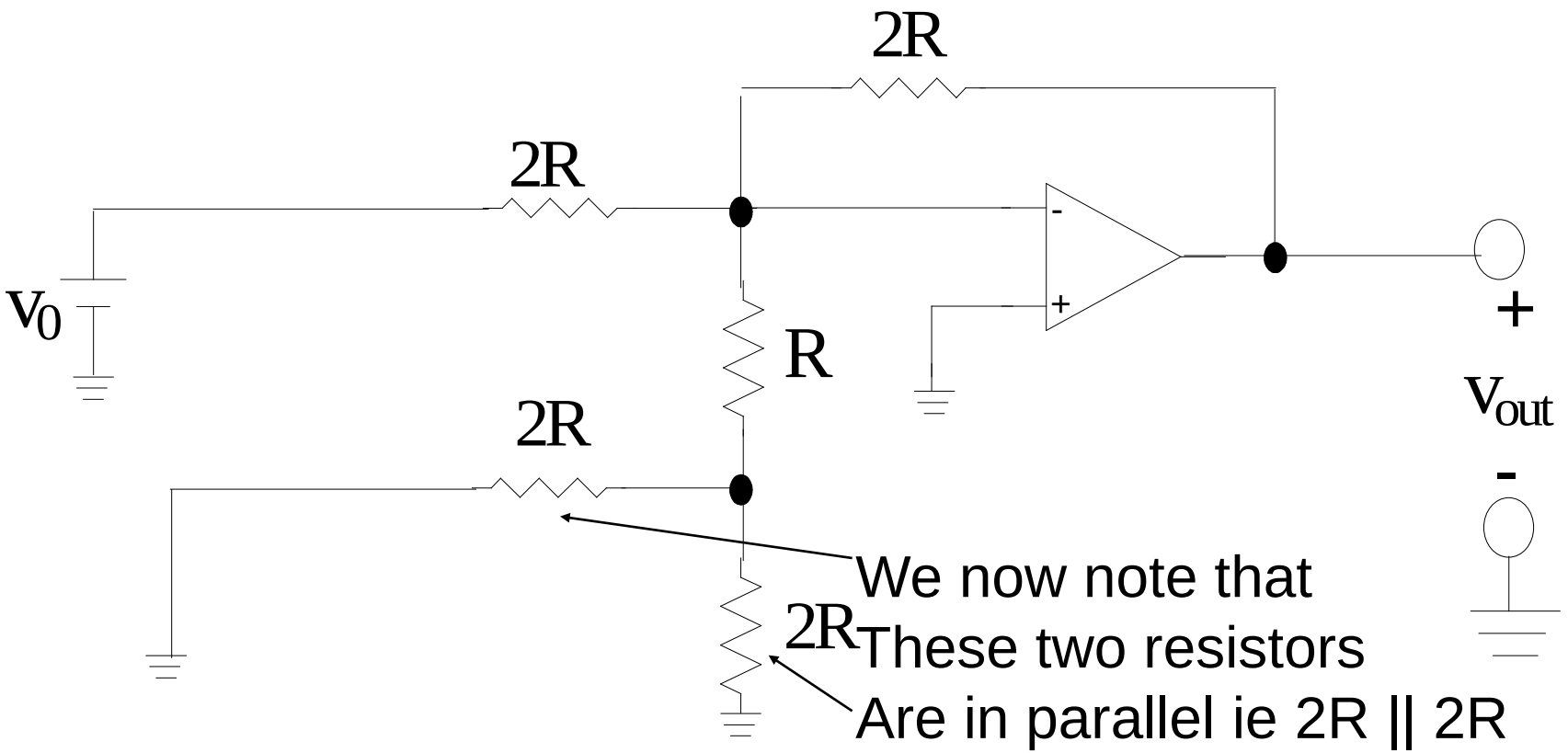


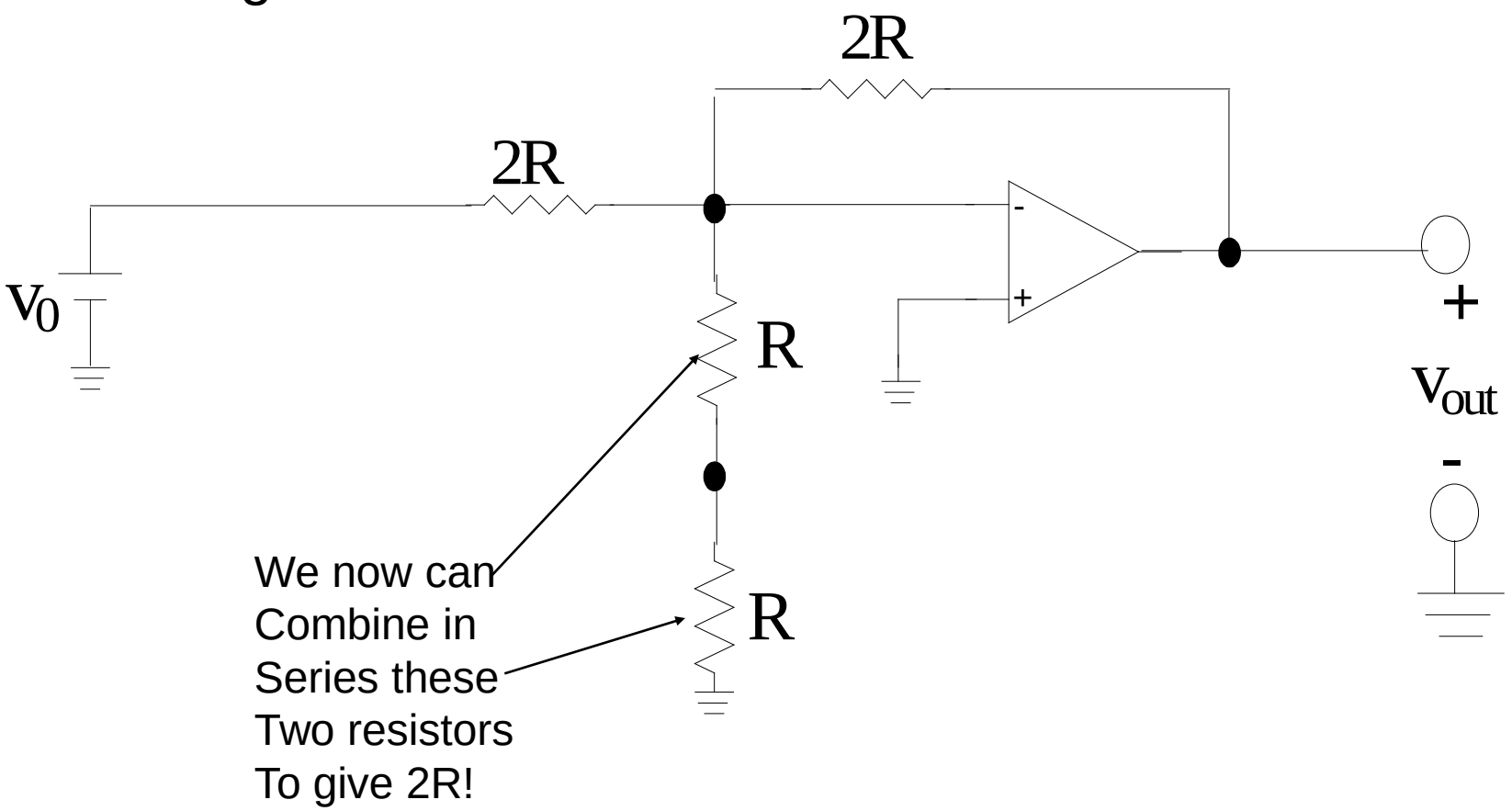
Digital to Analog Converters
R/2R ladder D/A

Which gives:



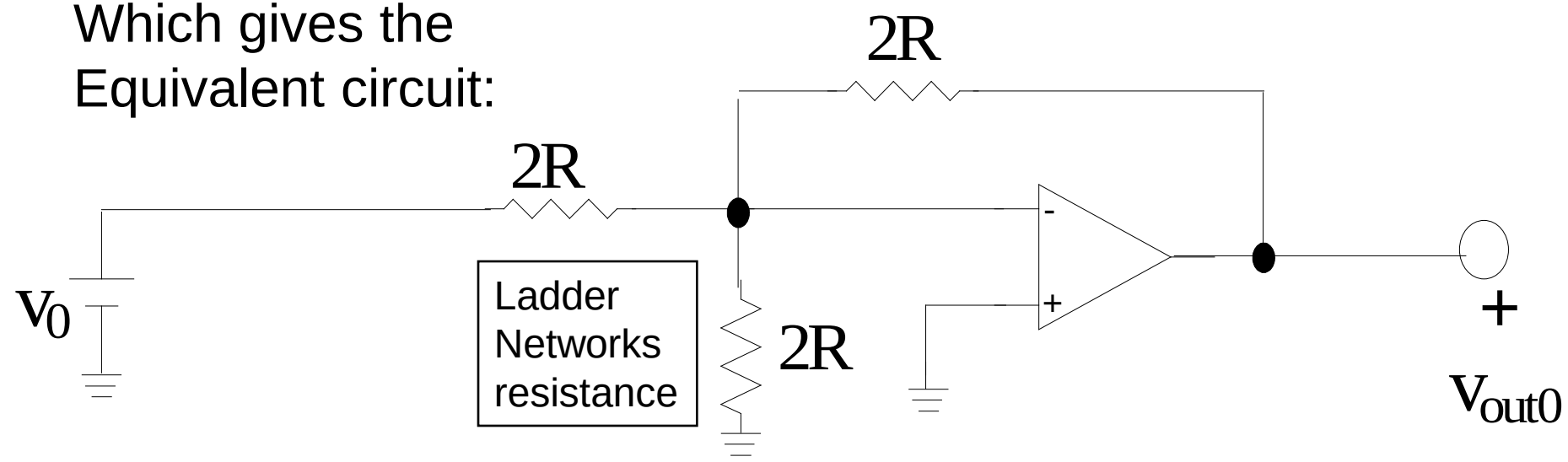
Digital to Analog Converters
R/2R ladder D/A

Which gives:



Digital to Analog Converters
R/2R ladder D/A

Which gives the
Equivalent circuit:



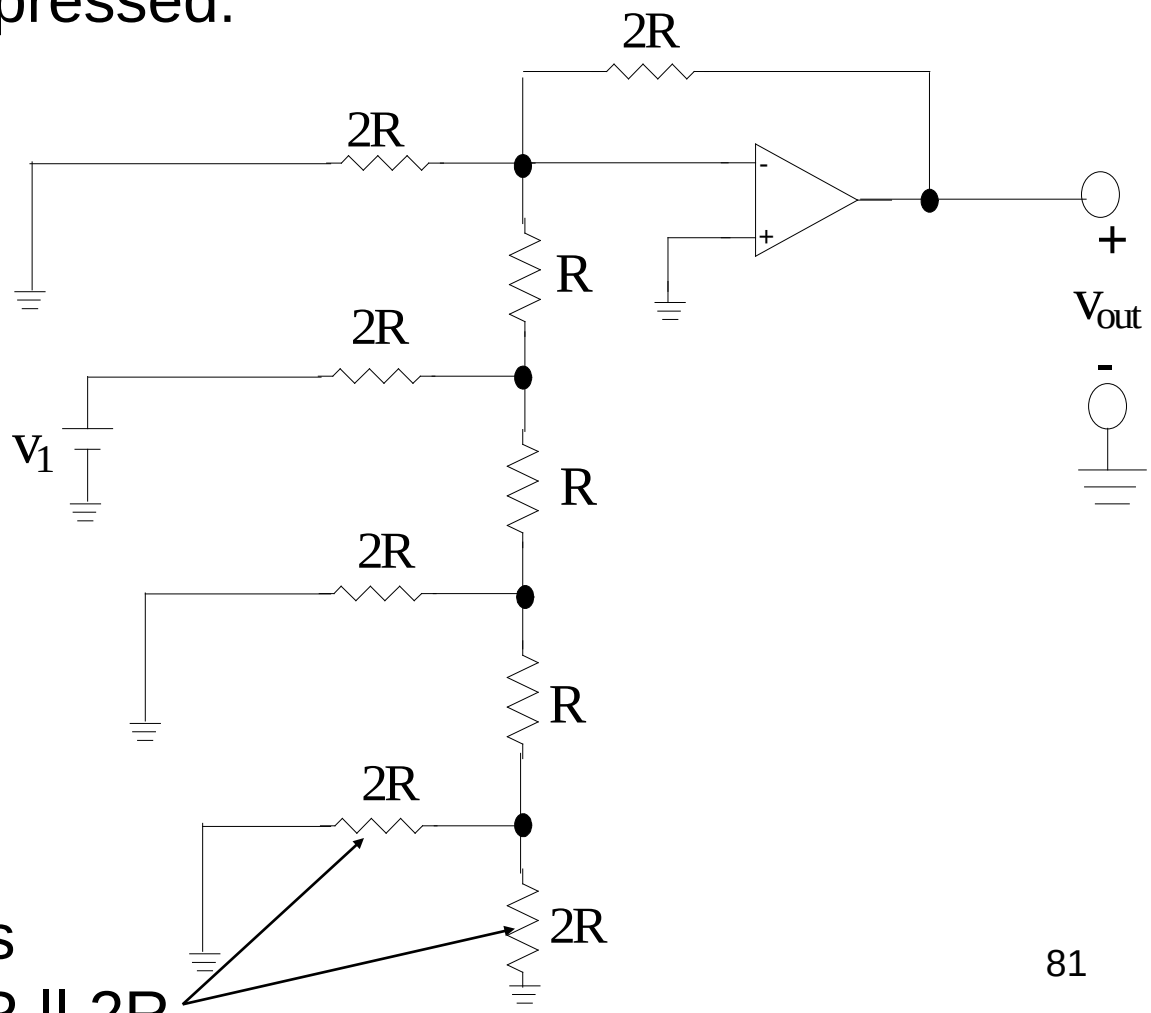
Now writing an expression for v_{out}
In terms of v_0 using the virtual ground and noting
No current will flow in the ladder networks
Resistor (2R) we get:

$$v_{out} = v_{out0} = -\frac{2R}{2R} v_o = -v_o$$

V_0 is either +5V or 0V

Digital to Analog Converters
R/2R ladder D/A

With v_0, v_2 & v_3 suppressed:



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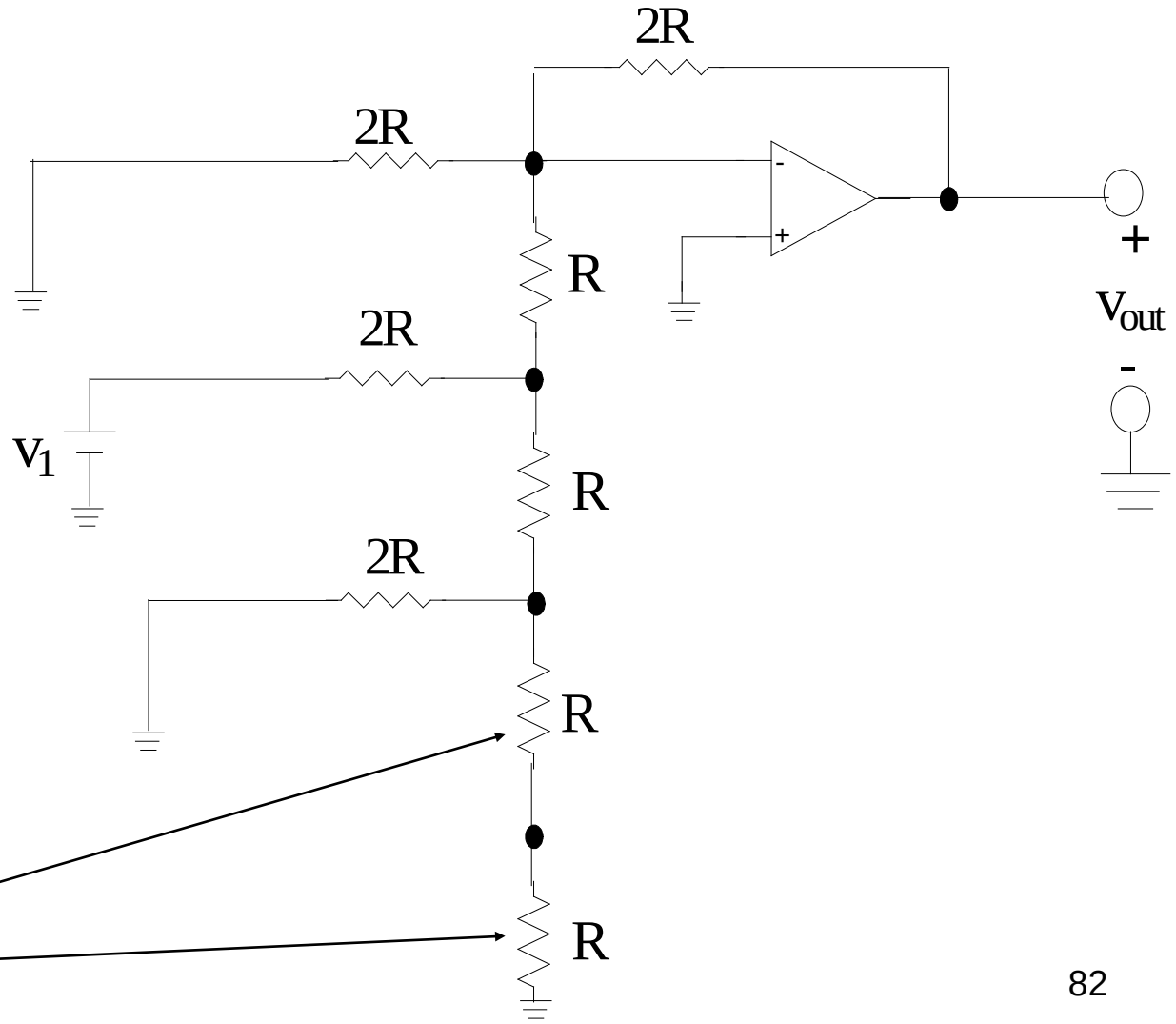
Digital to Analog Converters
R/2R ladder D/A

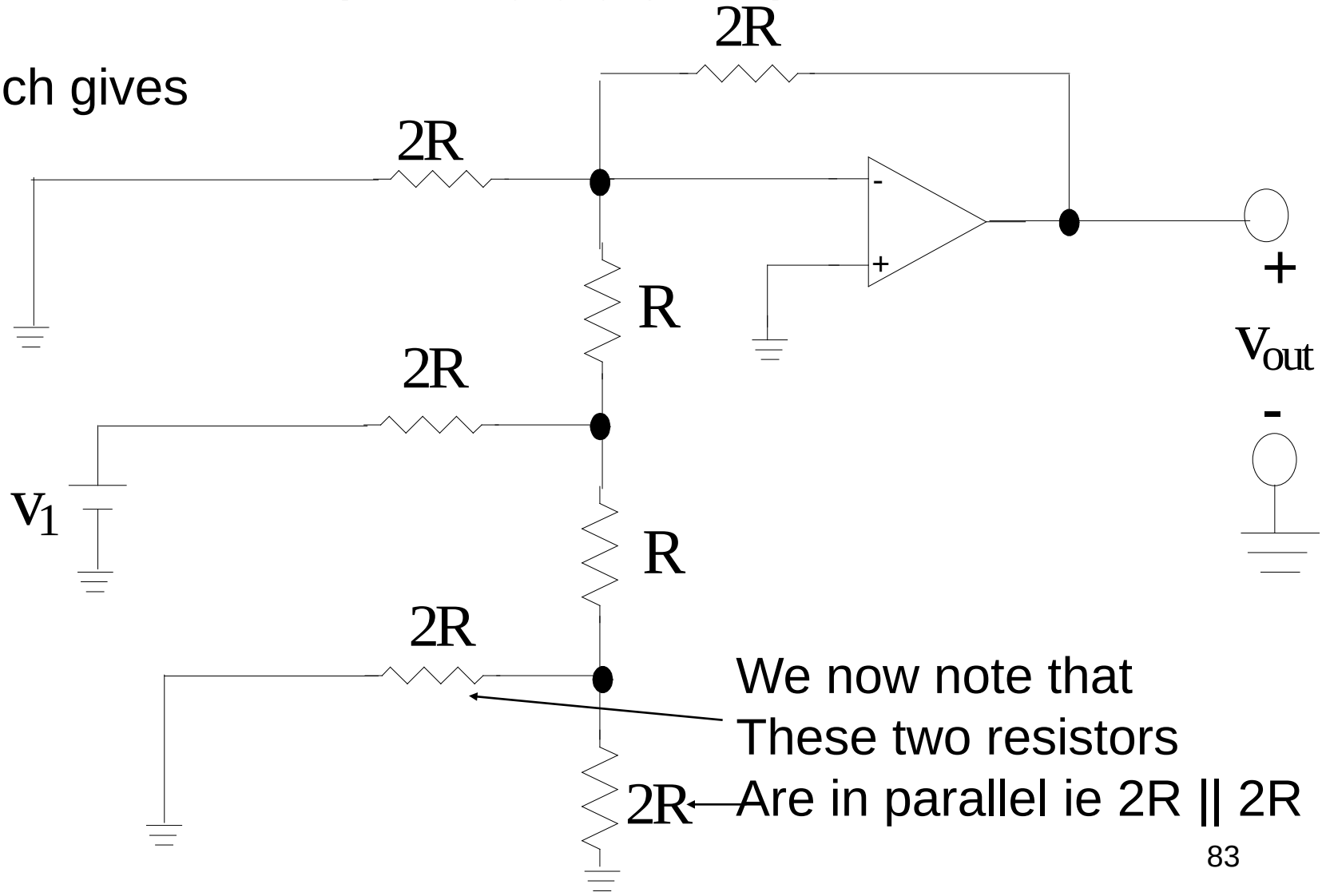
Which gives



We now can
Combine in
Series these
Two resistors
To give 2R!

Digital to Analog Converters
R/2R ladder D/A

Which gives



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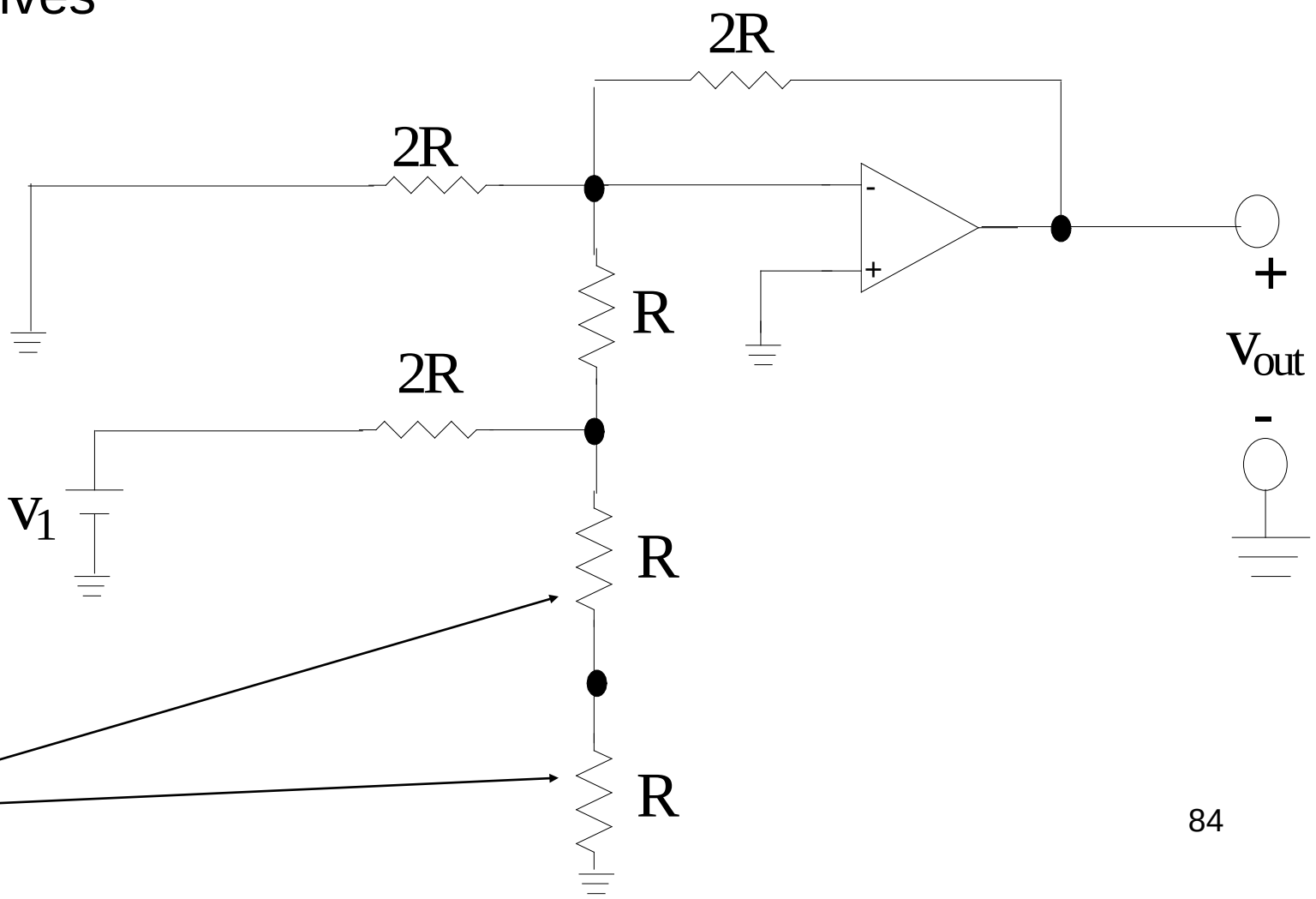

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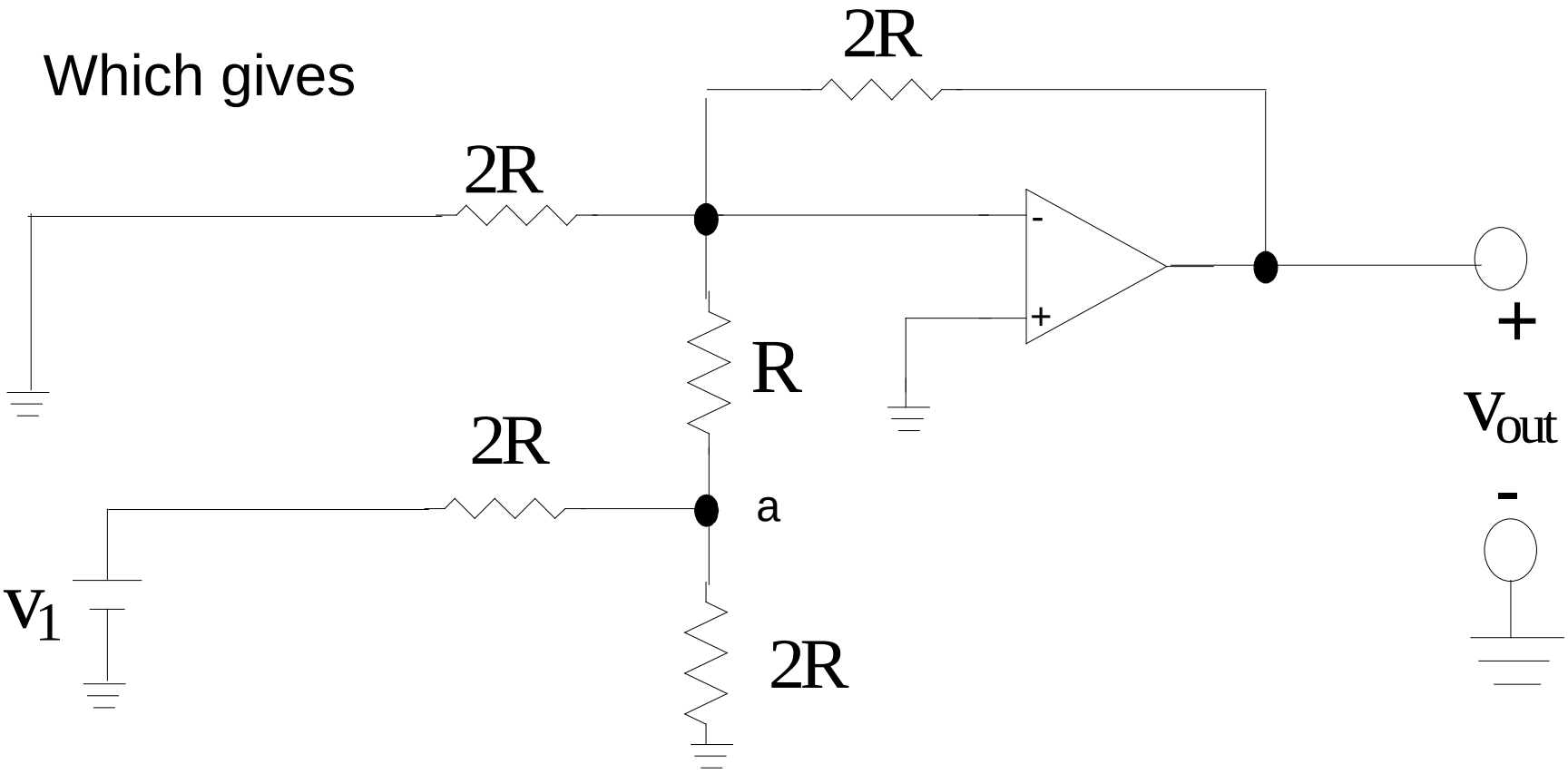
Digital to Analog Converters
R/2R ladder D/A

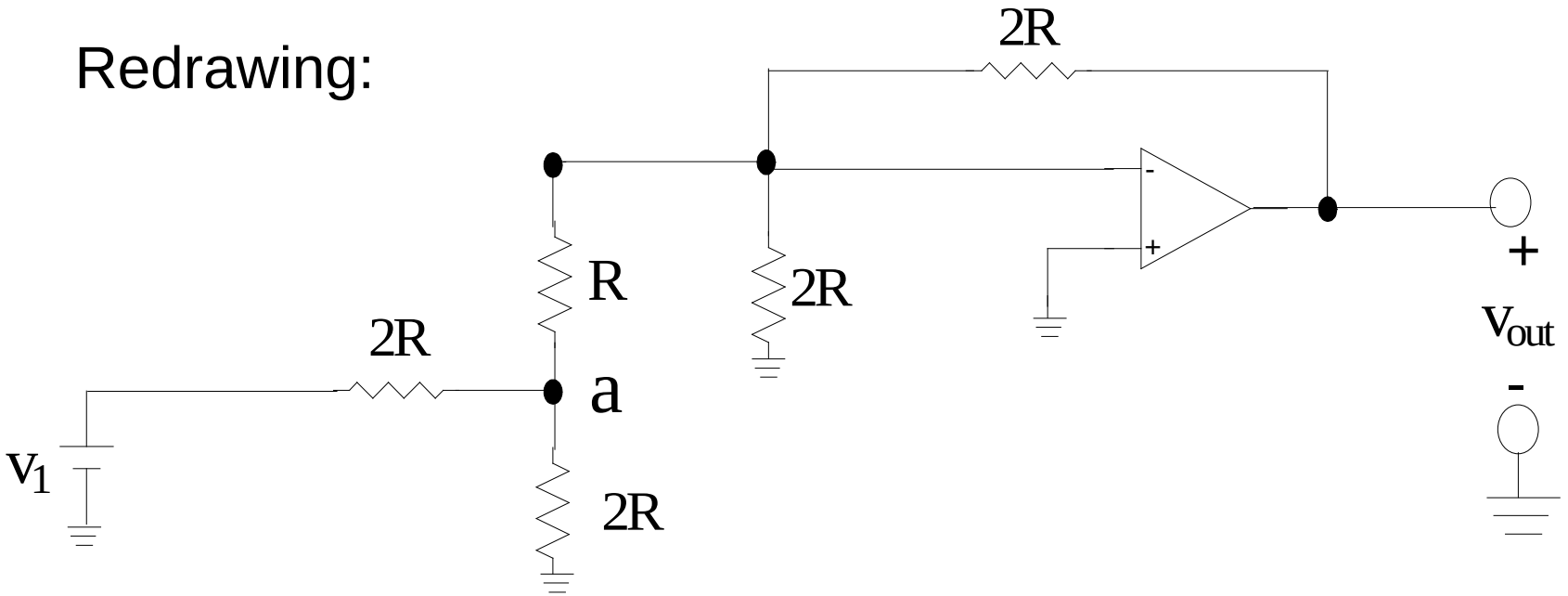
Which gives



Using node ‘a’ to ground we need to calculate the Thevenin equivalent Voltage and Resistance!

Digital to Analog Converters
R/2R ladder D/A

Redrawing:



Thevenin voltage from node ‘a’ to ground is:

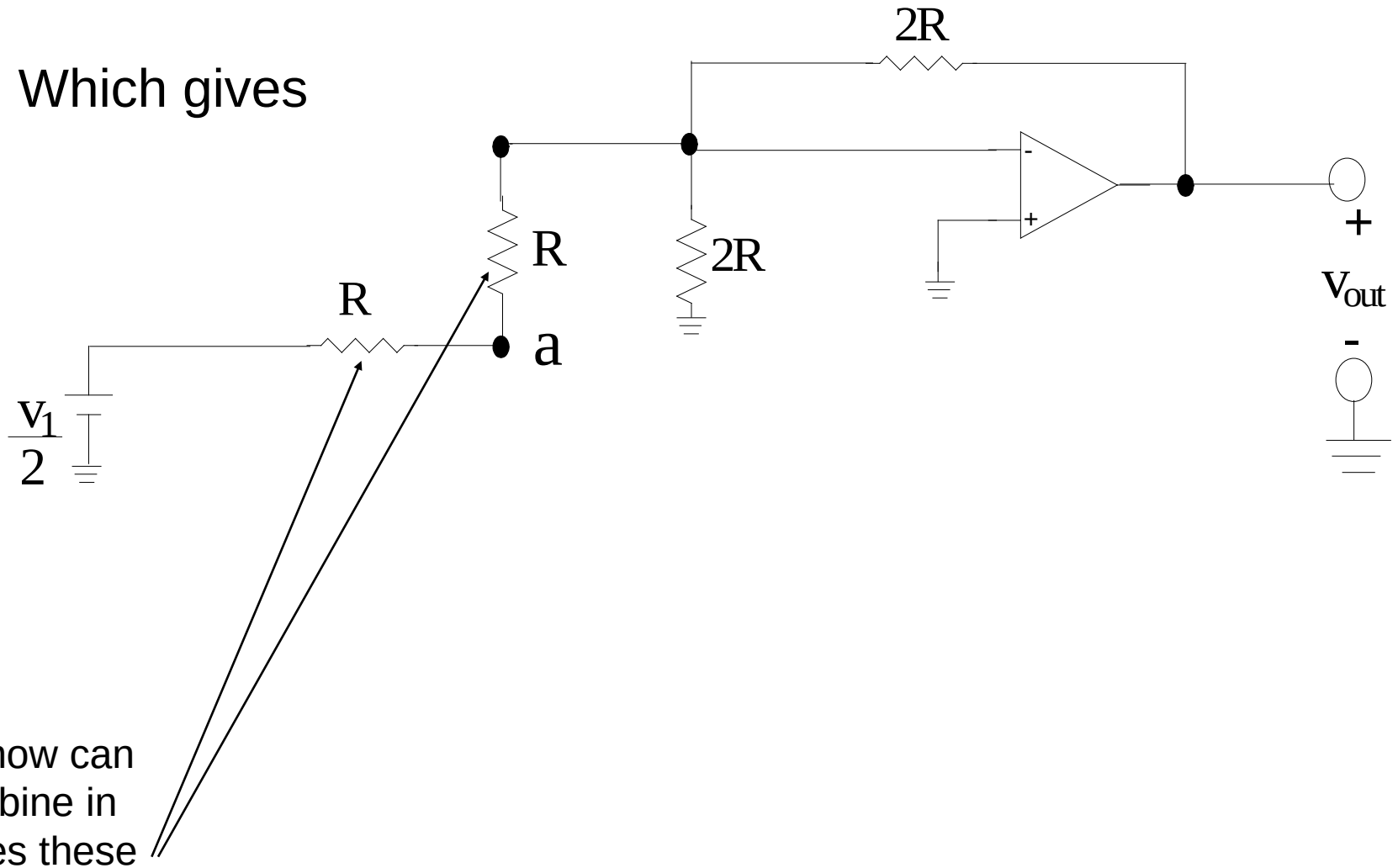
$$E_{Th} = \frac{2R}{2R+2R} v_1 = \frac{v_1}{2}$$

Thevenin resistance from node ‘a’ to ground is (suppressing v_1):

$$2R \parallel 2R = R = R_{Th}$$

Digital to Analog Converters
R/2R ladder D/A

Which gives



We now can
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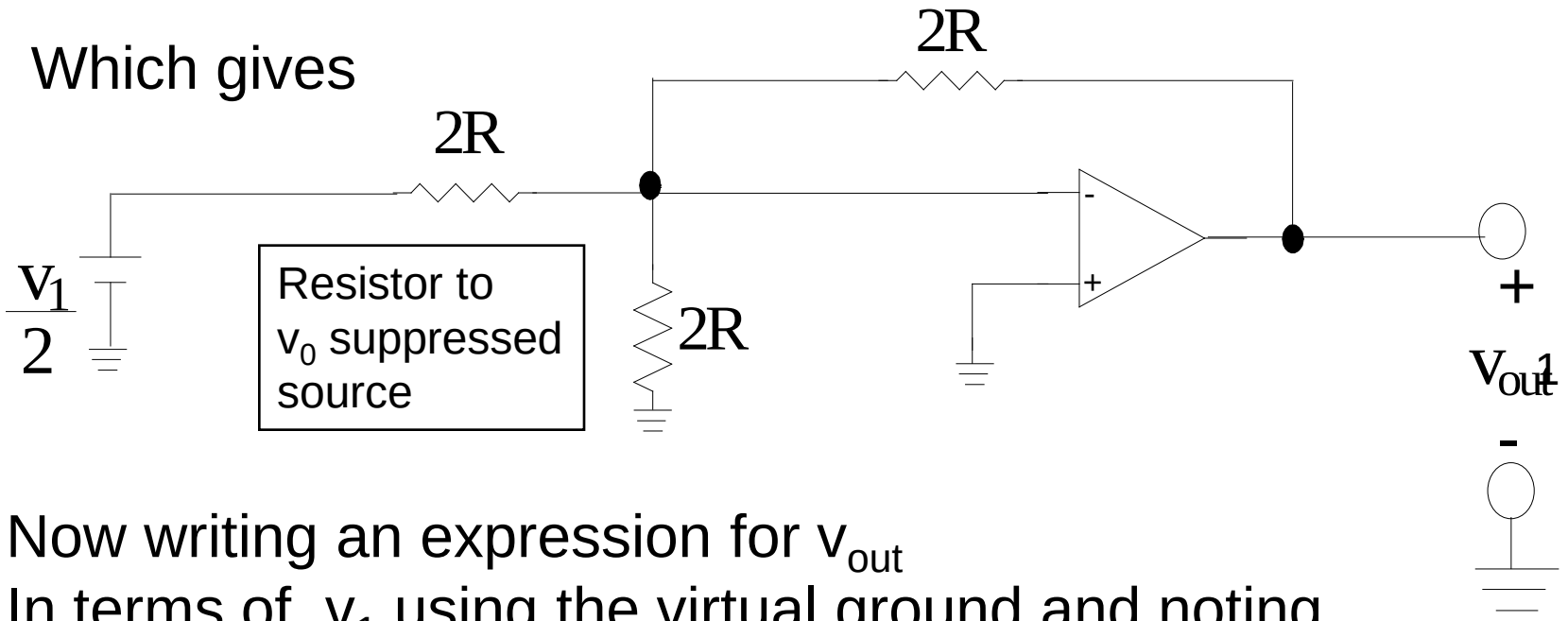
To give 2R!

Digital to Analog Converters
R/2R ladder D/A

Which gives



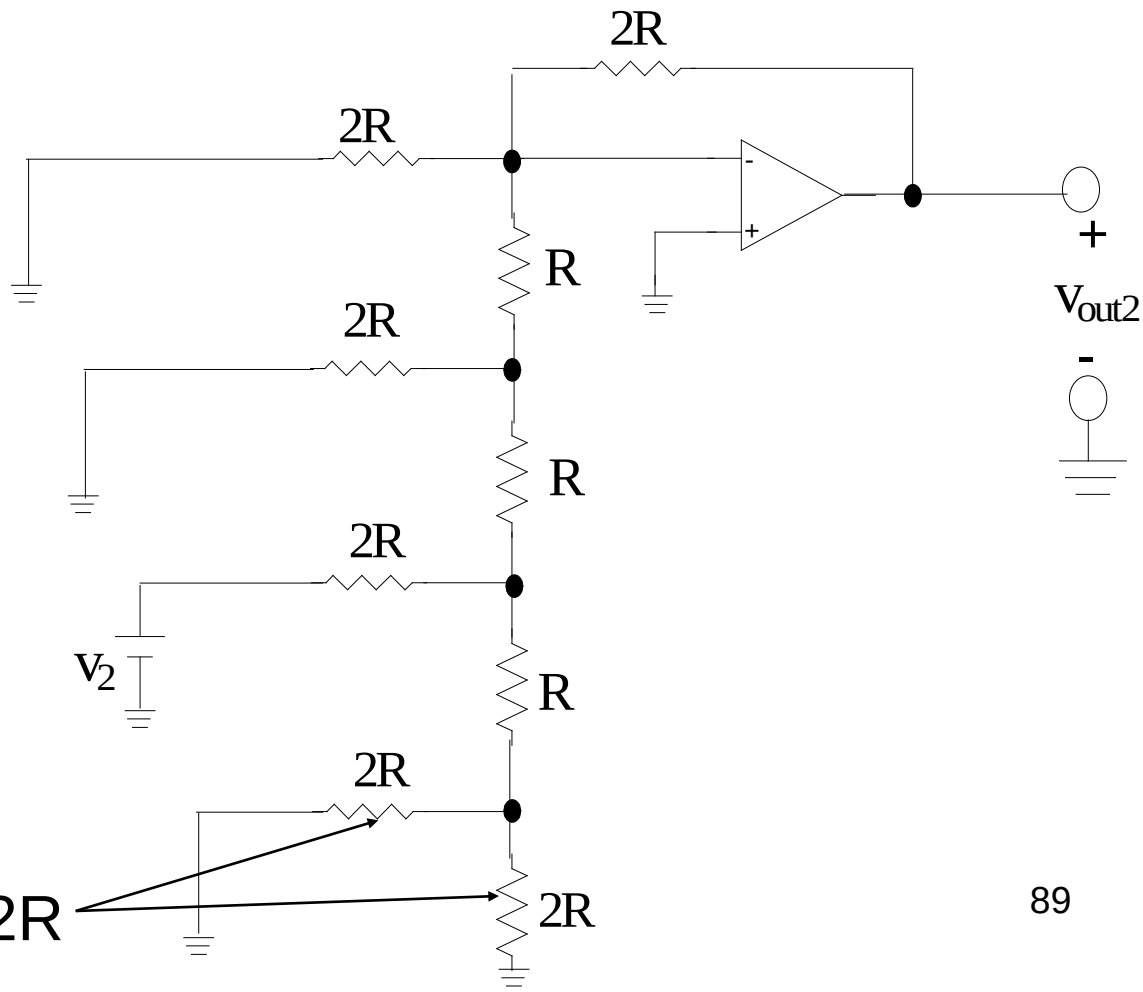
Now writing an expression for v_{out}
In terms of v_1 using the virtual ground and noting
No current will flow in the resistor to v_0's
Suppressed source (2R) we get:

$$v_{out} = v_{out1} = -\frac{2R}{2R}\frac{v_1}{2} = -\frac{v_1}{2}$$

v_1 is either +5V or 0V

Digital to Analog Converters
R/2R ladder D/A

With v_0, v_1 & v_3 suppressed:



We now note that
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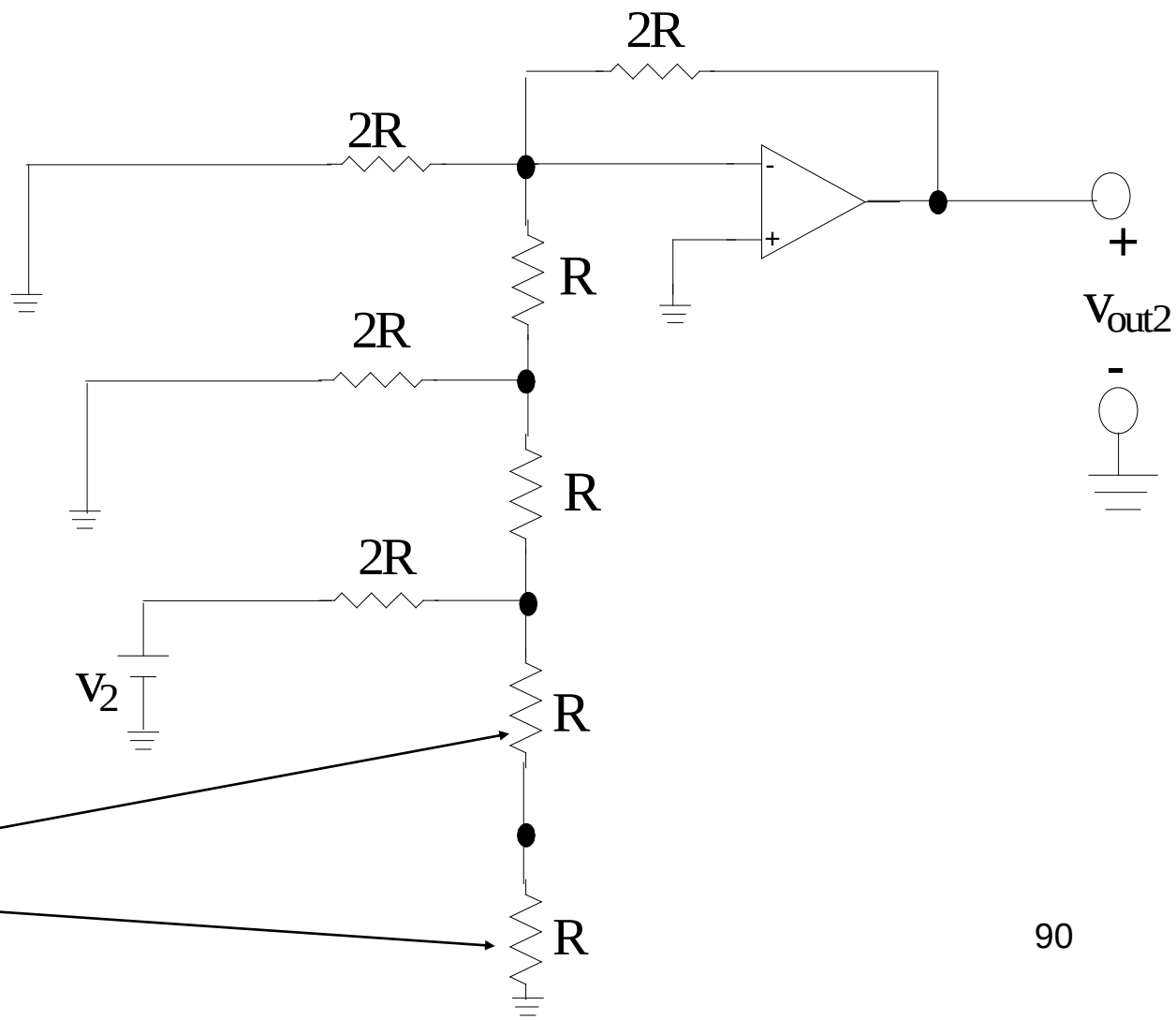
Are in parallel ie 2R || 2R

Digital to Analog Converters
R/2R ladder D/A

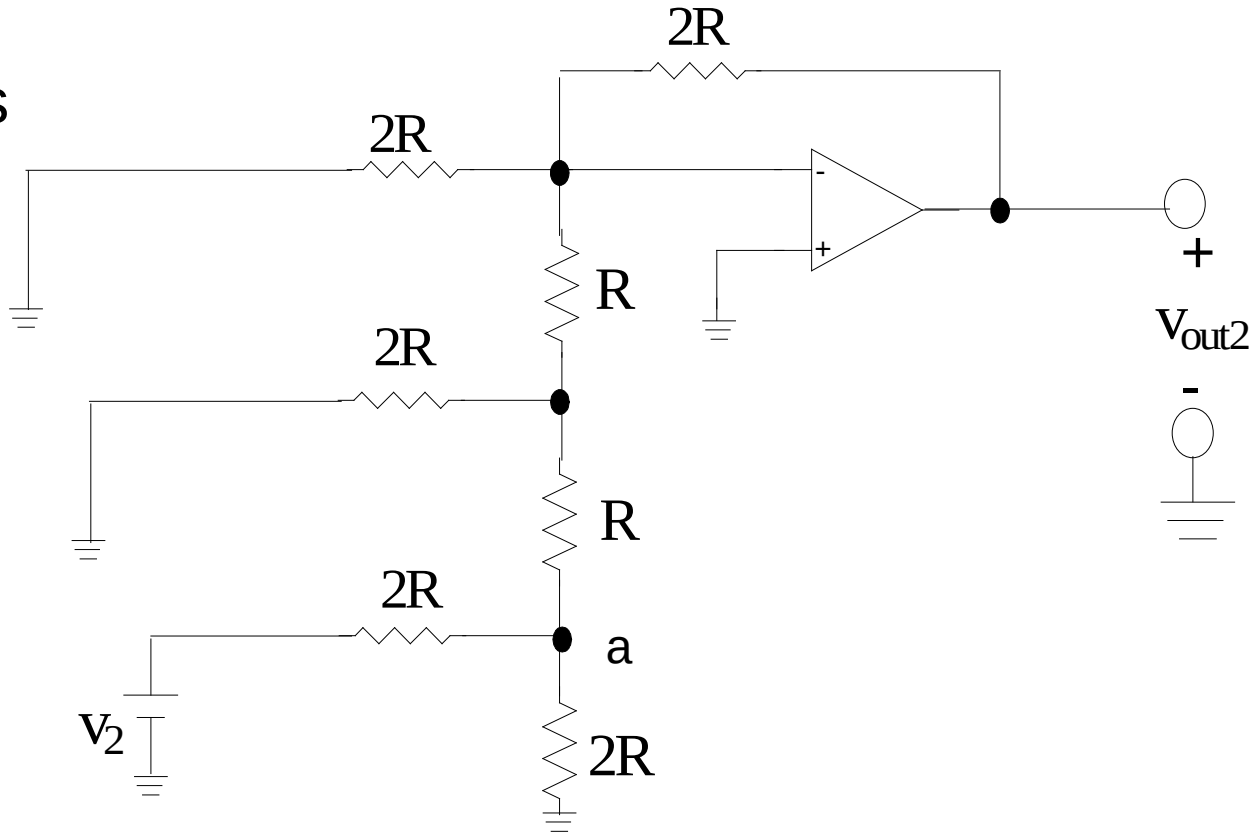
Which gives



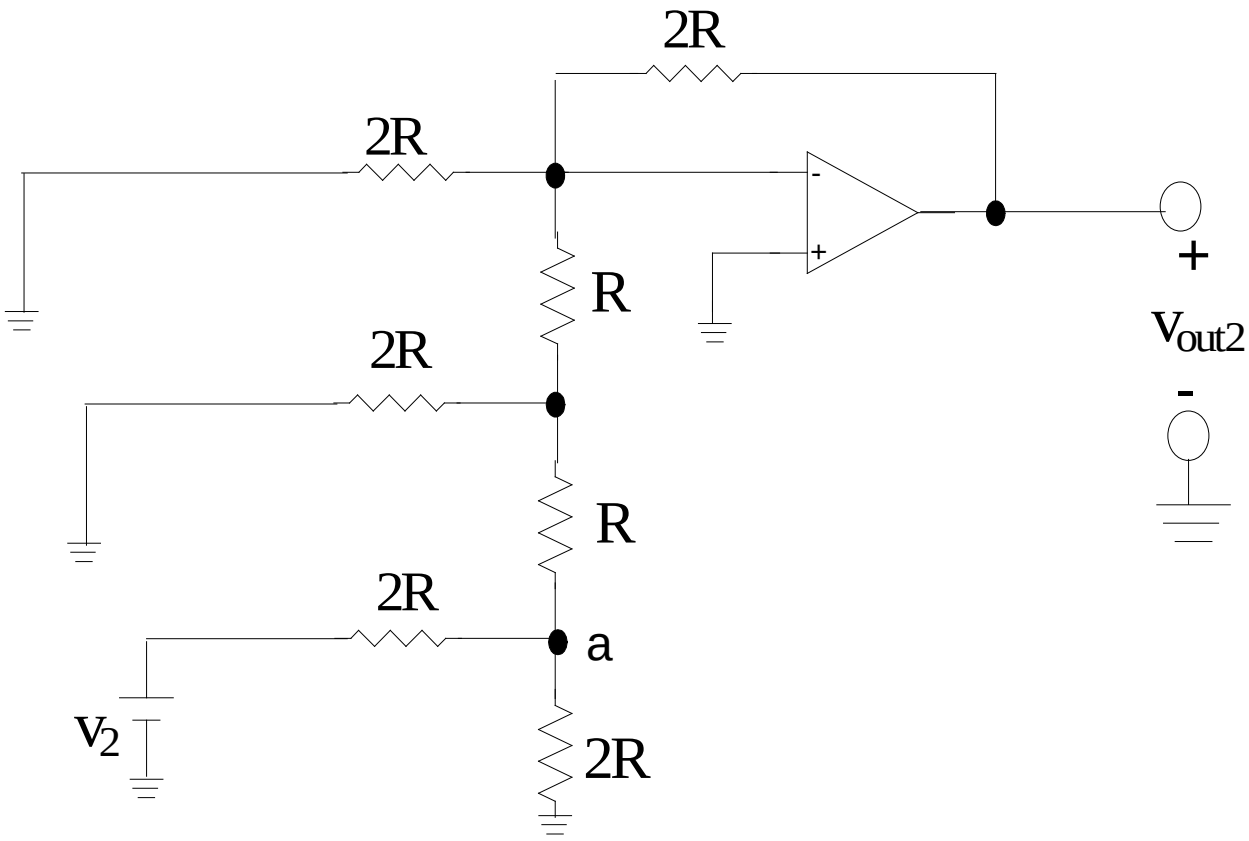
We now can
Combine in
Series these
Two resistors
To give 2R!

Digital to Analog Converters
R/2R ladder D/A

Which gives



Using node ‘a’ to ground we need to calculate the Thevenin equivalent Voltage and Resistance!

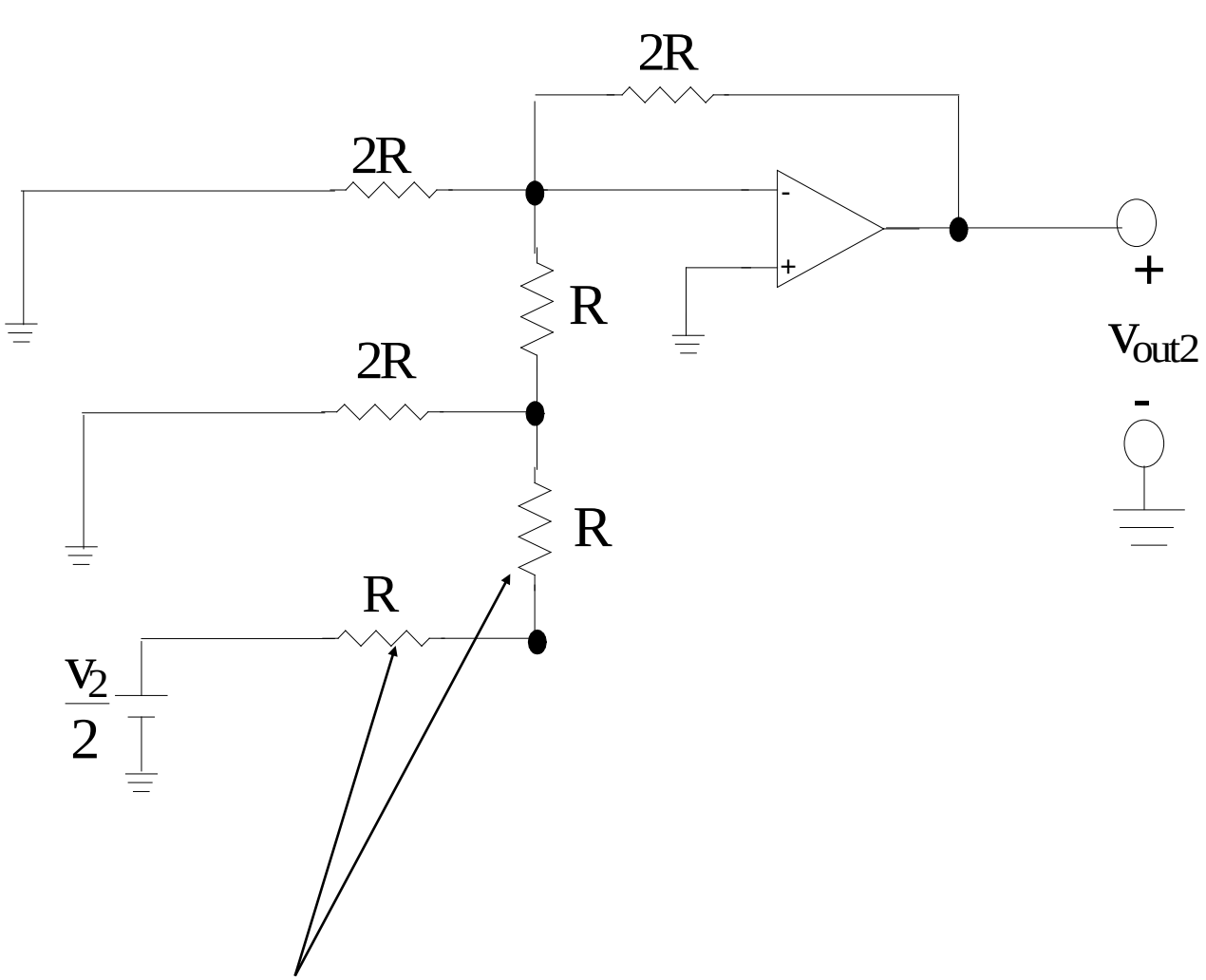


Thevenin voltage from node ‘a’ to ground is:

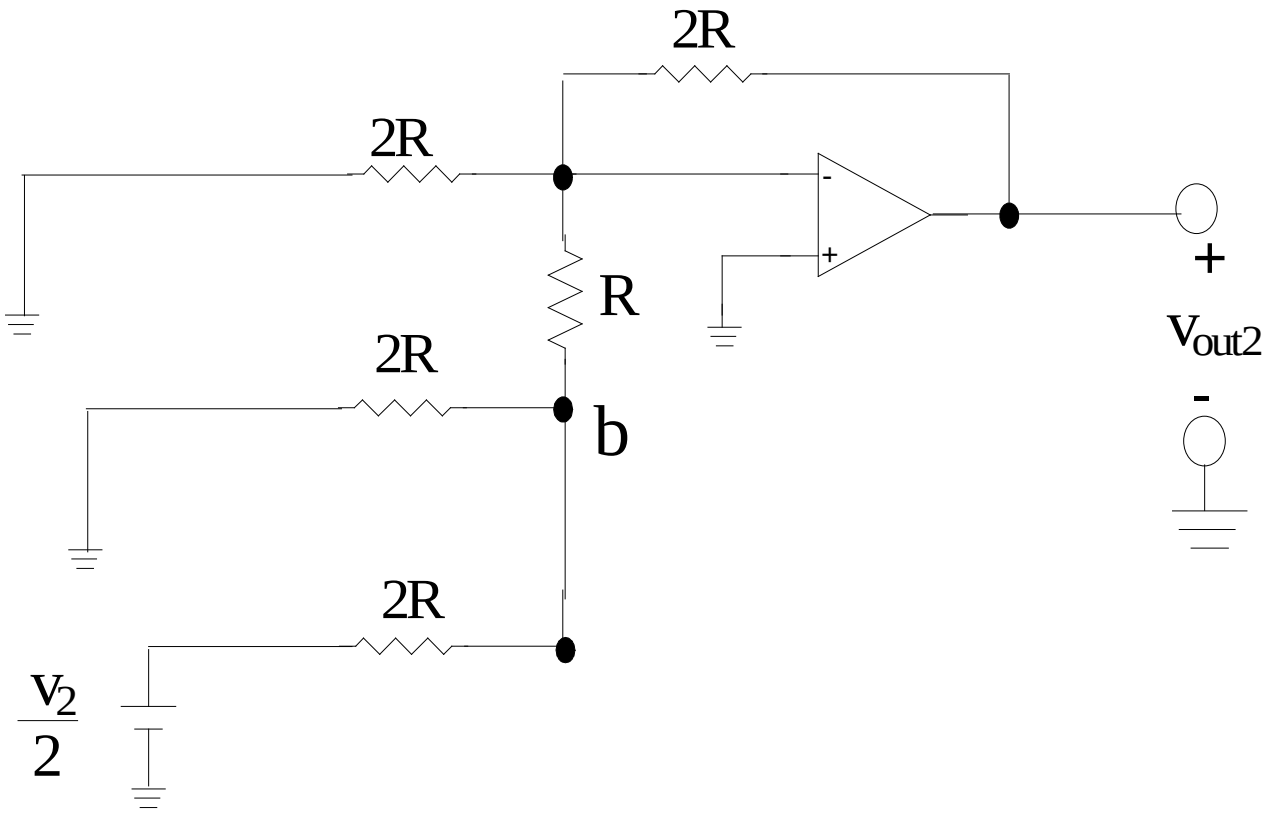
$$E_{Th} = \frac{2R}{2R+2R} v_2 = \frac{v_2}{2}$$

Thevenin resistance from node ‘a’ to ground is (suppressing v_2):

$$2R \parallel 2R = R = R_{Th}$$



We now can
Combine in
Series these
Two resistors
To give 2R!

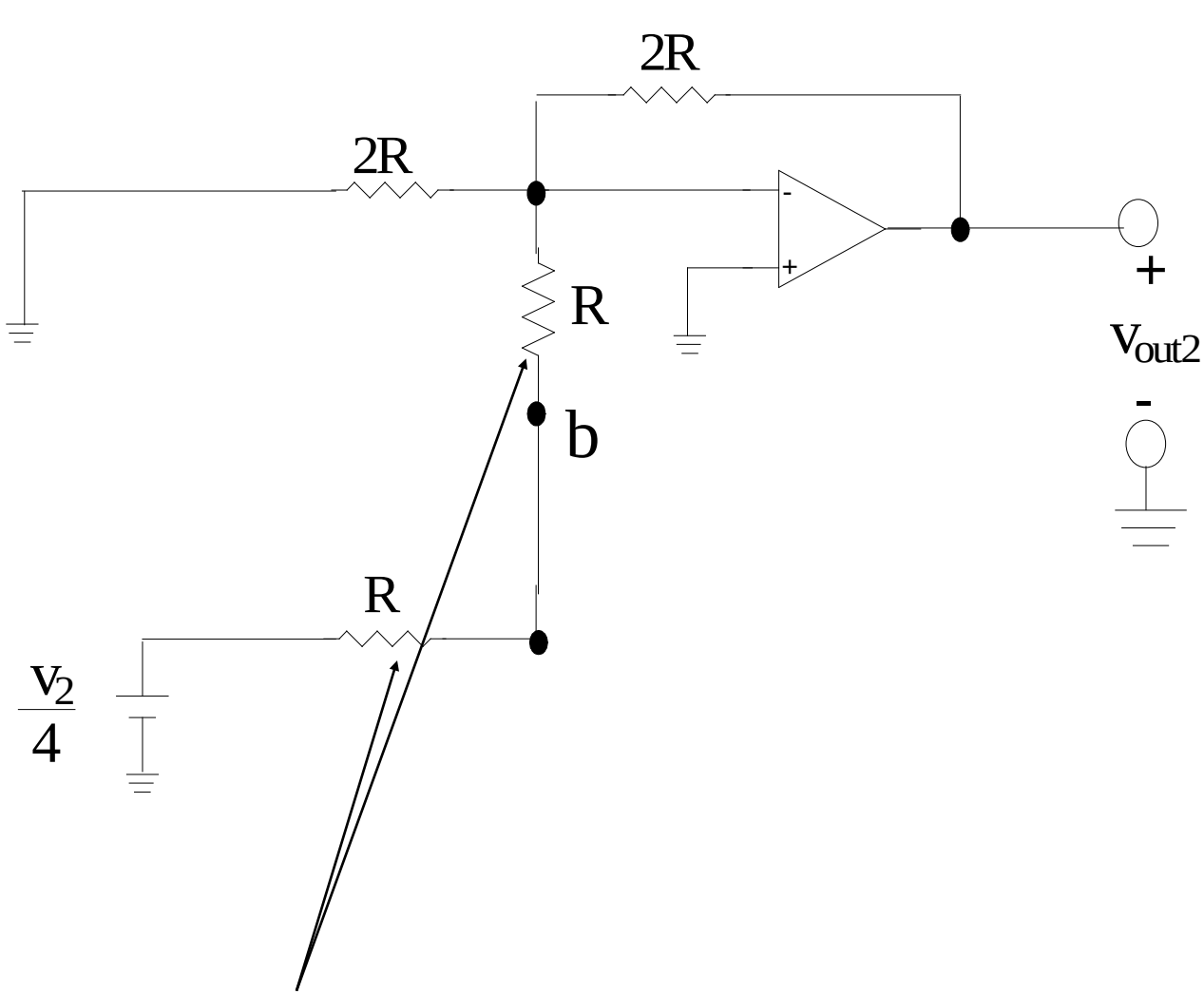


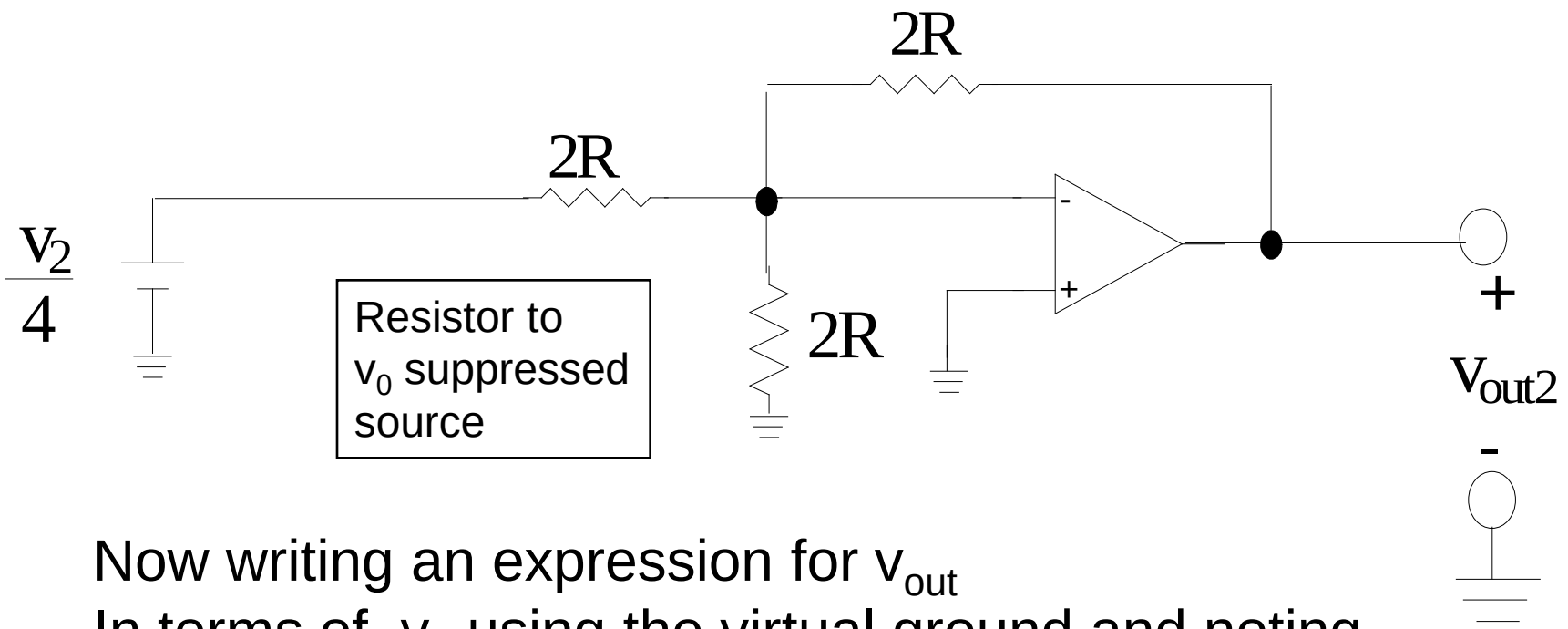
Thevenin voltage from node ‘b’ to ground is:

$$E_{Th} = \frac{2R}{2R+2R}\frac{v_2}{2} = \frac{v_2}{4}$$

Thevenin resistance from node ‘b’ to ground is (suppressing v_2):

$$2R \parallel 2R = R = R_{Th}$$


2R
2R
R
b
R
$\frac{V_2}{4}$
V_{out2}
+
-
We now can
Combine in
Series these
Two resistors
To give 2R!



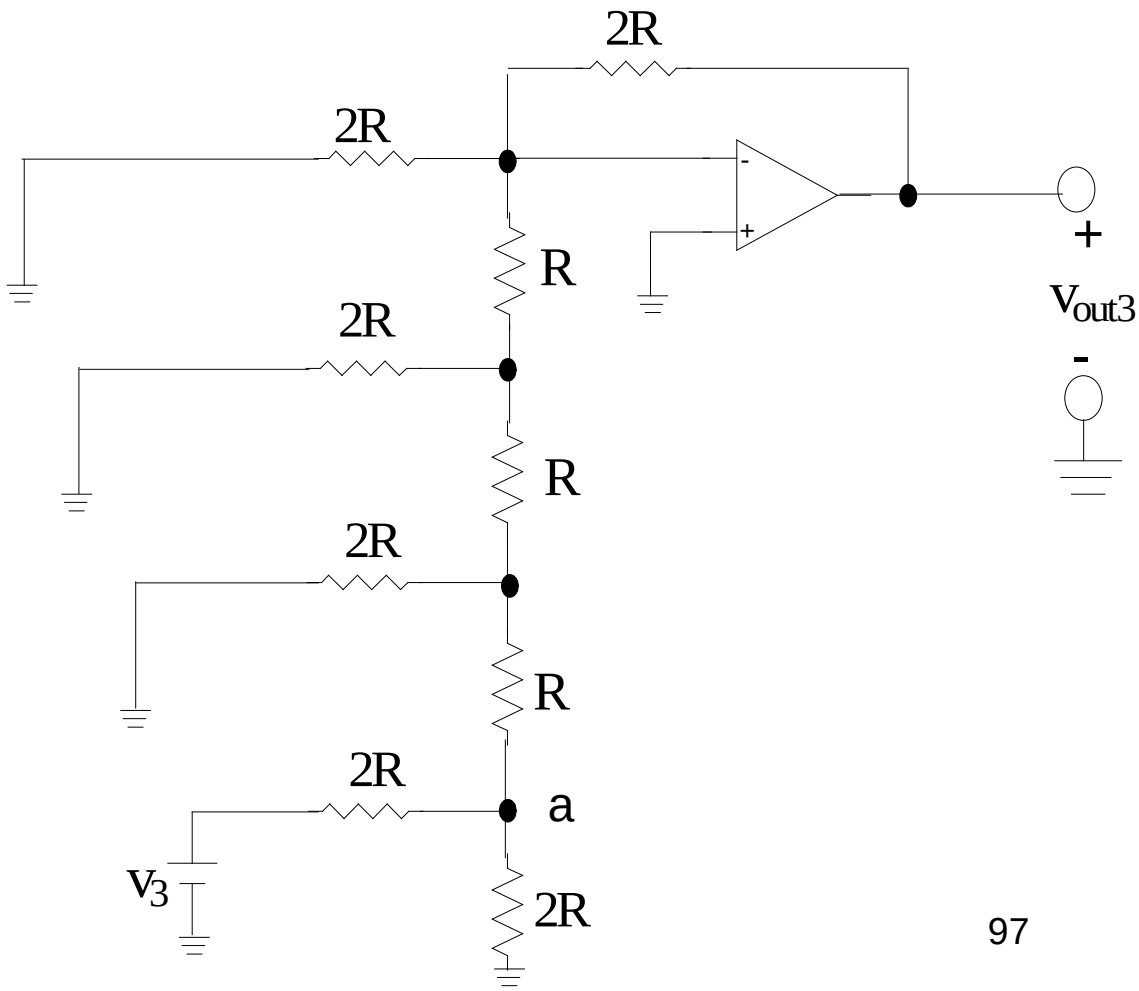
Now writing an expression for v_{out}
In terms of v_2 using the virtual ground and noting
No current will flow in the resistor to v_0's
Suppressed source (2R) we get:

$$v_{out} = v_{out2} = -\frac{2R}{2R}\frac{v_2}{4} = -\frac{v_2}{4}$$

v_2 is either +5V or 0V

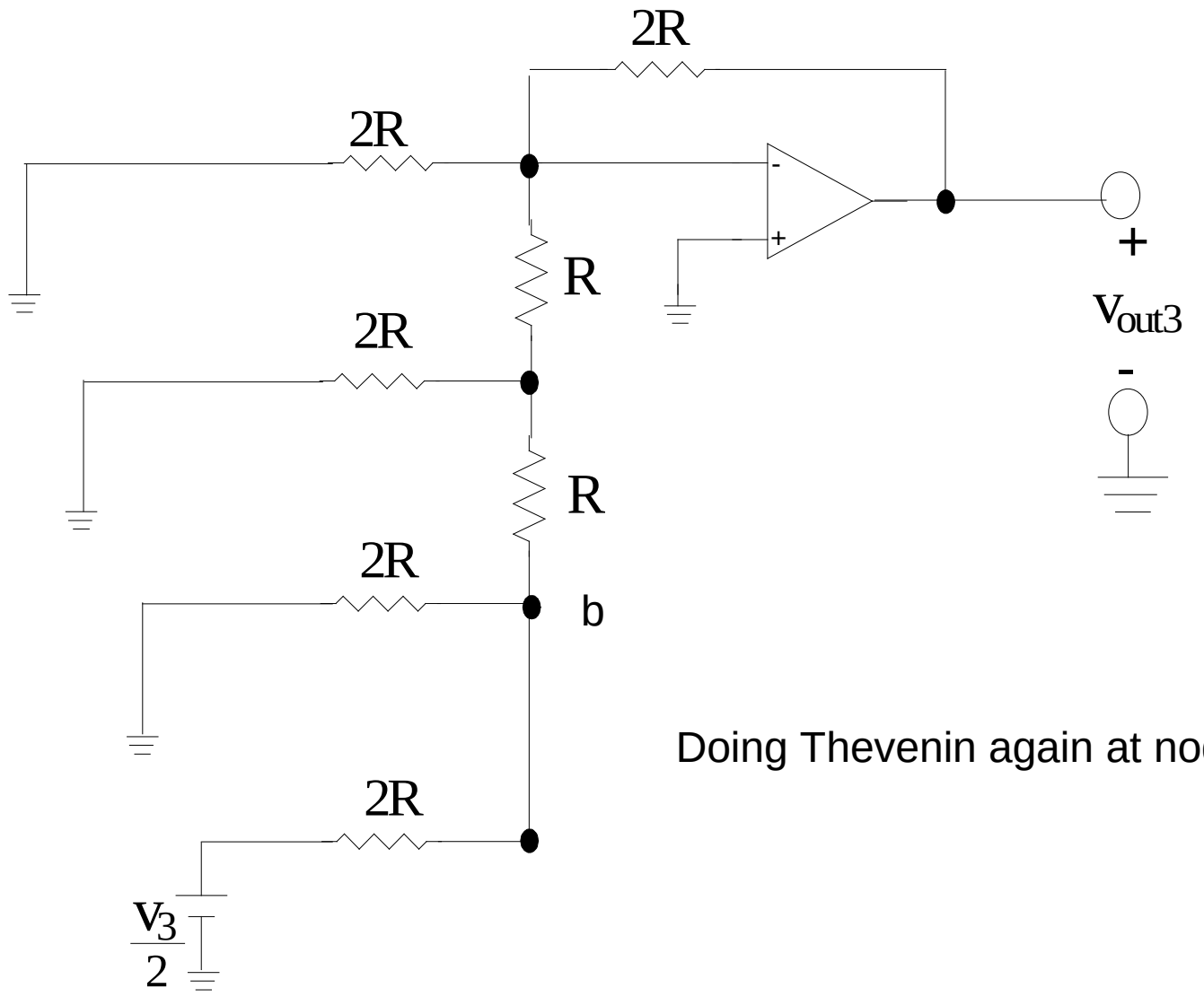
Digital to Analog Converters
R/2R ladder D/A

With v_0, v_1 & v_2 suppressed:



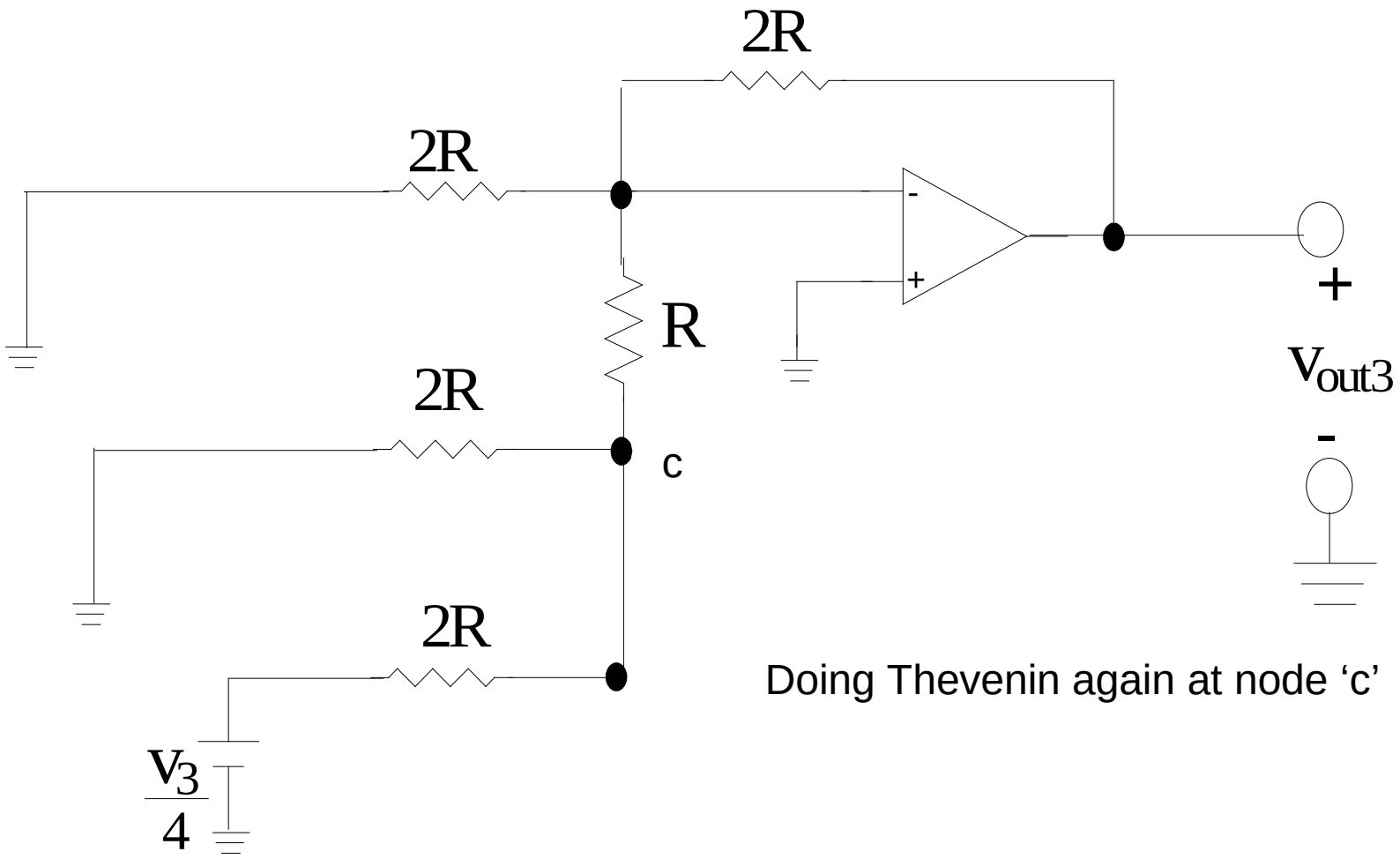
Calculating Thevenin
Equivalent at node ‘a’
To ground

Gives:



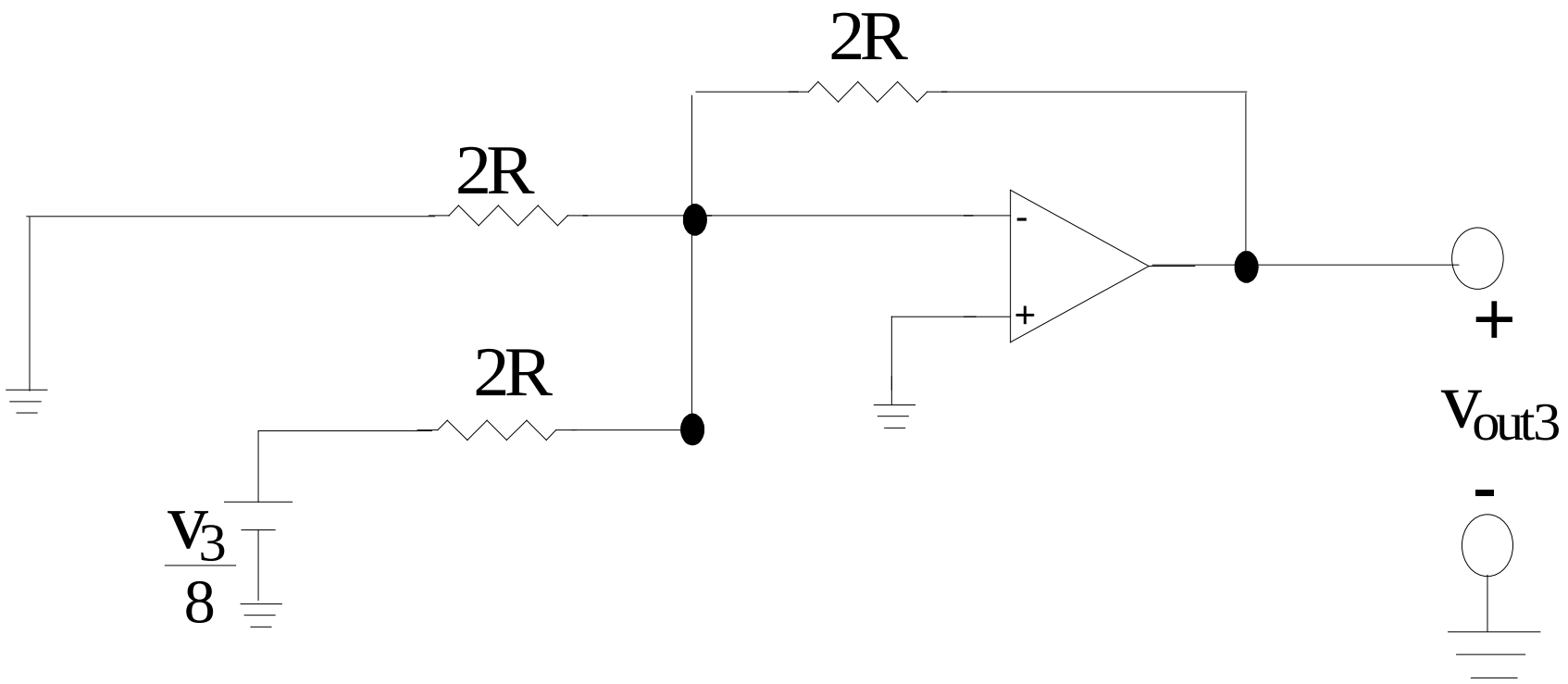
Doing Thevenin again at node ‘b’

Gives:

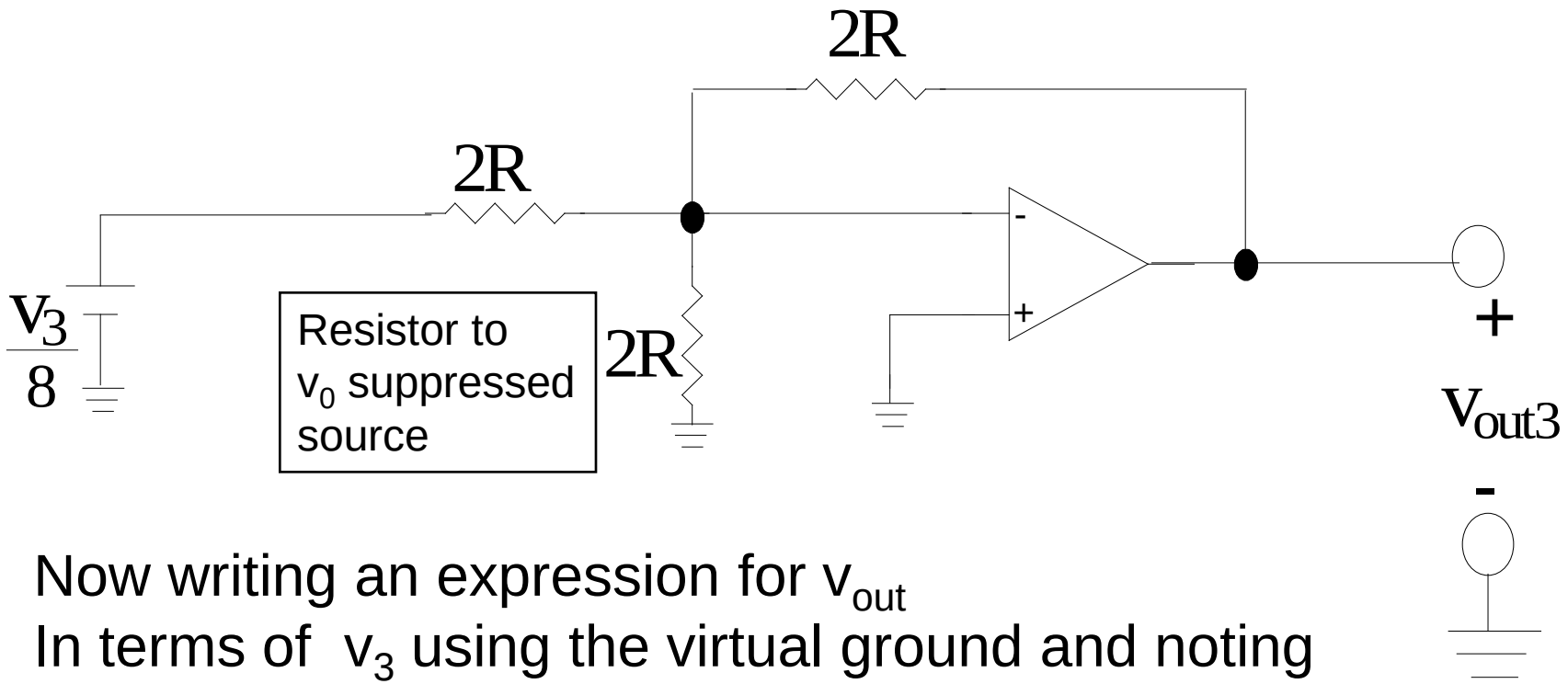


Doing Thevenin again at node ‘c’

Gives:



Redrawing:



Now writing an expression for v_{out}
In terms of v_3 using the virtual ground and noting
No current will flow in the resistor to v_0's
Suppressed source (2R) we get:

$$v_{out} = v_{out3} = -\frac{2R}{2R}\frac{v_3}{8} = -\frac{v_3}{8}$$

v_3 is either +5V or 0V

Digital to Analog Converters
R/2R ladder D/A

Summing all the contributions we get:

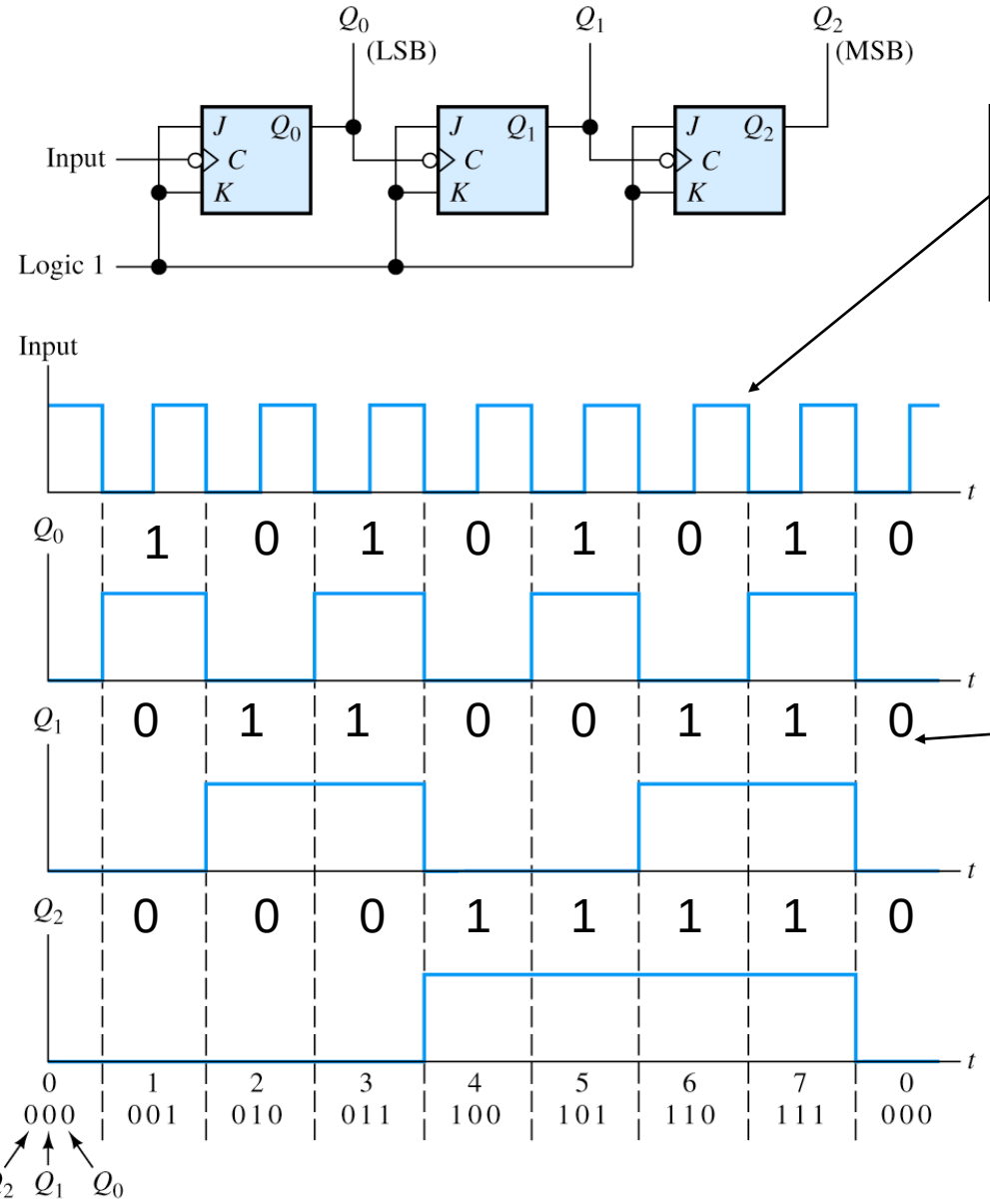
$$v_{out} = v_{out0} + v_{out1} + v_{out2} + v_{out3}$$

$$v_{out} = -v_o - \frac{v_1}{2} - \frac{v_2}{4} - \frac{v_3}{8}$$

Registers (see ECTE233)

- Registers can be considered to be groupings of flip flops/ bistables
- Each flip-flop in the register represents 1 bit
- When the flip flops state is changed this represents the storing of a bit (either its reset (0) or set(1))
- Thus each flip flop in a register of flip flops stores the data (for example 8 bits needing 8 flip flops) for some ‘short’ period of time (till the next Set or Reset command is received from another ‘write’ command)
- Of course using a lot of flip-flops would be wasteful, so registers and counters are available with the flip flops built in
- We should note that a **flip flop** on its own is an **asynchronous device** ie we do not know when the Set / Reset inputs will occur in time
- A system where we know when a state change is possible for a circuit element is known as a synchronous system and typically has a ‘clocked’ or periodic pulsed input

Counters (see ECTE233)



Ripple counter.

Cousin of shift register as now
We are counting clocked pulses
On falling edge of clock!

Roll's over back to '000'

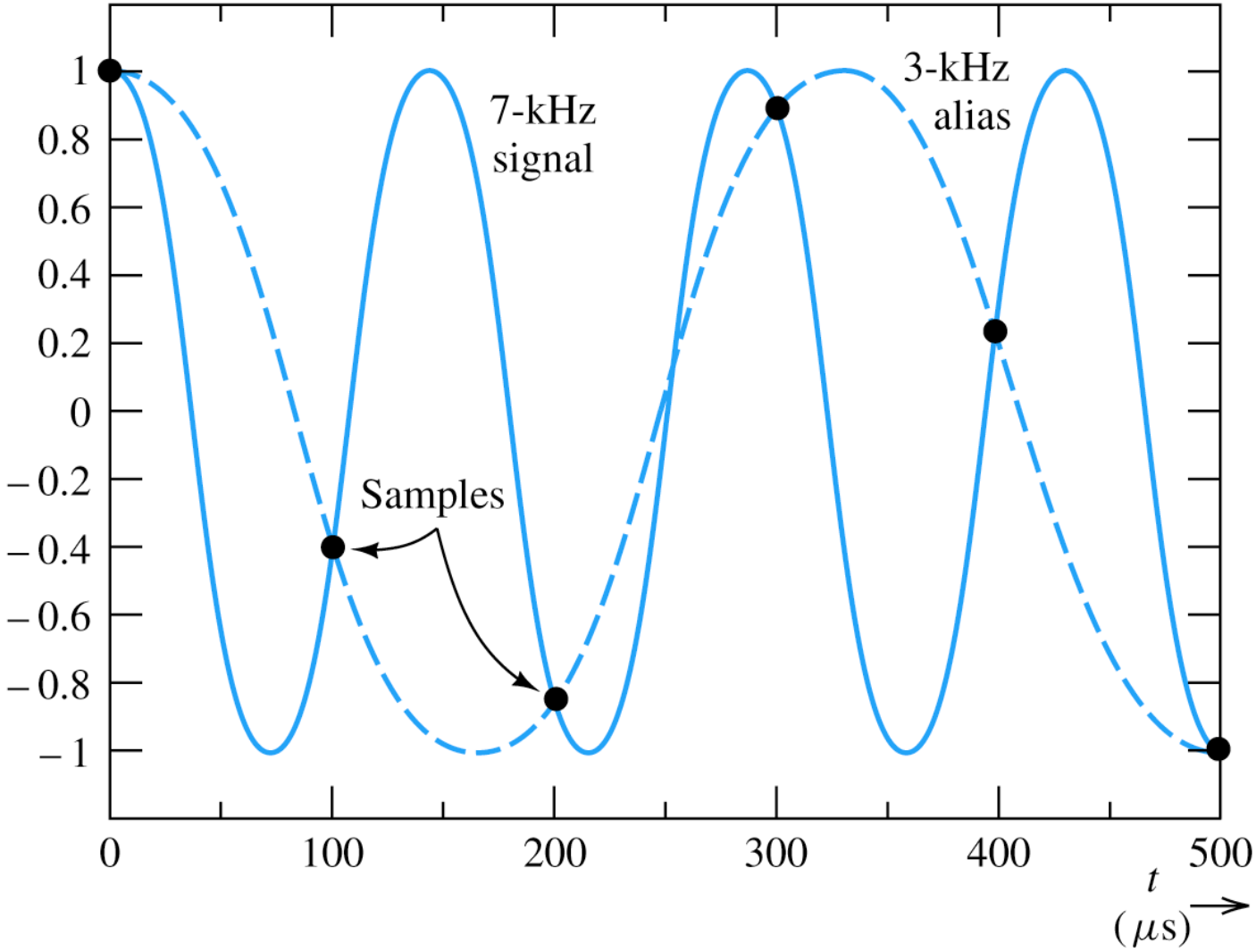
Sampling Theorem

If a signal contains no components with frequencies higher than f_H , all of the information contained in the signal is present in its samples, provided that the sampling rate is selected to be more than twice f_H .

$$f_S \geq 2 f_H$$

ANALOG-TO-DIGITAL CONVERSION

Analog-to-digital conversion is a two-step process. First, the signal is sampled at uniformly spaced points in time. Second, the sample values are quantised so they can be represented by words of finite length, for example 8 bits.



When a 7-kHz sinusoid is sampled at 10 kHz, the sample values appear to be those of a 3-kHz sinusoid.

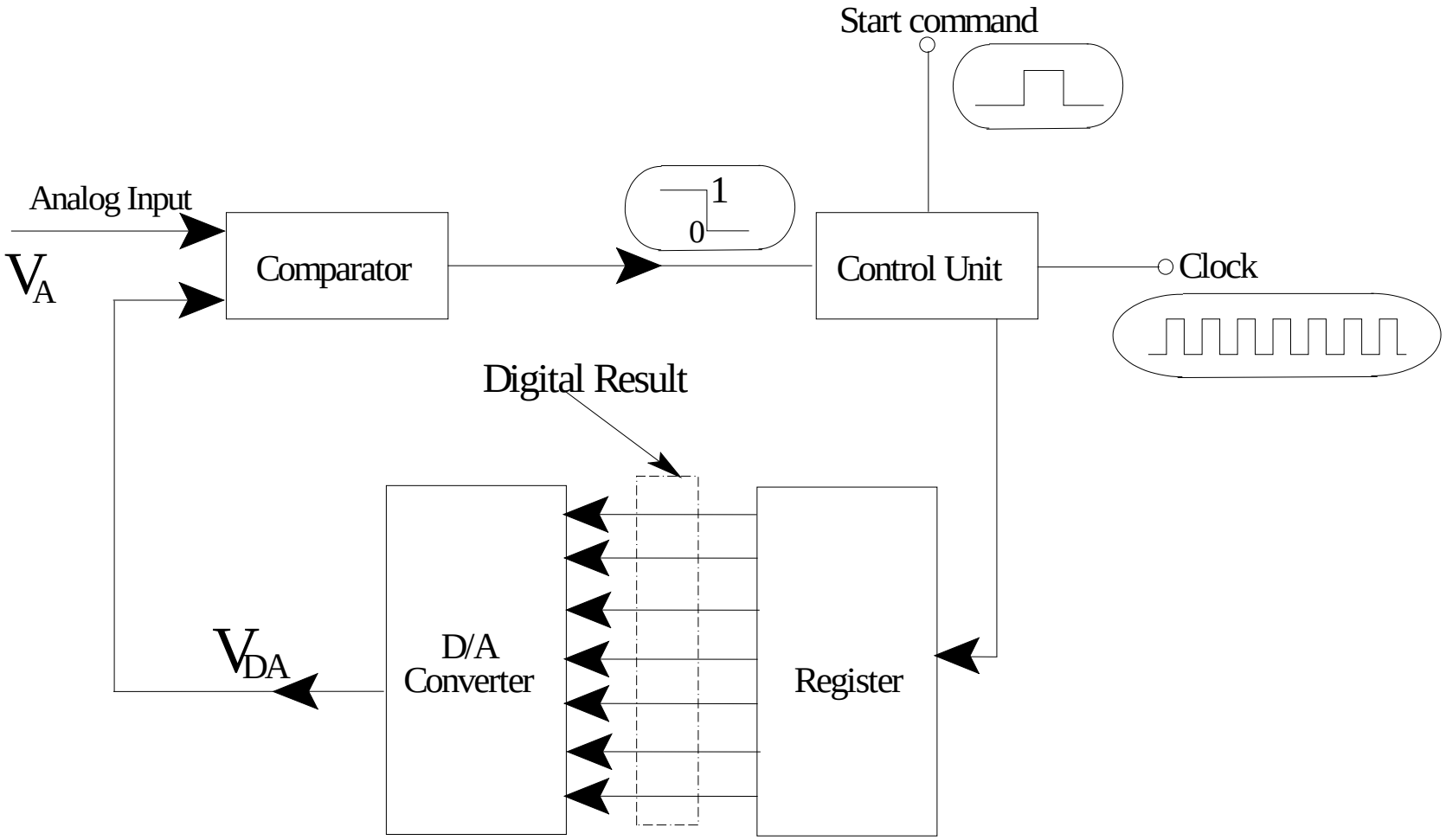
As a result before we sample any waveform
We should ensure that the frequencies
At the analog input are at most half frequency
At which the signal is to be sampled!

We most often do this by using a Low Pass Filter as an **anti-aliasing filter**, ie we Filter out or attenuate all frequencies above Half the sampling frequency:

ANALOG-TO-DIGITAL CONVERSION

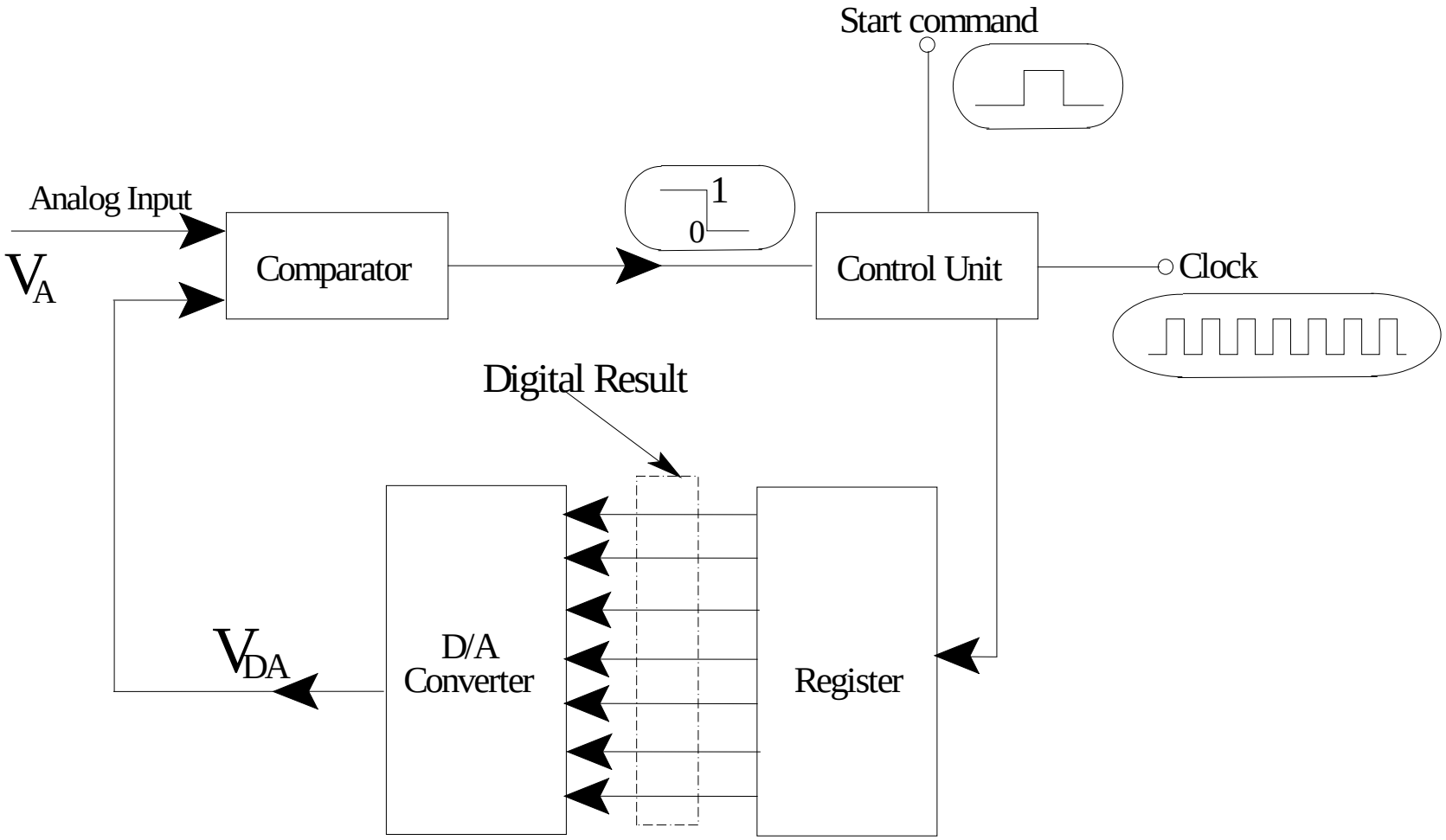
- The analogue to digital converter (A/D converter or ADC) samples an analog signal to produce a digital output code
- Due to the process there is a significant delay between sampling the analog input signal and presentation of the resultant digital output code
- Often these are built into IC’s
- A Common form for the ADC is the successive approx. device

ANALOG-TO-DIGITAL CONVERSION



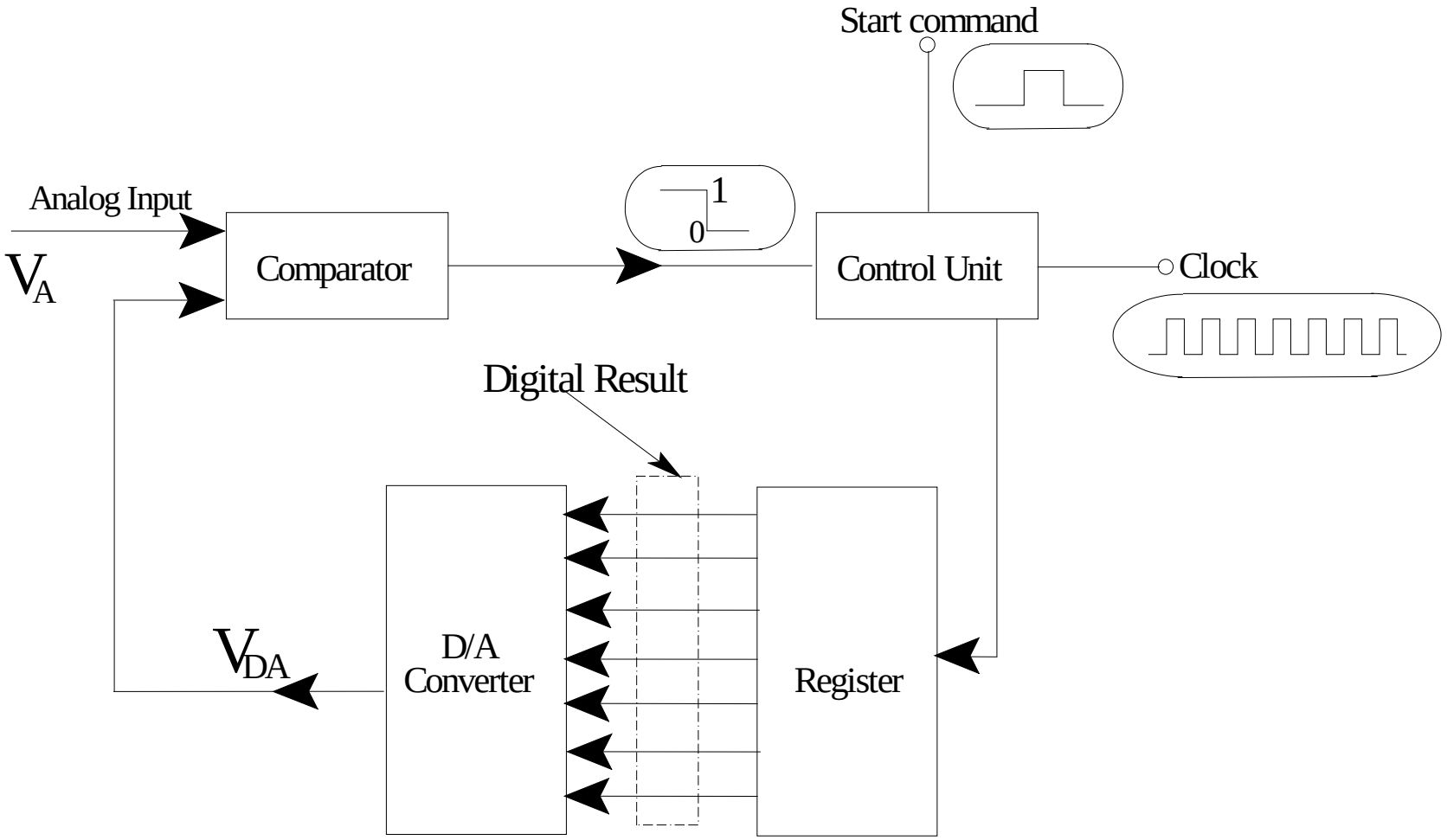
- Works by comparison of the analog input with the output of the Digital to Analog converter

ANALOG-TO-DIGITAL CONVERSION



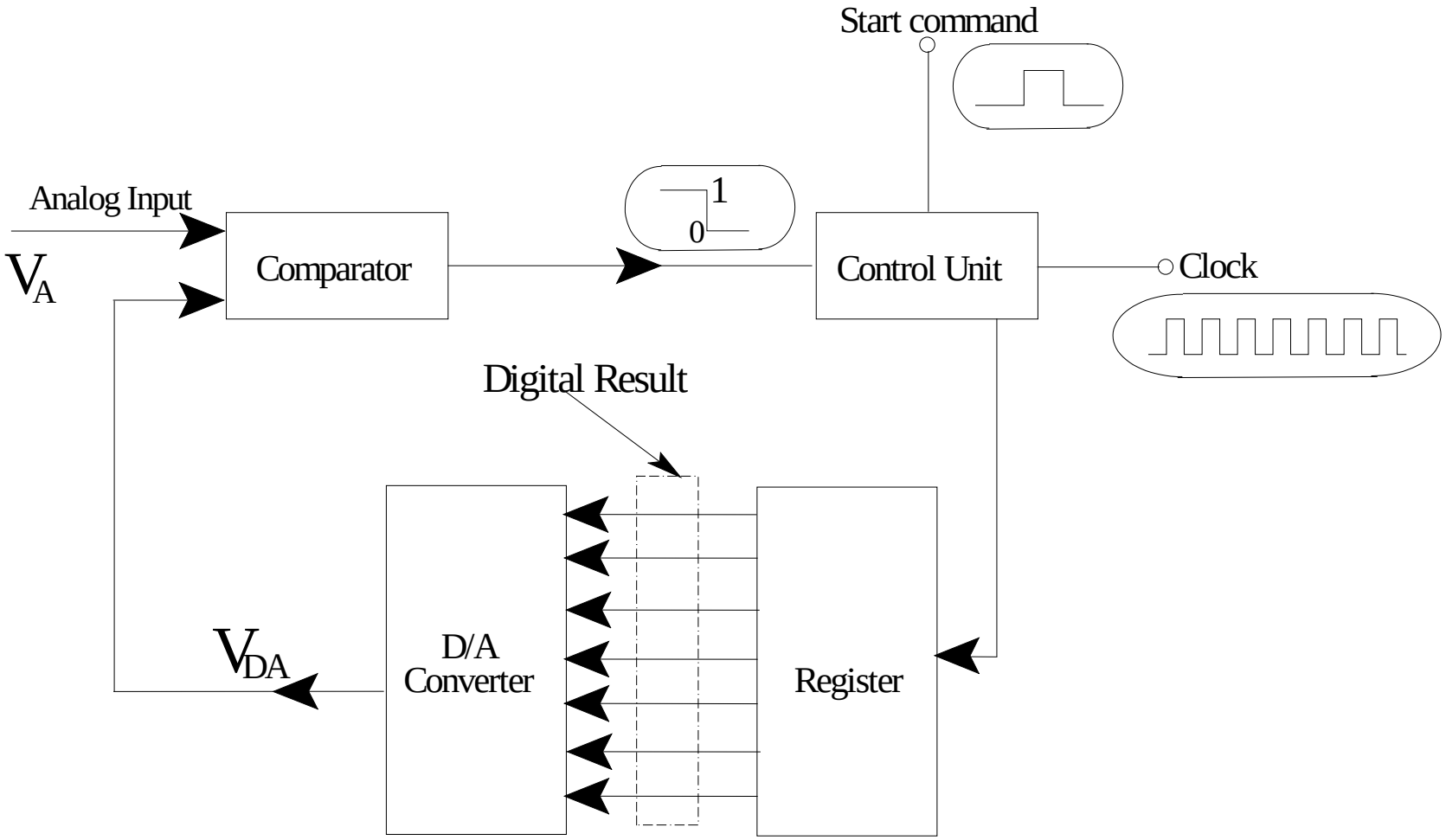
- The control unit has three inputs, a start command, the output of the comparator and a clock input
- It contains logic which is triggered by the start command (possibly a state machine with flip flops for memory of state)

ANALOG-TO-DIGITAL CONVERSION



- The clock input determines the rate at which data is sent to the register which holds a binary number that is then both converted to an analog signal and used as the result when the comparator output indicates the process is complete

ANALOG-TO-DIGITAL CONVERSION



For the comparator we can identify the following:

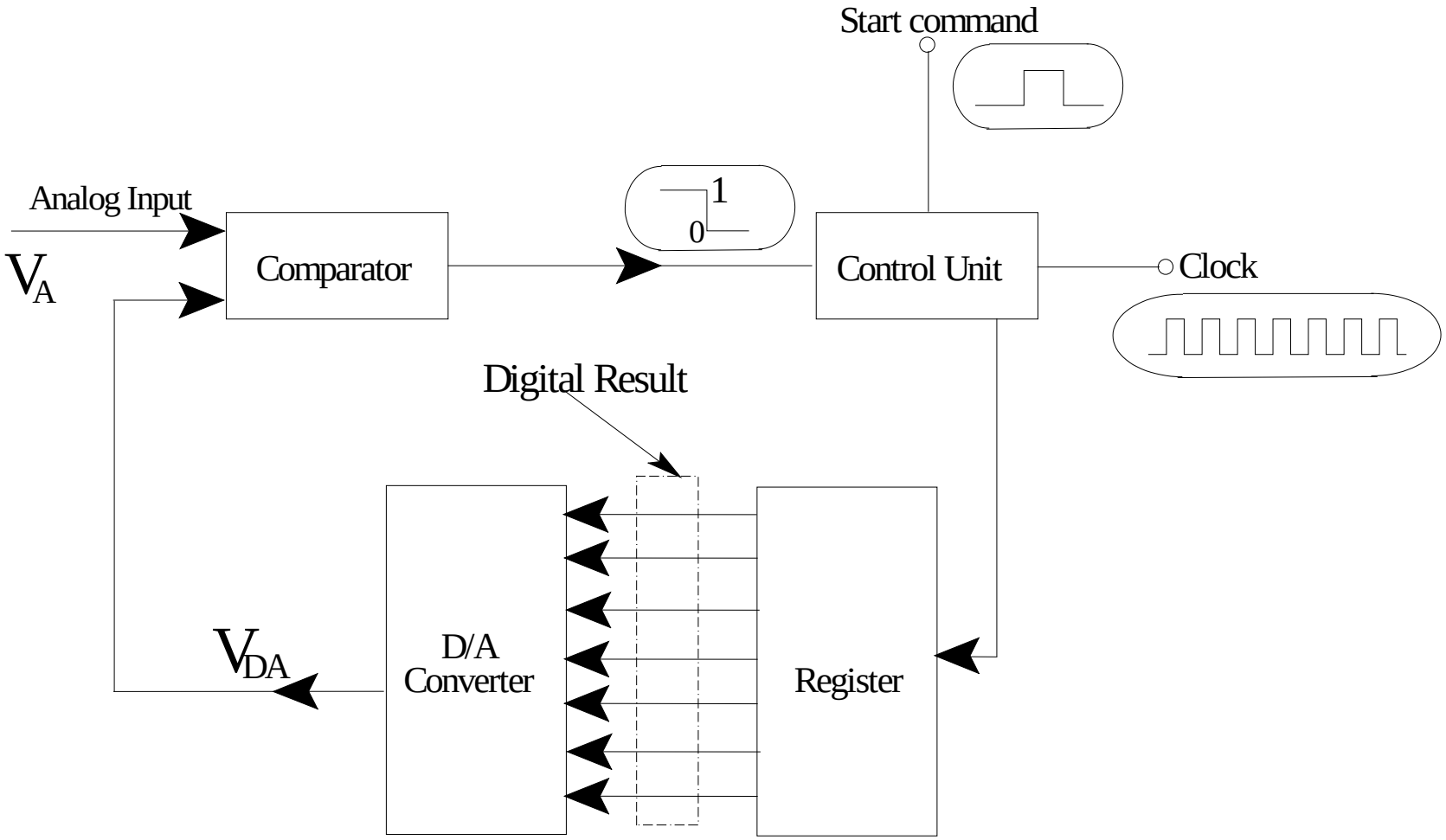
If $V_{DA}<V_A$ the comparator output is HIGH

If $V_{DA}=V_A$ the comparator output is LOW

If $V_{DA}>V_A$ the comparator output is LOW

If the comparator output is LOW then the comparator Stops the process of modifying the binary number stored in the register!

ANALOG-TO-DIGITAL CONVERSION



For the comparator we can identify the following:

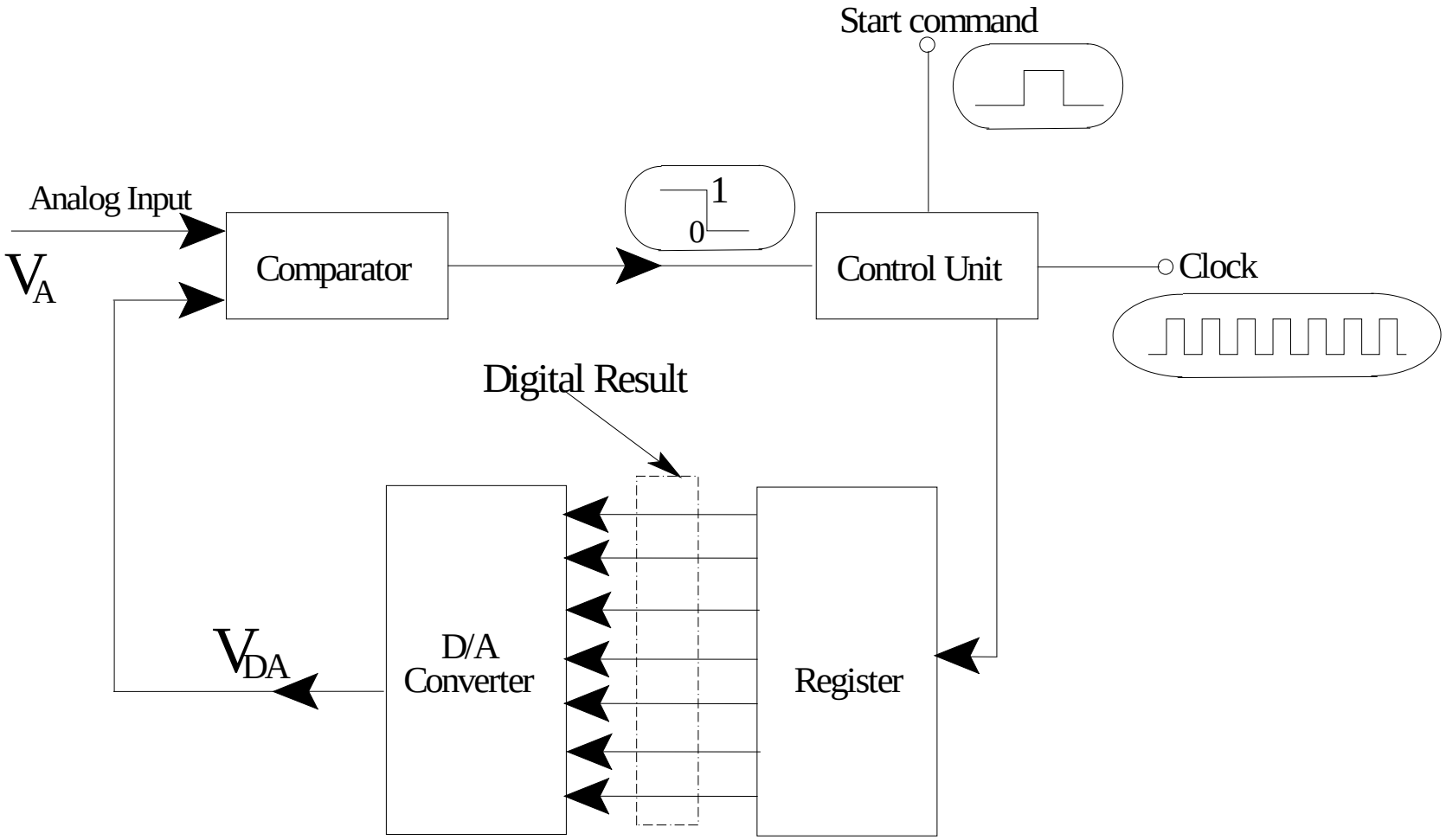
If $V_{DA}<V_A$ the comparator output is HIGH

If $V_{DA}=V_A$ the comparator output is LOW

If $V_{DA}>V_A$ the comparator output is LOW

If the comparator output is LOW then most likely the value in the Register is close to the analog Input value V_A

ANALOG-TO-DIGITAL CONVERSION



For the comparator we can identify the following:

If $V_{DA}<V_A$ the comparator output is HIGH

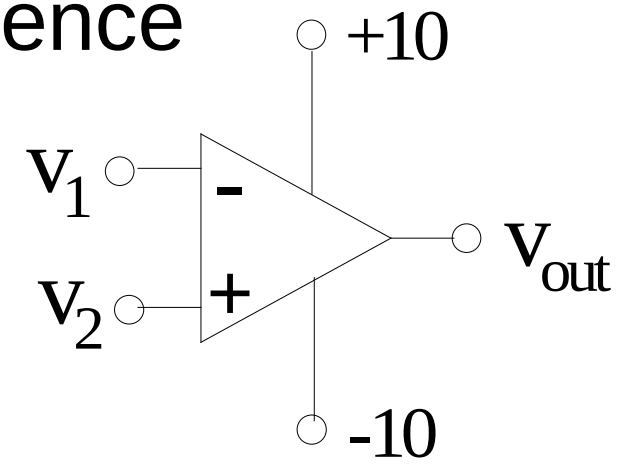
If $V_{DA}=V_A$ the comparator output is LOW

If $V_{DA}>V_A$ the comparator output is LOW

If the comparator output is HIGH then the process of modifying the binary number stored in the Register continues

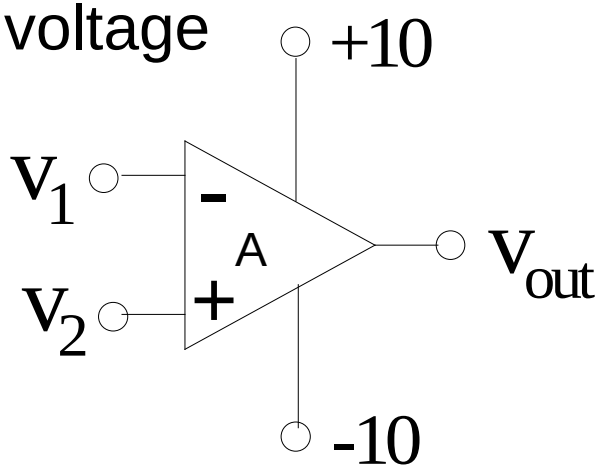
Simple Comparator

- We can implement the comparator using an op-amp in its high gain differential mode
- High gain is important since we want to obtain the required output from the smallest possible input difference



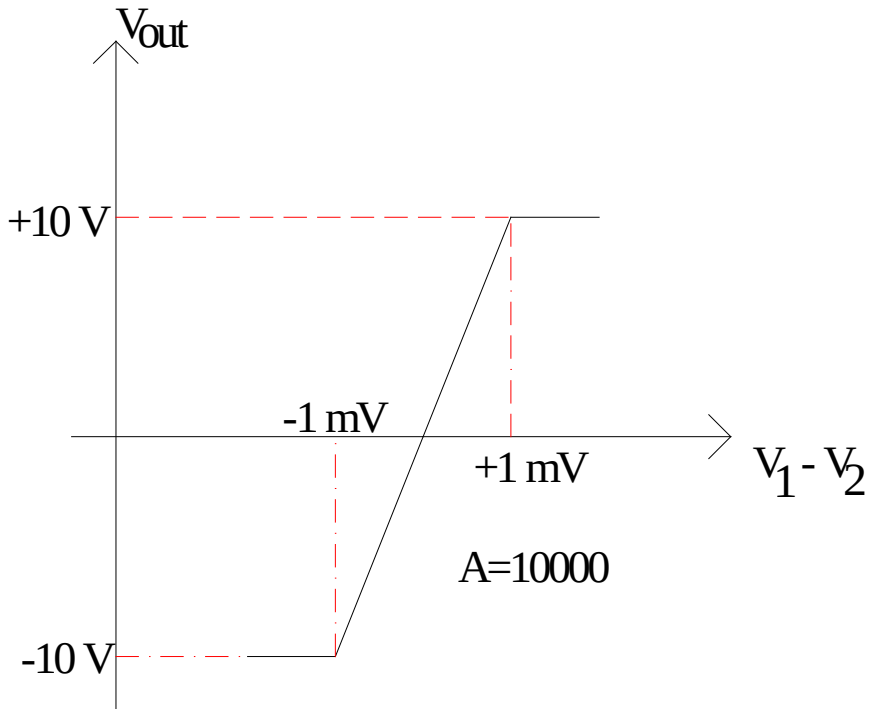
Simple Comparator

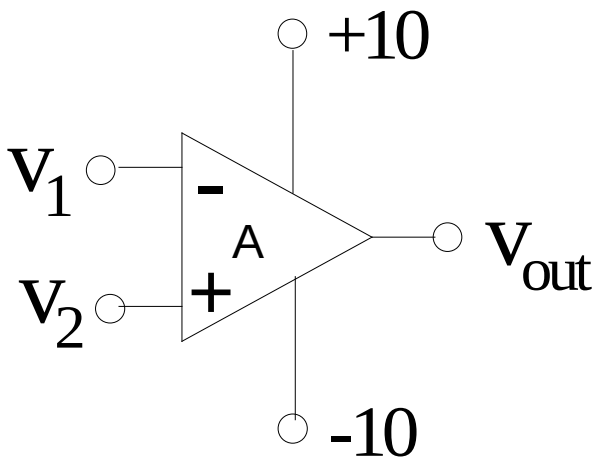
- For the circuit shown we would have an output of either +10 or -10 Volts for large gain A (in ideal case this is INFINITE!)
- This amplifies (in open loop) the difference between the two inputs (see week 10 lecture)
- When the difference between V_1 and V_2 is so small that the output lies between the two voltage rails we say that it is below the '<u>threshold voltage</u>' ie the voltage where the output 'saturates' to the applied rail voltage



Simple Comparator

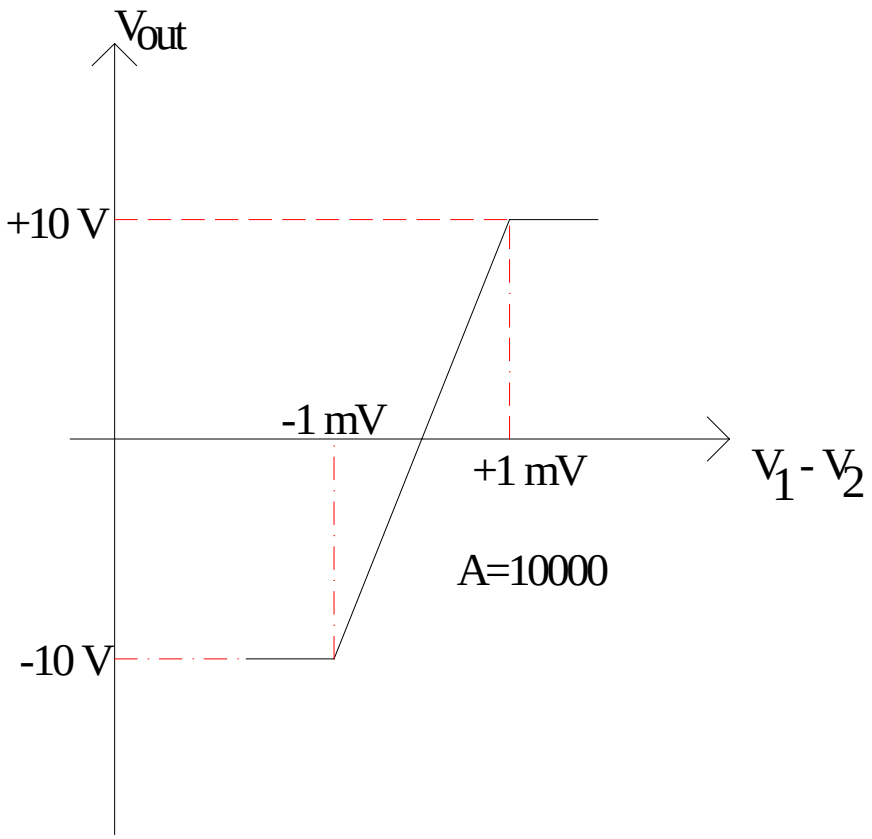
- If the difference between V_1 and V_2 is less than the value of the threshold voltage then the output is equal to the open loop gain A times the difference between the input voltages
- Assuming A=10000 we can draw the v_{out} vs V_1-V_2 characteristic:





Simple Comparator: Example

A comparator has the output/input characteristic:



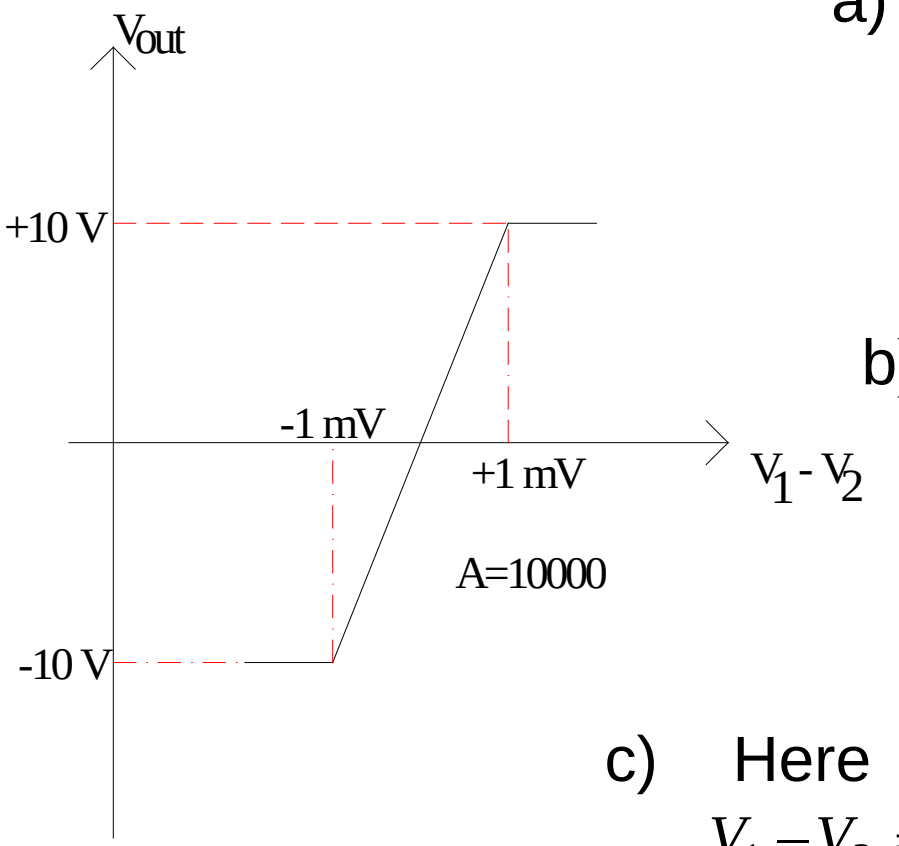
Determine:

a) The threshold voltage

b) The output voltage for V_1=7.5750 V and V_2=7.5745 V

c) The output voltage for V_1=6.550 V and V_2=6.600 V

Simple Comparator: Answer



a) The Threshold voltage is 1 mV since V_{out} saturates at 10 V when $V_1 - V_2 \geq 1 \quad mV$

b) Here

$$V_1 - V_2 = 7.5750 \quad - \quad 7.5745 \quad = \quad 0.5 \quad mV$$

which is less than the threshold voltage, thus:

$$V_{out} = A(V_1 \quad - \quad V_2) = +5 \quad V$$

c) Here

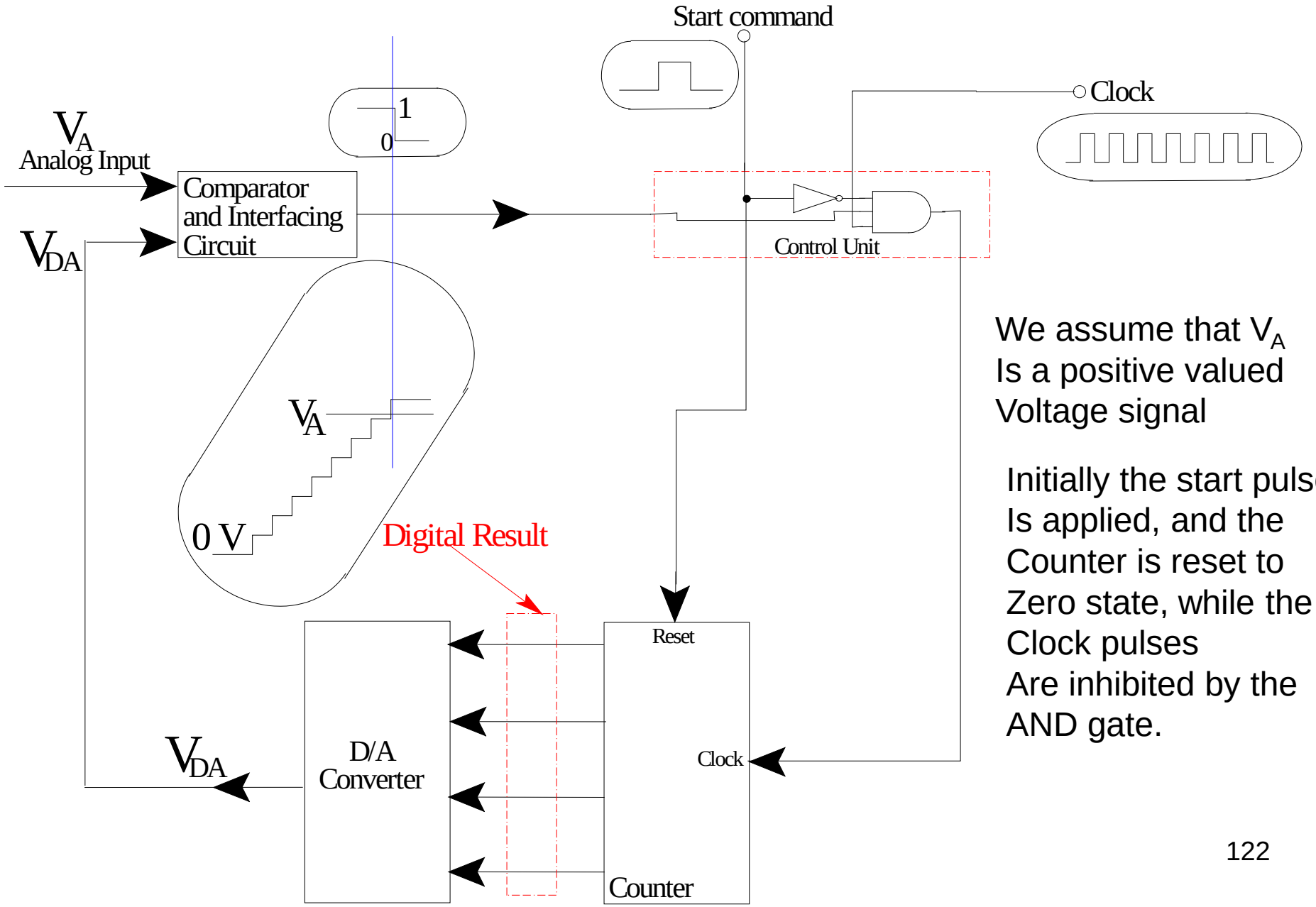
$$V_1 - V_2 = 6.550 \quad - \quad 6.600 \quad = \quad -50 \quad mV$$

which is greater than the threshold voltage, thus: $V_{out} = -10 \quad V$

Digital Ramp A/D Converter

- Based on Successive Approximate ADC but uses a counter instead of a Register
- Its output characteristic looks like a ramp
- Here we assume that the start pulse will also reset the counter
- An AND gate is used which will have three inputs, one from the start pulse ensures that the counter starts at zero and no false clock signals affect the counter while its being reset (to all zero count)
- The other input for the AND gate is the output of the comparator after the voltage has been changed to 0 to 5 Volt level by an interfacing circuit (using either a transistor or a Diode and Zener Diode with a voltage buffer as we will see in the EWB simulation)

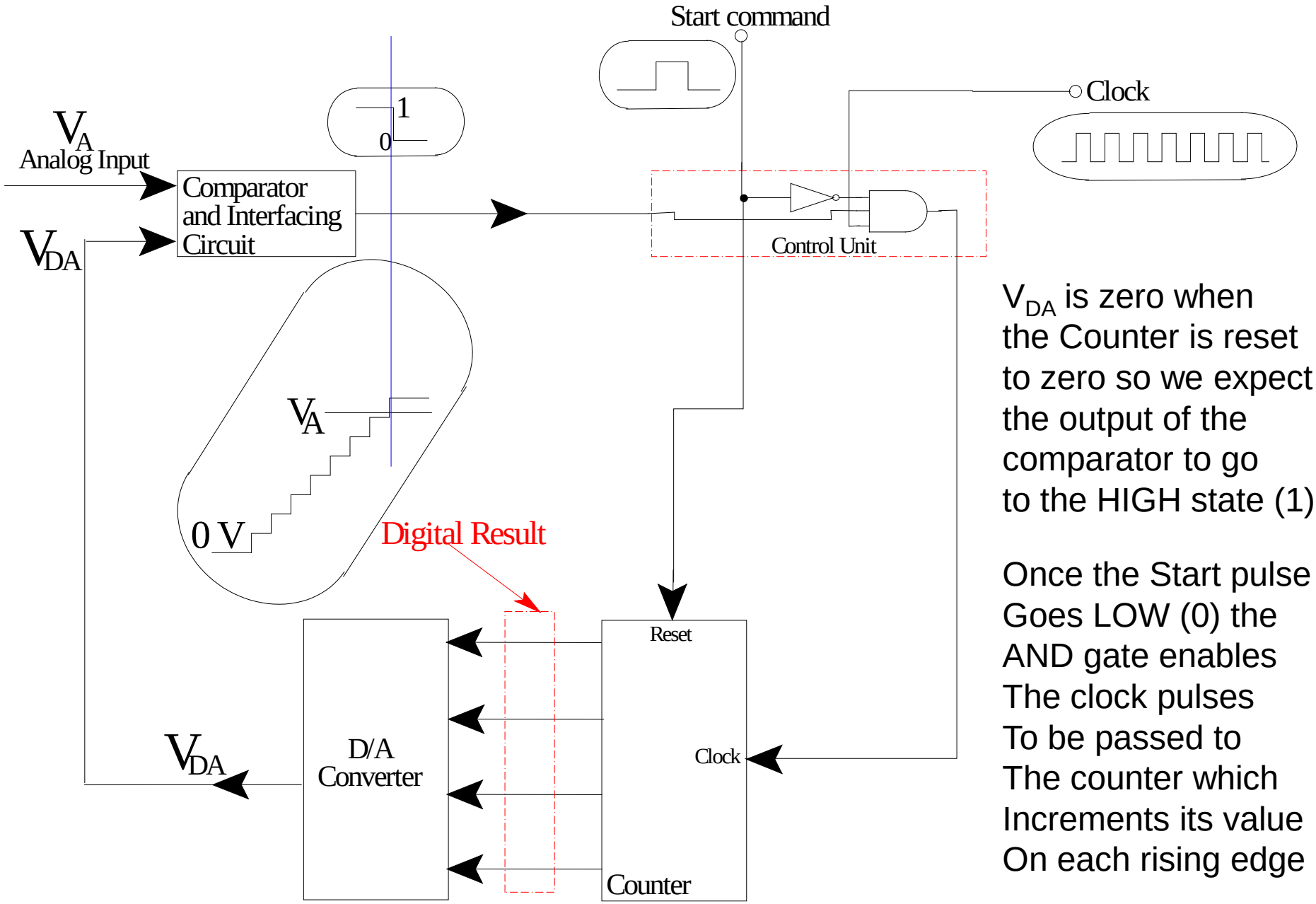
Digital Ramp A/D Converter



We assume that V_A Is a positive valued Voltage signal

Initially the start pulse Is applied, and the Counter is reset to Zero state, while the Clock pulses Are inhibited by the AND gate.

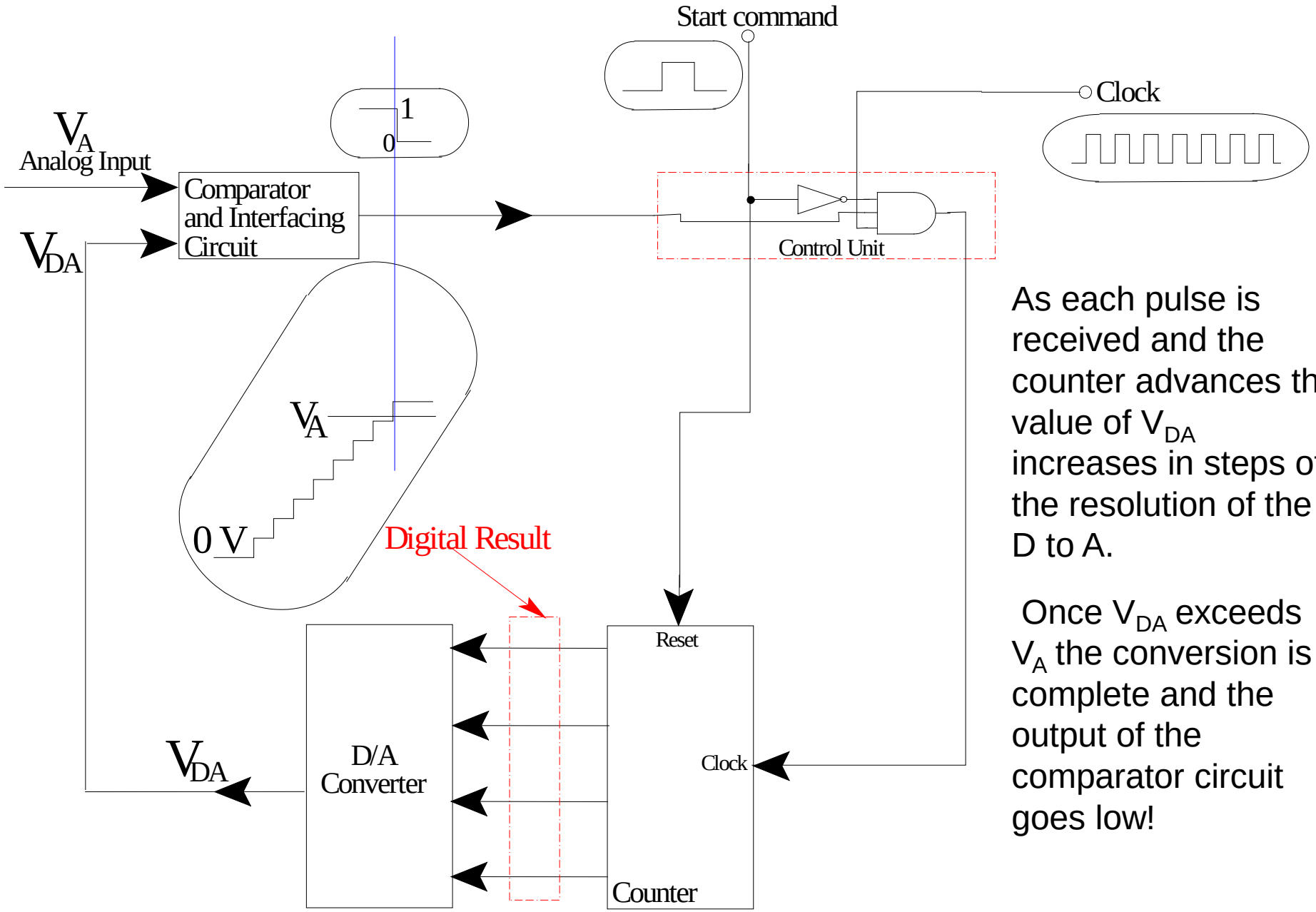
Digital Ramp A/D Converter



V_{DA} is zero when the Counter is reset to zero so we expect the output of the comparator to go to the HIGH state (1)

Once the Start pulse Goes LOW (0) the AND gate enables The clock pulses To be passed to The counter which Increments its value On each rising edge

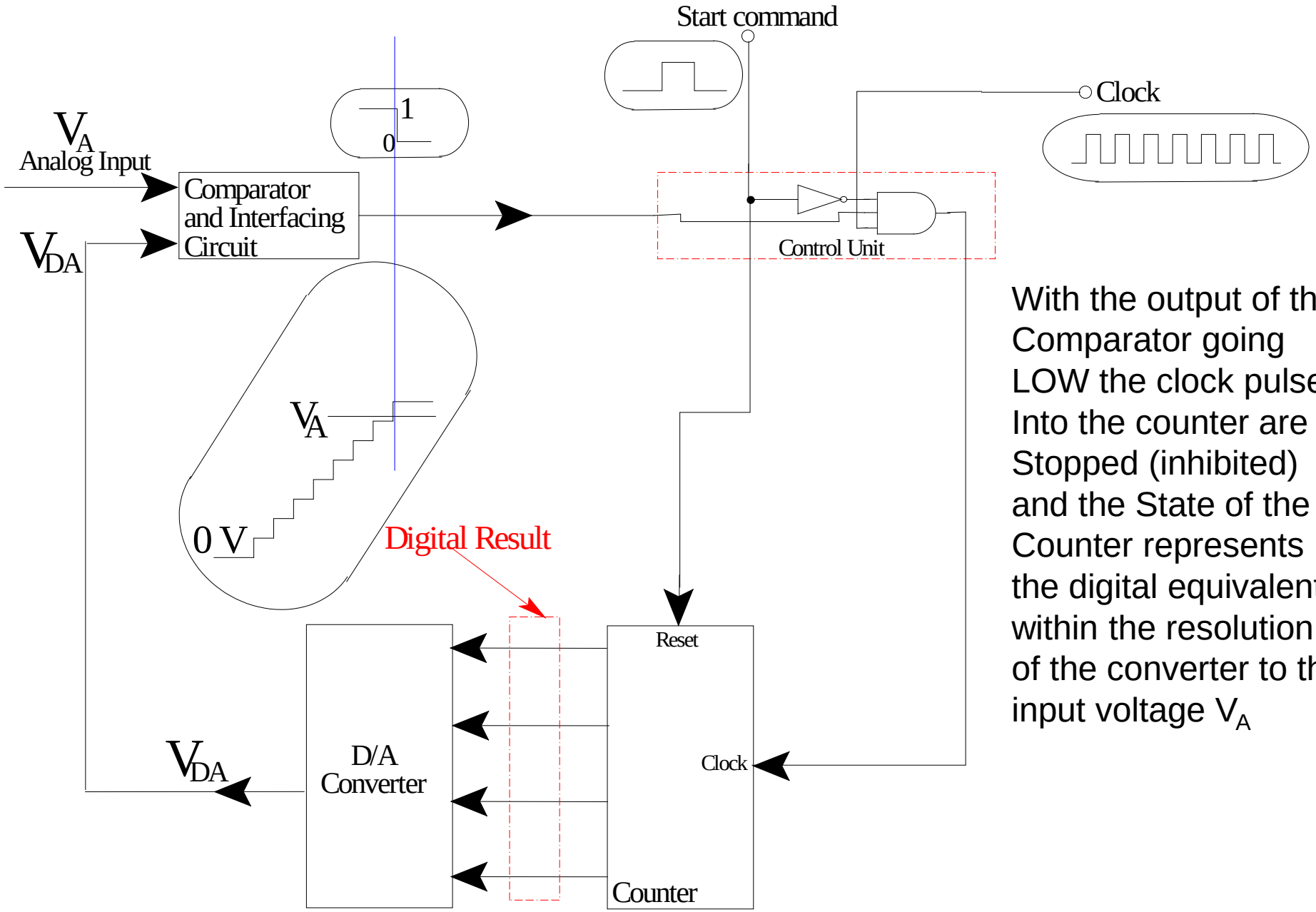
Digital Ramp A/D Converter



As each pulse is received and the counter advances the value of V_{DA} increases in steps of the resolution of the D to A.

Once V_{DA} exceeds V_A the conversion is complete and the output of the comparator circuit goes low!

Digital Ramp A/D Converter



With the output of the Comparator going LOW the clock pulses Into the counter are Stopped (inhibited) and the State of the Counter represents the digital equivalent within the resolution of the converter to the input voltage V_A

Simulation: Digital Ramp A/D converter

- We have an EWB simulation to demonstrate!
- Name: \ewb5\comparatorforadcc.ewb
- ‘R’ resets the counter
- ‘Space Bar’ switches between 5V and 3V signal for V_A

Example

An A/D converter has a clock frequency of 100 kHz. The full scale output of the D/A is 8.255 Volts with a 8-bit input. The comparator threshold voltage is 1mV. If V_A=4.528 Volts determine:

a) The digital number obtained from the counter

b) The conversion time

c) The converter resolution

Answer

a) The digital number obtained from the counter

We have an 8-bit input thus total possible steps is:

$$2^{n-1}-1=2^{8-1}-1=128-1=127$$

With the full scale voltage being 8.255 volts then step size Is given by:

$$\frac{full\quad scale\quad voltage}{number\quad of\quad steps}=\frac{8255}{127}=65\quad mV$$

Given V_A=4.528 V and that the threshold voltage is 1mV then V_{DA} must be 4.529 V or more before a comparator change in state is possible, which means that the voltage will need to rise to the largest nearest multiple of 65mV which is 4550 mV and then the number of steps needed is:

$$\frac{4550}{65}=70\quad steps$$

Answer

a) The digital number obtained from the counter

Hence the digital number at the output of the A/D will be 70 or in 8 bit binary 01000110

b) The conversion time

We have a clock frequency of 100kHz or 10μsec between pulses, so the time taken is simply 70 times 10 μsec or 700 μsecs, the maximum time is the maximum count, which here Would be 127 times 10μsec or 1.27ms

c) The converter resolution

We find resolution from the step size of the D/A which here is 65mV. This can also be expressed as a percentage:

$$\frac{65}{8255} \times 100 = 0.79\%$$

Errors due to resolution have a Special name → Quantisation error!