UNIVERSITY OF WOLLONGONG IN DUBAI

ECTE250

ENGINEERING DESIGN AND MANAGEMENT 2

Winter 2025 / Spring 2025

Practical Electronics 3

Outline

- Issues with Digital IC's
- Schmitt Trigger
- Debouncing Circuits
- External Asynchronous Control Signal
- Super Diodes
- 4 bit Digital to Analog op-amp converters
- 4 bit successive approximation Analog to Digital

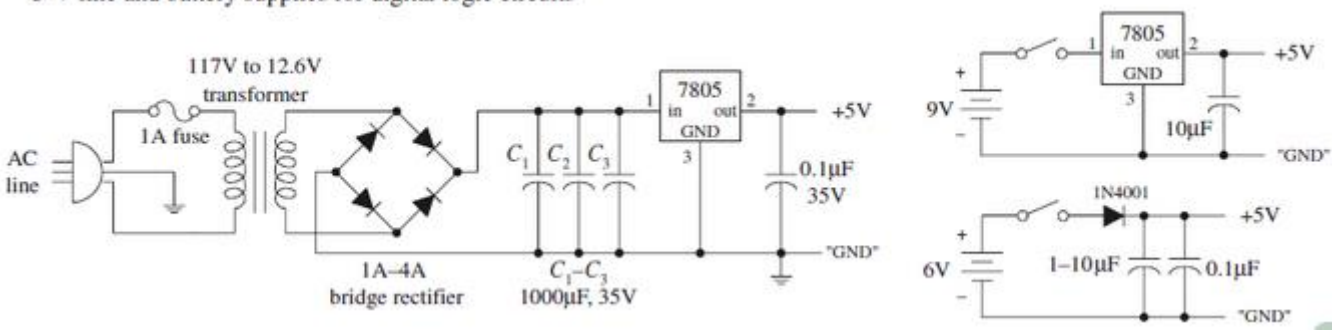
Issues with Digital IC's

- As most of you have done ECTE233, I'll expect that you have some knowledge of digital circuits.
- However, there are things which you should keep in mind, especially when building large projects that have a large digital switching component (which to some extent the ECTE250 project will have).
- Next slides are from Chapter 12 of "Practical Electronics for Inventors" to show important practical aspects of the design **which have nothing to do with functionality directly**!

Powering and Testing Logic IC's

- Most TTL and CMOS logic devices will work with 5 *V* ± 0.25 *V* (5 percent) supplies like the ones shown above
- The battery supplies should be avoided when using certain TTL families like the 74*xx*, 74S, 74AS, and 74F, which dissipate considerably more current than, say, the CMOS 74HC series (HC here stands for High Speed CMOS TTL compatible family – some of the IC's in the ECTE250 parts is from this family, so possibly not a major concern in your projecy).
- Also, I'm not expecting DC battery supplies in ECTE250 projects, though its not prohibited – it will need to be included in the power budget, though!

5-V line and battery supplies for digital logic circuits



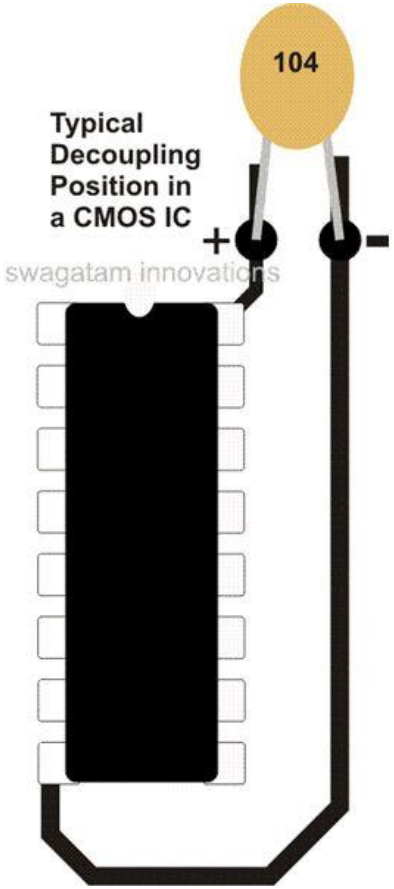
Power Supply Decoupling

- When a TTL device makes a low-to-high or a high-to-low level transition, there is an interval during which the conduction times in the upper and lower totem-pole output transistors overlap.
- During this interval, a drastic change in power supply current occurs, which results in a sharp, high-frequency current spike within the supply line.
- If a number of other devices are linked to the same supply, the unwanted spike can cause false triggering of these devices or it could cause unwanted Electro Magnetic radiation
- To avoid unwanted spikes within TTL systems, ***decoupling capacitors*** can be used.

Power Supply Decoupling

- A ***decoupling capacitor***, typically multilayer ceramic, from 0.01 to 0.1 µF (>5 V), is placed directly across the V_{CC}-to-Ground (GND) pins of each IC in the system.
- The capacitors absorb the spikes and keep the V_{CC} level at each IC constant, thus reducing the likelihood of false triggering and generally EM radiation
- **Decoupling capacitors should be placed as close to the ICs as possible** to keep current spikes local, instead of allowing them to propagate back toward the power supply
- As a rule of thumb you can usually get by with using one decoupling capacitor for every five to ten gates or one for every five counter or register ICs.
- *If in your projects you see unexpected operation and you have not included decoupling capacitors, maybe you should think about using them*, they may save you some time in 'debugging' your circuit, especially at the Perfo Board prototyping stage.

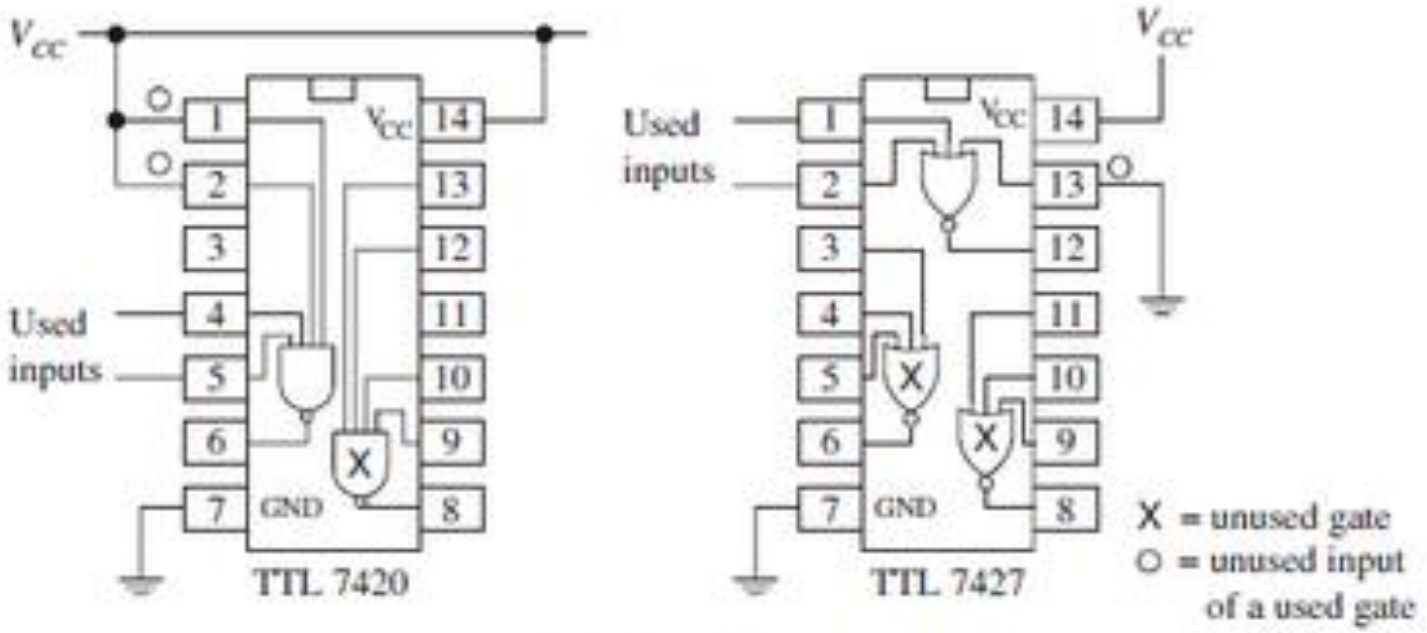
Power Supply Decoupling



Unused Inputs of Used Gates

- If using a logic gate, but don't need all the inputs you need **to ensure that these inputs being left floating do not effect your logical outcome.**
- So the rule is that:
  - Unused inputs that affect the logical state of a chip should not be allowed to float
- Reason:
  - floating inputs are liable to pick up external electrical noise, which leads to erratic output behaviour
- Instead, they should be tied high or low, as necessary
- Examples:
  - a 4-input NAND TTL gate that uses only 2 inputs should have its 2 unused inputs held HIGH to maintain proper logic operation
  - A 3-input NOR gate that uses only 2 inputs should have its unused input held low to maintain proper logic operation
  - the CLEAR and PRESET inputs of a flip-flop should be grounded or tied high, as appropriate

Unused Inputs of Used Gates

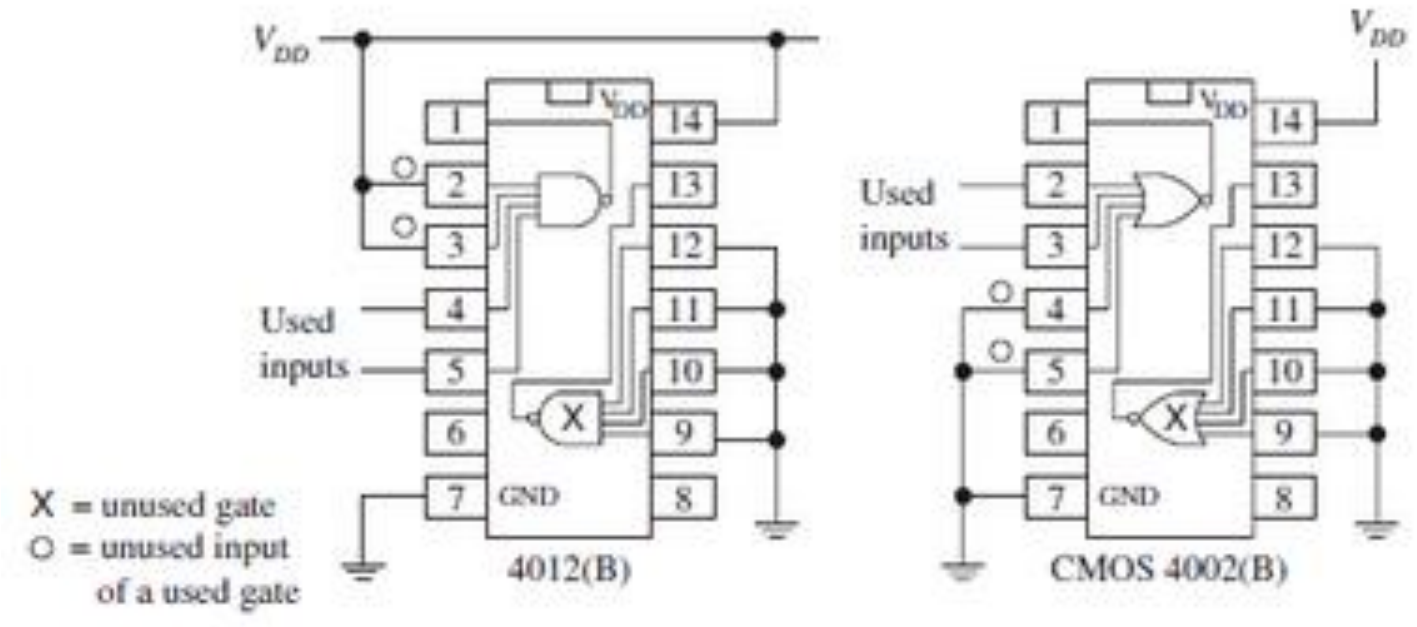


Connect unused inputs of a used NAND gate HIGH to maintain proper logic function. Don't assume they'll be naturally HIGH for TTL. Connect unused input of a NOR gate LOW to maintain proper logic function. Inputs of unused TTL gates can be left unconnected.

Unused Inputs of Unused Gate

- You would think that if your not using a particular gate in an IC package that you can just leave it alone and it will not affect the overall operation of your circuit
- However, you would be totally wrong if using CMOS based technology
- The rule is:
  - **If there are unused sections within an IC, the inputs that link to these sections can be left unconnected for TTL but not for CMOS.**
- When unused inputs are left unconnected in CMOS devices, the inputs may pick up unwanted charge and may reach a voltage level that causes output MOS transistors to conduct simultaneously, resulting in a large internal current spike from the supply (V_{DD}) to ground.
- **The result can lead to excessive supply current drain and IC damage**
- To avoid this fate, inputs of unused sections of a CMOS IC should be grounded
- Another final **important** rule is:
  - **never drive CMOS inputs** when the IC's supply voltage is removed. Doing so can damage the IC's input protection diodes.

Unused Inputs of Unused Gate



Connect unused inputs of a used NAND gate HIGH to maintain proper logic function. Connect unused inputs of a used NOR gate LOW to maintain proper logic function. Inputs of unused CMOS gates should be grounded.

Need to tie all CMOS inputs one way or another (probably to ground), but don't need to worry about the outputs!

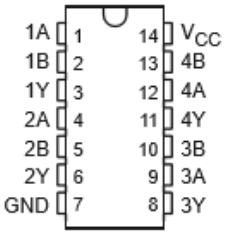
Schmitt Trigger

The part list for for ECTE250 projects include a NAND logic gate with a Schmidtt Trigger for hysteresis.

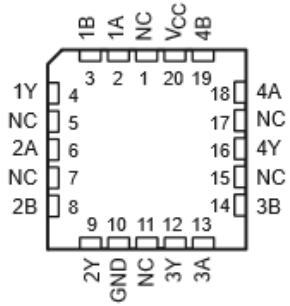
SN54HC132, SN74HC132
QUADRUPLE POSITIVE-NAND GATES
WITH SCHMITT-TRIGGER INPUTS
SCLS034C – DECEMBER 1982 – REVISED MAY 1997

- Operation From Very Slow Input Transitions
- Temperature-Compensated Threshold Levels
- High Noise Immunity
- Same Pinouts as 'HC00
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

SN54HC132 . . . J OR W PACKAGE
SN74HC132 . . . D, DB, OR N PACKAGE
(TOP VIEW)



SN54HC132 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

Each circuit functions as a NAND gate, but because of the Schmitt action, it has different input threshold levels for positive- and negative-going signals. The 'HC132 perform the Boolean function $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

These circuits are temperature compensated and can be triggered from the slowest of input ramps and still give clean jitter-free output signals.

The SN54HC132 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC132 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

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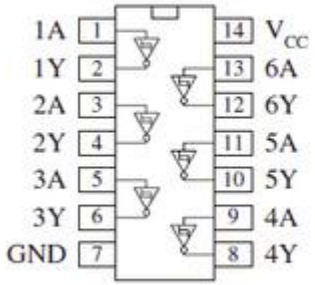
Schmitt Trigger

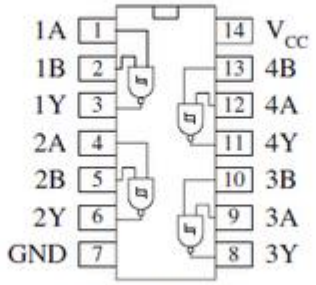
- Schmitt-triggered gates are special-purpose logic gates that come with Schmitt-triggered inputs
- Unlike the conventional logic gates, Schmitt-triggered gates have two input threshold voltages: the *positive threshold voltage* (V_T^+) and the *negative threshold voltage* (V_T^-)
- Examples include:

Hex Schmitt-triggered inverter



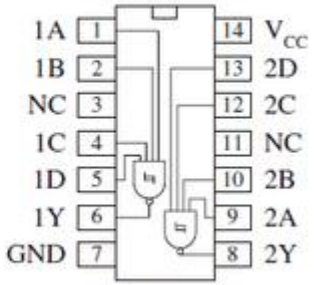
7414, 74LS14, 74F14, 74HC14, etc.

Quad Schmitt-trigger 2-input NAND



74132, 74LS132, 74F132, 74HC132, etc.

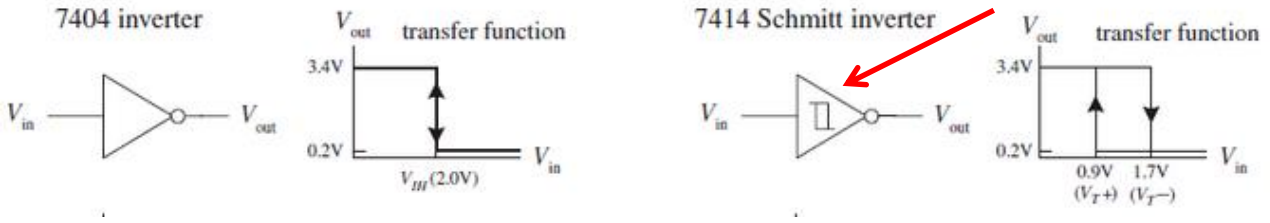
Dual Schmitt-trigger 4-input NAND



7413, 74LS13, 74F13, 74HC13, etc.

Schmitt Trigger

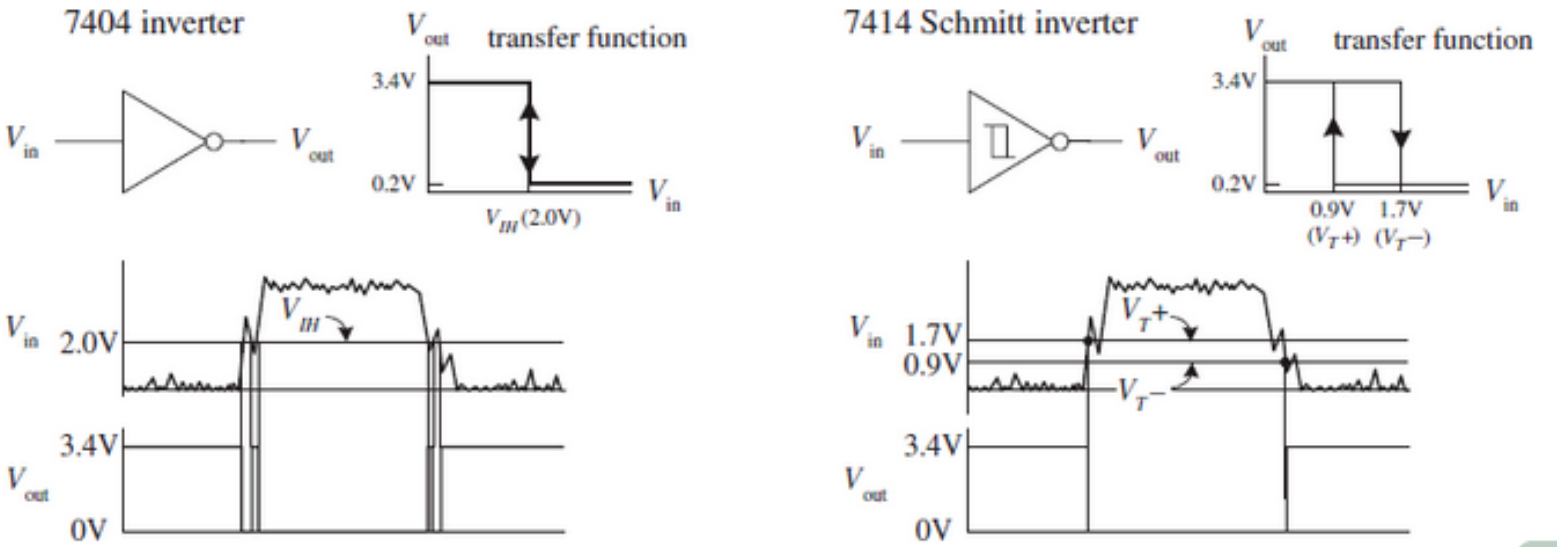
comparing the Schmitt-triggered 7414 inverter gate with a conventional inverter gate, the 7404:



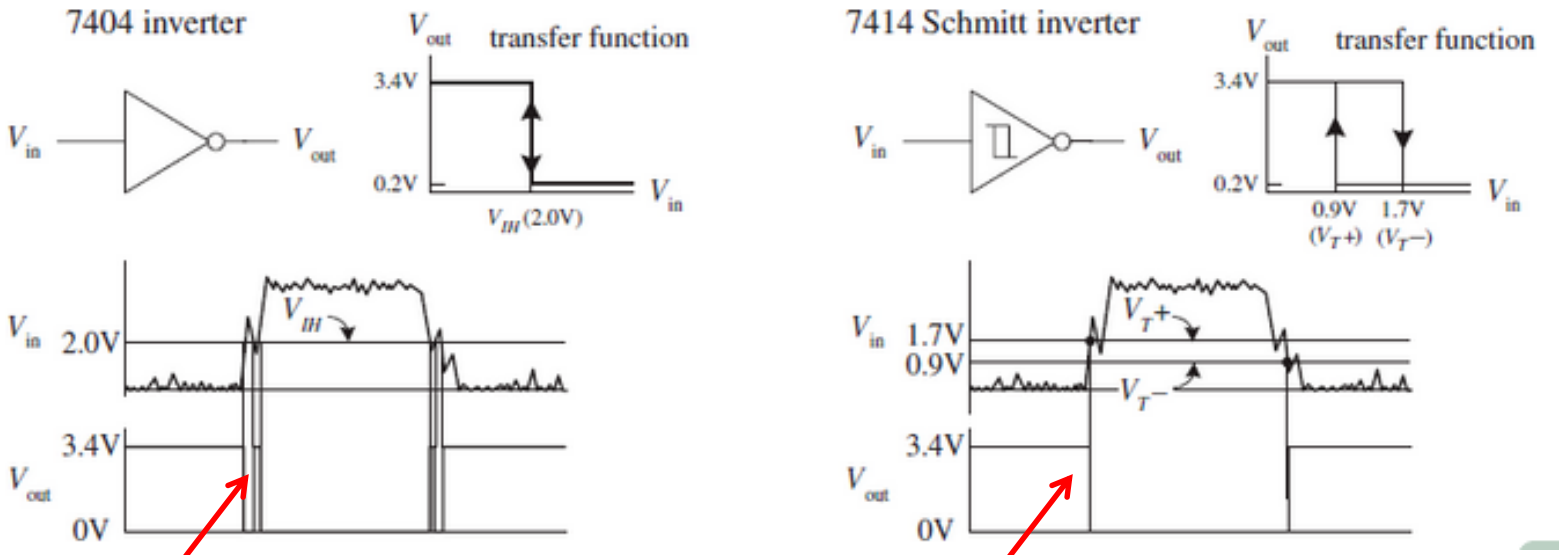
- **With the 7404**, to make the output go from high to low or from low to high, the input voltage must fall above or below the single 2.0-V threshold voltage.
- **With the 7414**, to make the output go from low to high, the input voltage must dip below V_T^- (which is +0.9 V for this particular IC) and To make the output go from high to low, the input voltage must pop above V_T^+ (which is +1.7 V for this particular IC) ➔The difference in voltage between V_T^+ and V_T^- is called the *hysteresis voltage*
- The symbol used to designate a Schmitt trigger is based on the appearance of its transfer function:

Schmitt Trigger: Applications

- Schmitt-triggered devices are quite handy for transforming noisy signals or signals that waver around critical threshold levels into sharply defined, jitter-free output signals.
- This is illustrated in the lower graphs shown:



Schmitt Trigger: Applications

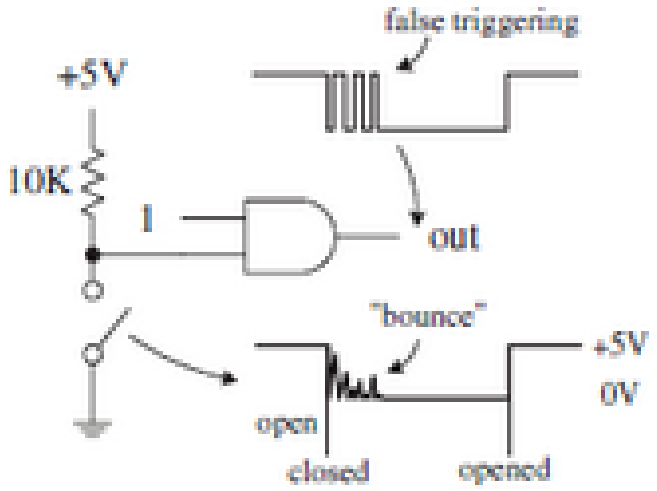


The conventional 7404 experiences an unwanted output spike resulting from a short-term spike present during low-to-high and high-to-low input voltage transitions.

The 7414 Schmitt-triggered inverter ignores these spikes because it incorporates hysteresis

De-bouncing digital input switches

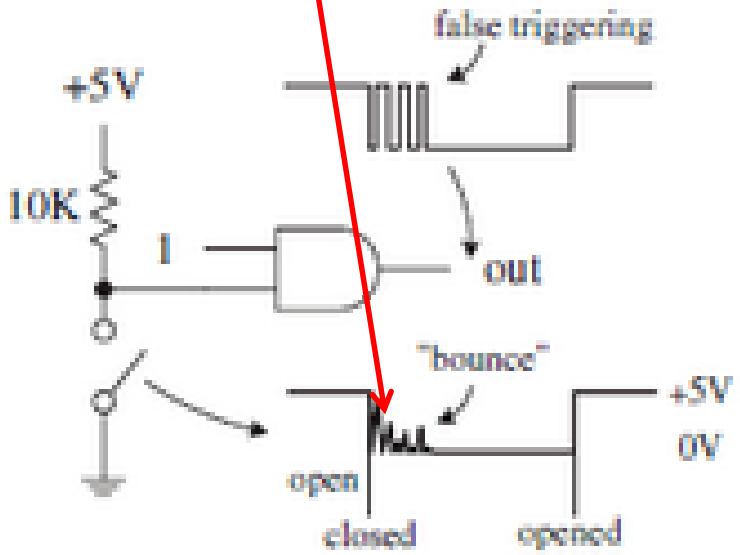
Use the far-left switch/pullup resistor circuit to drive an AND gate's input high or low (the other input is fixed high):



- When the switch is open, the AND gate should receive a high
- When the switch is closed, the gate should receive a low
- That's what should happen, but that's not what actually happens. Why? Because of switch bounce.

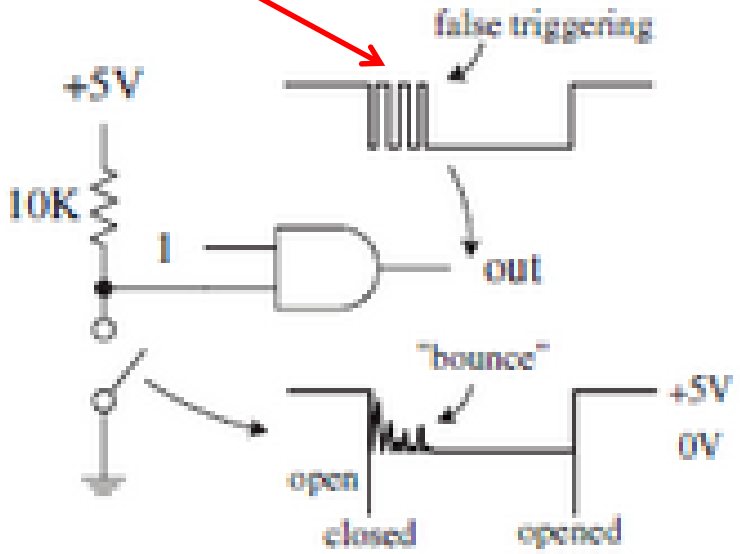
De-bouncing digital input switches

When a switch is closed, the metal contacts bounce a number of times before coming to rest due to inherent **spring-like** characteristics of the contacts.



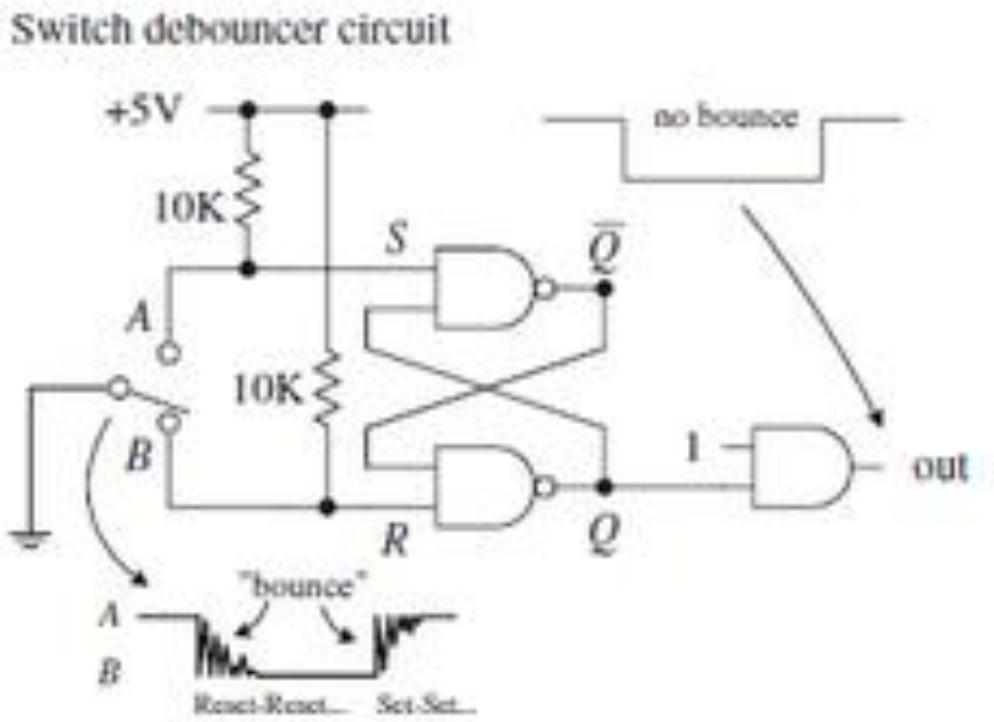
De-bouncing digital input switches

Though the bouncing typically lasts no more than 50 ms, the results can lead to unwanted false triggering



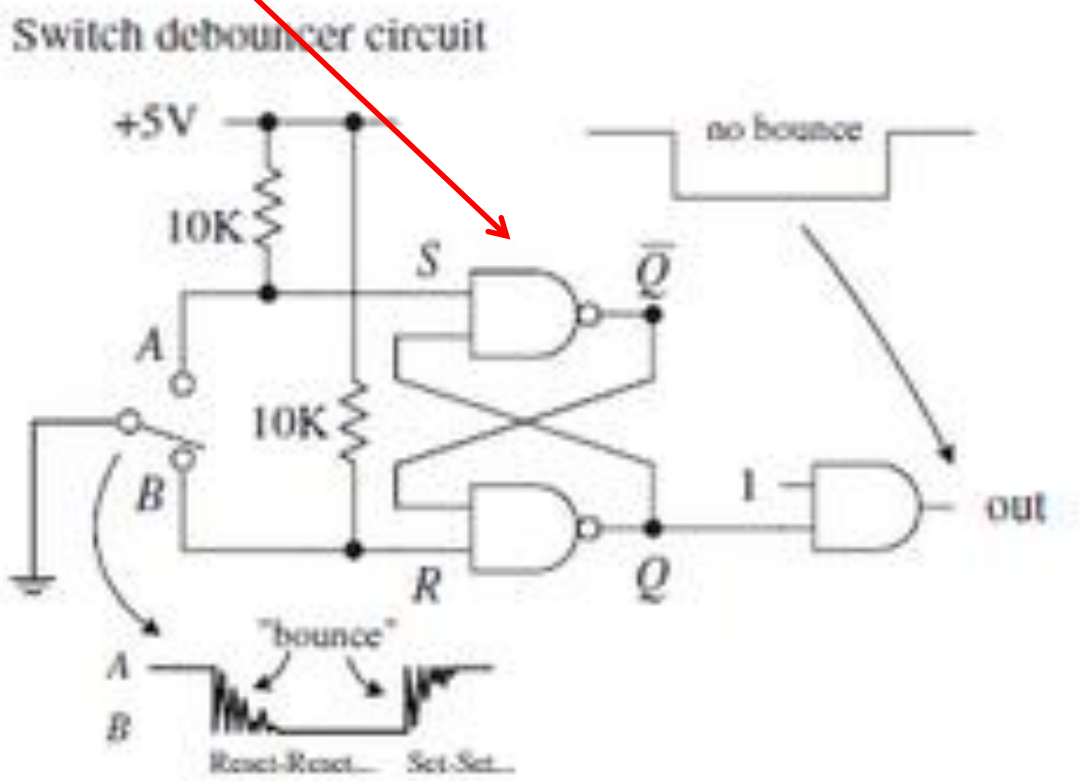
De-bouncing digital input switches

A simple way to get rid of switch bounce is to use the switch debouncer circuit (note that in the figure there is a 3 terminal switch, i.e. SPDT).



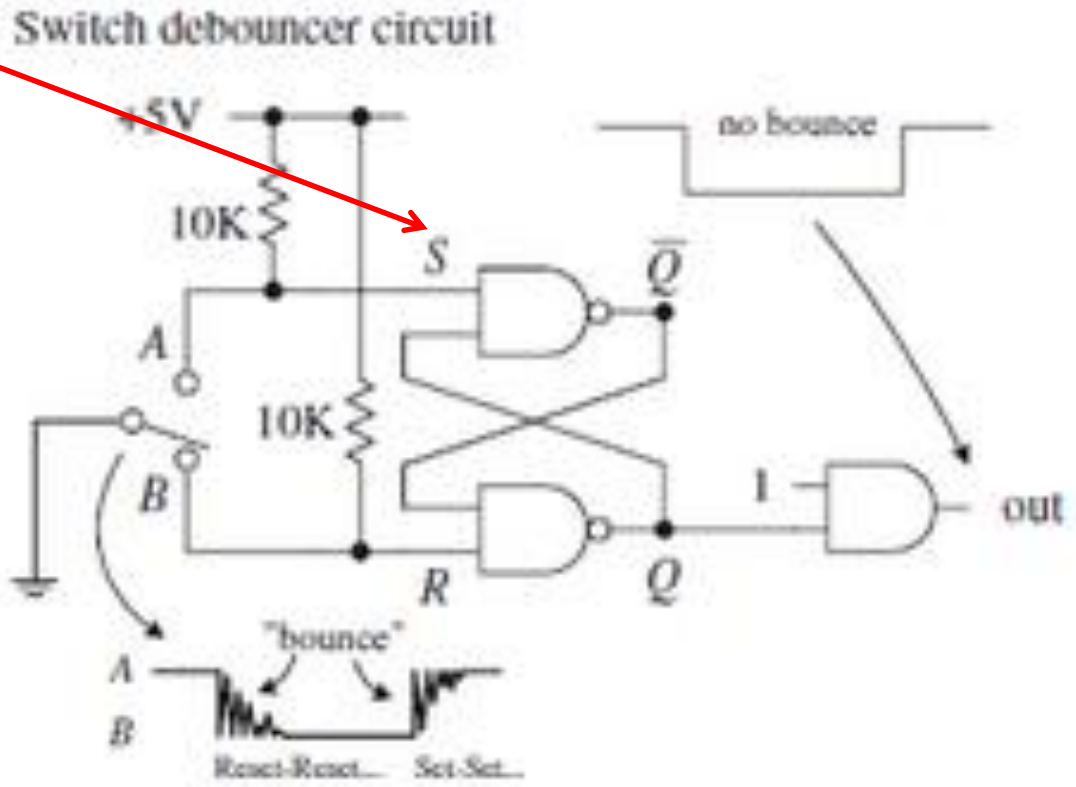
De-bouncing digital input switches

This circuit uses an SR flip-flop to store the initial switch contact voltage while ignoring all trailing bounces:



De-bouncing digital input switches

when the switch is thrown from the *B* to *A* position, the flip-flop is set

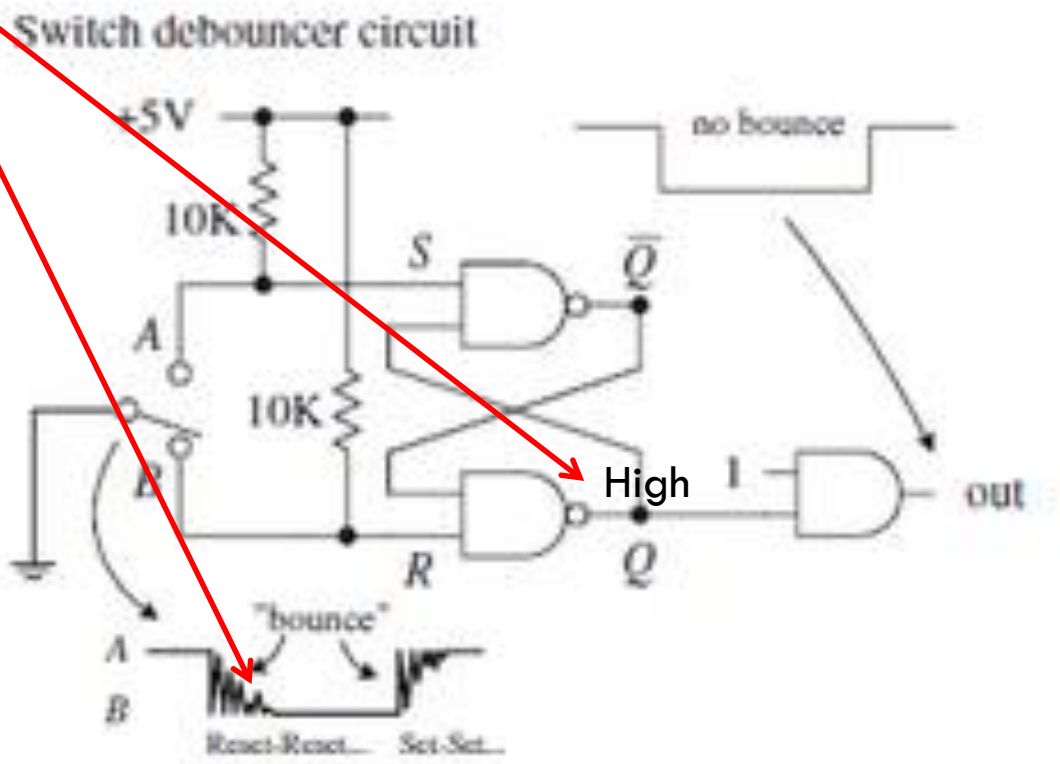


De-bouncing digital input switches

As the switch bounces alternately high and low, the Q output remains high, because when the switch contact bounces away from *A*

the *S* input receives a low (*R* is low, too), but that's just a hold condition; the output stays the same.

The same debouncing feature occurs when the switch is thrown from position *A* to *B*

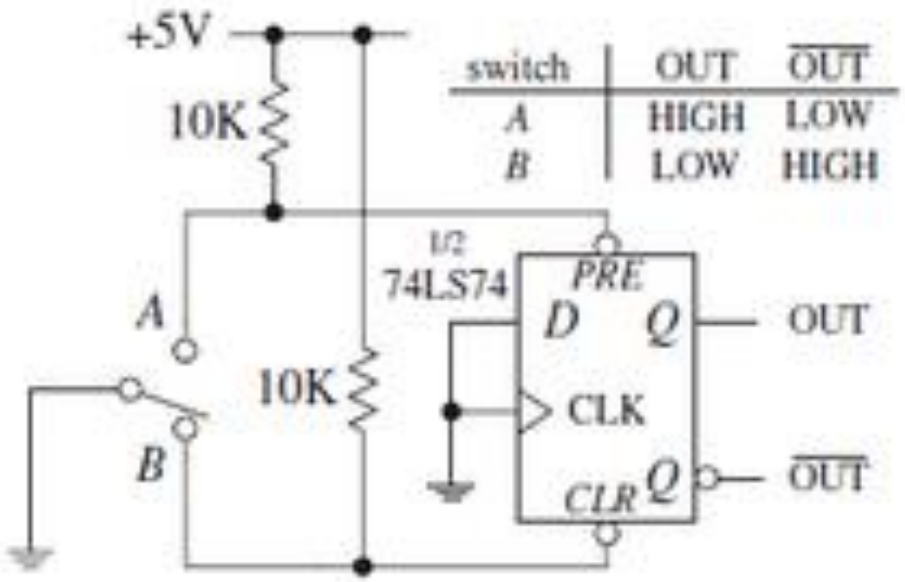


De-bouncing digital input switches

We can also use a D flip flop to debounce switches:

The *D* input and *CLK* input are tied to ground so that the only two modes that can be enacted are the preset and clear modes. Also, the pullup resistors will always make either the preset input or clear input high, regardless of whether the switch is bouncing

From this and the truth table you can show yourself that this also debounces the SPDT switch

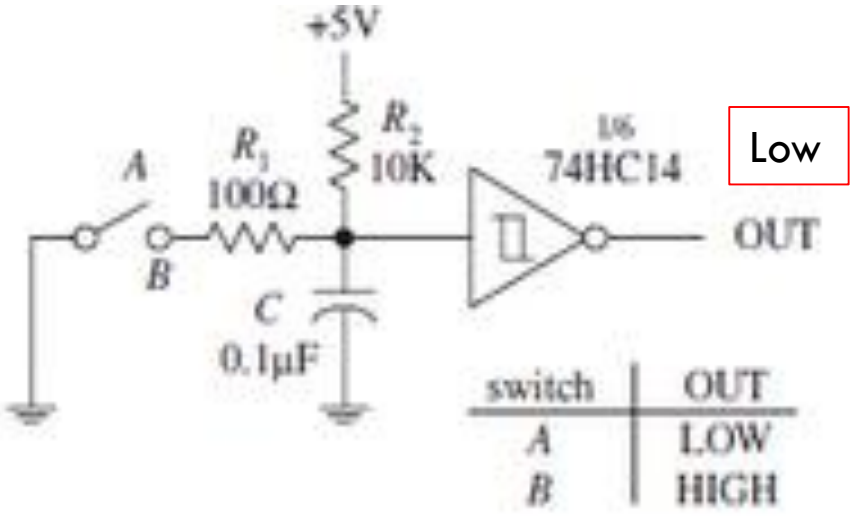


SPDT switch debouncer using 74LS74 dual D-type flip-flop.

De-bouncing digital input switches

We can also use a Schmitt trigger inverter (or a Schmitt trigger 2 input NAND gate with both inputs connected together) and an unique RC timing circuit to debounce a SPST switch input:

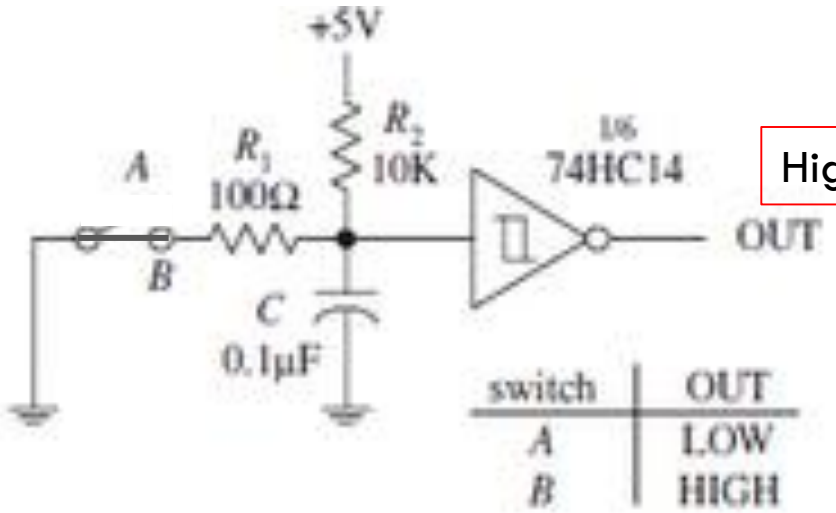
When the switch is open, the capacitor is fully charged (+5 V), and the output is low.



SPST switch debouncer using 74HC14 hex Schmitt-triggered inverter.

De-bouncing digital input switches

- When the switch is closed, the capacitor discharges rapidly to ground through the 100-Ω resistor, causing the output to go high.



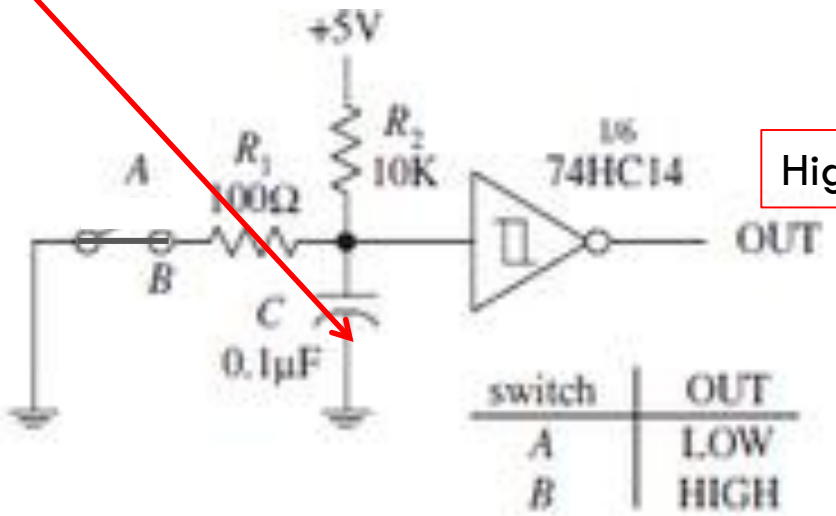
SPST switch debouncer using 74HC14 hex Schmitt-triggered inverter.

De-bouncing digital input switches

As the switch bounces, the capacitor will repeatedly attempt to charge slowly back to +5 *V* via the 10-k resistor, and then again will discharge rapidly to zero through the 100-ohm resistor, making the output high.

By making the 10-k pullup resistor larger than the 100-Ω discharge resistor, the voltage across the capacitor or the voltage applied to the inverter's input will not get a chance to exceed the positive threshold voltage (V_T^+) of the inverter during a bounce.

Hence, the output remains high, regardless of the bouncing switch

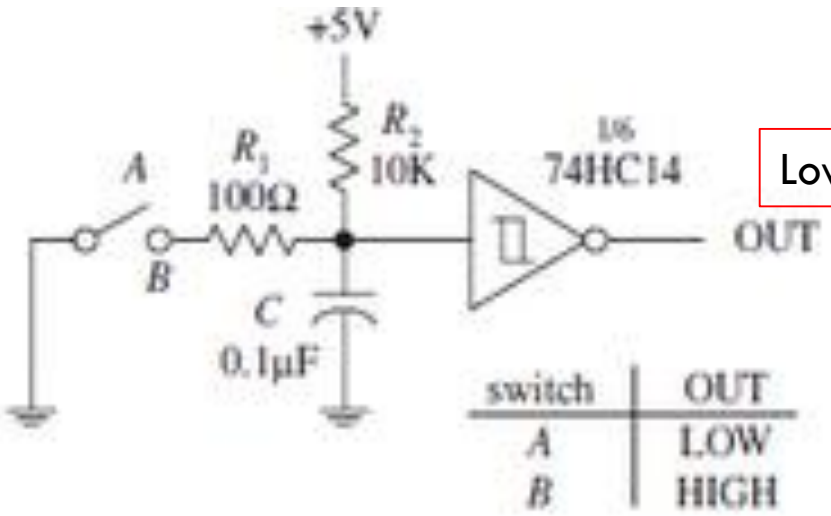


SPST switch debouncer using 74HC14 hex Schmitt-triggered inverter.

De-bouncing digital input switches

In this example the charge-up time constant ($R_2C = 10\ k \times 0.1\ \mu F$) ensures sufficient leeway.

When the switch is reopened, the capacitor charges up toward +5 V and when the capacitor's voltage reaches V_T^+, the output switches low.



SPST switch debouncer using 74HC14 hex Schmitt-triggered inverter.

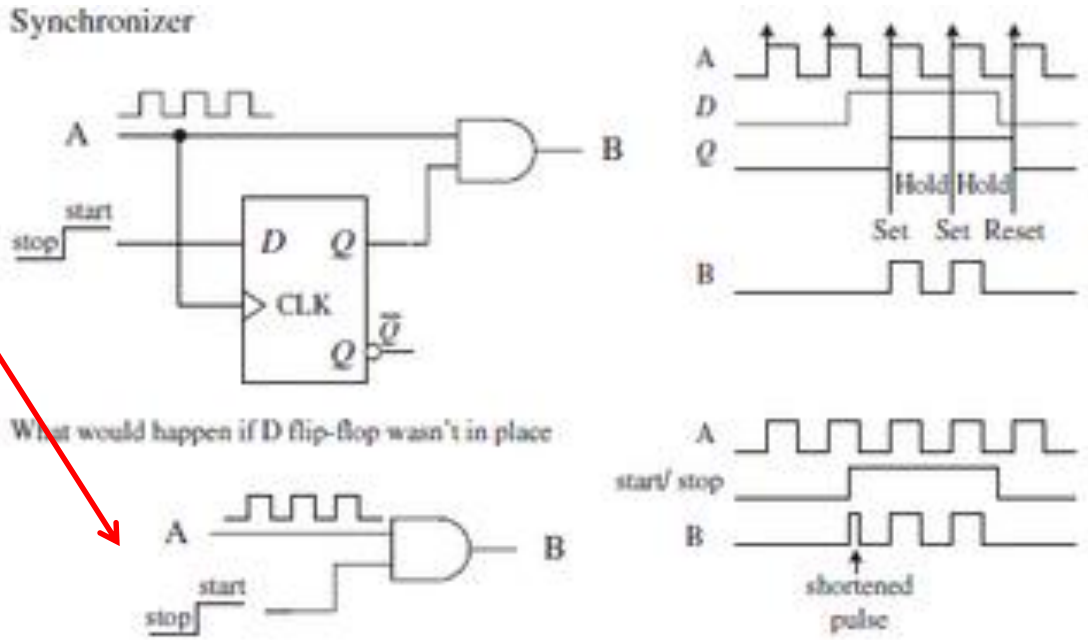
External Asynchronous Control Signal

- A synchronizer is used when you want to use an external asynchronous control signal (perhaps generated by a switch or other input device) to control some action within a synchronous system

- The synchronizer provides a means of keeping the phase of the action generated by the control signal in synch with the phase of the synchronous system.

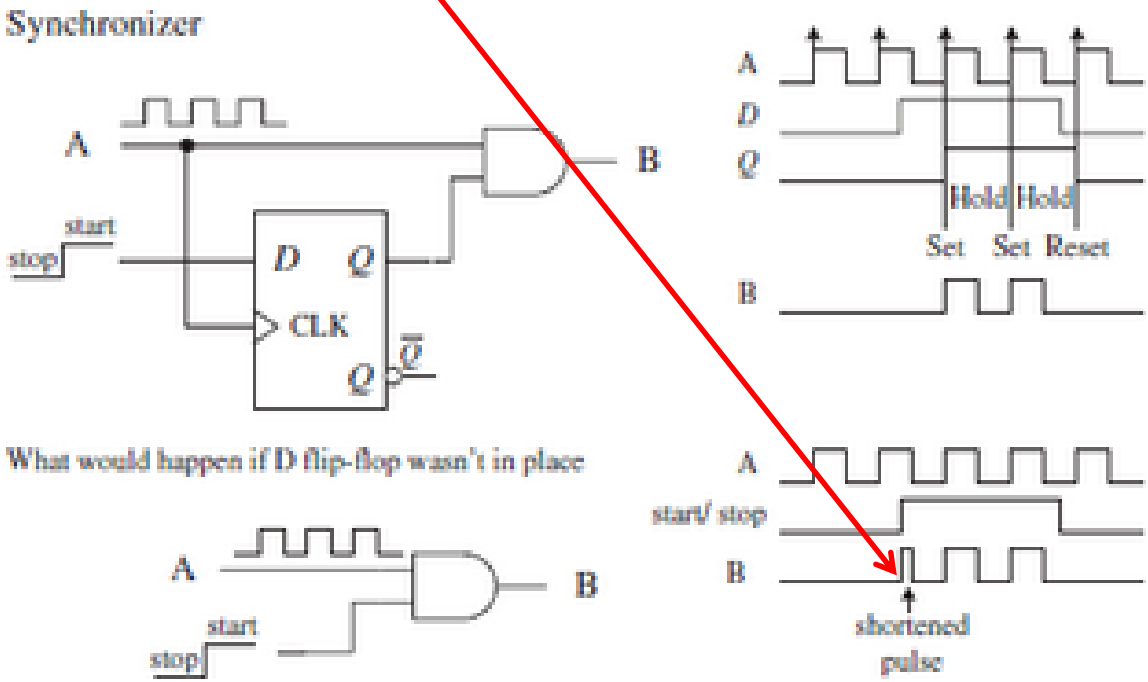
External Asynchronous Control Signal

- For example, say you want an asynchronous control signal to control the number of clock pulses that get from point A to point *B* within a synchronous system
- You might try using a simple enable gate, as shown below the synchronizer circuit:



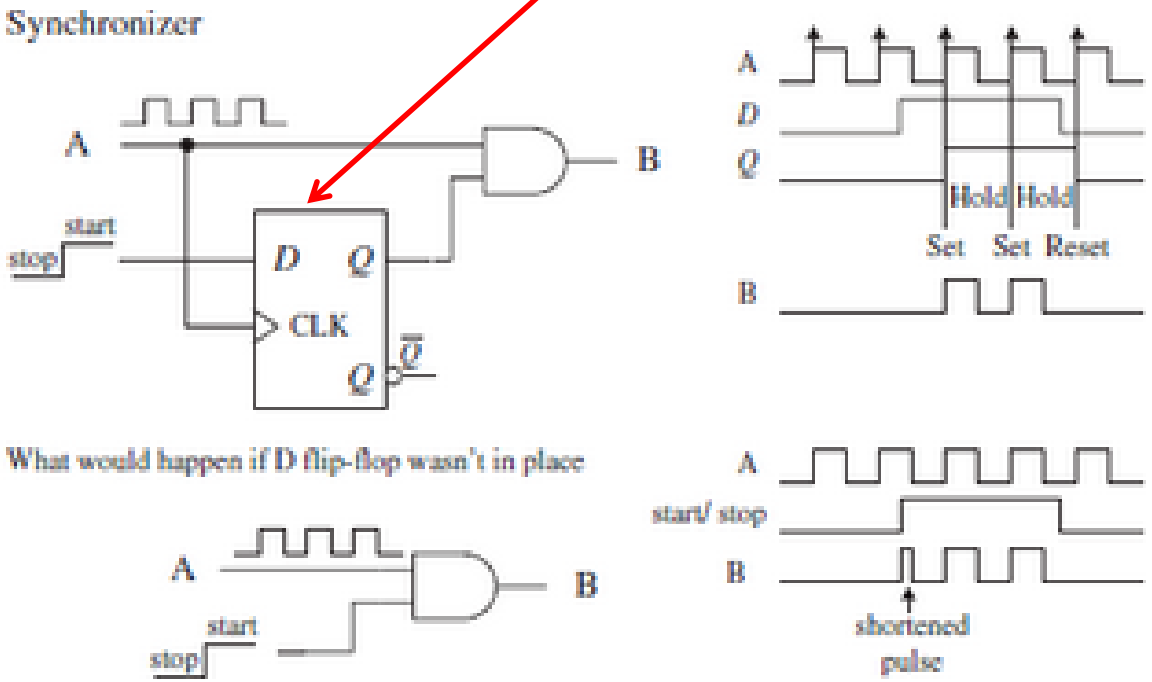
External Asynchronous Control Signal

- However, because the external control signal is not synchronous (in phase) with the clock, when you apply the external control signal, you may shorten the first or last output pulse, as shown in the lower timing diagram:



External Asynchronous Control Signal

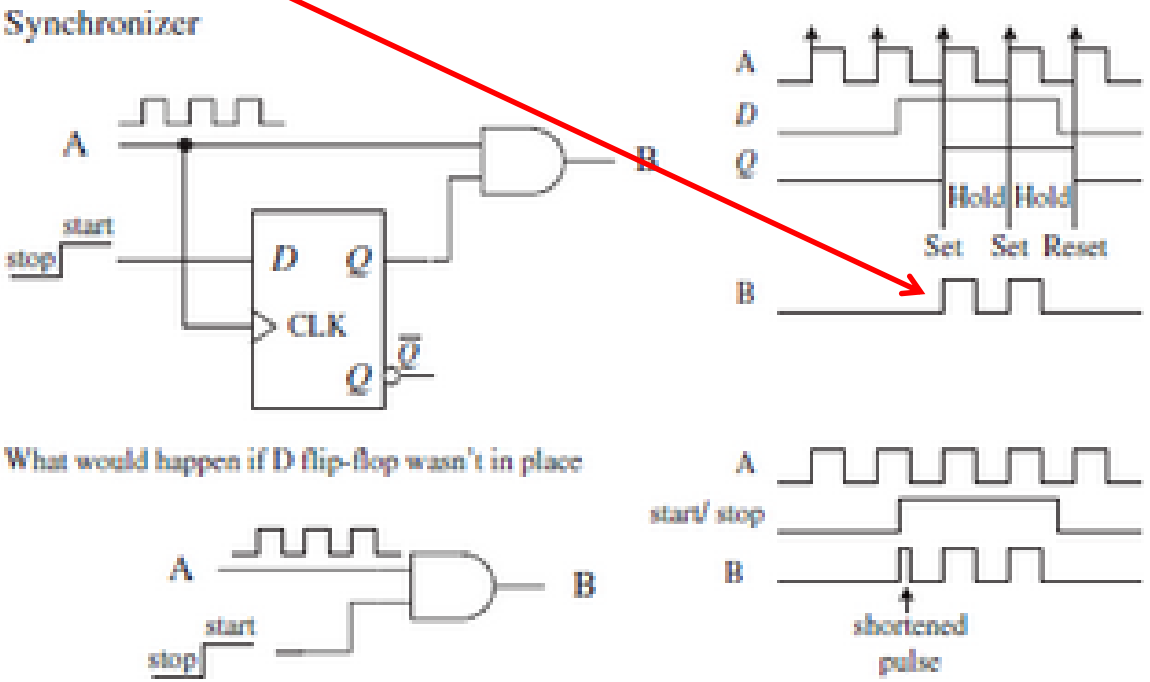
- To avoid shortened pulses, throw in an edge-triggered D-type flip-flop to create a synchronizer.:



External Asynchronous Control Signal

- With this arrangement, there will never be shortened clock pulses because the Q output of the flip-flop will not supply enable pulses to the AND gate that are out of phase with the input clock signal

This is due to the fact that after the flip-flop's CLK input receives a positive clock edge, the flip-flop ignores any input changes applied to the *D* input until the next positive clock edge

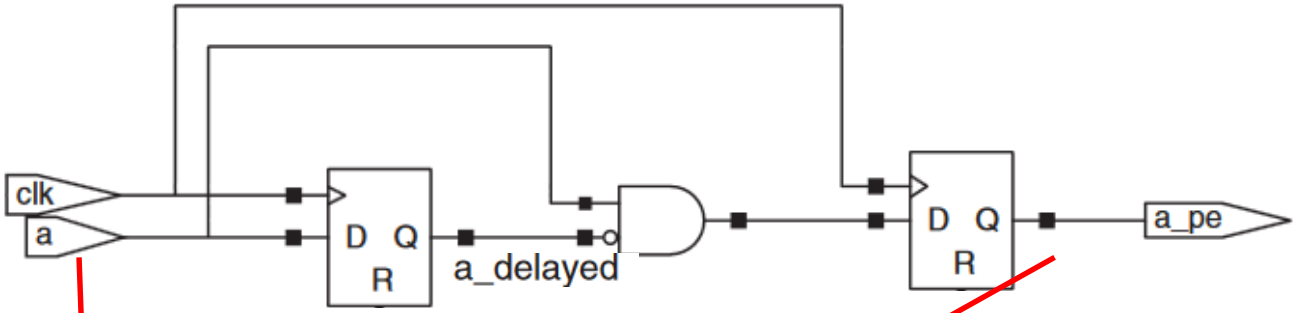


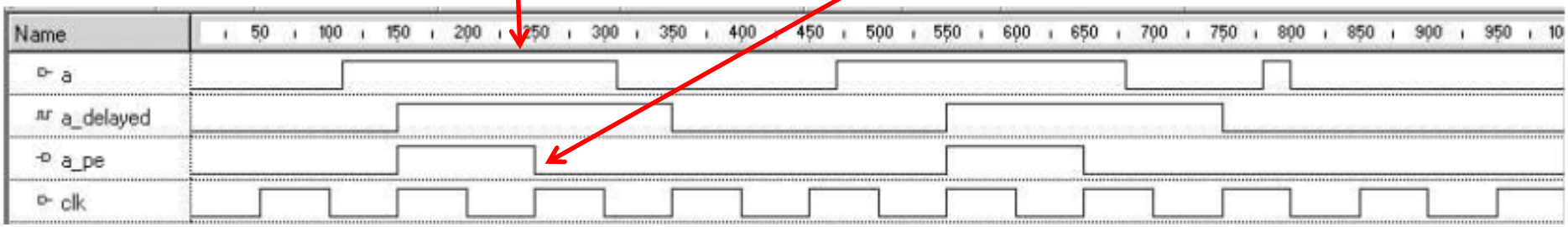
External Asynchronous Control Signal

- **Synchronous Edge Detector**

It detect the rising front of the input a, generating at the output a pulse with duration of 1 clock cycle.

Useful in state machines with identical transitions on consecutive states.

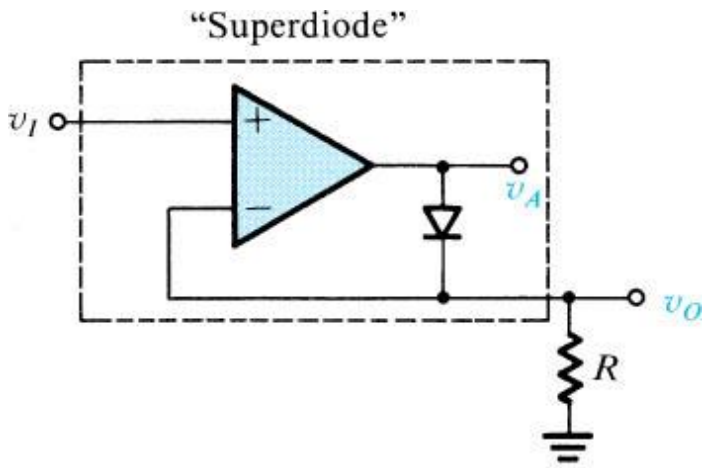




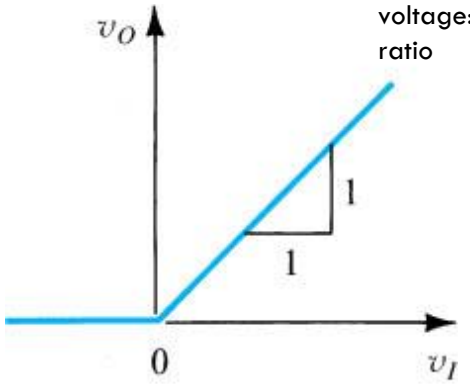
Super Diode

Consider this op-amp circuit and its output voltage vs input voltage transfer characteristic:

for negative input voltage, the output voltage is zero. For positive input voltage, the output voltage: input voltage is 1:1 ratio



(a)



(b)

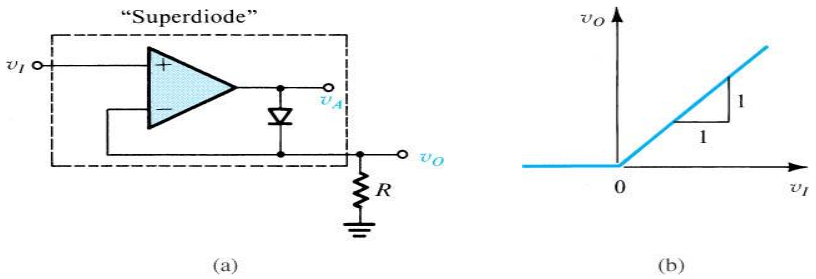
Super diodes are also known as *precision rectifiers*.

Super Diode

- When the input voltage, v_i, is +ve then the output voltage v_A goes +ve and the diode will conduct

- Which establishes a closed feedback path between the op-amps output and its negative input, this results in a voltage follower type situation with the virtual short occurring so the voltage at the positive input will equal the voltage at the negative input i.e.

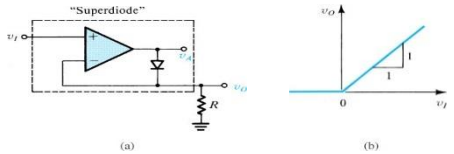
$$v_o = v_i \qquad v_i \geq 0$$



- For this op-amp to start operation the input voltage needs to exceed 0.7/(open loop gain of Op-Amp,A) →as the op-amp gain is typically very large, this voltage will be very small!

Super Diode

- Example if Open Loop Gain, A=100,000 then this voltage is 7μV. What about v_i negative?



- When negative the diode will become reverse biased, ie it will open circuit. This will force the op-amp into open loop mode and the output v_a will swing to the negative voltage rail, as no current can pass through the op-amps –ve terminal or diode (in real devices insignificant currents) then no current flows through the load resistor R and the output v_o is also 0V's as shown ie:

$$v_o = 0 \qquad v_i < 0$$

- This circuit is suitable for low frequency and small voltages eg rectification of 100 mV sinusoidal/AC signal

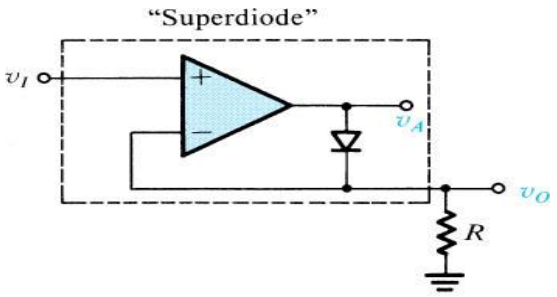
Super Diode

Disadvantages:

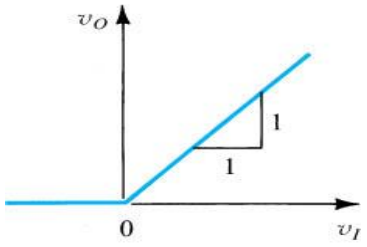
- When input voltage is negative and output voltage is zero all of the input voltage's magnitude appears across the two input terminals of the op-amp - if this is greater than a few volts the op-amp will need **overvoltage protection** (most modern op-amps have this) or it could be damaged

- When the input voltage is negative the op-amp will be saturated and to return to the op-amps linear operation will take time (hence the low frequency requirement)

An improved circuit is possible!



(a)



(b)

Super Diode with 2 Diodes

This circuit does not suffer from the problems of the original circuit – delay and need for over-voltage protection

Operation:

- D_2 , for *positive input* voltage, closes the –ve feedback loop around the op-amp resulting in a virtual ground appearing across the inverting input and the op-amp output is clamped at one diode forward bias voltage drop below ground; this means that D_1 is reverse biased and thus no current flows through R_2 (since there is no current return path) so then v_o is zero!

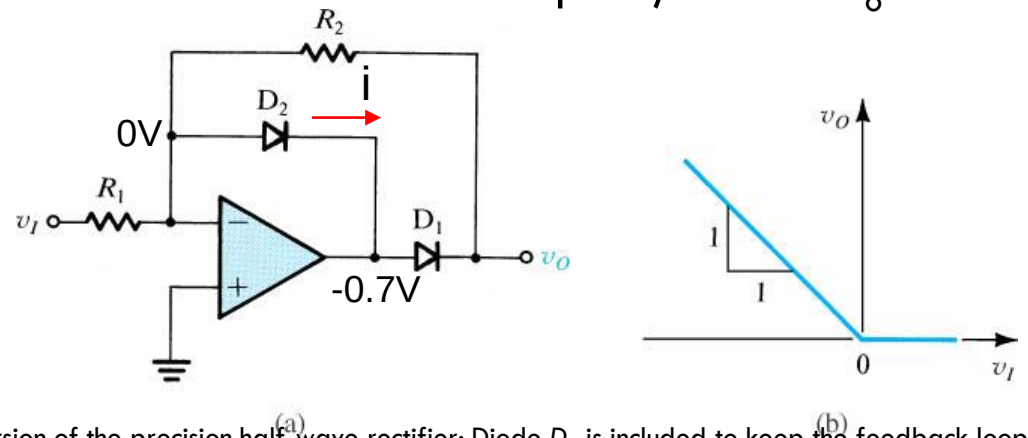
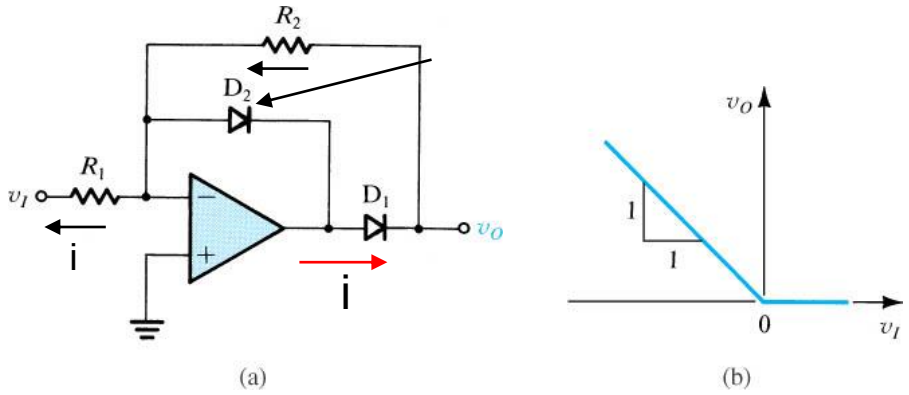


Figure 13.34 **(a)** An improved version of the precision half-wave rectifier: Diode D_2 is included to keep the feedback loop closed around the op amp during the off times of the rectifier diode D_1, thus preventing the op amp from saturating. **(b)** The transfer characteristic for $R_2 = R_1$.

pp.1208 Sedra and Smith

Super Diode with 2 Diodes

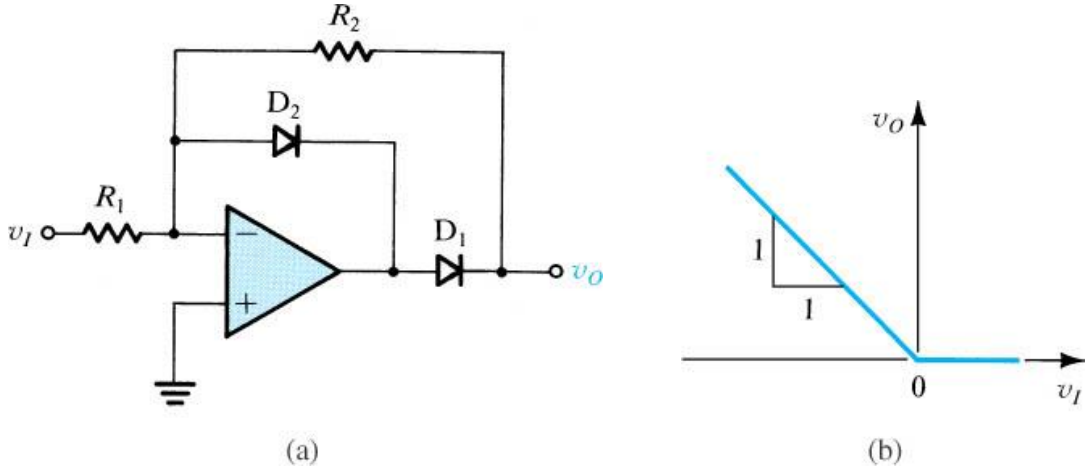


Called Catching diode: since it "catches" the op-amp voltage as it goes negative and clamps it to a diode drop below ground!

Operation:

- D_2 , for *negative input* voltage, is reverse biased as the the –ve input will now tend to go negative, with the output voltage going positive BUT now D_1 will be able to conduct (and will since its forward biased) via R_2 which results in a closed negative feedback path around the op-amp ; forcing a virtual ground to appear at the –ve input – as no current passes into the op-amp (ideal) or very little (real) - then all the current passes through R_1 and R_2 and this current is equal

Super Diode with 2 Diodes



- The output voltage is then given by:

$$v_o = -\frac{R_2}{R_1} v_i \quad for \quad v_i \leq 0$$

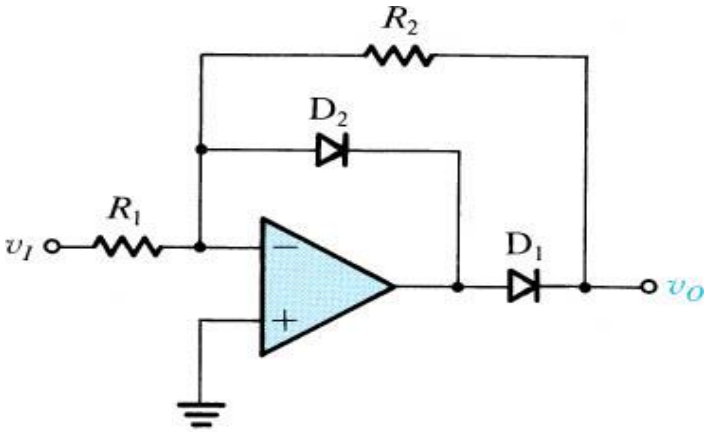
- If $R_1 = R_2$ the output voltage will be:

$$v_o = -v_i \quad for \quad v_i \leq 0$$

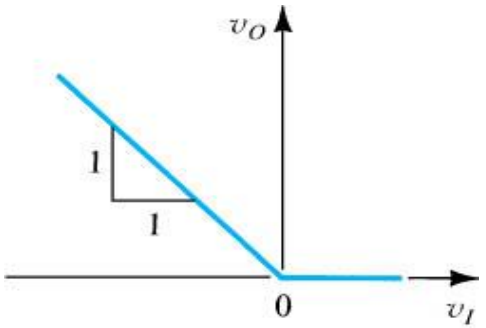
Super Diode with 2 Diodes

Advantages:

- feedback loop remains closed at all times and thus the op-amp remains in its linear region avoiding the possibility of saturation and the associated time delay to get out of saturation.
- It also now can be used without worrying too much about over-voltage protection required for the original super-diode (we have a virtual ground in operation)

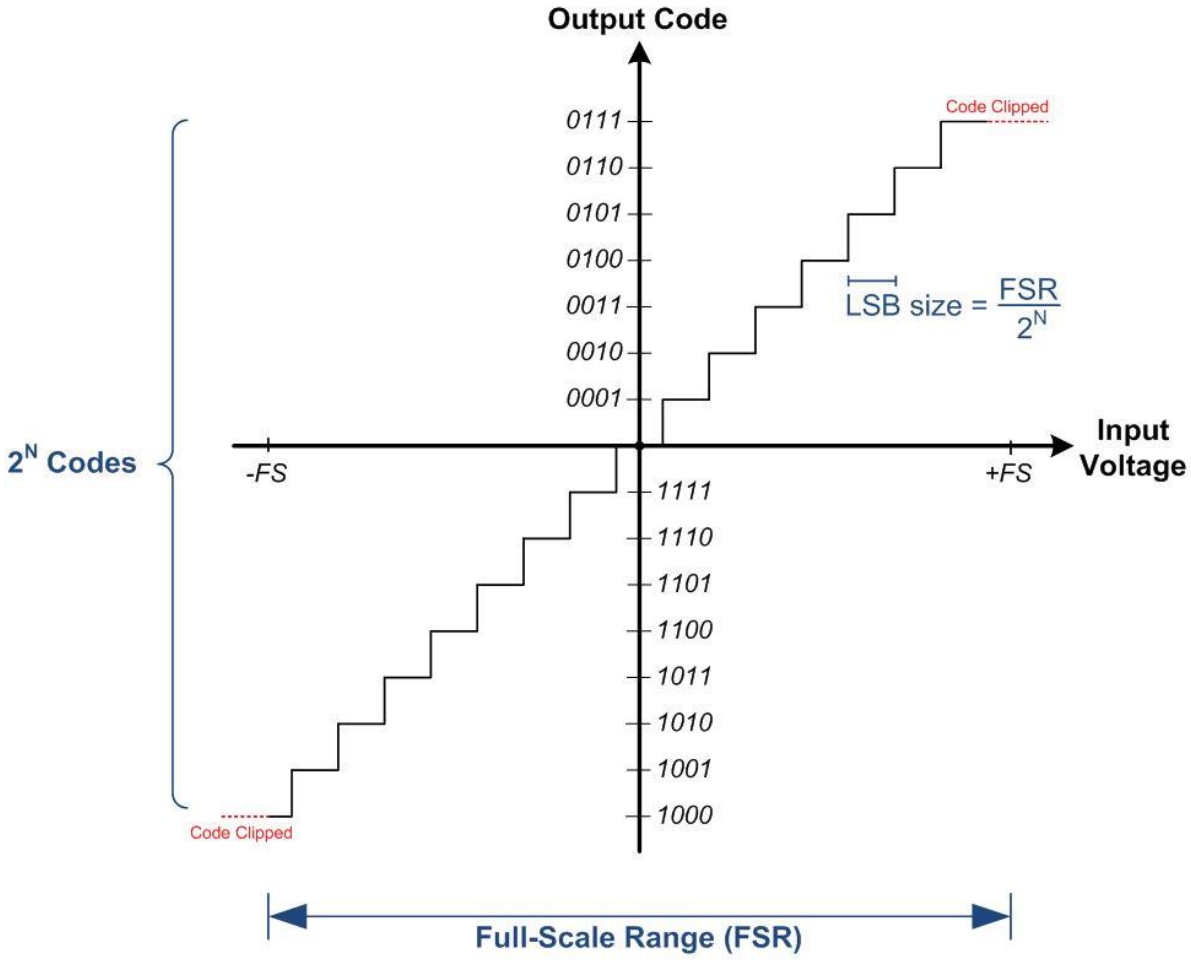


(a)



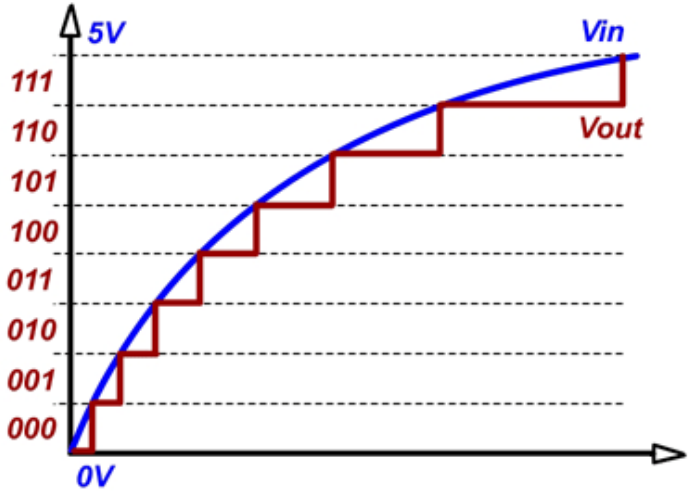
(b)

Digital To Analog Conversion

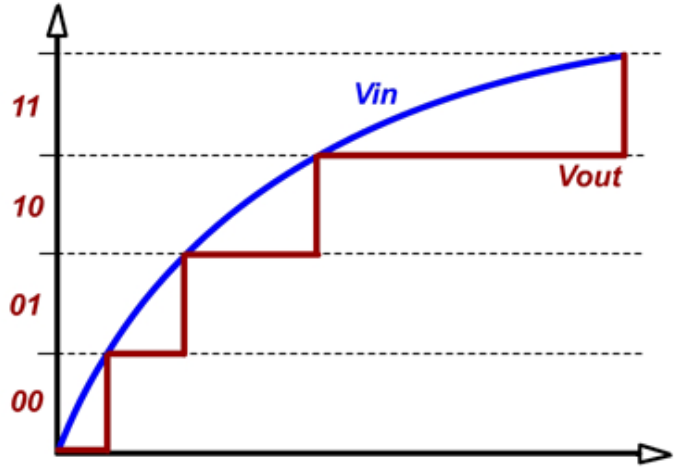


Digital To Analog Conversion

3 bit ADC



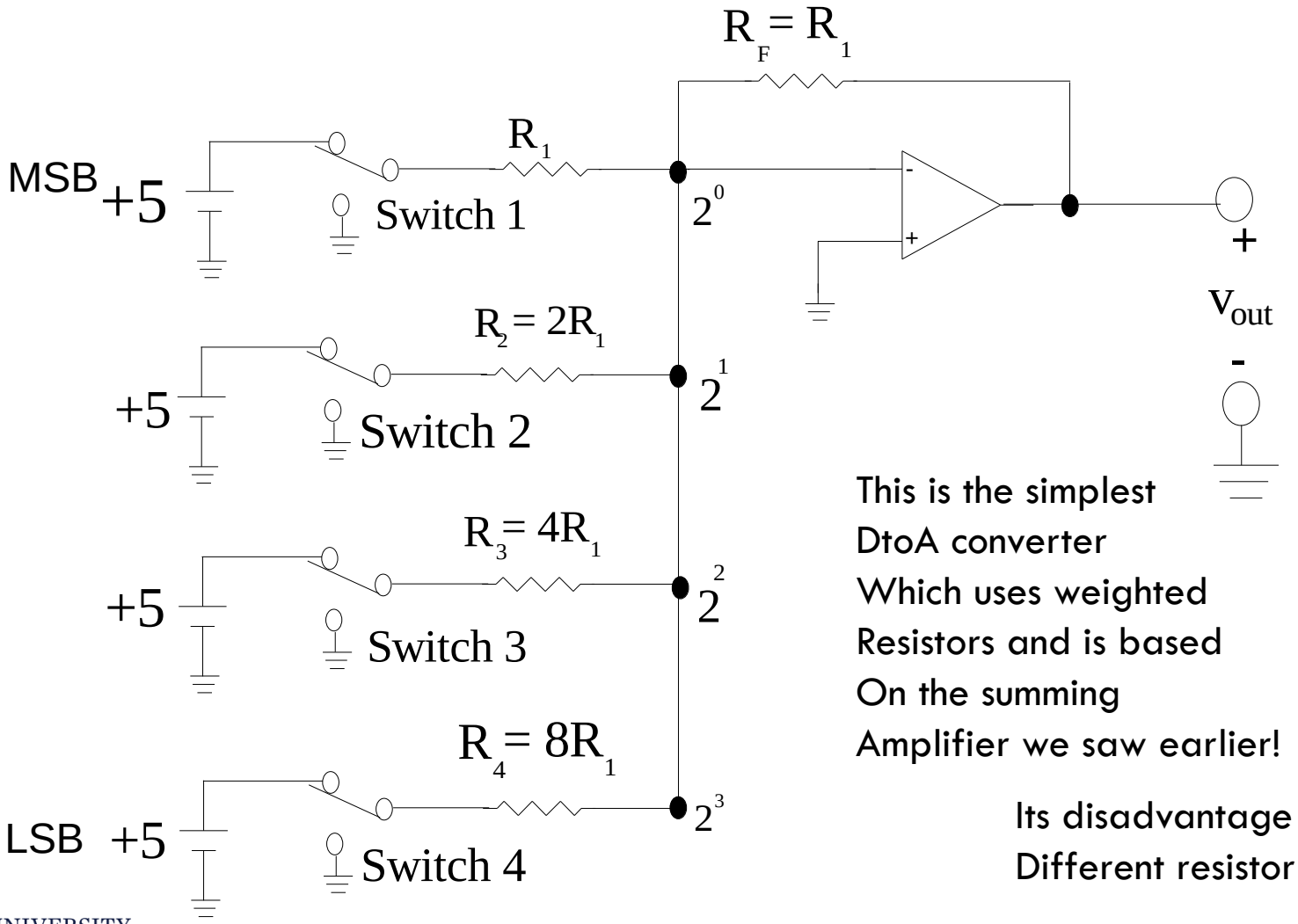
2 bit ADC



4 bit Digital to Analog Converter

- The next two circuits are 4 bit DAC circuits using a standard op-amp
- It should be of interest how we convert a digital signal to analog and vice-a-versa
- We use D/A or DAC as abbreviations for these devices
- Remember that you can use op-amp based DAC in your project implementation (they are easy to design).
- They are also available in specialised IC 'chips' and also built into various microprocessor boards

4 bit Digital to Analog Converters



This is the simplest
DtoA converter
Which uses weighted
Resistors and is based
On the summing
Amplifier we saw earlier!

Its disadvantage is it needs
Different resistor values!

4 bit Digital to Analog Converters

Here the switches are digital providing either 0V for ‘0’ and +5V for ‘1’

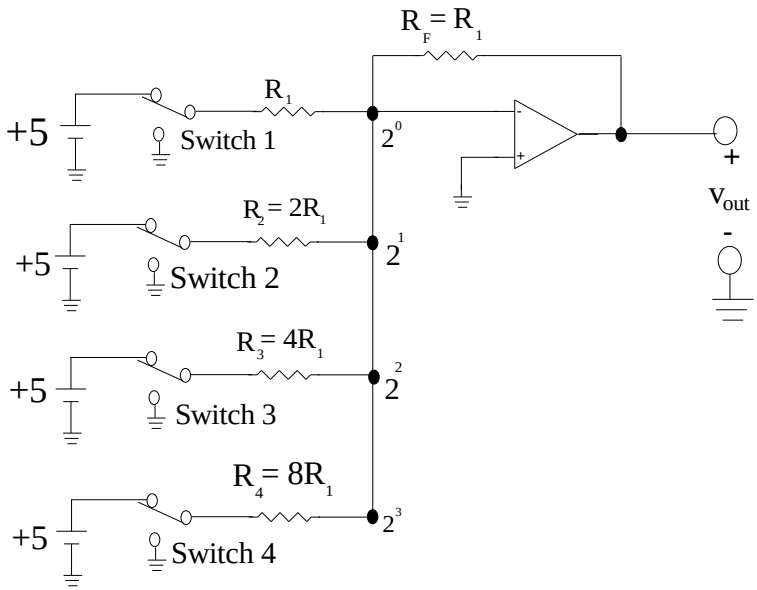
The output voltage is given by:

$$v_{out} = -R_F \cdot \left(\frac{v_{S0}}{R_{S0}} + \frac{v_{S1}}{R_{S1}} + \frac{v_{S2}}{R_{S2}} + \frac{v_{S3}}{R_{S3}} \right)$$

Where v_{S0} is the first digital input, v_{S1} is 2nd etc…

$$\therefore v_{out} = -R_1 \cdot \left(\frac{v_{S0}}{R_1} + \frac{v_{S1}}{2R_1} + \frac{v_{S2}}{4R_1} + \frac{v_{S3}}{8R_1} \right)$$

$$= -\left(v_{S0} + \frac{v_{S1}}{2} + \frac{v_{S2}}{4} + \frac{v_{S3}}{8} \right)$$



4 bit Digital to Analog Converters

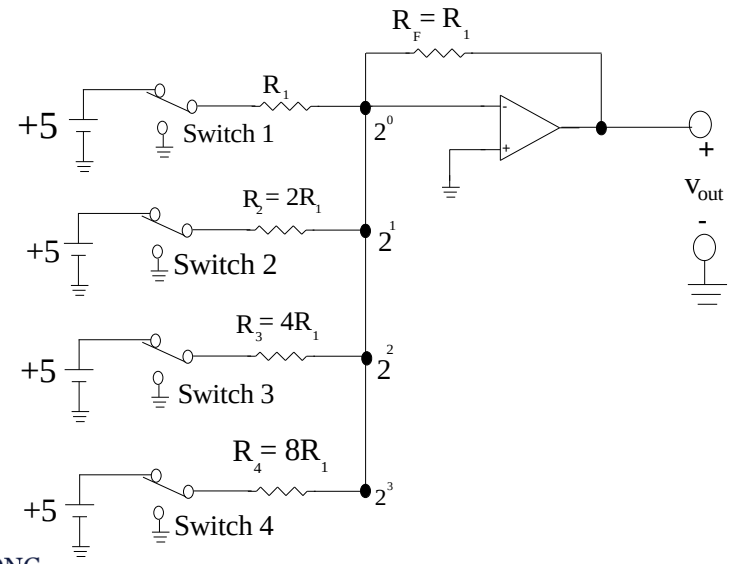
Example

If $R_1 = 1k\Omega$ and switch 1, 2 & 3 are connected to ground, with switch 4 connected to +5V, what will be the output voltage of the DtoA shown?

$$v_{out} = -\left(v_{S0} + \frac{v_{S1}}{2} + \frac{v_{S2}}{4} + \frac{v_{S3}}{8} \right)$$

$$= -\left(0 + \frac{0}{2} + \frac{0}{4} + \frac{5}{8} \right)$$

$$= -0.625 \quad volts$$



This would correspond to the binary number '0001' and also shows the resolution of the Converter (it changes in steps of 0.625 volts!)

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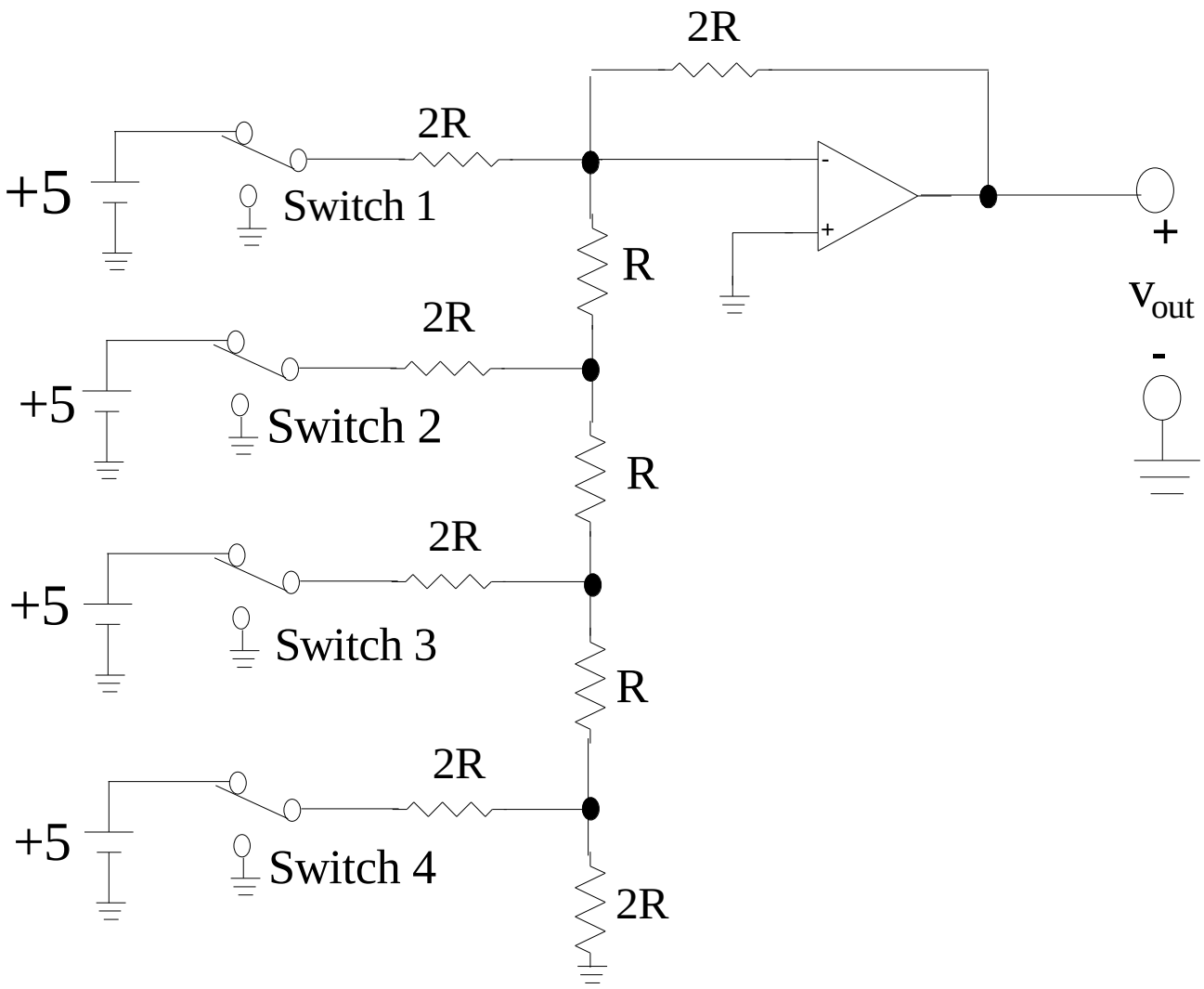
4 bit DAC - R/2R ladder D/A

Has the advantage of only needing two resistor values, 2R and R



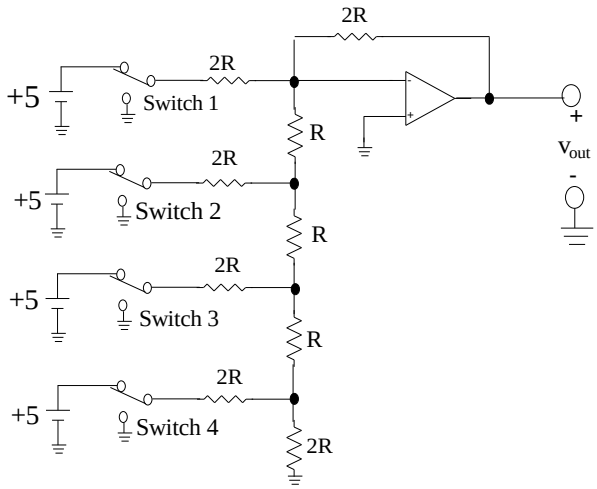
4 bit DAC - R/2R ladder D/A

It can be shown (needs repeated application of thevenin's theorem and series and parallel equivalent resistor Calculations) that:

$$v_{out} = v_{out0} + v_{out1} + v_{out2} + v_{out3}$$

To get:

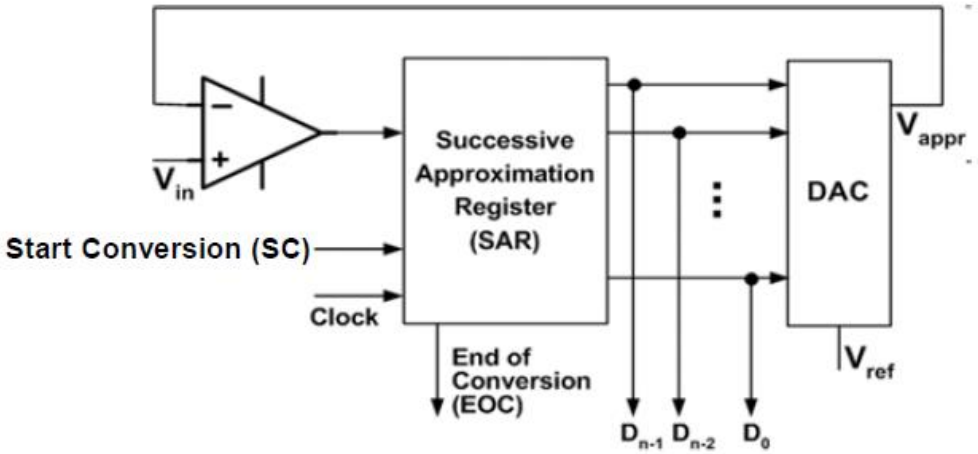
$$v_{out} = -v_o - \frac{v_1}{2} - \frac{v_2}{4} - \frac{v_3}{8}$$



Successive-approximation ADC

- The analog to digital converter (A/D converter or ADC) samples an analog signal to produce a digital output code
- Due to the process there is a significant delay between sampling the analog input signal and presentation of the resultant digital output code
- Often these are built into IC's
- A Common form for the ADC is the successive approx. device

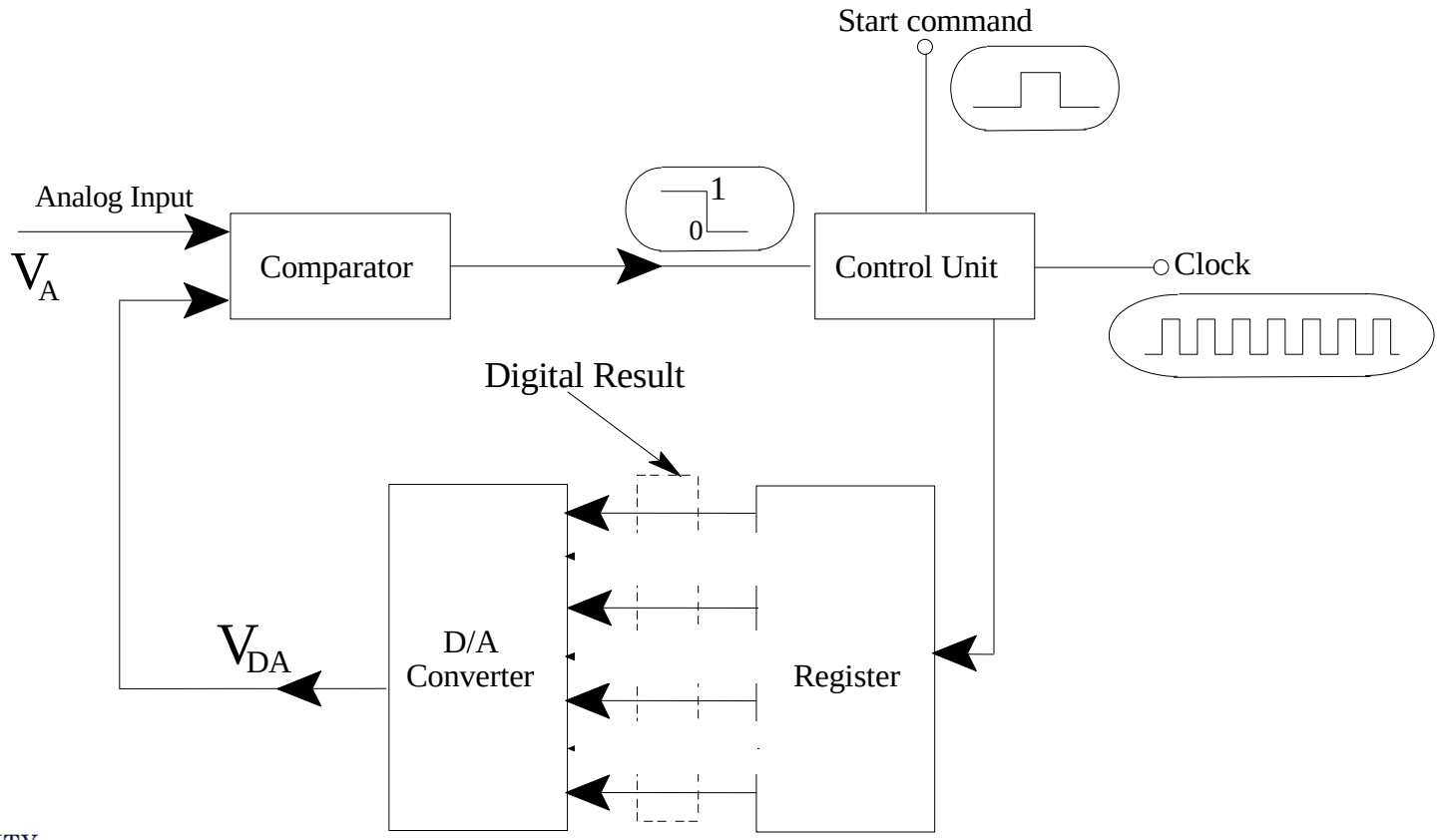
Successive-approximation ADC



- A DAC is used to generate approximations of the input voltage.
- A comparator is used to compare V_{in} and V_{appr}.
- In each cycle, SAR finds one output bit using comparator
  - start setting $D_{n-1} = 1$ and reset it to 0 if $V_{in} < V_{ref} / 2$
  - proceed similarly for every bit until D_0.
- To start conversion, set SC = 1. When conversion ends, EOC = 1.
- Quite fast (slower than flash) , one of the most widely used design for ADCs.

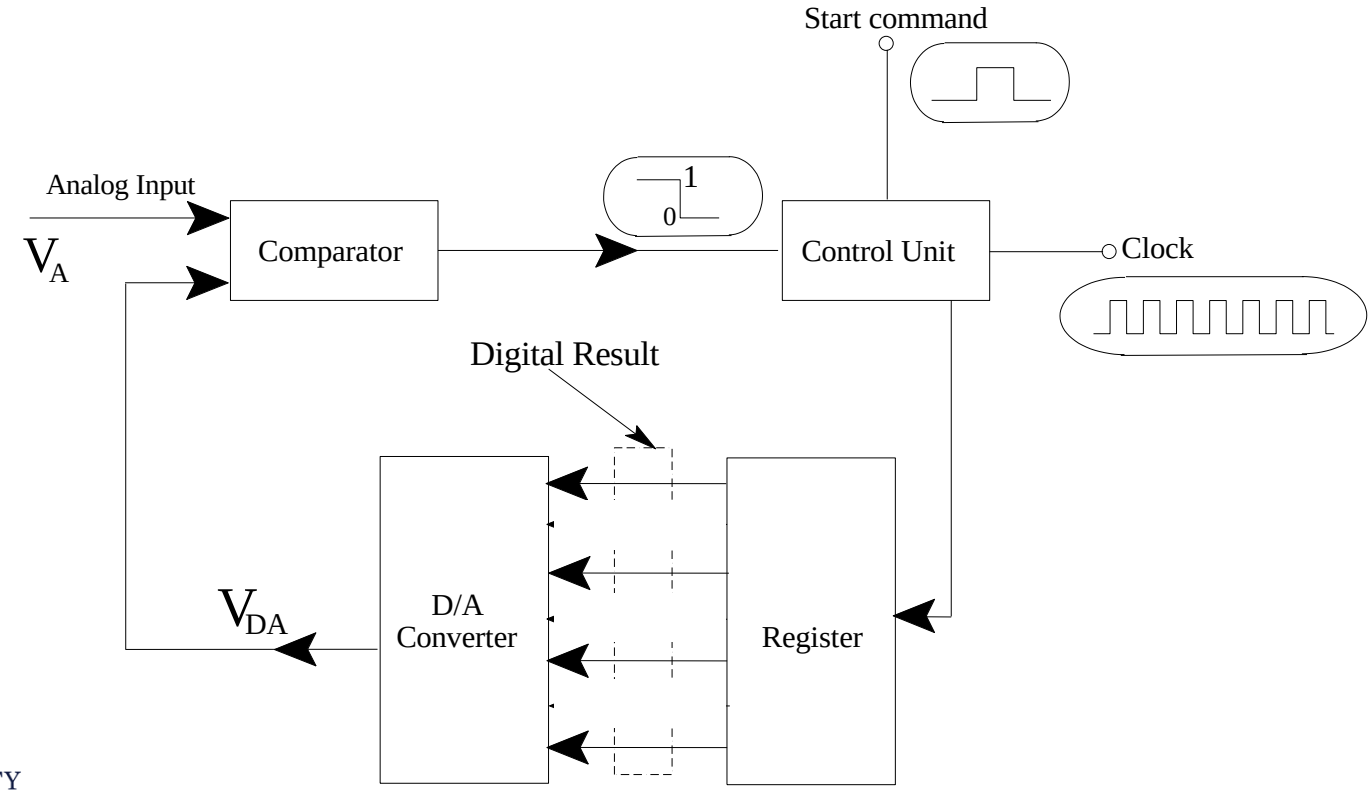
4 bit Successive-appx ADC

- Works by comparison of the analog input with the output of the Digital to Analog converter



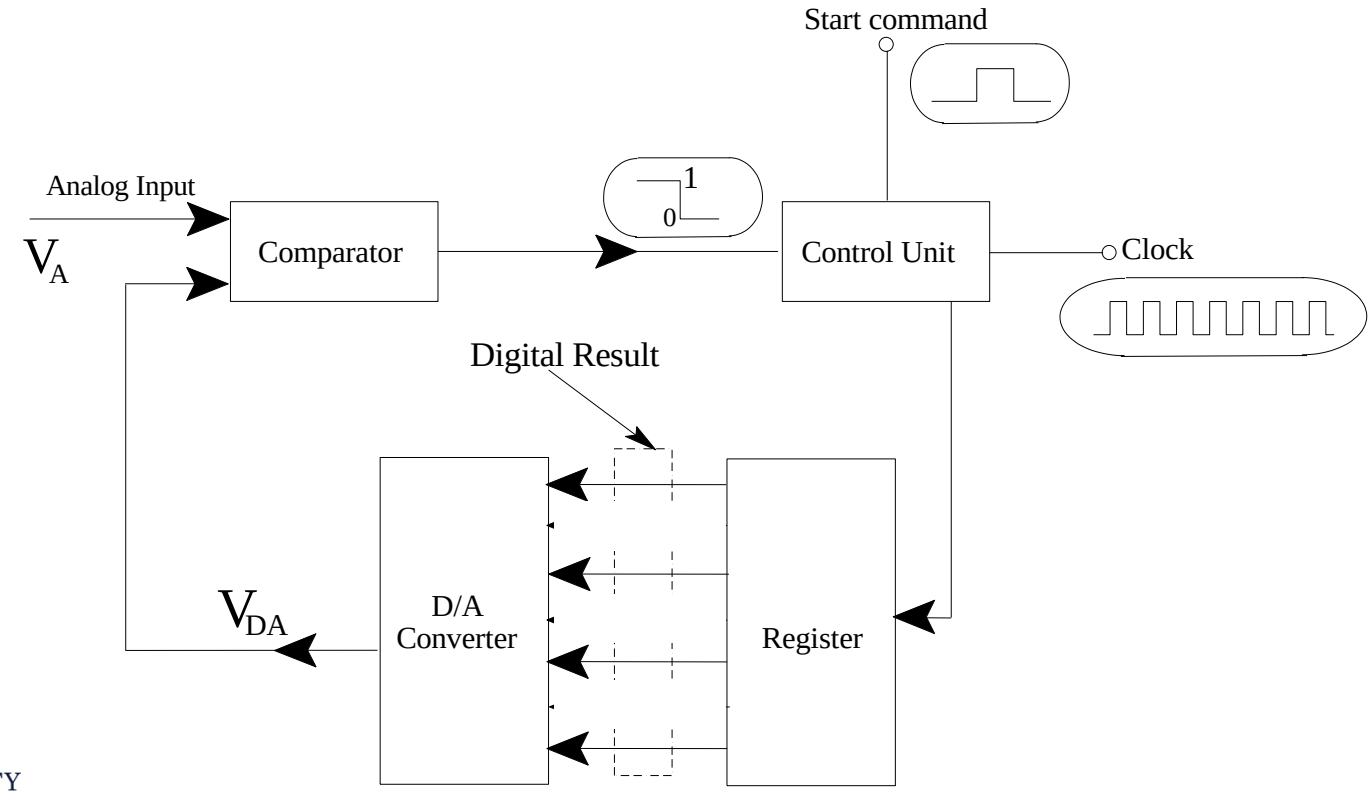
4 bit Successive-appx ADC

- The control unit has three inputs, a start command, the output of the comparator and a clock input
- It contains logic which is triggered by the start command (possibly a state machine with flip flops for memory of state)



4 bit Successive-appx ADC

- The clock input determines the rate at which data is sent to the register which holds a binary number that is then both converted to an analog signal and used as the result when the comparator output indicates the process is complete



4 bit Successive-appx ADC

For the comparator we can identify the following:

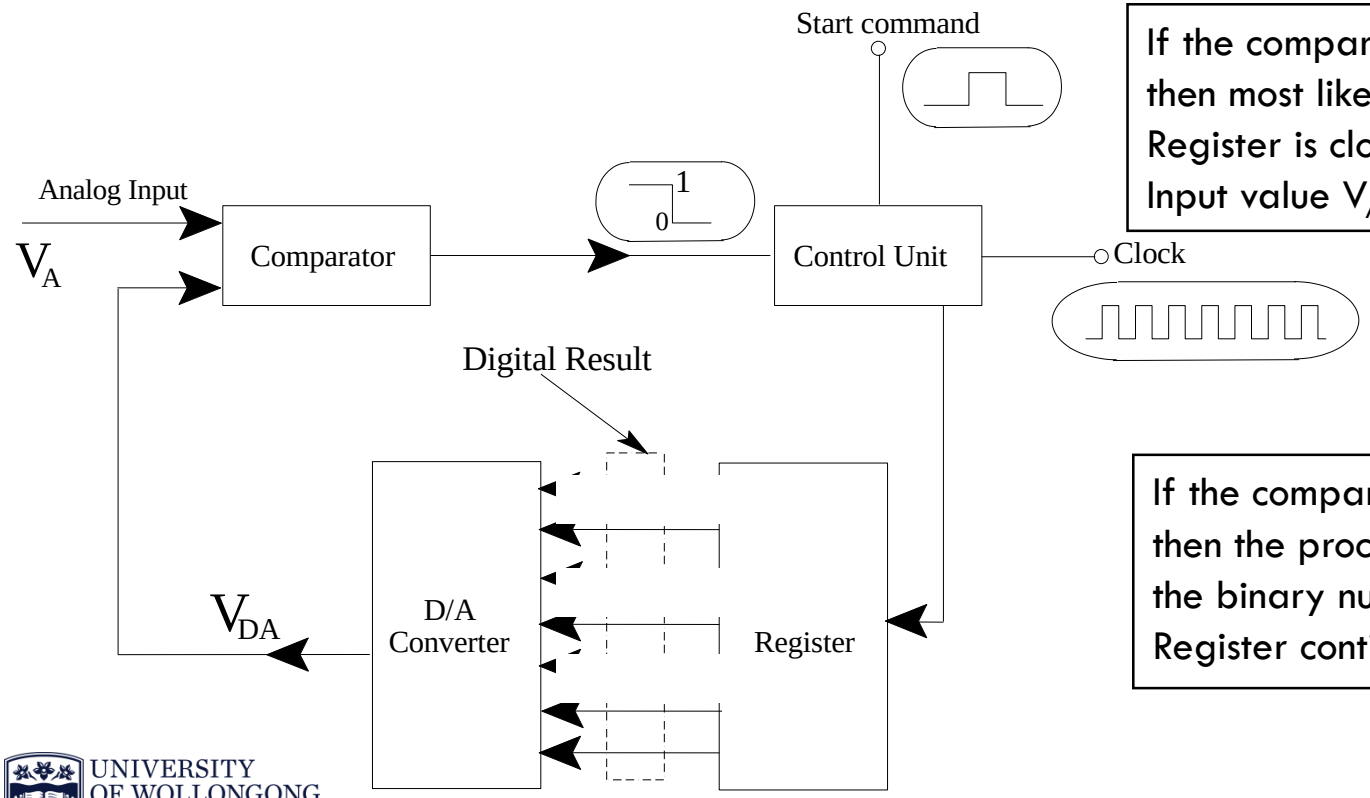
If $V_{DA}<V_A$ the comparator output is HIGH

If $V_{DA}=V_A$ the comparator output is LOW

If $V_{DA}>V_A$ the comparator output is LOW

If the comparator output is LOW then the comparator Stops the process of modifying the binary number stored in the register!

If the comparator output is LOW then most likely the value in the Register is close to the analog Input value V_A

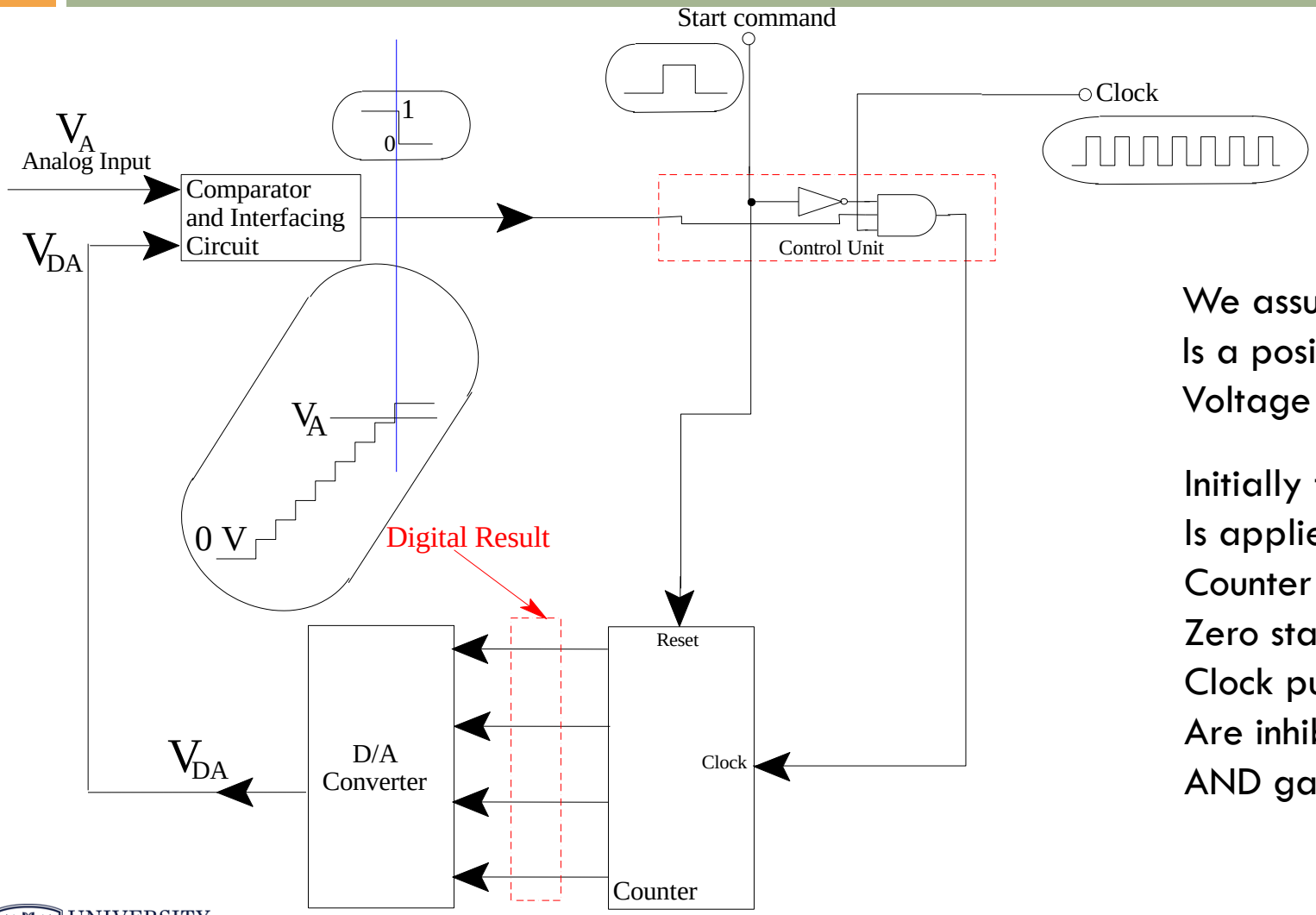


If the comparator output is HIGH then the process of modifying the binary number stored in the Register continues

Digital Ramp ADC Converter

- Based on Successive Approximate ADC but uses a counter instead of a Register
- Its output characteristic looks like a ramp
- Here we assume that the start pulse will also reset the counter
- An AND gate is used which will have three inputs, one from the start pulse ensures that the counter starts at zero and no false clock signals affect the counter while its being reset (to all zero count)
- The other input for the AND gate is the output of the comparator after the voltage has been changed to 0 to 5 Volt level by an interfacing circuit (using either a transistor or a Diode and Zener Diode with a voltage buffer as we will see in the EWB simulation)

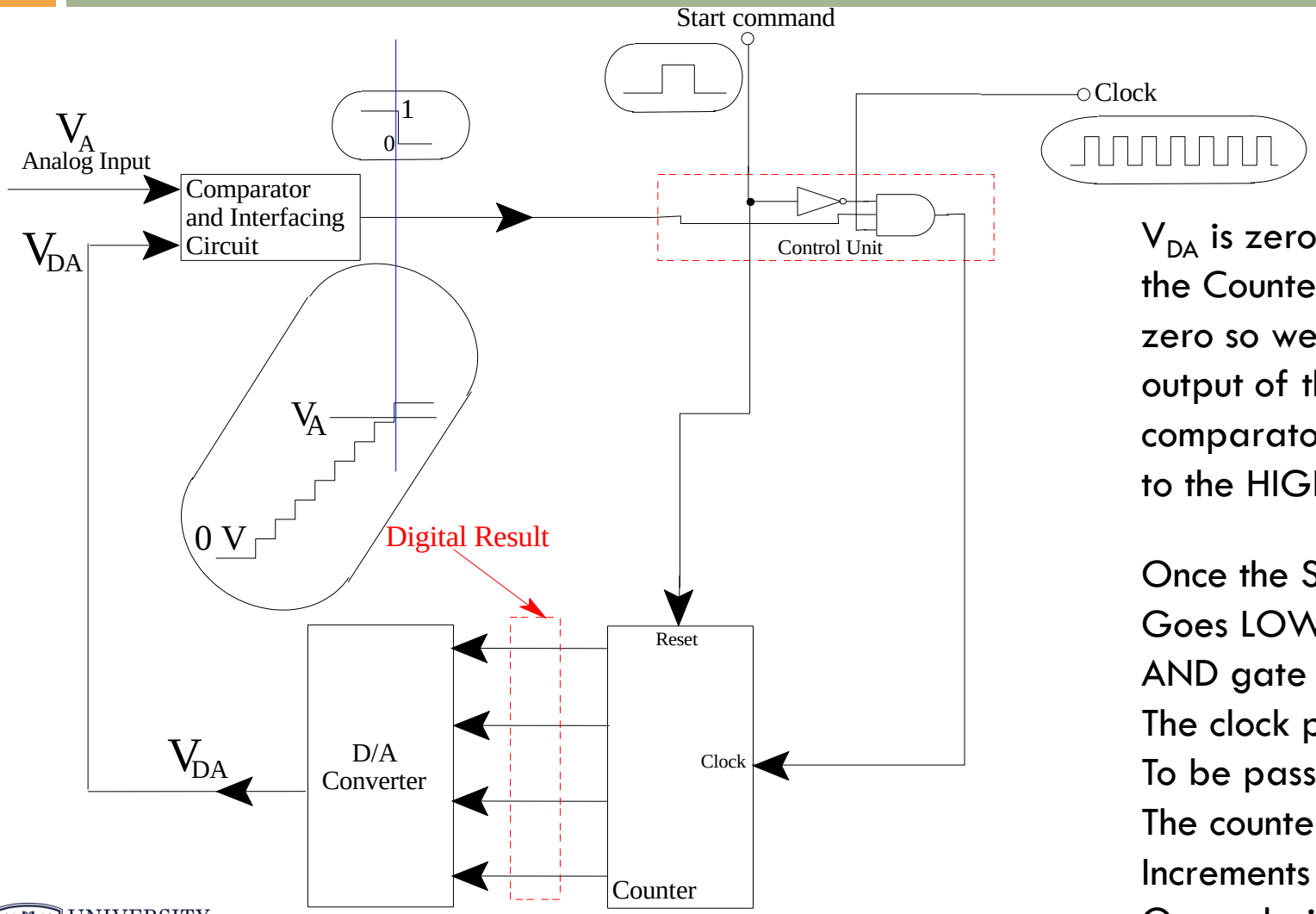
Digital Ramp ADC Converter



We assume that V_A Is a positive valued Voltage signal

Initially the start pulse Is applied, and the Counter is reset to Zero state, while the Clock pulses Are inhibited by the AND gate.

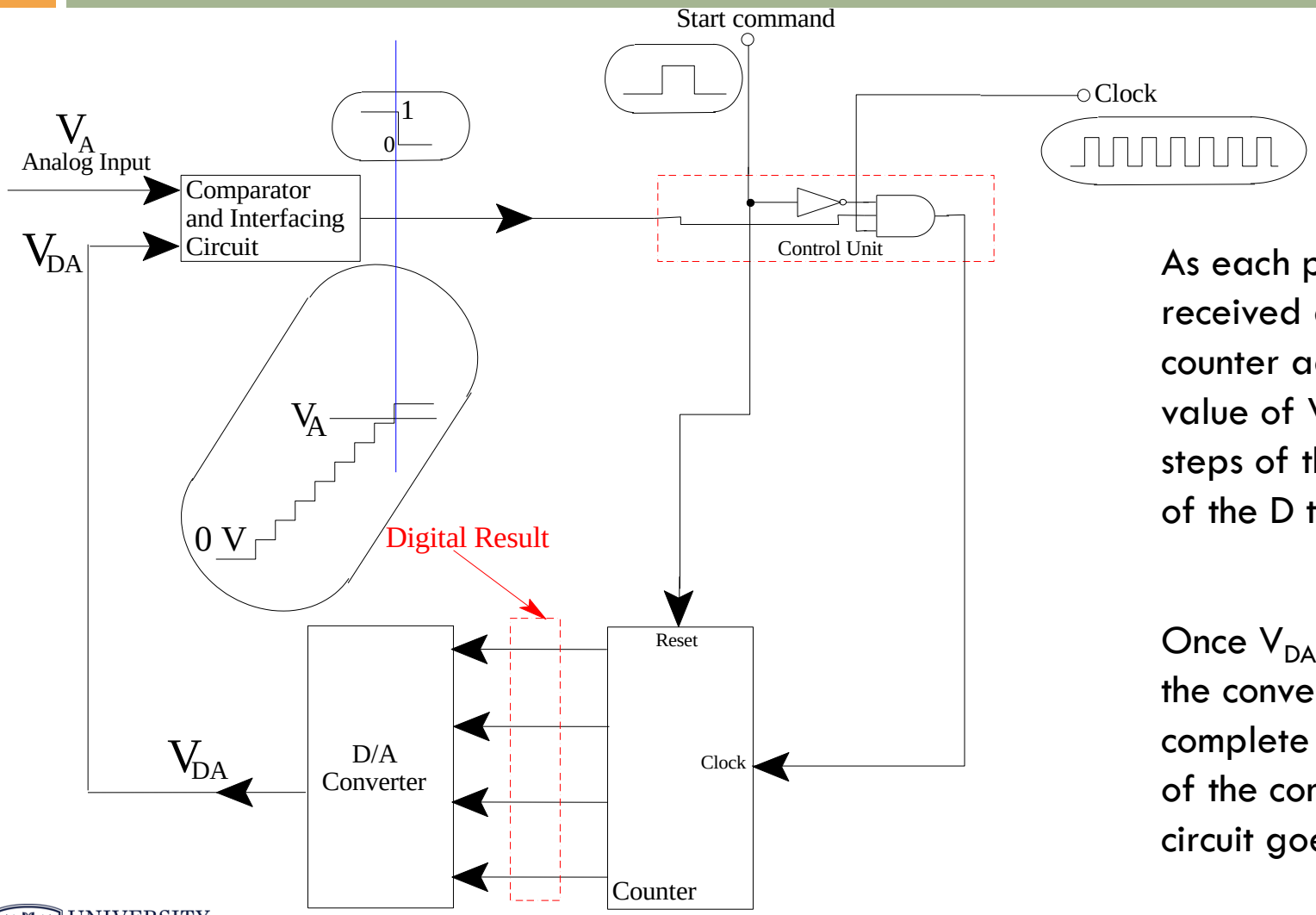
Digital Ramp ADC Converter



V_{DA} is zero when the Counter is reset to zero so we expect the output of the comparator to go to the HIGH state (1)

Once the Start pulse Goes LOW (0) the AND gate enables The clock pulses To be passed to The counter which Increments its value On each rising edge

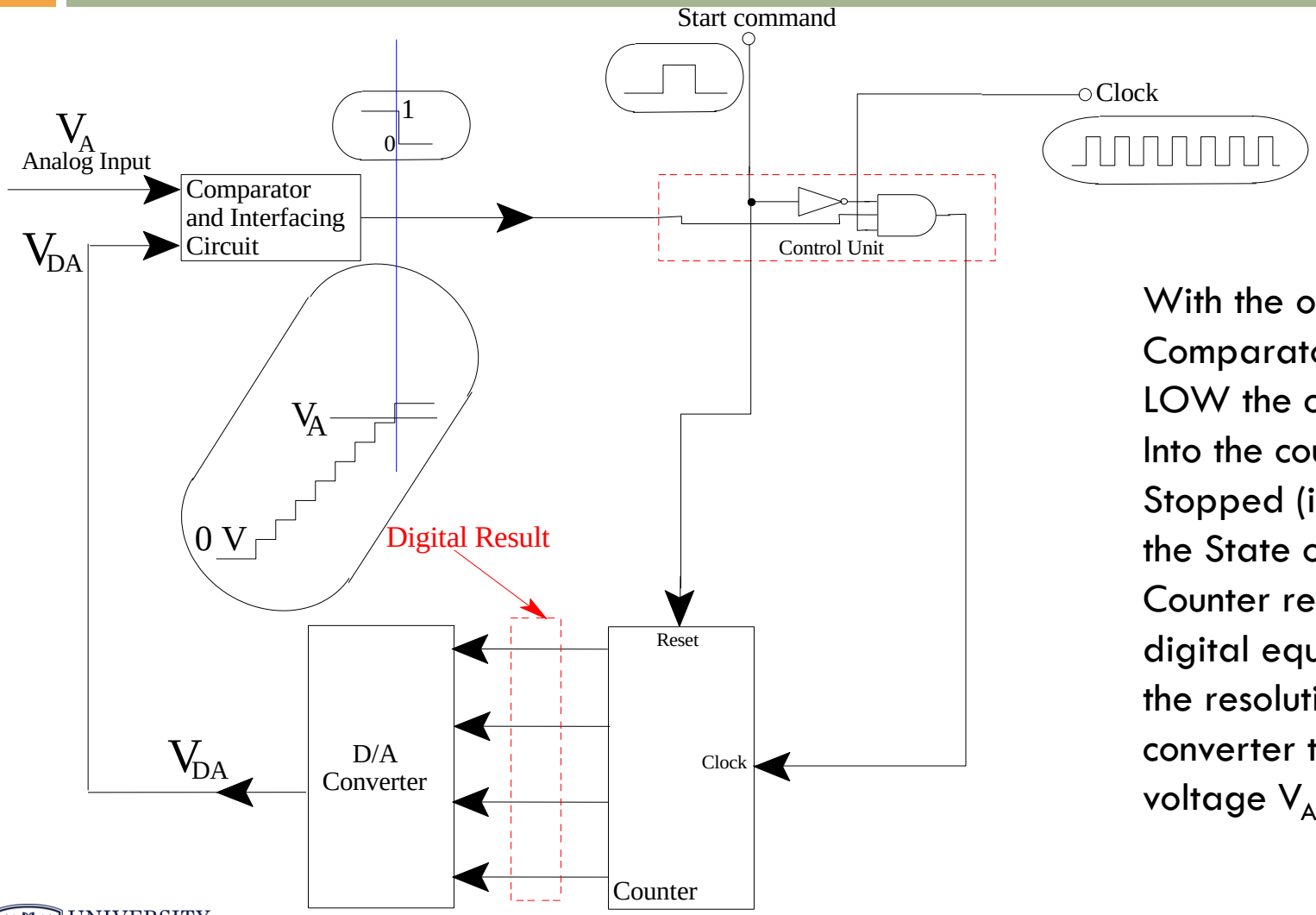
Digital Ramp ADC Converter



As each pulse is received and the counter advances the value of V_{DA} increases in steps of the resolution of the D to A.

Once V_{DA} exceeds V_A the conversion is complete and the output of the comparator circuit goes low!

Digital Ramp ADC Converter

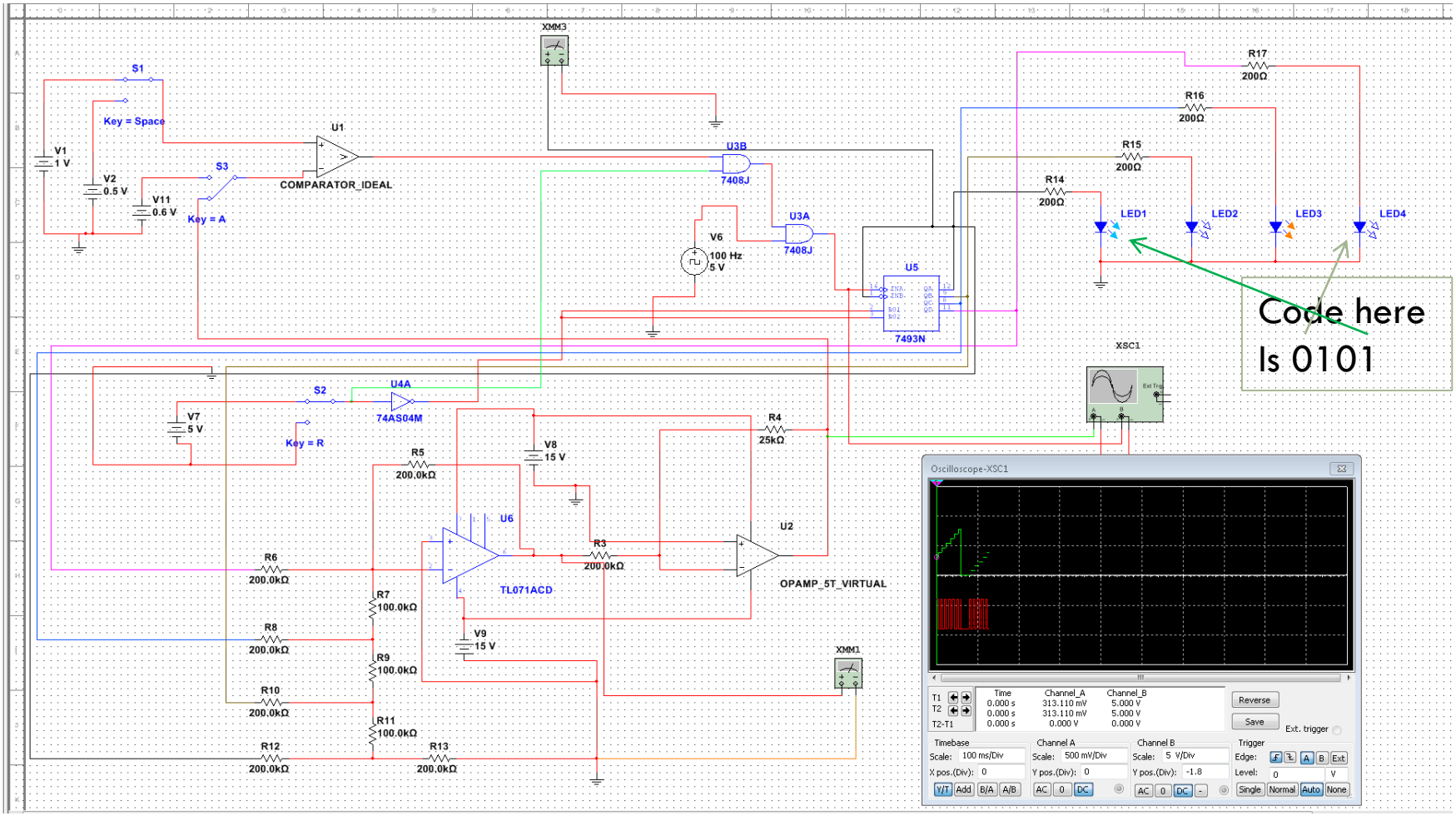


With the output of the Comparator going LOW the clock pulses Into the counter are Stopped (inhibited) and the State of the Counter represents the digital equivalent within the resolution of the converter to the input voltage V_A

Digital Ramp ADC Converter Simulation

- There is a Multisim 12 simulation on Moodle
- Toggling 'R' resets the counter (must be +5V to enable counter)
- 'Space Bar' switches between 1V and 0.5V signal for V_A

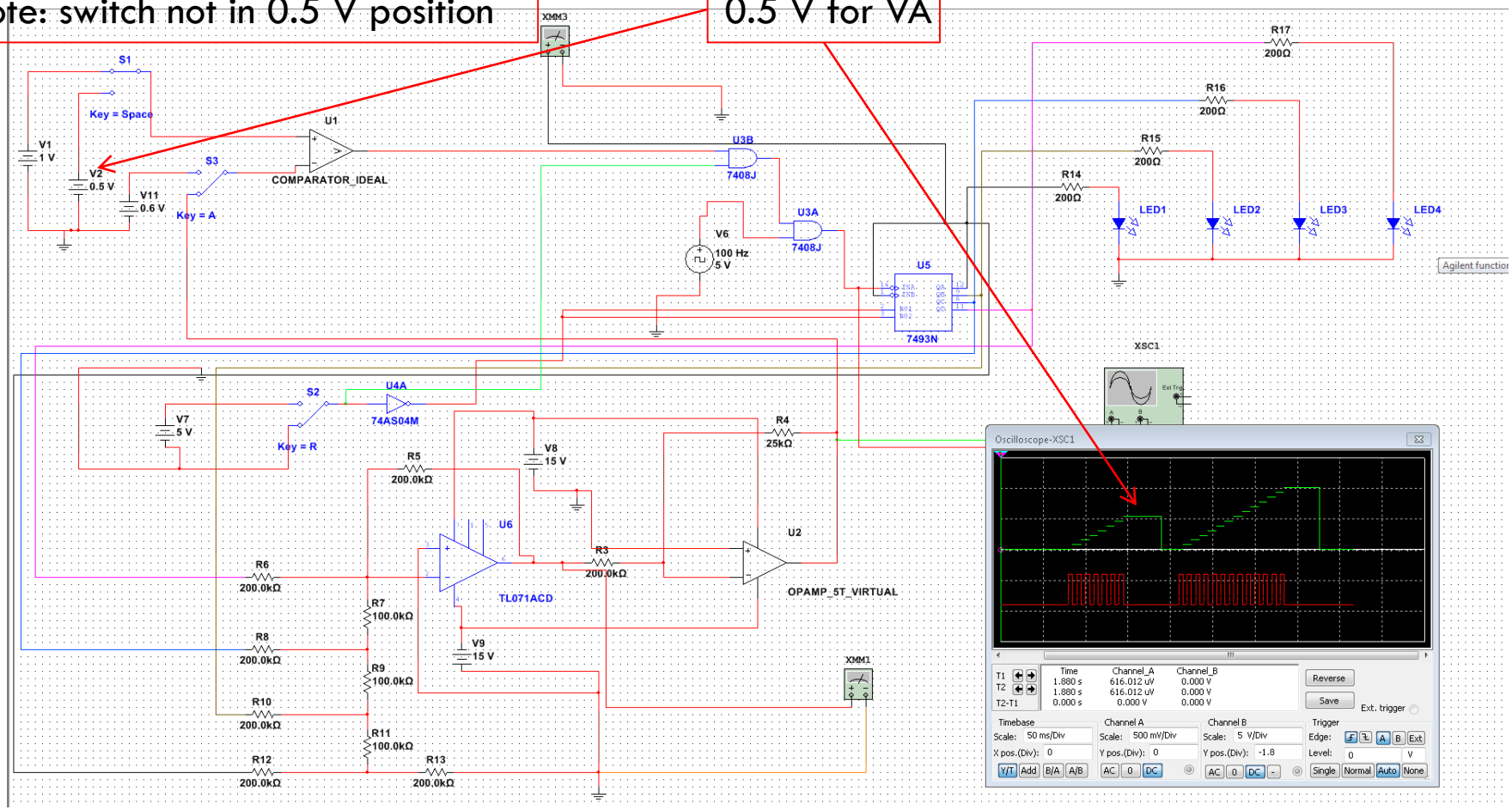
Digital Ramp ADC Converter Simulation



Digital Ramp ADC Converter Simulation

Note: switch not in 0.5 V position

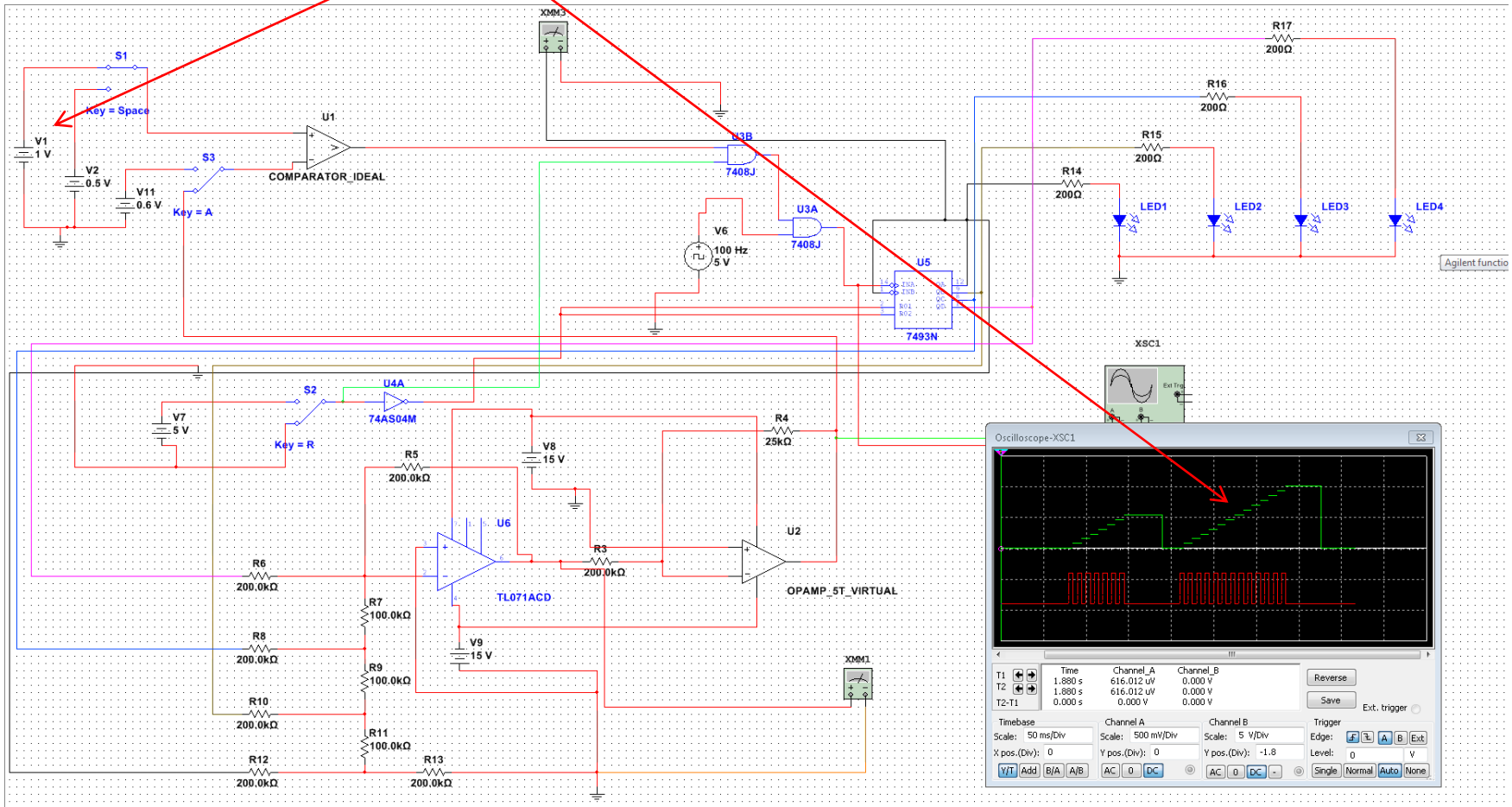
0.5 V for VA



Digital Ramp ADC Converter Simulation

1 V for VA

Note: This design has a Vref of about 1.1V



Example

An A/D converter has a clock frequency of 10 kHz. The full scale output of the D/A is 4.13 Volts with a 3-bit input. The comparator threshold voltage is 1mV. If V_A=2.1 Volts determine:

a) The digital number obtained from the counter

b) The conversion time

c) The converter resolution

Answer

a) We have an 3-bit input thus total possible steps is:

$$2^n = 2^3 = 8$$

With the full scale voltage being 4.130 Volts then step size

Is given by:

$$\frac{full \quad scale \quad voltage}{number \quad of \quad steps} = \frac{4130}{8} = 516.25 \quad mV$$

Given V_A=2.1 V and that the threshold voltage is 1mV then V_{DA} must be 2.101V or more before a comparator change in state is possible, which means that the voltage will need to rise to the largest nearest multiple of 516.25mV which is 2581.25mV and then the number of steps needed is:

$$\frac{2581.25}{516.25} = 5 \quad steps$$

Hence the digital number at the output of the A/D will be 5 or in 3 bit binary 101

Answer

b) We have a clock frequency of 10kHz or 100msec between pulses, so the time taken is simply 5 times 100 msec or 500 msecs, the maximum time is the maximum count, which here Would be 7 times 100msec or 0.7 ms

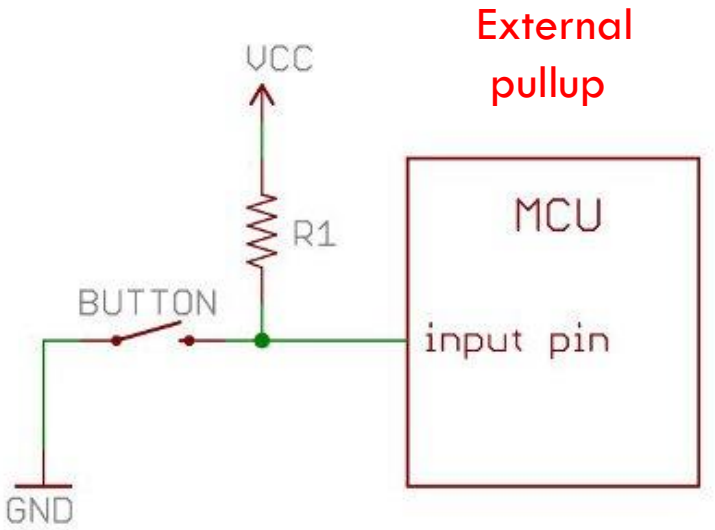
c) We find resolution from the step size of the D/A which here is 516.25mV. This can also be expressed as a percentage:

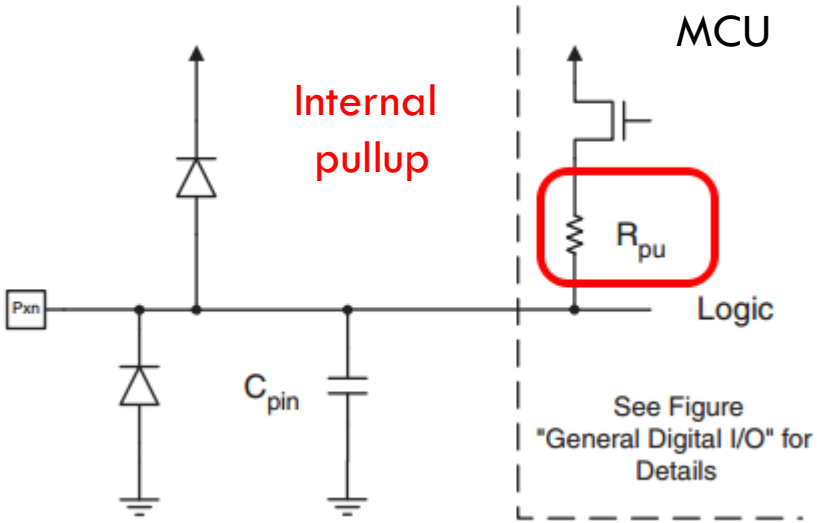
$$\frac{516.25}{4130} \times 100 = 12.5\%$$

Errors due to resolution have a Special name →Quantization error!

Arduino I/O

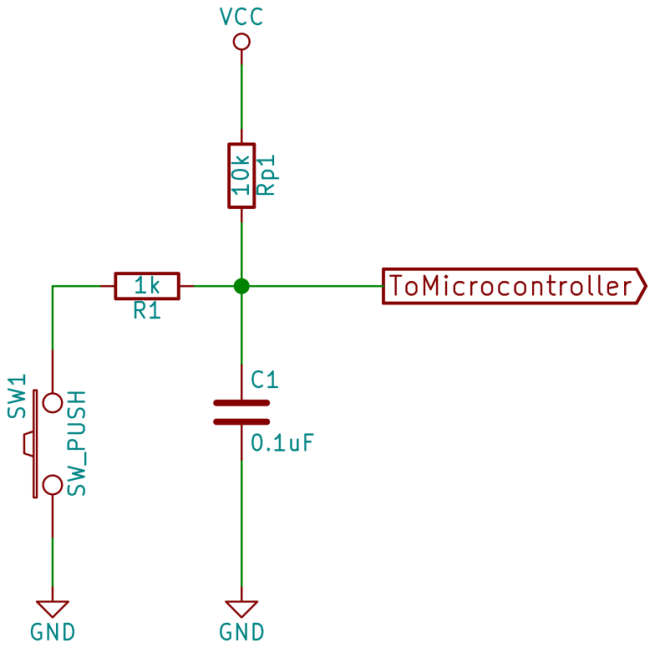
- If needed Arduino Pins can provide internal Pull Up to avoid floating input pins
  - pinMode(ledPin, INPUT PULLUP);
  - Use optoisolator or series resistor to limit the current of the I/O pins





Arduino I/O

- Simpler debounce circuit
  - Fine non edge sensitive Arduino input (slower, may not filter out all bounces).



Acknowledgement

- Peter Vial, UOW; Stefano Fasciani, Oslo University