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1. INTRODUCTION

This specification describes the Personal Computer Memory Card International Association (PCMCIA) and the Japan Electronics and Information Technology Industries Association (JEITA) ***ExpressCard Standard***. It covers the ExpressCard electrical specifications, module specifications, connector specifications, and host system requirements.

1.1 ExpressCard Standard Overview

An ExpressCard module is a small, modular add-in card technology based on PCI Express and Universal Serial Bus (USB) interfaces. ***Figure 1-1*** illustrates two examples of ExpressCard applications in desktop and mobile computing host systems.

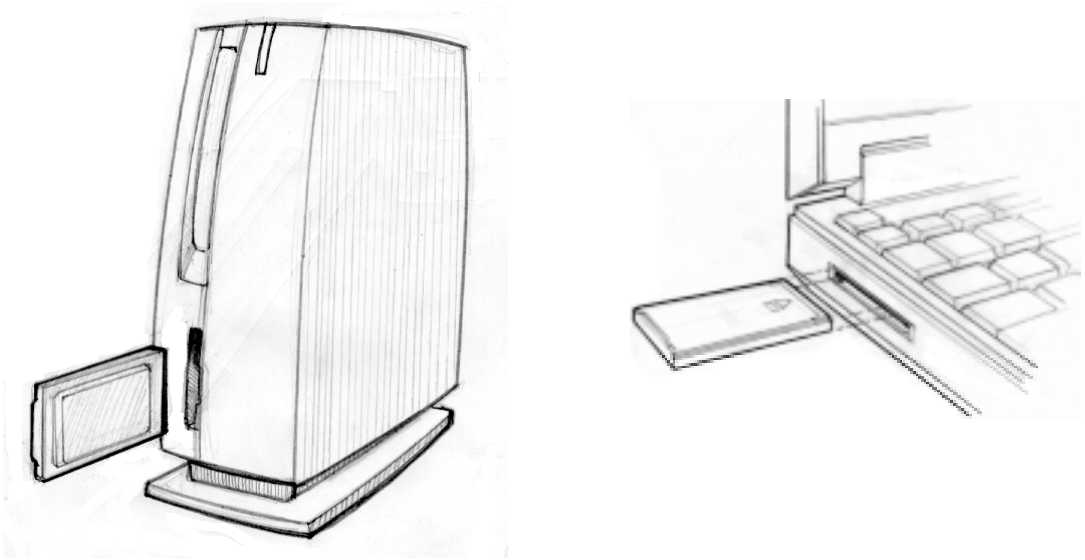

Figure 1-1: ExpressCard concepts in desktop and mobile computing host systems

The ExpressCard solution accommodates the replacement of conventional parallel buses for I/O devices with scaleable, high-speed serial interfaces. Two classes of serial interfaces are implemented by this solution, PCI Express, a high performance, integrated I/O interconnect solution, and USB for the ease of upgrading PC Card technologies and integrating popular external peripheral functionality via the ExpressCard module form-factor.

Two standard module formats are specified: an ExpressCard/34 module and an ExpressCard/54 module. The ExpressCard solution is designed to support a universal slot configuration that allows either ExpressCard/34 or ExpressCard/54 modules to function in the same slot. Host solutions that implement slots that only support ExpressCard/34 modules are also allowed by this standard.

The ExpressCard architecture is based on an extensible, modular implementation, allowing multiple slots as illustrated in ***Figure 1-2***. In any multi-slot host implementation, all slots provide equivalent I/O interface functionality and the choice of which slot to use for any given module is irrelevant. Both module formats afford access to the same I/O interface performance and source power although

the larger ExpressCard/54 module affords the application nominally 140% the internal volume and 160% the thermal dissipation capacity over the ExpressCard/34 module.

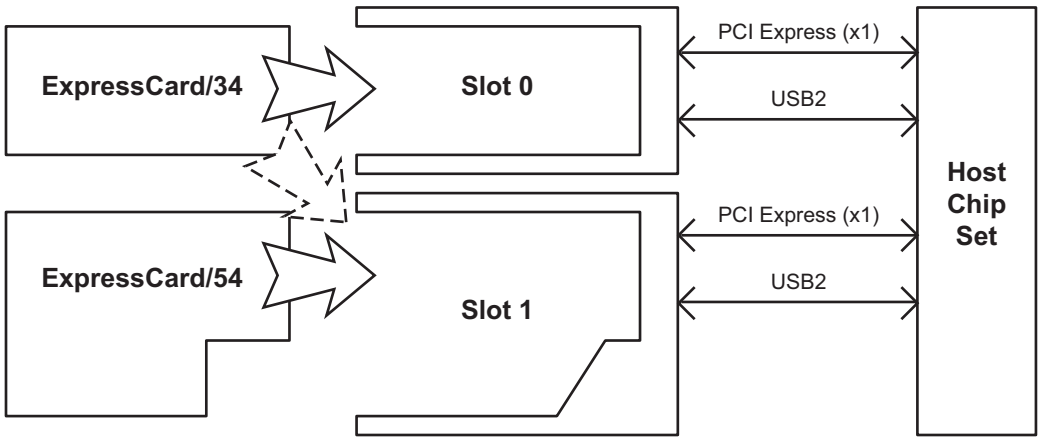

Figure 1-2: Modular implementation concept

PCI Express is a dual-simplex 2.5 Gbps (with optional support for 5.0 Gbps) differential serial link solution standardized by the PCI Special Interest Group (PCI-SIG). USB 2.0 is a full-duplex 480 Mbps differential serial bus solution standardized by the USB Implementers Forum (USB-IF). USB 3.0 SuperSpeed is a standardized extension to USB 2.0 that adds a dual-simplex 5.0 Gbps differential serial link. The ***ExpressCard Standard*** defines the modular implementation of the PCI Express and USB based on normative references to each interface's baseline specifications as defined within their respective parent organizations.

Each slot of the ExpressCard host interface must support a single PCI Express lane (x1) operating at the baseline 2.5 Gbps data rate as defined by the ***PCI Express Base Specification***. The ExpressCard host interface must also support the low-, full- and high-speed USB data rates as defined by the ***USB 2.0 Specification***. Support of both interfaces at these baseline rates is a condition for being an ExpressCard-compliant host system. With the introduction of ExpressCard Standard 2.0, optional support for extending both the PCI Express and USB data interfaces for operating at 5.0 Gbps data rate is defined. Given the 5.0 Gbps data rate is implemented, the host interface must support the use of this data rate in both the PCI Express and USB interface protocols with the ability to dynamically configure to the appropriate protocol based on the capabilities available on the module inserted into the slot.

To assist in applications that require special sideband system management features, ExpressCard host systems may also connect a two-wire SMBus interface to the slot. If available, ExpressCard modules may provide support for such features as remote alerting and sideband radio control.

For wake-up support when an ExpressCard module and its host system is in a low-power state, a sideband wake signal is available in the slot to bring the host system out of a sleep state, re-power the interface and allow the module to initiate an appropriate power management event via the native I/O interface. The sideband wake signal is only supported and implemented by ExpressCard PCI Express functions. ExpressCard USB functions do not use the sideband wake signal protocol.

1.2 Relationship to the PC Card Standard

The ***ExpressCard Standard*** is a member of the family of standards published by the PCMCIA. The ***PC Card Standard***, which defines the popular CardBus™ and 16-bit PC Card add-in cards based on a 68-pin connector, represents the first and second generations of the PC Card modular form-factor model in which ExpressCard technology bases its heritage.

ExpressCard technology is complimentary to CardBus PC Card technology. Systems implementers may determine that host systems will be best served by having both solutions supported in a single host system as the migration from traditional 68-pin PC Cards may occur gradually over an extended period in the market.

1.3 Conventions

This section is intended to give general descriptions of notation conventions used in this document.

1.3.1 Signal Naming

All signals are named with respect to their asserted state as follows:

a) Each signal which is not a logic signal, such as **+3.3V**, has a name which does not end with the "#" character.

b) Each logic signal whose name does not end with the "#" character has logic high as the asserted state and logic low as the negated state.

c) Each logic signal whose name ends with the "#" character has logic low as the asserted state and logic high as the negated state.

1.3.2 Numeric Representation

Numbers are expressed as follows:

a) Individual bits are expressed as "0" for zero, "1" for one, or "X" for "any value".

b) Groups of bits (fields) are expressed in hexadecimal number that begin with one or more digits and are followed by an "H". Each digit represents 4 bits and is indicated by the characters "0" through "9" and "A" through "F" giving each digit a value of 0 to 15 (decimal). An "X" is used to indicate a digit of "any value". The number of bits in the field determines how many bits in the hexadecimal number are significant.

1.4 Terms and Abbreviations

This section is intended to give definitions for terms and abbreviations found within this document.

ACPI	Acronym for Advanced Configuration and Power Interface
asserted	A signal is asserted when it is in the state that is indicated by the name of the signal. Opposite of Negated.
Average (current)	The averaged current value over the 1-second period that represents the steady-state maximum current consumption for the given module application.
BIOS	Acronym for Basic Input/Output System. When BIOS is in Read-Only Memory devices it may be referred to as ROM BIOS.
ExpressCard/34 module	The smallest standard width module defined by this standard, characterized by its 34 mm width.
ExpressCard/54 module	The largest standard width module defined by this standard, characterized by its 54 mm width and nominally 140% the volume of the ExpressCard/34 module.
extended module	Any ExpressCard module that is more than 75 mm long.
host	A computer system or other equipment that contains hardware (a slot) and software for utilizing an ExpressCard module.
host System	Same as host
I/O	An abbreviation for Input/Output.
JEITA	Acronym for Japan Electronic and Information Technology Industry Association
Max (current)	The absolute maximum current value that may be measured outside of the initial in-rush current that is allowed during the power ramp-up period.
negated	A signal is negated when it is in the state opposed to that which is indicated by the name of the signal. See the Conventions section. Opposite of Asserted.
operating system	Software on a host system that manages resources and provides services, including power management services, device drivers, user mode services, and/or kernel mode services.
optional	A characteristic or feature that is not mandatory, but is specifically permitted. If an optional characteristic or feature is present, it must be implemented as described in this the ***ExpressCard Standard***. Optional characteristics or features are specifically identified.
PC Card	A memory or I/O card compatible with the ***PC Card Standard***. When cards are referred to as PC Cards, what is being addressed are those characteristics common to both 16-bit PC Cards and CardBus PC Cards.
PC Card Standard	The ***PC Card Standard*** published by the PCMCIA and providing the specifications for PC Cards.
PCI	Acronym for the Peripheral Component Interface bus
PCI Express	A scaleable full-simplex serial bus standard which operates at 2.5Gbps and offers both asynchronous and isochronous data transfers.
PCI-SIG	Acronym for PCI Special Interest Group.
PCMCIA	Acronym for the Personal Computer Memory Card International Association
plug-n-play	An ability to insert and put into operation, or remove a module without cycling the system power, re-booting the system, or requiring a manual user intervention for configuration.
power management	Mechanisms in software and hardware to minimize system power consumption, manage system thermal limits, and maximize system battery life. Power management involves tradeoffs among system speed, noise, battery life, and AC power consumption.
pull-ups	Resistors used to insure that signals maintain stable values when no agent is actively driving the bus or signal.
Rx (or RX)	Differential Receiver Input
slot	The slot is the hardware, 26-pin slot, in the host which is responsible for accepting an ExpressCard module into the host and mapping the host's internal signals to the ExpressCard interface signals.
Tx (or TX)	Differential Transmitter Output
Universal Serial Bus	A two-wire, half-duplex serial bus standard which allows operation at up to 480 Mbps and offers both asynchronous and isochronous data transfer.
universal slot	Any slot that accepts either an ExpressCard/34 module or an ExpressCard/54 module.
USB	See Universal Serial Bus.

USB-IF	Acronym for USB Implementers Forum

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2. RELATED DOCUMENTS

The following reference documents provide normative requirements as specified in the body of this standard.

- ***PCI Express Base Specification 2.0*** – PCI Special Interest Group (PCI-SIG)
- ***USB Specification, Release 2.0*** – Universal Serial Bus Implementers Forum (USB-IF)
- ***USB Specification, Release 3.0*** – Universal Serial Bus Implementers Forum (USB-IF)
- ***System Management Bus (SMBus) Specification, Version 2.0*** - Smart Battery System Implementer's Forum (SBS-IF)
- ***EIA-364-1000.01: Environmental Test Methodology for Assessing the Performance of Electrical Connectors and Sockets Used in Business Office Applications***
- ***PCI Express Card Electromechanical (CEM) Specification 2.0*** – PCI Special Interest Group (PCI-SIG)
- *PHY Electrical Test Specification for PCI Express Architecture* (PCI SIG)

The following reference documents are provided as informative sources for related information.

- ***ExpressCard Implementation Guidelines*** - Personal Computer Memory Card International Association (PCMCIA)/Japan Electronics and Information Technology Industries Association (JEITA)
- ***PC Card Standard, Release 8.1*** – Personal Computer Memory Card International Association (PCMCIA)/Japan Electronics and Information Technology Industries Association (JEITA)
- ***Advanced Configuration and Power Interface (ACPI) Specification, Revision 3.0b*** – Compaq Computer Corporation, Intel Corporation, Microsoft Corporation, Phoenix Technologies Ltd., Toshiba Corporation
- ***PCI Bus Power Management Interface Specification, Revision 1.2*** – PCI Special Interest Group (PCI-SIG)
- ***PCI Express to PCI/PCI-X Bridge Specification, Revision 1.0*** – PCI Special Interest Group (PCI-SIG)
- ***PCI Firmware Specification, Revision 3.0*** - PCI Special Interest Group (PCI-SIG)

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3. ELECTRICAL SPECIFICATIONS

The Electrical Specification describes the connector pin out, interface protocol, signaling environment, interface timings, and specifics of module insertion, removal, and power up.

3.1 Signal Descriptions

There are two primary I/O interface standards supported by the ***ExpressCard Standard***: PCI Express and USB. An ExpressCard module may implement either one or both of the standard interfaces depending on what the requirements are for the application. ***Table 3-1*** summarizes the list of signals.

Table 3-1: ExpressCard interface – List of Signals

Signal Group	Signal	Direction	Description
PCI Express	**PETp0** **PETn0** **PERp0** **PERn0**	Input/Output	PCI Express x1 data interface. One differential transmit pair and one differential receive pair (Note: these signals overlay the USB 3.0 data interface at the slot connector.)
	REFCLK+ **REFCLK-**	Input	PCI Express differential, spread-spectrum reference clock
	PERST#	Input	PCI Express functional reset
Universal Serial Bus (USB)	**USBD+** **USBD-**	Input/Output	USB serial data interface
	SSTX+ **SSTX-** **SSRX+** **SSRX-**	Input/Output	USB 3.0 SuperSpeed serial data interface. One differential transmit pair and one differential receive pair (Note: these signals overlay the PCI Express x1 data interface at the slot connector)
SMBus	**SMBDATA** **SMBCLK**	Input/Output Input/Output	SMBus management channel
System auxiliary signals	**CPPE#**	Output	This signal is used for PCI Express-based module detection and power control
	CPUSB#	Output	This signal is used for USB-based module detection and power control
	USB3#	Input/Output	This signal is used for USB 3.0-based interface detection
	CLKREQ#	Output	This signal is used to indicate when REFCLK is needed for the PCI Express interface
	WAKE#	Output	This signal is to request that the host system return from a sleep/suspended state to service a PCI Express function initiated wake event
Power	**+3.3V** (2 pins)		Primary voltage source
	+3.3VAUX (1 pin)		Auxiliary voltage source
	+1.5V (2 pins)		Secondary voltage source
	GND (4 pins)		Return current path

3.1.1 Pin Assignments

This section identifies the required and optional signals for modules and host systems. The physical definition of the slot and pin numbers for module and host connectors will be given in ***Section 5.1 – Module Connector*** and ***Section 5.2 – Host Connector,*** respectively.

Table 3-2 lists the pin assignments for the standard connector that is used for ExpressCard modules and host slots. The I/O column of this table indicates the nature of the signal from the module's perspective.

Table 3-2: ExpressCard interface – Pin assignments for ExpressCard connectors

Pin No.	Signal	I/O	Interface Type(s) on module			Host	Notes
			PCI Express	USB	Both		
26	GND		R	R	R	R	
25	PETp0/SSTX+	I	R	Opt	R	R	4
24	PETn0/SSTX-	I	R	Opt	R	R	4
23	GND		R	R	R	R	
22	PERp0/SSRX+	O	R	Opt	R	R	5
21	PERn0/SSRX-	O	R	Opt	R	R	5
20	GND		R	R	R	R	
19	REFCLK+	I	R	NC	R	R	
18	REFCLK-	I	R	NC	R	R	
17	CPPE#	O	R	NC	R	R	3
16	CLKREQ#	O	R	NC	R	Opt	2
15	+3.3V		R	R	R	R	
14	+3.3V		R	R	R	R	
13	PERST#	I	R	NC	R	R	
12	+3.3VAUX		Opt	Opt	Opt	R	7
11	WAKE#	O	Opt	NC	Opt	Opt	2
10	+1.5V		Opt	Opt	Opt	R	
9	+1.5V		Opt	Opt	Opt	R	
8	SMBDATA	I/O	Opt	Opt	Opt	Opt	6
7	SMBCLK	I/O	Opt	Opt	Opt	Opt	6
6	RESERVED		NC	NC	NC	NC	1
5	USB3#	I/O	NC	Opt	NC	Opt	3
4	CPUSB#	O	NC	R	R	R	3
3	USBD+	I/O	NC	R	R	R	
2	USBD-	I/O	NC	R	R	R	
1	GND		R	R	R	R	

"I" indicates that the signal is input to the module, "O" indicates that the signal is output from the module.

"R" indicates the signal is required, "Opt" indicates the signal is optional, and "NC" indicates the signal is not to be connected.

1. Reserved for future use by the module interface. Compliant ExpressCard modules and host slots shall leave these pins unconnected.
2. If implemented, a host pull-up resistor (≥5 KΩ) tied to no higher than +3.3VAUX is required on this pin. Please refer to the ***ExpressCard Implementation Guidelines*** for more information regarding pull-up resistor values.
3. When implemented, a host pull-up resistor in the range of 100KΩ– 200KΩ is required on these pins.
4. PETp0 and PETn0 shall be connected to the transmitter differential pair on the host and to the receiver differential pair on the ExpressCard module. For USB 3.0 use, SSTX+ and SSTX- shall be similarly connected within the host and the module.
5. PERp0 and PERn0 shall be connected to the receiver differential pair on the host and to the transmitter differential pair on the ExpressCard module. For USB 3.0 use, SSRX+ and SSRX- shall be similarly connected within the host and module.
6. If SMBus is not implemented, module pins cannot exceed the electrical characteristics of an unpowered SMBus node as described in the SMBus specification.

7. USB modules that support remote wakeup from USB bus suspend states may use +3.3VAUX to implement this capability as the host system may remove +3.3V power during a host system suspend state.

3.1.2 Signal/Pin Description

For the signal/pin descriptions, signal types are indicated as follows:

in	Input is a standard input-only signal.
out	Totem Pole Output is a standard active driver.
i/o	Input/Output is a bi-directional signal.
diff	Low-voltage differential signal pair.
o/d	Open Drain allows multiple devices to share a signal as a wire-OR.
DC	DC refers to power or ground pins that are not used for any information transfer.

3.1.2.1 PCI Express Pins

PETp0, PETn0	diff	These pins are required to implement the system's transmit lane of a PCI Express x1 interface. These pins shall be connected to the transmitter differential pair in the system and to the receiver differential pair on the module. The ***PCI Express Base Specification*** defines all electrical characteristics, enumeration, protocol, and management features for this interface. Note: For host systems that implement USB 3.0 support, these pins are shared with the USB 3.0 SuperSpeed interface and the selection of which interface is to be activated for a given ExpressCard module is determined by the state of the **USB3#** signal.
PERp0, PERn0	diff	These pins are required to implement the system's receive lane of a PCI Express x1 interface. These pins shall be connected to the receiver differential pair in the system and to the transmitter differential pair on the module. The ***PCI Express Base Specification*** defines all electrical characteristics, enumeration, protocol, and management features for this interface. Note: For host systems that implement USB 3.0 support, these pins are shared with the USB 3.0 SuperSpeed interface and the selection of which interface is to be activated for a given ExpressCard module is determined by the state of the **USB3#** signal.
REFCLK+, REFCLK-	diff	These pins are used to implement the reference clock of a PCI Express interface. ***The PCI Express Base Specification*** defines all electrical characteristics, protocol, and management features for this interface
PERST#	in	This signal is to indicate to the ExpressCard module that power supplied via the **+3.3V** and **+1.5V** sources are stable. It is intended that PCI Express modules will use this signal as a hardware reset as needed. (***See Section 3.2.2 – PCI Express functional reset (PERST#)*** for further definition of this signal.)

3.1.2.2 Universal Serial Bus (USB) Pins

USBD+, USBD-	diff	These pins are required to implement USB functionality. USB 2.0 in all three modes (LS, FS, and HS) is supported. The USB 2.0 Specification defines all electrical characteristics, enumeration, and bus protocol and bus management features for this interface.
SSTX+, SSTX-	diff	These pins are required to implement the system's transmit path of a USB 3.0 SuperSpeed interface. These pins shall be connected to the transmitter differential pair in the system and to the receiver differential pair on the module. The ***USB 3.0 Specification*** defines all electrical characteristics, enumeration, protocol, and management features for this interface. Note: For host systems that implement USB 3.0 support, these pins are shared with the PCI Express interface and the selection of which interface is to be activated for a given ExpressCard module is determined by the state of the **USB3#** signal.
SSRX+, SSRX-	diff	These pins are required to implement the system's receive path of a USB 3.0 SuperSpeed interface. These pins shall be connected to the receiver differential pair in the system and to the transmitter differential pair on the module. The ***USB 3.0 Specification*** defines all electrical characteristics, enumeration, protocol, and management features for this interface. Note: For host systems that implement USB 3.0 support, these pins are shared with the PCI Express interface and the selection of which interface is to be activated for a given ExpressCard module is determined by the state of the **USB3#** signal.

3.1.2.3 SMBus Pins

SMBDATA	i/o, o/d	This pin is for the data path for an optional implementation of the SMBus. The ***SMBus Specification*** defines the functionality of this interface.
SMBCLK	i/o, o/d	This pin is for the clock for an optional implementation of the SMBus. The ***SMBus Specification*** defines the functionality of this interface.

3.1.2.4 System Auxiliary Pins

CPPE#	out	This signal is hard-wired to GND on modules that use the PCI Express interface. (See ***Section 3.2.1 – Module presence pins (CPPE# and CPUSB#)*** for further definition of this signal.)
CPUSB#	out	This signal is hard-wired to GND on modules that use the USB interface. (See ***Section 3.2.1 – Module presence pins (CPPE# and CPUSB#)*** for further definition of this signal.)
USB3#	in, out	This signal is only used on modules that implement the USB 3.0 SuperSpeed interface. (See Section 3.2.7.2 Modules Implementing USB 3.0 for further definition of this signal.)
WAKE#	out, o/d	The module asserts this signal to request that the host interface return to full operation and respond to PCI Express requests. (See ***Section 3.2.8.1 – PCI Express WAKE#*** for further definition of this signal.)
CLKREQ#	out, o/d	A PCI Express module asserts this signal to request that REFCLK be enabled to allow the PCI Express interface to be active. (See ***Section3.2.3 PCI Express Reference Clock (REFCLK+ / REFCLK-)*** for further definition of this signal.)

3.1.2.5 Power Pins

+3.3V	DC	Primary voltage source that establishes signaling interface voltage; this source may only be present when either **CPPE#** or **CPUSB#** is true (0)
+3.3VAUX	DC	Auxiliary voltage source supplied to allow the module to support limited operation and create wake requests while the host is suspended; this source may only be present when either **CPPE#** or **CPUSB#** is true (0).
+1.5V	DC	Secondary voltage source that is intended to support silicon core power requirements; this source may only be present when either **CPPE#** or **CPUSB#** is true (0)
GND	DC	Return current path

3.1.3 Voltages and Grounds

+3.3V, **+1.5V**, and **+3.3VAUX** are used to supply power to the module. **GND** pins are used as the return current path for all the voltage sources. The placement of the **GND** pins has been selected such that they provide a ground reference to the differential signal paths as they pass through the connector.

All voltage and ground pins are longer on the module connector such that they mate first on module insertion and disconnect last on module removal to help address ESD suppression and minimize opportunity for latch-up conditions in module silicon. The time difference for first mate/last disconnect relative to the remaining interface signals is not specified as this is directly related to the physical module insertion and removal speed as dictated by user handling. Pin length dimensions are defined in ***Section 5.1 – Module Connector***.

For electrical characteristics of the voltage sources, see ***Section 3.3 – Electrical Requirements***.

3.1.4 SMBus Support

SMBus is a system management feature that is optional for both host systems and modules. Potential applications include client alerting, wireless RF management, and any sideband management applications that can be standardized within the generic SMBus protocol.

The performance specifications and application usage for SMBus is outside of the scope of this standard. Refer to the ***System Management Bus (SMBus) Specification, Version 2.0*** and other applicable documents as needed to implement these functions.

An address resolution protocol (ARP) is defined in the ***SMBus Specification, Version 2.0*** that is used to assign slave addresses to SMBus devices. Although optional in the ***SMBus Specification, Version 2.0***, it is required that systems and modules that connect the SMBus via the ExpressCard slot implement the ARP for assignment of SMBus slave addresses to SMBus interface devices on ExpressCard modules.

When power is applied to an SMBus device, it must perform default initialization of internal state as specified in the ***SMBus Specification, Version 2.0***. SMBus device interface logic is not affected by PERST#. This normally allows the SMBus to support communications when the PCI Express or USB interfaces cannot.

A host system that does not support the optional SMBus interface must provide individual pull-up resistors (~5 kΩ) on the SMBCLK and SMBDAT pins for the ExpressCard slot connectors. A host system that supports the SMBus interface must provide pull-up devices (passive or active) on SMBCLK and SMBDAT as defined in the ***SMBus 2.0 Specification***. The pull-ups must be connected

to the power source attached to the **+3.3VAUX** pin of the ExpressCard connector for host systems with the optional auxiliary power supply and to **+3.3V** supply for host systems without the optional supply.

3.2 Module Detection and Operation

Module detection and operation consists of the following fundamental elements.

- Module physical presence and power control in the slot based on the state of **CPPE#** and **CPUSB#**
- Module power state and functional reset based on the state of **PERST#** (for PCI Express-based modules only)
- Control of REFCLK to the slot based on the state of **CPPE#** and/or **CLKREQ#** (for PCI Express-based modules only)
- Wakeup requests based on the state of **WAKE#** (PCI Express-only) and the in-band wakeup protocols of PCI Express and USB
- I/O interface detection, set-up and operation based on the state of **USB3#** and the in-band capabilities of the appropriate interface, either PCI Express, USB, or both

I/O interface detection, set-up and operation varies based on which interface is being used. All other module interface functions are specified identically independent of interface type of the module.

3.2.1 Module presence pins (CPPE# and CPUSB#)

For all modules, the module presence pin is a required signal that is used to facilitate module detection and control power to the slot. **CPPE#** is used to indicate module presence for PCI Express-based modules and **CPUSB#** is used to indicate module presence for USB-based modules. If the module implements both PCI Express and USB interfaces, then both **CPPE#** and **CPUSB#** are both used. **CPPE#** and **CPUSB#** are outputs from the module and is required to be pulled-up by the host system.

Figure 3-1 illustrates module detect logic as a generalized schematic and shows example modules inserted into example slots. For all modules, the appropriate module presence pin is to be internally strapped to ground (**GND**).

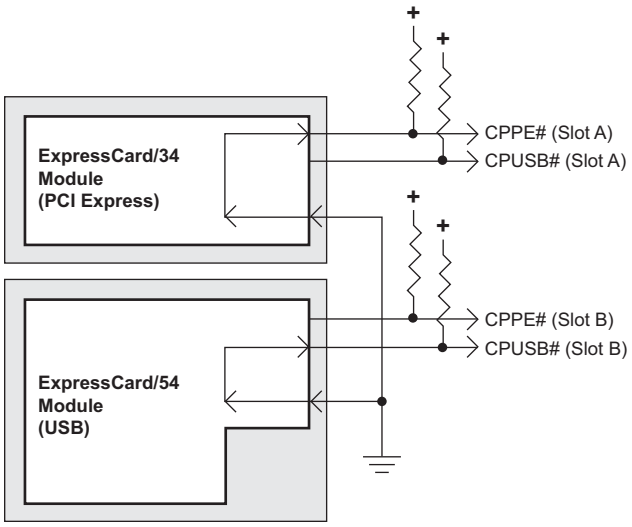


Figure 3-1: Module presence pin schematic examples

The primary purpose for the module detect logic is to inform the host system that a module is present in the slot and be used by the system to turn on power to the slot. There are three common system conditions during which a module insertion is likely.

1. The module is inserted prior to system power being available, e.g. host system is off. In this case, no immediate action as the result of module insertion is allowed. Once system power is available, the module slot will be powered following the power control and timing of the host system's boot process.
2. The module is inserted during normal system operation, e.g. host system is on and fully functional. In this case, module detection should be immediate and slot power will be made available to the module.
3. The module is inserted while the host system is in a sleep state, e.g. system auxiliary power is on but primary power is off. In this case, no immediate action as the result of the module insertion is allowed. Once the host system exits the sleep state and primary power is restored, the module slot will be powered following the power control and timing of the host system's return from sleep state process.

3.2.2 PCI Express functional reset (PERST#)

For PCI Express-based modules, the functional reset (**PERST#**) signal is asserted by the host system whenever the module is to be placed in a reset state. During changes in power state, the state of **PERST#** indicates to the module the status of the primary power rails (i.e. **PERST#** is asserted while primary power is un-stable or off and is de-asserted when primary power is on and stable within specified voltage tolerance) and the reference clock (REFCLK) is available and stable to the module.

PERST# should be used to initialize the module functions once power sources stabilize. Whenever a module is not present, the host shall keep **PERST#** asserted (grounded).

Timing for **PERST#** operation is defined in ***Section 3.2.5 – PCI Express module power control operation***. **PERST#** timing may vary depending on if the module is already installed and is being powered up at the time that the host system is turning on, or if it is being powered up resulting from a module insertion into the slot during normal system operation. Given that system power

reset is longer than the slot power reset timing, **PERST#** timing shall be extended to reflect the longer reset timing of the system.

For PCI Express-based modules, hardware must return all port registers and state machines to the initial state as specified by the ***PCI Express Base Specification*** based on the state of the **PERST#** signal. Given that the **PERST#** signal is asserted (**PERST#** = 0), even without power to the module being removed, the module must respond by entering a reset condition.

3.2.3 PCI Express Reference Clock (REFCLK+ / REFCLK-)

The **REFCLK+/REFCLK-** signals are used to assist the synchronization of the modules's PCI Express interface timing circuits. Availability of the reference clock at the module interface may be gated by the **CLKREQ#** signal as described in ***Section 3.2.4***. When the reference clock is not available, it will be in a parked state. A parked state is when the clock is not being driven by a clock driver and both **REFCLK+** and **REFCLK-** are pulled to ground by the ground termination resistors.

3.2.4 PCI Express clock request (CLKREQ#)

For PCI Express-based modules, the clock request (**CLKREQ#**) is an open drain, active low signal that is asserted to the host system whenever the module needs to have reference clock (**REFCLK+/REFCLK-**) available (active clock state) for the PCI Express interface to operate. The operation of the **CLKREQ#** signal is determined by the state of the dynamic clock management enable bit in the Link Control Register (offset 010h). When disabled, the **CLKREQ#** signal shall be asserted at all times whenever auxiliary power is applied to the module.

Whenever dynamic clock management is enabled and when a module stops driving **CLKREQ#** low, it indicates that the device is ready for the reference clock to transition from the active clock state to a parked (not available) clock state. Reference clocks are not guaranteed to be parked by the host system when **CLKREQ#** gets de-asserted and module designs shall be tolerant of an active reference clock even when **CLKREQ#** is de-asserted by the module.

The module must drive this signal low during power up, whenever it is reset, and whenever it requires the reference clock to be in the active clock state. Whenever **PERST#** is asserted, including when the device is not in D0, **CLKREQ#** shall be asserted.

It is important to note that the PCI Express device must delay de-assertion of its **CLKREQ#** signal until it is ready for its reference clock to be parked. Also, the device must be able to assert its clock request signal, whether or not the reference clock is active or parked, when it needs to put its link back into the ***L0*** link state. Finally, the device must be able to sense an electrical idle break on its up-stream-directed receive port and assert its clock request, whether or not the reference clock is active or parked.

The assertion and de-assertion of **CLKREQ#** are asynchronous with respect to the reference clock.

CLKREQ# has additional electrical requirements over and above standard open drain signals that allow it to be shared between devices that are powered off and other devices that may be powered on. The additional requirements include careful circuit design to ensure that a voltage applied to the **CLKREQ#** signal network never causes damage to a component even if that particular component's power is not applied.

Additionally, the device must ensure that it does not pull **CLKREQ#** low unless **CLKREQ#** is being intentionally asserted in all cases, including when the related function is in D3cold. This means that any component implementing **CLKREQ#** must be designed such that:

- Unpowered **CLKREQ#** output circuits are not damaged if a voltage is applied to them from other powered "wire-ORed" sources of **CLKREQ#**.
- When power is removed from its **CLKREQ#** generation logic, the unpowered output does *not* present a low impedance path to ground or any other voltage.

These additional requirements ensure that the **CLKREQ#** signal network continues to function properly when a mixture of powered and unpowered components have their **CLKREQ#** outputs wire-ORed together. It is important to note that most commonly available open drain and tri-state buffer circuit designs used "as is" do not satisfy the additional circuit design requirements for **CLKREQ#**.

This signal is required to be left unconnected on ExpressCard modules that don't implement PCI Express.

When in the L1 link state, a link is allowed to stop its internal PLL and request that the reference clock also be stopped. Modules that implement the **CLKREQ#** are allowed to stop their internal PLLs on host systems that do not honor the de-assertion of **CLKREQ#** and continue to supply **REFCLK+** and **REFCLK-** as if the **CLKREQ#** protocol had been honored.

3.2.4.1 Dynamic Clock Control

After a PCI Express device has powered up and whenever its upstream link enters the *L1* link state, it shall support allowing its reference clock to be turned off (put into the parked clock state). To accomplish this, the device de-asserts **CLKREQ#** (high) and it shall allow that the reference clock will transition to the parked clock state within a delay (T_{CRHoff}).

To exit *L1*, the device shall assert **CLKREQ#** (low) to re-enable the reference clock. After the device asserts **CLKREQ#** (low) it shall allow that the reference clock will continue to be in the parked clock state for a delay (T_{CRLon}) before transitioning to the active clock state. The time that it takes for the device to assert **CLKREQ#** and for the system to return the reference clock to the active clock state are serialized with respect to the remainder of *L1* recovery. This time shall be taken into account when the device is reporting its *L1* exit latency.

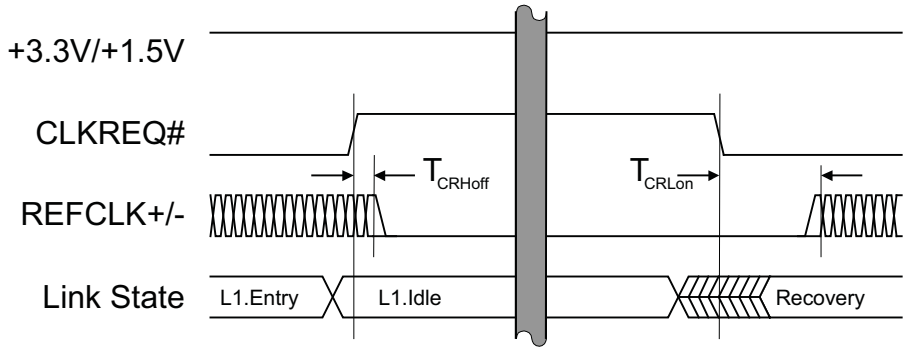


Figure 3-2: CLKREQ# Clock Control Timing

All links attached to a PCI Express device must complete a transition to the *L1.Idle* state before the device can de-assert **CLKREQ#**. The device must assert **CLKREQ#** when it detects an electrical idle break on any receiver port. The device must assert **CLKREQ#** at the same time it breaks electrical idle on any of its transmitter ports in order to minimize *L1* exit latency.

Table 3-3: CLKREQ# Clock Control Timing

Symbol	Parameter	Min	Max	Units
T_{CRHoff}	**CLKREQ#** de-asserted high to clock parked	0		ns
T_{CRLon}	**CLKREQ#** asserted low to clock active		400	ns

There is no maximum specification for T_{CRHoff} and no minimum specification for T_{CRLon}. This means that the system is not required to implement reference clock parking or that the implementation may not always act on a device de-asserting **CLKREQ#**.

A device should also de-assert **CLKREQ#** when its link is in *L2* or *L3*, much as it does during *L1*.

3.2.4.2 Clock Request Support Reporting and Enabling

Support for the **CLKREQ#** dynamic clock protocol shall be reported using bit 18 in the PCI Express link capabilities register (offset 0C4h). To enable dynamic clock management, bit 8 of the Link Control Register (offset 010h) is provided which shall be disabled by default upon initial power up and in response to any reset issued by the host system. Host system software is responsible for enabling this feature. See the *PCI Express Base Specification 1.1* (or later) for more information regarding these bits.

3.2.5 PCI Express module power control operation

This section describes power control operation at the ExpressCard interface for PCI Express-based modules. No power on either **+3.3V**, **+3.3VAUX** and **+1.5V** can be enabled to the module slot unless **CPPE#** is asserted by a module inserted into the slot.

See ***Section 3.3.3 – Power Supply Limits*** for current limits. A power supply is deemed to be within operating limits if the specified voltage is within the voltage tolerances as specified in ***Table 3-8: DC Specification for 3.3V Signaling***.

3.2.5.1 Initial power up for PCI Express-based modules

On power up, the de-assertion of **PERST#** is delayed (by T_{PVPERL}) from the power rails achieving specified operating limits to allow adequate time for the power to stabilize on the module and for the reference clock (**REFCLK+**/**REFCLK-**) to be enabled and stabilized.

CLKREQ# is asserted in response to **PERST#** assertion. On power up, **CLKREQ#** must be asserted by a PCI Express device within a delay (T_{PVCRL}) from the power rails achieving specified operating limits and **PERST#** assertion. This delay is to allow adequate time for the power to stabilize on the module and certain system functions to start prior to the module starting up. **CLKREQ#** may not be de-asserted while **PERST#** is asserted.

Prior to the de-assertion of **PERST#**, the reference clock (**REFCLK+**, **REFCLK-**) must be stable at least $T_{PERST\#-CLK}$.

Once **PERST#** is de-asserted, the module functions can start up.

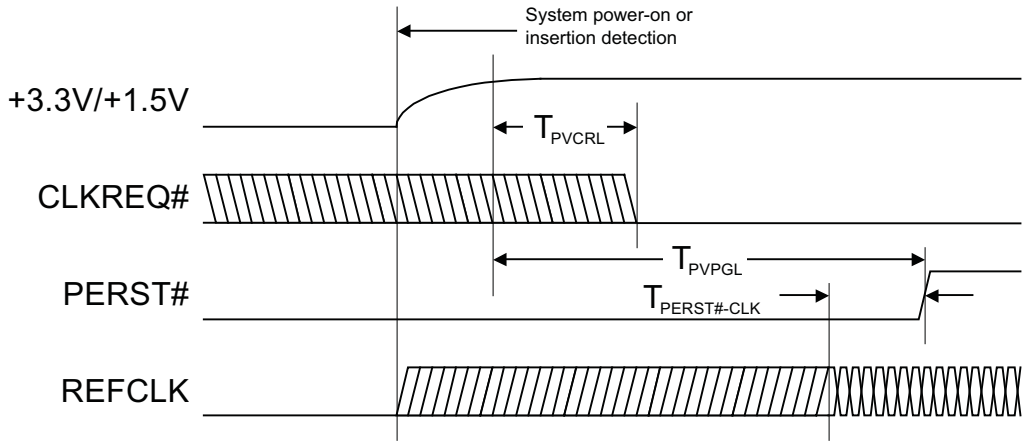


Figure 3-3: Power up timing for PCI Express-based modules

Table 3-4: Power up timing for PCI Express-based modules

Symbol	Parameter	Min	Max	Units	Notes
T_{PVCRL}	Power Valid to **CLKREQ#** output active		100	µs	
T_{PVPERL}	Power stable to **PERST#** inactive	1		ms	1
$T_{PERST\#-CLK}$	REFCLK stable before **PERST#** active	100		µs	2

1. Power supply stability is defined in Section 3.3.3 – Power Supply Limits.
2. The REFCLK is stable when it meets the requirements specified for the reference clock.

The host system is required to have the reference clock for a PCI Express device in the parked clock state prior to device power-up. The state of the reference clock is undefined during device power-up, but it must be in the active clock state for a setup time $T_{PERST\#-CLK}$ prior to **PERST#** de-assertion.

3.2.5.2 Power state transitions (S0 to S3/S4 to S0) for PCI Express-based modules

If the host system enters a power saving state that will cause the primary power sources to turn off, e.g. S3 or S4, a module must be placed into a D3 state prior to any power transitions at the slot. In this case, **PERST#** is asserted in advance of power changes.

For PCI Express-based modules, the reference clock to the module may go inactive and stay inactive until a wake event.

During the D3 state, both **+3.3V** and **+1.5V** may be turned off while **+3.3VAUX** remains powered. See ***Section 3.3.3 – Power Supply Limits*** for specifications regarding auxiliary current limits.

On a wakeup event, the host system's power manager restores the primary power and **REFCLK**, and **PERST#** is de-asserted after the power and clocks (as required) are stable.

Once **PERST#** is asserted, it must remain asserted for a minimum of T_{PERST} time.

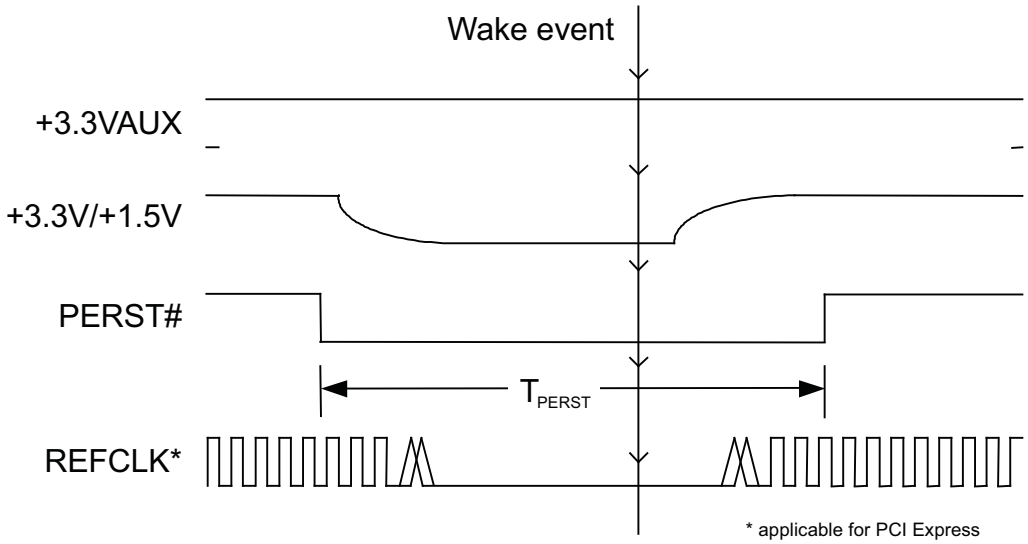


Figure 3-4: Power state transition timing for PCI Express-based

Table 3-5: Power state transition timing for PCI Express-based modules

Symbol	Parameter	Min	Max	Units	Notes
T_{PERST}	PERST# active time	100		µs	

3.2.5.3 Power down for PCI Express-based modules

As soon as the supplies are out of their specified tolerance range, **PERST#** is asserted. Modules should not assume that **PERST#** would provide advanced warning of a loss of power. **+3.3VAUX** may remain valid for host system sleep and off states even if the device is not enabled for wakeup events.

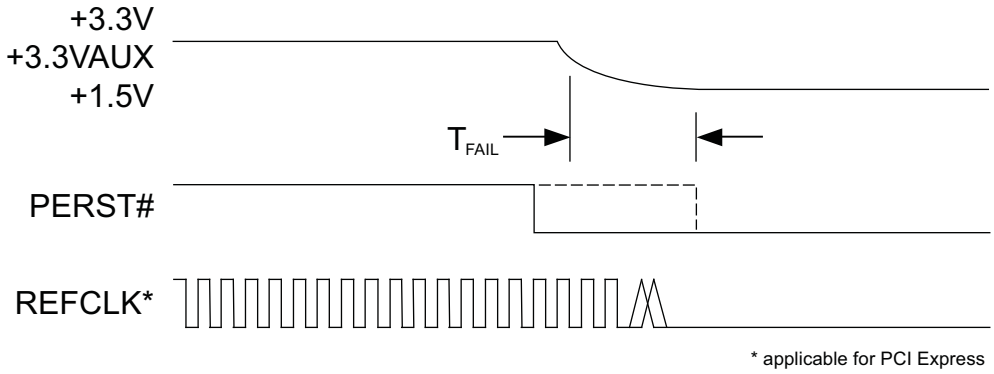


Figure 3-5: Power down timing for PCI Express-based modules

Table 3-6: Power down timing for PCI Express-based modules

Symbol	Parameter	Min	Max	Units	Notes
T_{FAIL}	Power level invalid to PERST# active		500	ns	1

1. The **PERST#** signal must be asserted within T_{FAIL} of any supplied supply going out of specification. T_{FAIL} shall be measured from the power fail detection point selected by the system designer, provided the power fail detection point falls within the 'Out of tolerance threshold windows' specified in ***Figure 3-6***.

3.2.6 USB power control operation

This section describes power control operation at the ExpressCard interface for USB-based modules. No power on either **+3.3V**, **+3.3VAUX** and **+1.5V** can be enabled to the module slot unless **CPUSB#** is asserted by a module inserted into the slot.

USB modules are responsible for deriving any necessary functional reset based on the state of the power being supplied to the module.

Since the ExpressCard slot does not supply USB cable power (V_{BUS}), all USB module functions shall indicate that they are self-powered devices. Self-powered USB functions rely on external power sources and for the ExpressCard slot, **+3.3V** and **+1.5V** are deemed as being logically equivalent to external power sources. When external power sources are not powered, USB functions are allowed to disconnect from the bus. ***Table 3-7: ExpressCard slot power relationships to USB power state*** summarizes the relationship between USB power states and the ExpressCard slot power.

Table 3-7: ExpressCard slot power relationships to USB power state

USB Power State	Acceptable USB Connection Behavior	ExpressCard Slot Power	
		Primary (+3.3V and +1.5V)	Auxiliary (+3.3VAUX)
External Power On with V_{BUS} On	Connected / Attached	ON	ON
External Power Off with V_{BUS} On	Disconnected / De-attached	OFF	ON
	Connected / Attached[1]	OFF	ON
External Power Off with V_{BUS} Off	Disconnected / De-attached	OFF	OFF

1. Module must respond to host-initiated resume events and may initiate remote wakeup (if capable and enabled).

USB modules are responsible for meeting the data interface termination requirements as dictated by the applicable USB specification. Per the USB specification, self-powered USB functions in the connected state are to monitor and/or use the bus power ($\mathbf{V_{BUS}}$) supplied at the USB connector for purposes of maintaining proper data line termination under both operational and bus suspend modes of operation. USB functions shall also not actively drive the data lines whenever $\mathbf{V_{BUS}}$ is not supplying power. To accomplish this in an ExpressCard module implementation, the **+3.3VAUX** power state is deemed to be logically equivalent to $\mathbf{V_{BUS}}$. Since **+3.3VAUX** power is always available whenever **+3.3V** is powered, a USB module may alternatively use **+3.3V** state as the indication of the $\mathbf{V_{BUS}}$ power state. The module may use either of these power sources to establish the necessary termination.

USB modules are responsible for combining as needed primary and auxiliary power to meet the needs of the application while maintaining required isolation between the separately supplied power rails (**+3.3V**, **+3.3VAUX** and **+1.5V**). See ***Section 3.3.3 – Power Supply Limits*** for current limits.

3.2.7 I/O interface detection, set-up and operation

For all ExpressCard modules, the module must be detected before the slot can be powered and the supported interfaces can be enabled. To power up a module, **+3.3V**, **+3.3VAUX** and **+1.5V** must be enabled by the assertion of the **CPPE#** and/or the **CPUSB#** pin.

PCI Express module insertion model

Once power is applied, the PCI Express interface must be enabled on both the module and the host in order that the native detection and configuration protocols of the data interface can begin as defined by the ***PCI Express Base Specification***.

Consistent with the PCI model, host systems pre-allocate bus number, memory windows, and I/O range resources to each ExpressCard slot to support the requirements of modules that may appear in the slot as part of the hot-plug insertion model. The most extensive resource requirements will be for module applications that incorporate additional PCI bus structures such as the use of a PCI Express-to-PCI bridge to enable legacy PCI silicon reuse or using a PCI Express switch to implement multi-function devices. Module developers need to take care not to exceed the resource allocations of the host system or their module may not enumerate properly when hot-plug inserted. Please refer to ***Section 6.3.2 Supporting PCI Bridging on ExpressCard Modules*** for further information regarding host resource allocation requirements.

USB module insertion model

Once power is applied, the USB module operation closely follows the USB connection model that exists with USB walk-up connectors and external USB devices. The primary difference is that a module connector mated with the host slot connector has replaced the connectors and cable of the walk-up solution.

With the optional availability of USB 3.0 support in host systems, USB module startup operation for those modules implementing the USB 3.0 interface are required to follow a pre-enumeration process to determine that the host system to which the module is inserted supports USB 3.0 operation prior to signaling across the USB 3.0 signaling pins. Please refer to ***Section 3.2.7.2 Modules Implementing USB 3.0*** for further information regarding the USB 3.0 startup operation.

3.2.7.1 Modules Implementing Both Interface Options

Module implementing both a PCI Express and USB function are required to implement a serial number feature of both parent specifications. The PCI Express function must implement the IEEE defined 64-bit extended unique identifier (EUI-64™) as described in ***Device Serial Number Capability*** section of the PCI Express Base Specification.

This requirement enables operating system software to identify the physical relationship between the two bus trees.

This PCI Express Vendor ID and the PCI Express Device ID and unique identifier are combined and become the USB serial number string.

As an example, assume the PCI Express function has the following Vendor ID, Device ID and GUI serial number:

PCI Express Vendor ID number:

```
8486
1000 0100 1000 0110
```

PCI Express Device ID number:

```
1023
0001 0000 0010 0011
```

PCI Express serial number:

```
9D66CCEACC7998E3
1001 1101 0110 0110 1100 1100 1110 1010 1100 1100 0111 1001 1001 1000 1110
0011
```

The USB serial number space would contain the value

```
8486 + 1023 + 9D66CCEACC7998E3
```

in Unicode

```
0038 0034 0038 0036 0031 0030 0032 0033 0039 0044 0036 0036 0043 0043 0045
0041 0036 0036 0037 0039 0039 0038 0045 0033
```


3.2.7.2 Modules Implementing USB 3.0

Modules implementing USB 3.0 shall use the **USB3#** signal pin to both determine if the host system has USB 3.0 interface support and to inform the host system that the module intends to use the USB 3.0 interface (given the host system indicates support).

Operation of the **USB3#** signal during module insertion and startup is as follows.

- Host systems that support USB 3.0 operation shall provide a pull-up resister on **USB3#** signal pin at the slot.
- USB 3.0-based modules shall hard-wire a ground to the **CPUSB#** signal pin to indicate the module is a USB-based module.
- Following insertion and the availability of power to the module, the module shall sense the presence of a USB 3.0-capable host system by detecting the presence of the pull-up resister on the **USB3#** signal pin in the slot.
- Given that the host system supports USB 3.0, the module shall then add a termination to ground on the **USB3#** signal pin to inform the host system that the module implements the USB 3.0 interface.
- The USB 3.0-based module shall wait a minimum of 10ms prior to driving any USB 3.0 in-band connect and enumeration signaling on the USB 3.0 signal pins. This delay is intended to allow the host system adequate time to set up its USB 3.0 signal interface prior to the module attempting to use it.

Modules implementing USB 3.0 shall provide a backward compatible fall-back mode when used in ExpressCard slots that don't support USB 3.0. Determination as to when a USB 3.0-based module should use an alternate interface instead of USB 3.0 can be made by sensing that the **USB3#** signal pin is open (i.e. lacking a pull-up resister) on the host system interface. In the backward compatible fall-back mode, the module may use either USB 2.0 or PCI Express as the alternately supported interface; for example the module may implement PCI Express operating at 2.5Gbps as the fall-back given the USB operating at 5.0Gbps isn't available in the slot.

An ExpressCard module may simultaneously operate USB 3.0 (SuperSpeed) and USB 2.0 interfaces only if the module is a USB compound device that incorporates an embedded USB 3.0 hub. Single-function or composite USB devices are only allowed to operate in either USB 3.0 (SuperSpeed) or USB 2.0 modes but not both.

3.2.8 Power management

The ExpressCard module is required to power manage itself when the host system enters power states other than S0. This system transition is indicated by the presence or absence of the primary and secondary voltage supplies (**+3.3V** and **+1.5V**), device power-state D3 and whether or not PME functionality is enabled or disabled. This requirement ensures minimum host power consumption for battery operated devices.

3.2.8.1 PCI Express WAKE#

The **WAKE#** signal is an open drain, active low signal that is driven low by a module's PCI Express function to wakeup (reactivate) the system's main power rails, host interfaces and reference clocks (as required).

If the module's PCI Express function has wakeup capabilities, the module shall implement the **WAKE#** signal function. Likewise, only system host systems that support the hardware **WAKE#** wakeup function need to connect to this pin, but if they do, they must fully support the **WAKE#** signal function. When supported, the **WAKE#** pin is required to be pulled-up by the host. If the wake process is used, then auxiliary current must be present on the **+3.3VAUX** supply and used for this function.

See Chapter 5 of the ***PCI Express Base Specification*** for more details on PCI compatible power management.

If the **WAKE#** signal is supported by a slot, the signal is connected to the host system's power management (PM) controller. **WAKE#** may be bused to all ExpressCard slot connectors, forming a single input connection at the PM controller or individual connectors can have individual connections to the PM controller.

Auxiliary power (+3.3VAUX) must be used by the asserting and receiving ends of **WAKE#** in order to revive the hierarchy. The system vendor must also provide a pull-up on **WAKE#** with its bias voltage reference being supplied by the auxiliary power source in support of Link reactivation. Note that the voltage that the system board uses to terminate the **WAKE#** signal can be lower than the auxiliary supply voltage to be compatible with lower voltage processes of the system PM controller. However, all potential drivers of the **WAKE#** signal must be 3.3 V tolerant.

Note: **WAKE#** is not **PME#** and should not be attached to the **PCI-PME#** interrupt signals. **WAKE#** causes power to be restored but must not directly cause an interrupt.

WAKE# has additional electrical requirements over and above standard open drain signals that allow it to be shared between devices that are powered off and those that are powered on using auxiliary power for example. The additional requirements include careful circuit design to ensure that a voltage applied to the **WAKE#** signal network never causes damage to a component even if that particular component's power is not applied.

Additionally, the device must ensure that it does not pull **WAKE#** low unless **WAKE#** is being intentionally asserted in all cases, including when the related function is in $\mathbf{D3}_{\mathrm{COLD}}$.

This means that any component implementing **WAKE#** must be designed such that:

- Un-powered **WAKE#** output circuits are not damaged if a voltage is applied to them from other powered "wire-ORed" sources of **WAKE#**.
- When power is removed from its **WAKE#** generation logic, the un-powered output does *not* present a low impedance path to ground or any other voltage.

These additional requirements ensure that the **WAKE#** signal network continues to function properly when a mixture of auxiliary powered, and un-powered components have their **WAKE#** outputs wire-ORed together. It is important to note that most commonly available open drain and tri-state buffer circuit designs used "as is" do not satisfy the additional circuit design requirements for **WAKE#**.

PCI Express module designers must be aware of the special requirements that constrain **WAKE#** and ensure that their modules do not interfere with the proper operation of the **WAKE#** network. The **WAKE#** input into the system may de-assert as late as 100 ns after the **WAKE#** output from the function de-asserts (i.e., the **WAKE#** pin must be considered indeterminate for a number of cycles after it has been de-asserted).

The value of the pull-up resistor for **WAKE#** on the system board must be derived taking into account the total possible capacitance on **WAKE#** to ensure that **WAKE#** charges up to a logic high voltage level in no more than 100 ns.

The assertion of **WAKE#** does not complete the wakeup process for a PCI Express function. Once power is restored by the host system's PM controller and the PCI Express interface is re-started, the PCI Express function is still required to issue the appropriate PME message via the PCI Express in-band message protocol. Refer to the ***PCI Express Base Specification*** for more information regarding PME messaging and the wakeup protocol for PCI Express.

Modules asserting **WAKE#** must release the assertion of **WAKE#** within 1ms of the de-assertion of the slot's **PERST#** signal.

3.2.8.2 PCI Express link power management

ExpressCard modules that implement PCI Express-based applications shall implement link power management including support for both Active State Link PM L0s and L1 (in addition to the primary L0 and L3) states. The enabling of these power management states are the responsibility of the host system as described in ***Section 6.5 PCI Express Link Power Management***. Refer to ***Section 5.4*** of the ***PCI Express Base Specification*** for more information regarding Active State Link PM.

3.2.8.3 USB Power Management

ExpressCard modules that implement USB-based applications are required to implement the power management features as required for USB compliance.

Refer to the applicable USB specification for more information regarding power management feature implementation requirements.

3.2.8.3.1 USB Remote Wakeup

ExpressCard modules that implement USB-based applications that support remote wakeup are required to use the in-band resume signaling protocol (across either the **USBD+/USBD-** or **SSRX+/SSRX-** pins) as defined in the applicable USB specification. When the host system is in a suspended state (e.g. S3) with remote wakeup enabled, the module should be able to support this capability solely on power available via the **+3.3VAUX** pins as the primary slot power (**+3.3V** and **+1.5V**) may be removed in this state.

Note: Special consideration may be needed if a module supports remote wakeup only when primary slot power (**+3.3V** and **+1.5V**) is available. Such a module, working in conjunction with available system software, shall assure that the remote wakeup feature is not enabled for situations where primary power may be removed by the host system. In some host system implementations, to assure this may mean disabling the module's remote wakeup capability in all host system states. If no system software is available to allow a module to disable remote wakeup when primary power is to be removed by the host system, it is acceptable behavior for a module that supports remote wakeup to simply "shut off" (i.e. disconnect) when primary power is removed.

See also ***Section 3.2.6 USB power control operation*** for more details.

3.3 Electrical Requirements

3.3.1 Signal Interface

Electrical specifications must be maintained to ensure data integrity.

Electrical specifications for the PCI Express data, PCI Express reference clock (**REFCLK**), USB data, and SMBus (clock and data) are defined by the referenced specifications for those interfaces. The module and connector electrical specifications will define the module and connector electrical requirements.

The 3.3V ExpressCard module logic levels for single-ended digital signals (**WAKE#**, **CLKREQ#**, **PERST#**) are given in Section ***4.2 Module Electrical Requirements***.

Table 3-8: DC Specification for 3.3V Signaling

Symbol	Parameter	Conditions	Min	Max	Units	Notes
+3.3V	Supply Voltage		3.0	3.6	V	3
+1.5V	Supply Voltage		1.35	1.65	V	3
+3.3VAUX	Supply Voltage		3.0	3.6	V	3
V_{IH}	Input High Voltage		2.0	3.6	V	1
V_{IL}	Input Low Voltage		-0.5	0.8	V	1
I_{OL}	Output Low Current for open-drain signals	0.4 V	4		mA	2
I_{IN}	Input leakage current	0 to 3.3 V	-10	+10	µA	1
I_{LKG}	Output leakage current	0 to 3.3 V	-50	+50	µA	2
C_{IN}	Input pin capacitance			7	pF	1
C_{OUT}	Output pin capacitance			30	pF	2

1. Applies to **PERST#**
2. Applies to **CLKREQ#** and **WAKE#**
3. As measured at the module connector pad

3.3.2 PCI Express Reference Clock (REFCLK) requirements

To reduce jitter and allow for future silicon fabrication process changes, low voltage swing, differential clocks are being used. The nominal single-ended swing for each clock is 0 to 0.7 V and a nominal frequency of 100 MHz ±300 PPM. The clock has a defined crossover voltage range and monotonic edges through the input threshold regions as specified in ***Section 4.2- Module Electrical Requirements***.

The reference clock pair is routed point-to-point to each slot connector from the system board according to best-known clock routing rules. The reference clock distribution to all devices must be matched to within 15 inches on the system board. The phase delay between the transmitter and receiver clock is assumed to be less than 10ns. The combination of the maximum reference clock mismatch and the maximum channel length will contribute approximately 7-8 ns and the remaining time is allocated to the difference in the insertion delays of the Tx and Rx devices. The routing of each signal in any given clock pair between the clock source and the slot connector must be well matched in length (< 0.005 inch) and appropriately spaced away from other non-clock signals to avoid excessive crosstalk.

The module is not required to use the reference clock on the connector. However, the module is required to maintain the 600-ppm data rate matching specified in both the ***PCI Express Base Specification*** and ***PCI Express Card Electromechanical Specification***.

Any terminations required by the clock are to be on the system board. EMI emissions will be reduced if clocks to empty slots are shut down at the clock source. The method for detecting the presence of a module in a slot and controlling the clock gating is host system specific. It is intended that this clock gating control be determined based on the state of the **CPPE#** and/or **CLKREQ#** pins.

The reference clocks may support spread spectrum clocking. Any given system design may or may not use this feature due to host system-level timing issues. The minimum clock period cannot be violated. The preferred method is to adjust the spread technique to not allow for modulation above the nominal frequency. This technique is often called "down-spreading." The requirements for spread spectrum modulation rate and magnitude are given in the ***PCI Express Base Specification***.

3.3.3 Power Supply Limits

Table 3-9 defines the power supply limits for any given ExpressCard module. For purposes of the following table, the definition of **Average** is the averaged current value over the 1-second period that represents the steady-state maximum current consumption for the given module application. **Max** is defined as the absolute maximum value that may be measured outside of the initial in-rush current that is allowed during the power ramp-up period defined in ***Section 3.3.4 - Power Supply Ramp-up Timing and Sequencing***.

Table 3-9: ExpressCard module power supply limits

Supply	Limits[2]	Notes
+3.3V[1]	1000 mA – **Average** 1300 mA – **Max**	Primary supply voltage
+3.3VAUX[1]	250 mA – **Average** 275 mA – **Max**	Auxiliary supply voltage; this current is also available during the power saving D3 state with wakeup enabled
	5 mA – **Average**	Auxiliary supply voltage during the power saving D3 state with wakeup disabled
+1.5V	500 mA – **Average** 650 mA – **Max**	Secondary supply voltage

1. The average power across both **+3.3V** and **+3.3VAUX** shall not exceed a total of 1000 mA, e.g. if the average power drawn by a module is 250mA on **+3.3VAUX**, then that module is only allowed to draw up to 750mA on the **+3.3V** power pins.
2. For purposes of calculating minimum load regulation requirements for the slot, the minimum current consumption by a module for any given power rail shall be assumed to be 0 mA.
3. The total max current drawn by a module across all the power rails shall not exceed 1.75 A.

A power supply is deemed to be valid or stable if the specified voltage is within the specified voltage tolerances as defined in ***Table 3-8: DC Specification for 3.3V Signaling***. Once a power supply is deemed stable, an invalid or unstable supply is defined as a supply that has dropped below the specified minimum voltage levels. For purposes of detecting an out-of-tolerance power source, the threshold for detection should be established in a window range of no more than 500mV below the specified minimum voltage level for 3.3V supplies (i.e. 2.5V) and 150mV below for 1.5V supplies (i.e. 1.2V). ***Figure 3-6: Out-of-tolerance threshold windows*** illustrates these threshold windows.

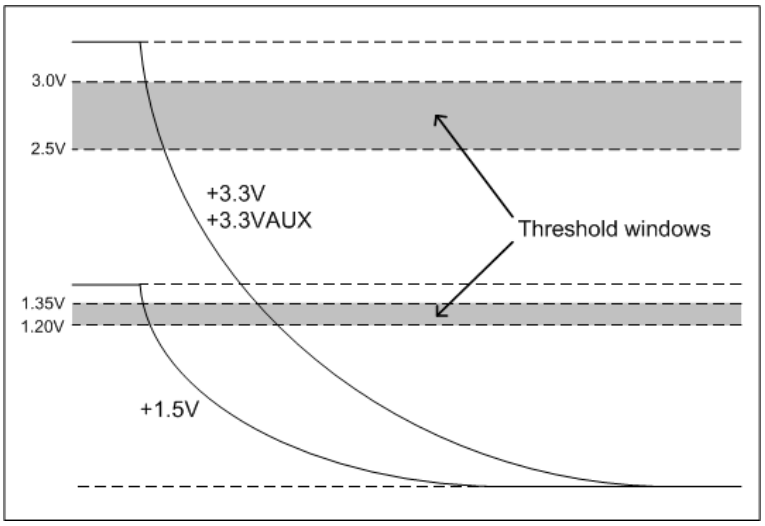


Figure 3-6: Out-of-tolerance threshold windows

All ExpressCard modules, independent of the amount of power drawn from the host system, shall not exceed the thermal power limits defined in ***Section 4.3 – Module Thermal Requirements***.

Any ExpressCard module that combines functionality using both PCI Express and USB interfaces on the same module shall not exceed the power supply limits defined for any given supply line.

Support for auxiliary current when a module is in a power saving state is only provided on the **+3.3VAUX** voltage pin.

+3.3VAUX and **+3.3V** must be isolated power planes within the module. The module cannot connect the **+3.3VAUX** to **+3.3V**.

3.3.4 Power Supply Ramp-up Timing and Sequencing

The power supply ramp-up time is defined as the linear transition from 10% to 90% of its defined stable level. The power supply inputs shall have a ramp-up time of no less than 0.1 ms and no more than 100 ms.

Peak current at start-up (in-rush current) is determined by ramp time and module capacitance. Overall load capacitance is defined as the capacitance on the host output and the module input. All modules shall limit the maximum input capacitance on each of its power supply inputs (**+3.3V**, **+3.3VAUX** and **+1.5V**) to 80 µF out of a maximum allowable overall load capacitance of 100 µF.

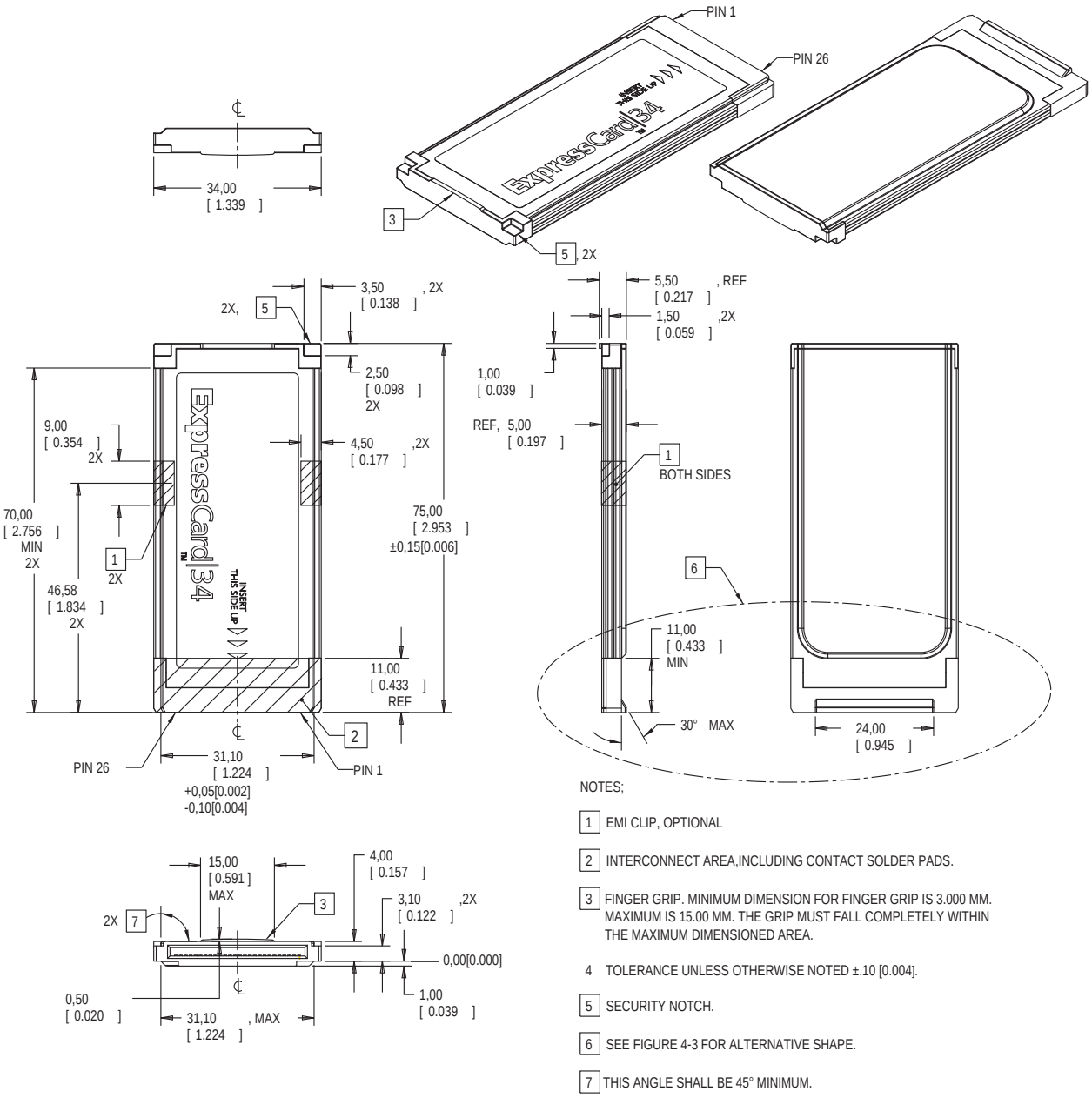
There is no specific requirement for power supply sequencing of each of the three power supply rails. They may come up or go down in any order. The system, however, must assert the PERST# signal whenever any of the three power rails goes invalid or unstable. Note: If a module requires power supply rail sequencing, it is the responsibility of the add-in module designer to provide appropriate circuitry on the module to meet any power supply rail sequencing requirements.

4. MODULE SPECIFICATIONS

The section defines the module's physical outline dimensions, electrical, mechanical, and environmental requirements. Each module manufacturer is responsible for qualification of their products to this specification.

4.1 Module Dimensions

There are two formats of the standard ExpressCard modules in this specification: the ExpressCard/34 module characterized by its 34 mm width and the ExpressCard/54 module characterized by its 54 mm width. ***Figure 4-1*** and ***Figure 4-2*** define the outline dimensions for the ExpressCard/34 module and ExpressCard/54 module, respectively.



NOTES;

1. EMI CLIP, OPTIONAL
2. INTERCONNECT AREA,INCLUDING CONTACT SOLDER PADS.
3. FINGER GRIP. MINIMUM DIMENSION FOR FINGER GRIP IS 3.000 MM. MAXIMUM IS 15.00 MM. THE GRIP MUST FALL COMPLETELY WITHIN THE MAXIMUM DIMENSIONED AREA.
4. TOLERANCE UNLESS OTHERWISE NOTED ±.10 [0.004].
5. SECURITY NOTCH.
6. SEE FIGURE 4-3 FOR ALTERNATIVE SHAPE.
7. THIS ANGLE SHALL BE 45° MINIMUM.

Figure 4-1: ExpressCard/34 module outline dimensions

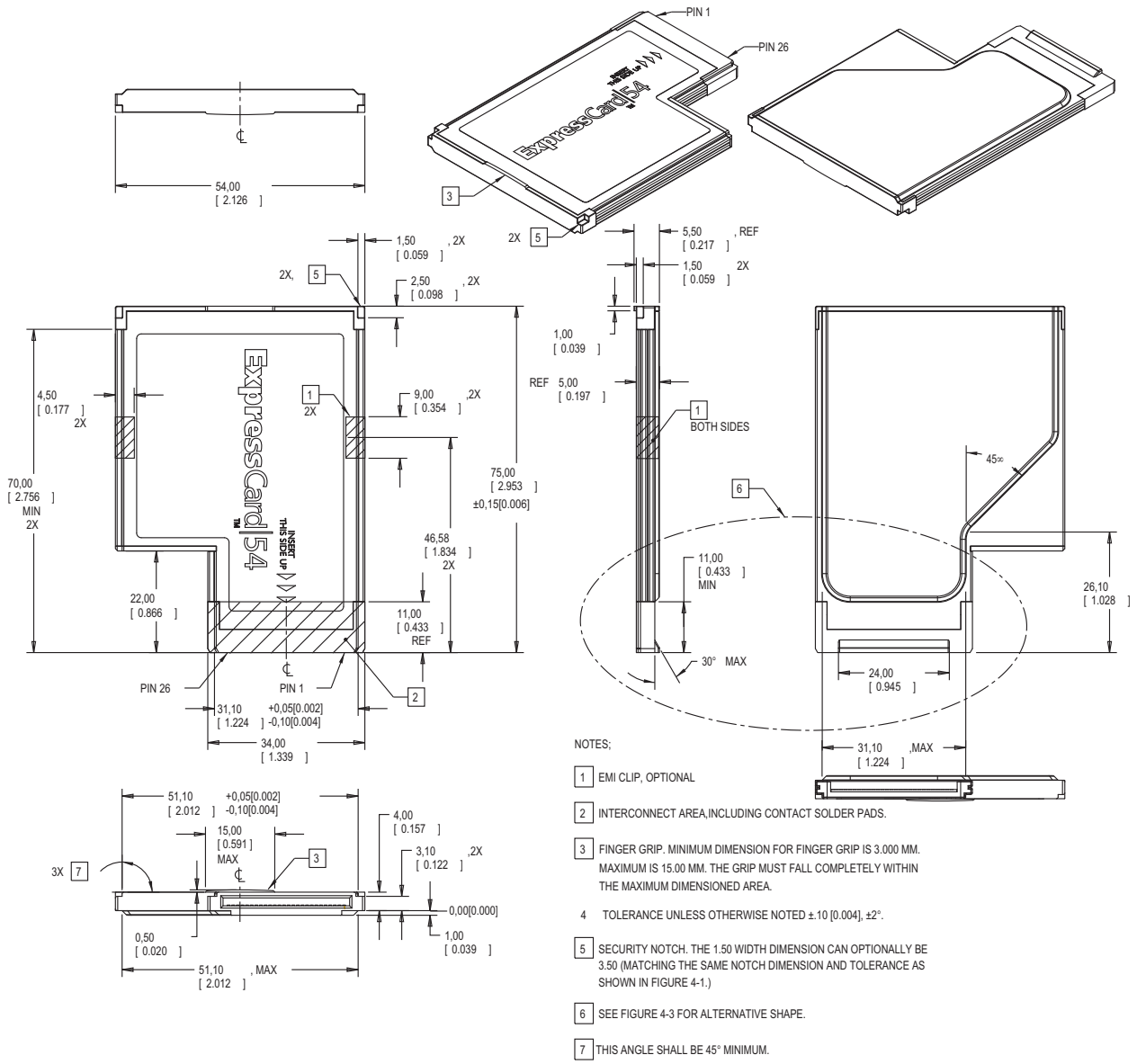


Figure 4-2: ExpressCard/54 module outline dimensions

The following features are worth noticing:

- The module thickness is 5 mm.
- The standard module length is 75 mm.
- The interconnect area dimension of 11.00 mm marked as Note 2 in ***Figure 4-1*** and ***Figure 4-2*** is for reference only. This area is intented for module connector placement. The connector surface-mount pads on the module printed circuit board are included in this interconnect area.
- ExpressCard/34 modules and ExpressCard/54 modules use the same connector interface. Dimensions of the module and host connectors will be covered in ***Chapter*** 5 ***– Connector Specifications***.

- The EMI ground clips on the module (Note 1 in ***Figure 4-1*** and ***Figure 4-2***) are optional. If implemented, they must be located in the positions specified in ***Figure 4-1*** and ***Figure 4-2***.
- The feature of 0.30 mm in height in the front of the module marked as Note 3 in ***Figure 4-1*** and ***Figure 4-2*** is to facilitate module removal with thumb-finger. A conventional push-button, or other module ejection mechanisms can also be implemented at each system OEM's discretion. See the ***ExpressCard Implementation Guidelines*** for more discussion regarding module removal.
- The notches marked as Note 5 in in ***Figure 4-1*** and ***Figure 4-2*** are defined in the front of the module to facilitate security lock. See the ***ExpressCard Implementation Guidelines*** for more on security lock implementations.
- An alternative shape, defined in ***Figure 4-3***, is allowed on the back side of the module in the connector placement area (marked as Note 6 in ***Figure 4-1*** and ***Figure 4-2***).

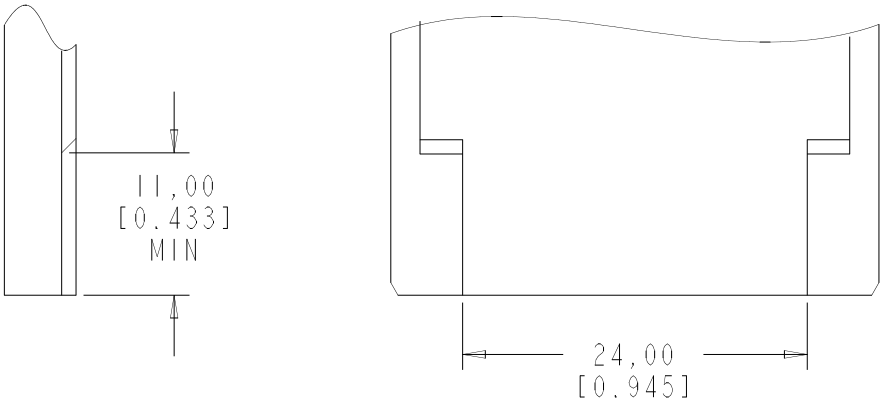
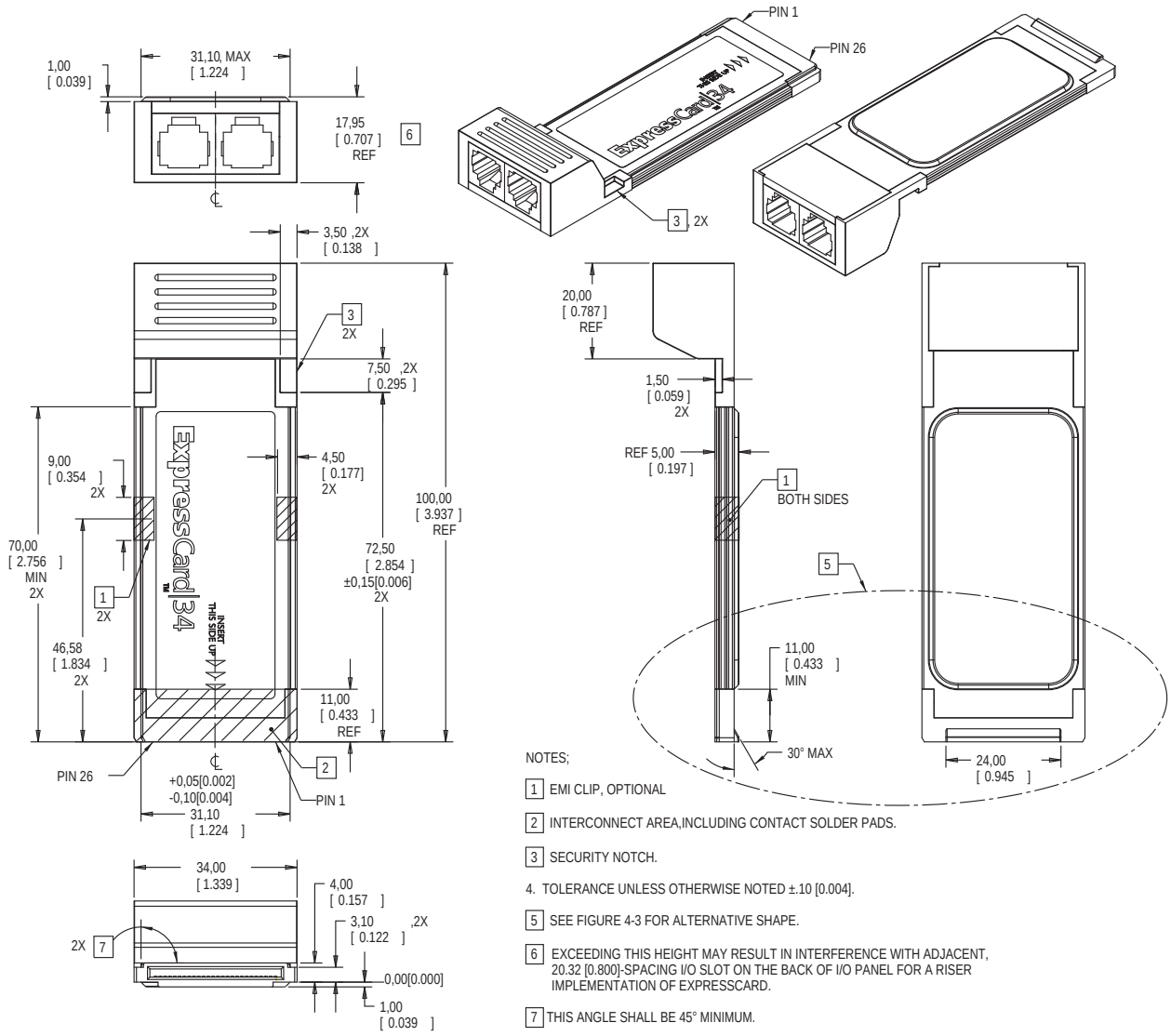


Figure 4-3: Alternate shape

This specification also defines extended module formats to allow applications to use existing standard I/O connectors, incorporate external antennas, or implement other extended applications. ***Figure 4-4*** and ***Figure 4-5*** specify the outline dimensions of the ExpressCard/34 extended modules and ExpressCard/54 modules, respectively.



NOTES;

1. EMI CLIP, OPTIONAL
2. INTERCONNECT AREA,INCLUDING CONTACT SOLDER PADS.
3. SECURITY NOTCH.
4. TOLERANCE UNLESS OTHERWISE NOTED ±.10 [0.004].
5. SEE FIGURE 4-3 FOR ALTERNATIVE SHAPE.
6. EXCEEDING THIS HEIGHT MAY RESULT IN INTERFERENCE WITH ADJACENT, 20.32 [0.800]-SPACING I/O SLOT ON THE BACK OF I/O PANEL FOR A RISER IMPLEMENTATION OF EXPRESSCARD.
7. THIS ANGLE SHALL BE 45° MINIMUM.

Figure 4-4: ExpressCard/34 extended module outline dimensions

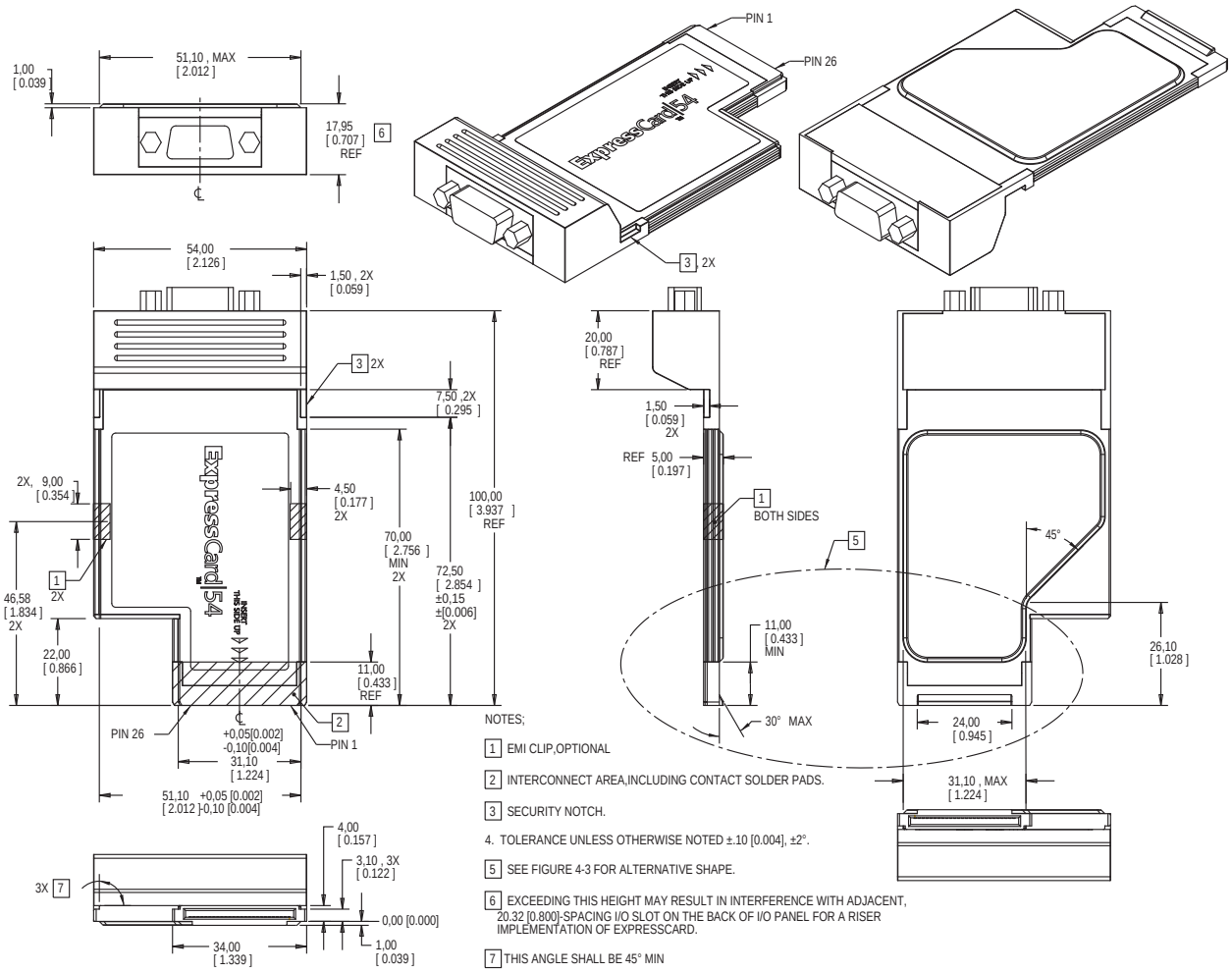


Figure 4-5: ExpressCard/54 extended module outline dimensions

The extended length of 20.00 mm in ***Figure 4-4*** and ***Figure 4-5*** is for reference only. Module manufacturers have the flexibility to increase or reduce it to suit their application needs. Similarly, the extended module height of 17.95 mm shown in ***Figure 4-4*** and ***Figure 4-5*** is also for reference only. Module manufacturers can decide their own extended module heights.

4.2 Module Electrical Requirements

This section defines the ExpressCard module electrical requirements that include the PCI Express lane signal integrity requirements and other module electrical requirements, such as electrical discharge, x-ray and EMI.

4.2.1 PCI Express Signal Integrity Requirements

Since a PCI Express ExpressCard module interface includes a PCI Express lane, it must meet the PCI Express electrical requirements, as specified in the ***PCI Express Card Electromechanical (CEM) Specification***. The remainder of this section will focus on identifying informative and normative

differences between the PCI Express CEM specification and requirements specifically for an ExpressCard implementation.

4.2.1.1 Informative Differences with the PCI Express CEM Specification

Table 4-1 provides guidance on the proper interpretation of the ***PCI Express CEM Specification*** terminology as it applies to an ExpressCard implementation.

Table 4-1: Adapting Terminology in the PCI Express CEM Specification for ExpressCard requirements

PCI Express CEM Specification	ExpressCard Standard
System Board Interconnect	Host System Interconnect
Add-in Card	ExpressCard Module

For the purpose of electrical budget allocation, the PCI Express Link is divided into two subsystems as illustrated in (***Figure 4-6***):

- ExpressCard module – From device package pin on the module to the module connector pad, excluding the module connector and the pad.
- Host system – From device package pin on the baseboard up to the ExpressCard host and module connectors, including the components (if any) associated with the ExpressCard-baseboard interface such as riser card, daughter card, cable and cable headers.

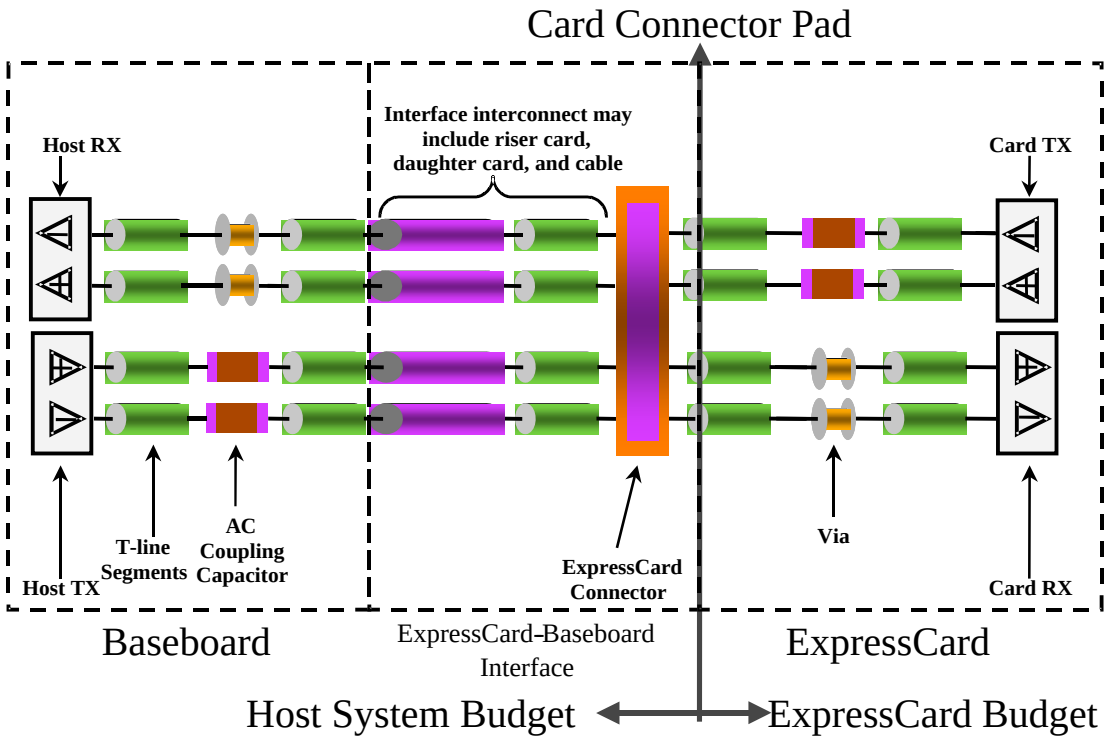


Figure 4-6: Generalized Link Definition for ExpressCard Implementations

The electrical impact of discontinuities on the Link such as via, bend, and test-points should be included in the respective subsystems.

4.2.1.2 Normative Differences with the PCI Express CEM Specification

Table 4-2 lists ExpressCard-specific requirements that supersede the requirements as given by the ***PCI Express CEM Specification***. These requirements were specifically adjusted for the ExpressCard implementation to account for the recognized differences in the system topology and specifically noting that the ExpressCard module form-factor is somewhat smaller than a typical PCI Express add-in card.

Table 4-2: ExpressCard requirements that supersede PCI Express CEM Specification requirements

PCI Express CEM Specification	ExpressCard Standard
Add-in Card Transmitter Path Compliance Eye Requirements at 2.5 GT/s:	The requirements for these parameters shall be adjusted as follows:
V_{TXA} minimum is 514 mV	V_{TXA} minimum is 538 mV
V_{TXA_d} minimum is 360 mV	V_{TXA_d} minimum is 368 mV
Add-in Card Transmitter Path Compliance Eye Requirements at 5 GT/s:	The requirements for these parameters shall be adjusted as follows:
V_{TXA} minimum @ 3.5 dB De-emphasis is 380 mV	V_{TXA} minimum @ 3.5 dB De-emphasis is 398 mV
V_{TXA_d} minimum @ 3.5 dB De-emphasis is 380 mV	V_{TXA_d} minimum @ 3.5 dB De-emphasis is 398 mV
V_{TXA} minimum @ 6 dB De-emphasis is 306 mV	V_{TXA} minimum @ 6 dB De-emphasis is 320 mV
V_{TXA_d} minimum @ 6 dB De-emphasis is 260 mV	V_{TXA_d} minimum @ 6 dB De-emphasis is 272 mV
Add-in Card Minimum Receiver Path Sensitivity Requirements at 2.5 GT/s:	The requirements for these parameters shall be adjusted as follows:
V_{RXA} minimum is 238 mV	V_{RXA} minimum is 227 mV
V_{RXA_d} minimum is 219 mV	V_{RXA_d} minimum is 214 mV
Add-in Card Minimum Receiver Path Sensitivity Requirements at 5 GT/s:	The requirements for these parameters shall be adjusted as follows:
V_{RXA} minimum is 300 mV	V_{RXA} minimum is 250 mV
V_{RXA_d} minimum is 300 mV	V_{RXA_d} minimum is 250 mV
System Board Transmitter Path Compliance Eye Requirements at 2.5 GT/s:	The requirements for these parameters shall be adjusted as follows:
V_{TXS} minimum is 274 mV	V_{TXS} minimum is 262 mV
V_{TXS_d} minimum is 253 mV	V_{TXS_d} minimum is 247 mV
System Board Transmitter Path Compliance Eye Requirements at 5 GT/s:	The requirements for these parameters shall be adjusted as follows:
V_{TXS} minimum is 300 mV	V_{TXS} minimum is 250 mV
V_{TXS_d} minimum is 300 mV	V_{TXS_d} minimum is 250 mV
System Board Minimum Receiver Path Sensitivity Requirements at 2.5 GT/s:	The requirements for these parameters shall be adjusted as follows:
V_{RXS} minimum is 445 mV	V_{RXS} minimum is 466 mV
V_{RXS_d} minimum is 312 mV	V_{RXS_d} minimum is 319 mV
System Board Minimum Receiver Path Sensitivity Requirements at 5 GT/s:	The requirements for these parameters shall be adjusted as follows:
V_{RXS} minimum @ 3.5 dB De-emphasis is 380 mV	V_{RXS} minimum @ 3.5 dB De-emphasis is 398 mV
V_{RXS_d} minimum @ 3.5 dB De-emphasis is 380 mV	V_{RXS_d} minimum @ 3.5 dB De-emphasis is 398 mV
V_{RXS} minimum @ 6 dB De-emphasis is 306 mV	V_{RXS} minimum @ 6 dB De-emphasis is 320 mV
V_{RXS_d} minimum @ 6 dB De-emphasis is 260 mV	V_{RXS_d} minimum @ 6 dB De-emphasis is 272 mV

4.2.1.3 Signal Integrity Board Design Considerations

Special consideration should be given to address both the connector-to-system board and connector-to-module board launches. The connector pad and anti-pad sizes should follow good electrical

design practices to minimize impedance discontinuity. On the both the system and module boards, the ground and power planes underneath the PCI Express high-speed signal pads should be removed. Otherwise the signal pads will have too much capacitance and will significantly degrade connector performance. Figure 4-7 illustrates an example of the area where ground and power planes should be removed. While it is recommended that at a minimum the removed plane areas should extend at least to the edges of the signal pads, the removed area could be extended further (as shown in the example) as a parameter for adjusting the effective capacitance of the design.

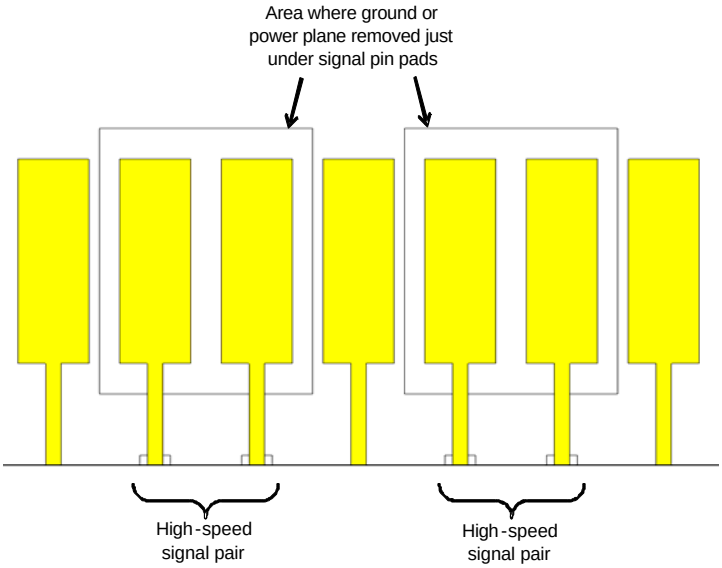


Figure 4-7: Example of ground/power voids underneath high-speed signal pads

4.2.2 Grounding/EMI clips

ExpressCard manufacturers may use the optional frame-mounted grounding/EMI Clips to reduce the electromagnetic emissions of ExpressCard modules. The clips create a path of least resistance to ground so that the external connections (e.g. RJ11 cable) through an I/O connector will not act like an antenna. With the clips, the module's emissions are directed back through the module and into the system instead of out the module into the surrounding area.

4.2.2.1 Contact resistance requirement and test procedure

The contact resistance between the ExpressCard module ground clip and the corresponding host slot chassis attachment point shall not degrade after life cycle testing by a certain value from its initial resistance measurement, to be specified by module or system manufacturers. The recommended contact resistance degradation value is 50 mΩ max.

The resistance of the module ground clip to the host interface shall be measured in accordance with ***EIA 364-23B: Low Level Contact Resistance Test Procedure for Electrical Connectors and Sockets***. The closest, accessible conductive surfaces on the module near the mating interface to the slot ground clip and near the host slot ground attach point shall be used as the contact resistance

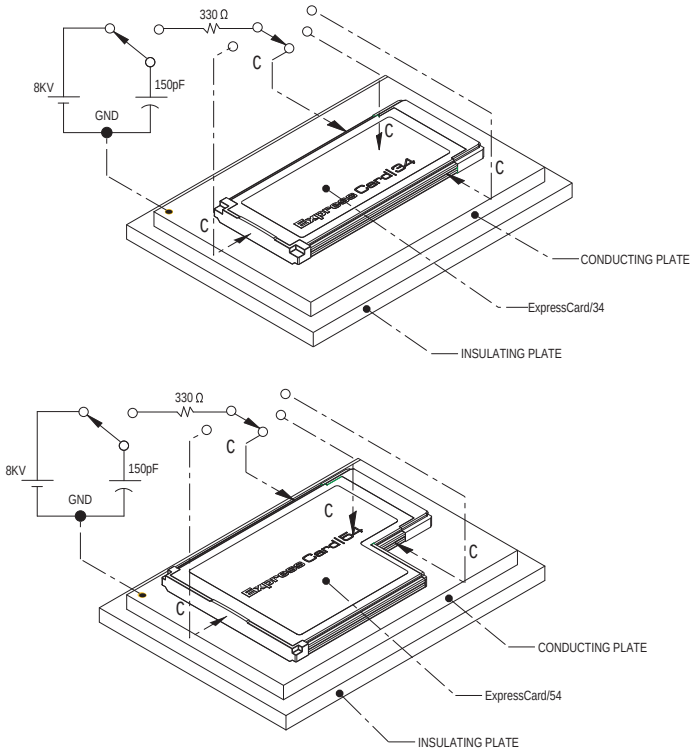
measurement test points. Both before and after measurements should be made from the same positions.

The testing procedures are described below:

Record the contact resistance of the ground clip interface and then subject the module to durability testing (5,000/10,000 insertion/extraction cycles). The ground clip to host contact resistance shall be measured using the same procedure outlined above. The contact interface is acceptable if the resistance has increased by no more than a user specified value (the recommended value is 50 mΩ).

4.2.3 Other Electrical Requirements

ITEM	STANDARD	TESTING
Electrical Discharge	ExpressCard module to function as specified after test and all non-volatile memory to retain the data stored prior to test. Refer to IEC61000-4-2 for detailed test specifications.	TEST 1: Discharge ten (10) times on module body as indicated in Figure 4-8. Change the polarity and repeat the test. TEST 2: Discharge ten (10) times each pin on any exposed connector or slot excluding host connector side. Change the polarity and repeat the test.
X-ray Exposure	ExpressCard module to function as specified after test and all non-volatile memory to retain the data stored prior to test	140 kV @ 5 mA Intensity 0.1Gy minimum or 10 Roentgen minimum for 1 hour minimum
Electromagnetic Field Interference	ExpressCard module to function as specified after test and all non-volatile memory to retain the data stored prior to test	Place module in uniform magnetic flux density of 1,000 Gauss. Exposure time 10 seconds For rotating media modules, the magnetic flux density is 100 Gauss. Exposure time 10 seconds



Notes:

1. Module to make contact with the conducting plate. Discharge to top cover, left side, non-connector end and right side ten (10) times each. If connectors and/or slots excluding host connector are used in the design, discharge ten (10) times on any exposed pin. Change the polarity and repeat the test.
2. The module cover facing the conducting plate should make mechanical contact with the conducting plate during test.

Figure 4-8: Electrostatic discharge Test-2 fixture

4.3 Module Thermal Requirements

Thermal Design Power (TDP) represents the average thermal power dissipated as heat into the host by the module over some period of time under reasonable but high performance usage conditions.

Electrical power consumption limits for ExpressCard modules are defined in ***Section 3.3.3 - Power Supply Limits***. For purposes of this specification, electrical power consumption is not necessarily directly related to the thermal design power within the system. Some power may be dissipated in a remote media interface such as an antenna or through a module extension.

Modules shall be designed to operate in a confined, still air environment with a maximum ambient temperature not to exceed 65ºC (the typical host system environment). As a result, module manufacturers should design their modules so as to function within that constraint and meet or exceed warranty specification statements to the following TDP requirement:

- the TDP for ExpressCard modules should be less than 2.1 W per module under reasonable but high performance usage conditions.

NOTES:

1. Actual design choices made by module manufacturers may reduce the power dissipation capability when constrained to ergonomically imposed enclosure temperature limits and a confined still air environmental temperature of 65ºC.
2. Thermal limits based on an assumption of uniformly heated module with a maximum case temperature of 90ºC in a host environment of 65ºC, and consider heating due to adjacent modules.
3. Various regulatory and safety agencies have established temperature limits for devices handled by operators, and these TDP limits may cause the modules to exceed some of these temperature limits, depending on module design choices.
4. For aid in making module and system design choices, refer to the thermal design guidelines in the module section of the ***ExpressCard Implementation Guidelines*** which contains design tradeoffs associated with host system configuration, environment, module non-uniform heating, module extensions (beyond the host system) and module enclosure material choice.
5. The reasonable but high performance usage conditions used to derive the thermal power design power are device and technology specific.

4.3.1 Module Thermal Compliance

Compliance to TDP requirements may be determined by several methods:

1. Measure Touch Temperature – the TDP requirements are satisfied when in a confined still air environment temperature of 65ºC, the average touch temperature of the module is no more than 90ºC under reasonable but high performance usage conditions. The top of the module shall be thermally probed in at least five locations as shown in Figure 4-9 and Figure 4-10. The average touch temperature shall be obtained from the five locations. The average touch temperature shall be measured after a steady state temperature condition is reached at each probe point. When the temperature of the module's surface is stable within ± 1°C over thirty minutes, the module has reached its steady state temperature. Additional locations may also be thermally probed to obtain a more precise average touch temperature value.
2. Perform a Calculation - the TDP may be determined by taking measurements under reasonable but high performance usage conditions and performing a calculation:

TDP = (Average Electrical Input Power)
– (Average Power Dissipated in a Remote Media Interface)
– (Average Power Dissipated through a Module Extension)

4.3.2 Host Thermal Compliance

With an un-powered module inserted in the slot, the maximum ambient temperature surrounding the module shall not exceed 65ºC under reasonable but high performance usage conditions.

The characteristics of an unpowered module should be typical of modules commonly available as ExpressCard product and should not simply be a block mass which introduces non-typical thermal characteristics (e.g. using a solid block of plastic or metal). Suggestions for providing an unpowered module include modifying a functional module such that the internal circuits are isolated from the power input pins or modifying the behavior of the host slot such that power is disabled to the slot during host slot thermal testing.

Compliance to the host thermal requirements is determined by the following procedure:

1. The host shall operate in an environment that provides the maximum ambient temperature advertised by the host.
2. The host shall run a performance metric application such as BAPCo SYSmark® (www.bapco.com). The performance metric application stresses host systems in a common fashion based upon real world applications. The host shall run either the most recent version of BAPCo Sysmark® or its immediately preceding version. If the host system is not designed to run BAPCo SYSmark® a similar performance metric application shall be run.
3. An unpowered ExpressCard/34 or ExpressCard/54 thermal probe module shall be inserted into the matching-sized slot of the host. The top of the module shall be thermally probed in at least five locations as shown in Figure 4-9 and Figure 4-10. The average touch temperature shall be obtained from the five locations. The average temperature shall not exceed 65ºC. The average temperature shall be measured after a steady state temperature condition is reached at each probe point. When the temperature of the module's surface is stable within ± 1°C over thirty minutes, the module has reached its steady state temperature. Additional locations may also be thermally probed to obtain a more precise average touch temperature value.

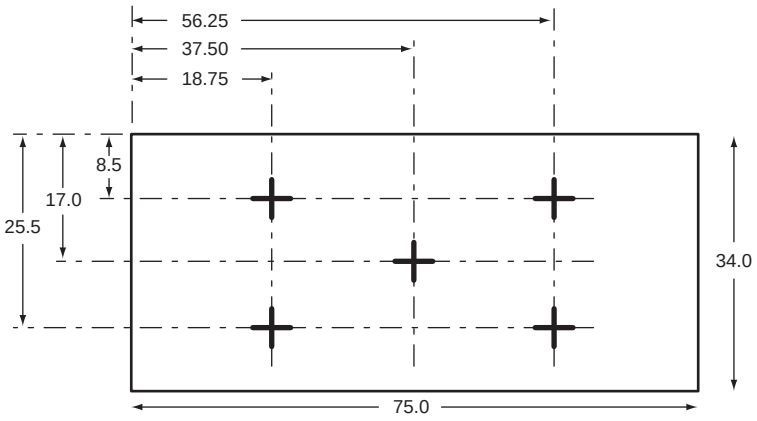


Figure 4-9: Thermal Probe Points for ExpressCard/34 Modules

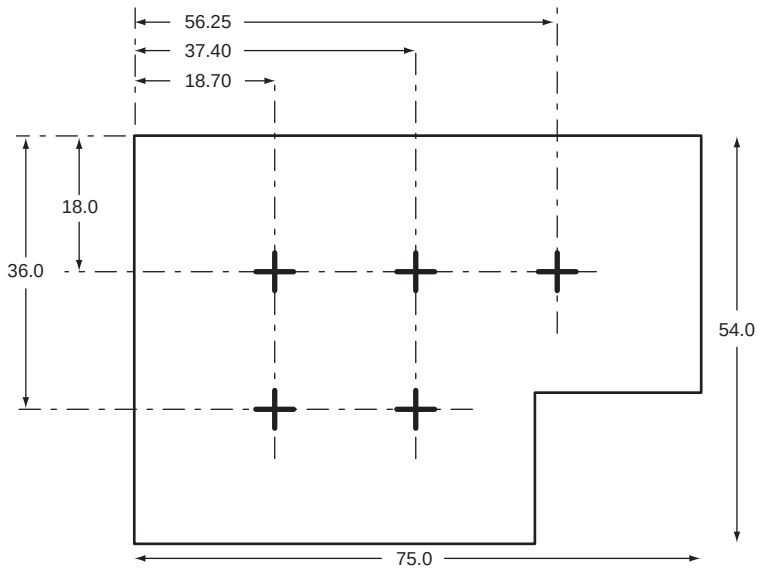


Figure 4-10: Thermal Probe Points for ExpressCard/54 Modules

4.4 Environmental and Mechanical Requirements

The ExpressCard module shall meet or exceed all environmental test requirements of this section. Unless otherwise specified, all test and measurements shall be made at:

Temperature	15°C to 35°C
Air pressure	86 to 106 kPa
Relative humidity	25% to 85%

If conditions must be closely controlled in order to obtain reproducible results, the parameters shall be:

Temperature	23°C ± 1°C
Air pressure	86 to 106 kPa
Relative humidity	50% ± 2%

See ***Section 4.5 – Approved Test Procedures*** for approved test procedures.

4.4.1 Environmental Performance

The ExpressCard module storage and operating environment are specified in this section.

4.4.1.1 Operating Environment

STANDARD
Operating Temperature: 0°C to +55°C Relative humidity: 95% maximum (non-condensing)

4.4.1.2 Storage Environment

STANDARD
Storage Temperature: -20°C to +65°C Relative humidity: 95% maximum (non-condensing)

4.4.1.3 High Storage Temperature

STANDARD	TESTING
Module to function as specified after test and all non-volatile memory to retain the data stored prior to test The form and dimensions must conform to the physical use requirements of these specifications after testing Scratches, color and other appearance items shall depend on the specifications of the manufacturer for each module and are not a basis for evaluation here	Test Condition 65°C and 90-95% RH for 96 hours minimum, all voltage inputs = 0

4.4.1.4 Low Storage Temperature

STANDARD	TESTING
Module to function as specified after test and all non- volatile memory to retain the data stored prior to test The form and dimensions must conform to the physical use requirements of these specifications after testing Scratches, color and other appearance items shall depend on the specifications of the manufacturer for each module and are not a basis for evaluation here	Test Condition -20°C for 96 hours minimum, all voltage inputs = 0

4.4.1.5 High Operating Temperature

STANDARD	TESTING
Module to function as specified after test and all non-volatile memory to retain the data stored prior to test The form and dimensions must conform to the physical use requirements of these specifications after testing Scratches, color and other appearance items shall depend on the specifications of the manufacturer for each module and are not a basis for evaluation here	Test Condition 55°C for 96 hours minimum All voltage inputs = manufacturer specified

4.4.1.6 Low Operating Temperature

STANDARD	TESTING
Module to function as specified after test and all non-volatile memory to retain the data stored prior to test. The form and dimensions must conform to the physical use requirements of these specifications after testing Scratches, color and other appearance items shall depend on the specifications of the manufacturer for each module and are not a basis for evaluation here	Test Condition 0°C for 96 hours minimum All voltage inputs = manufacturer specified

4.4.1.7 Thermal Shock

STANDARD	TESTING
Module to function as specified after test and all non-volatile memory to retain the data stored prior to test The form and dimensions must conform to the physical use requirements of these specifications after testing Scratches, color and other appearance shall depend on the specifications of the manufacturer for each module and are not a basis for evaluation here	<table><tr><th>TEST</th><th>TEMP (°C)</th><th>TIME†</th></tr><tr><td>1</td><td>-20</td><td>30</td></tr><tr><td>2</td><td>25</td><td><05</td></tr><tr><td>3</td><td>65</td><td>30</td></tr><tr><td>4</td><td>25</td><td><05</td></tr></table> Repeat for 100 cycles, all voltage inputs = 0 Module connector disengaged † Time in minutes.

4.4.1.8 Moisture Resistance

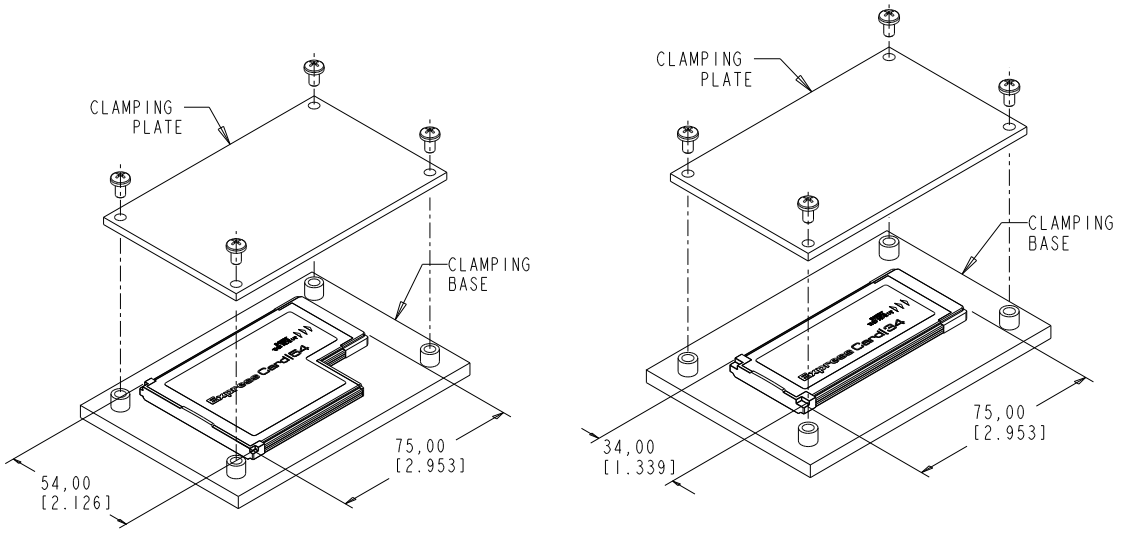
STANDARD	TESTING
Module to function as specified after test and all non-volatile memory to retain the data stored prior to test The form and dimensions must conform to the physical use requirements of these specifications after testing Scratches, color and other appearance items shall depend on the specifications of the manufacturer for each module and are not a basis for evaluation here	Maximum Temperature 55 °C. Minimum temperature 0 °C Steps 7a and 7b deleted from Method 106E MIL-STD 202. Repeat test for 10 cycles (excluding vibration) All voltage inputs = manufacturer specified, module connector disengaged.

4.4.1.9 Vibration and High Frequency

STANDARD	TESTING
Module to function as specified after test and all to retain the data stored prior to test	147 m/s^2 (15G) peak amplitude 10 to 2,000 Hz, 20 minute sweep, 12 cycles per axis, 36 cycles for 3 axes (12 hr) All voltage inputs = 0 See ***Figure 4-11*** for an appropriate test fixture

4.4.1.10 Shock

STANDARD	TESTING
Module to function as specified after test and to retain the data stored prior to test	Acceleration 490 m/s^2 (50G) Duration 11ms Semi-sine wave, velocity change: 3.44 m/s (11.3 ft/s) See ***Figure 4-11*** for an appropriate test fixture



Note: The module shock and vibration test fixture shall entrap the module such that all shock and vibration shall be transmitted into the sample module

Figure 4-11: ExpressCard module shock and vibration test fixture

4.4.1.11 Drop Test

STANDARD	TESTING
Module to function as specified after test and to retain the data stored prior to test The module must conform to the use requirements of these specifications after testing Scratches, color and other appearance items shall depend on the specifications of the manufacturer for each module and are not a basis for evaluation here	Drop module two(2) times in three(3) mutually exclusive axes from a height of 75 cm onto a non-cushioning, vinyl-tile surface For rotating media modules: Drop module (in a protective pouch) two(2) times in three (3) mutually exclusive axes from a height of 75 cm onto a non-cushioning vinyl-tile surface Drop module (in a protective pouch) two(2) times in three (3) mutually exclusive axes from a height of 75 cm onto a 0.635 cm nap industrial carpeted surface

4.5 Approved Test Procedures

Section	Test	EIA TP	IEC 512	Other
4.4.1.3	High Storage Temperature	364-31	6-11c	
4.4.1.4	Low Storage Temperature	364-59	6-11j	JIS C 0020[1]
4.4.1.5	High Operating Temperature	364-17	5-9b	
4.4.1.6	Low Operating Temperature	364-59	6-11j	JIS C 0020[1]
4.4.1.7	Thermal Shock	364-32	6-11d	
4.4.1.8	Moisture Resistance	364-31		
4.4.1.9	Vibration and High Frequency	364-28	4-6d	
4.4.1.10	Shock	364-27	4-6c	

1. JIS = Japanese Industrial Standard

4.6 Labeling (Marking)

The thickness of labeling, if used, shall not cause the ExpressCard module to exceed the thickness specified in the module outline figures (***Figure 4-1***, ***Figure 4-2***, Figure 4-4 and Figure 4-5).

The label, if used, must withstand all environmental test specified in ***Section 4.4 – Environmental and Mechanical Requirements***.

An "arrow" shall be printed on the top surface of the ExpressCard module, as illustrated in ***Figure 4-12*** for module examples, to indicate the orientation for module insertion. Some text such as "Insert with this side up" may be used.

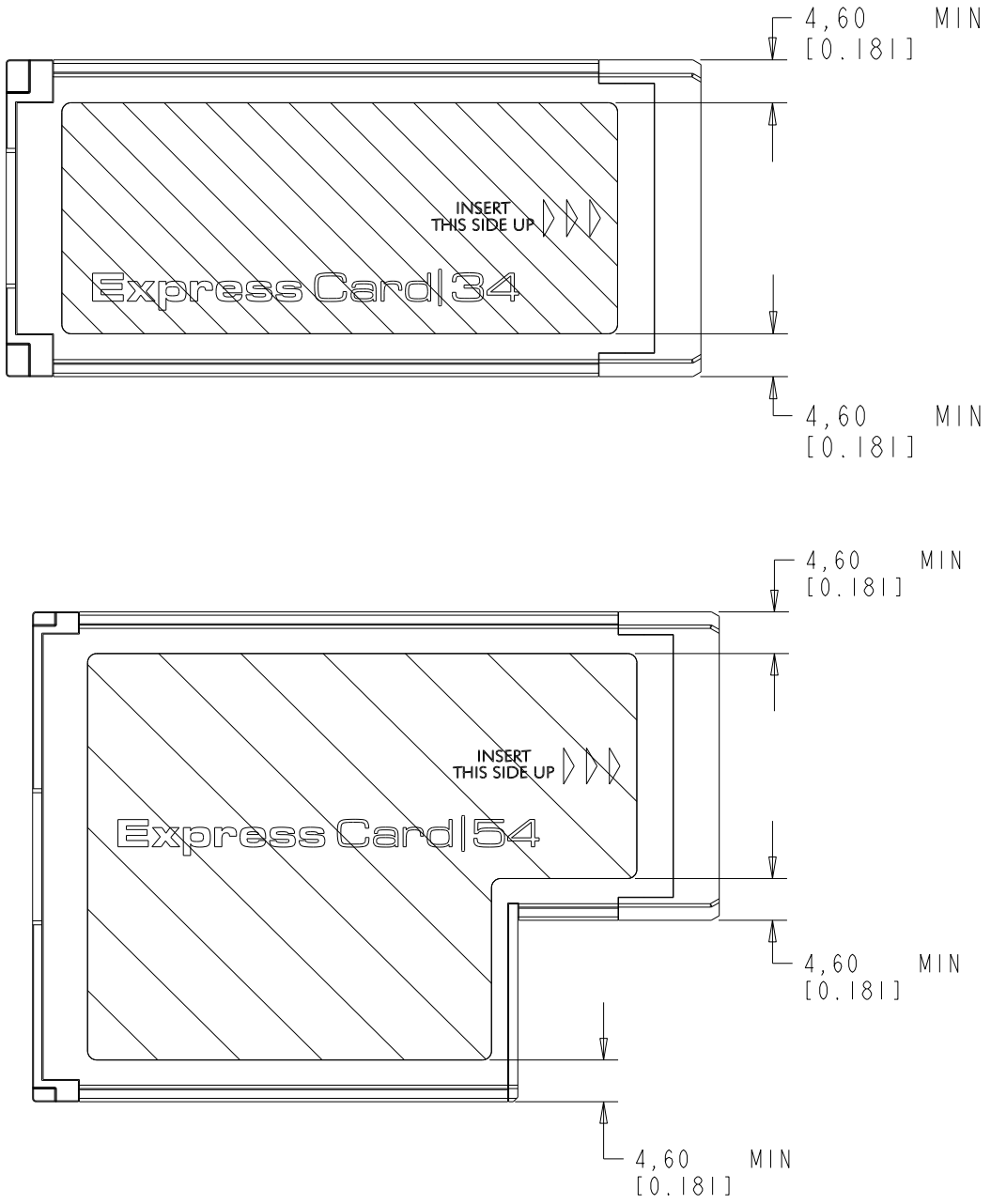


Figure 4-12: Label is allowed only in the crosshatched area

ExpressCard modules must be opaque (non see-through).

5. CONNECTOR SPECIFICATIONS

A beam-on-blade style connector is used for the ExpressCard interface. Although there are two module form factors (ExpressCard/34 module and ExpressCard/54 module), there is only one common connector interface for both module formats. This chapter defines the connector interface, as well as the electrical, mechanical, and environmental requirements.

5.1 Module Connector

The blade contacts are located on the ExpressCard module. ***Figure 5-1*** defines the ExpressCard module connector interface.

Only the front-end of the module connector that interfaces with the host connector is defined. The back-end of the connector that interfaces with the module printed circuit board is not defined. The offset between the solder tail and the module connector centerline is up to each connector and module manufacturer since this is considered to be implementation-specific.

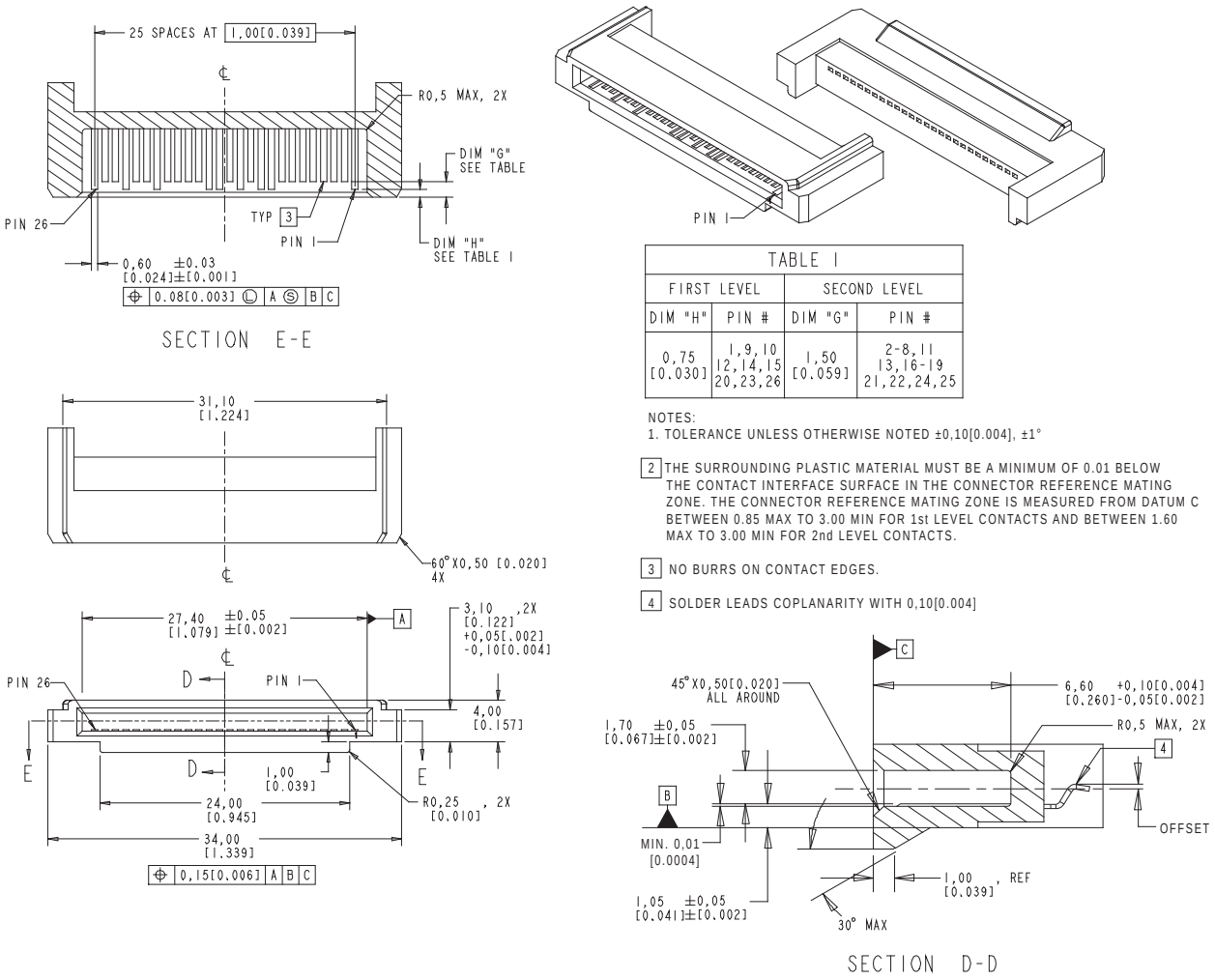


Figure 5-1: Module connector interface dimensions

It is recommended that the module connectors be surface-mounted, with the footprint shown in ***Figure 5-2***. The pads on the footprint shall be numbered in accordance to ***Figure 5-4;*** pin 1 shall always be on the right side of the connector in the top view.

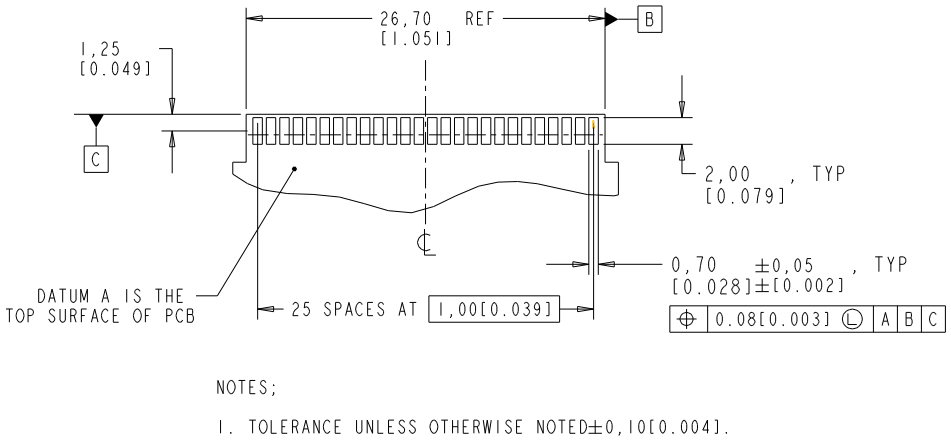


Figure 5-2: Recommended module connector footprint

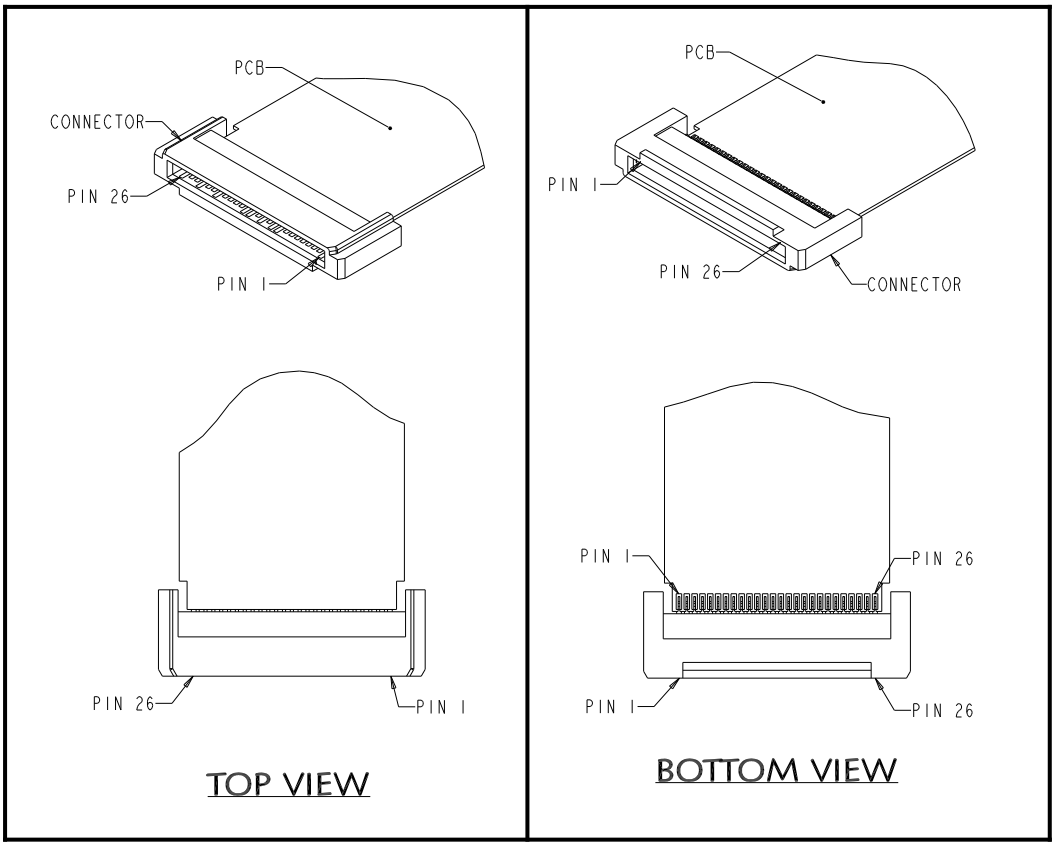


Figure 5-3: Recommended module connector footprint

Note that the recommended module connector footprint in ***Figure 5-2*** does not include any mechanical hold-down feature to protect the solder joints of the connector from being damaged during the repetitive module insertion/extraction. Module and connector manufacturers are responsible for ensuring the mechanical integrity of the ExpressCard module connector.

5.2 Host Connector

The ExpressCard host connector is defined in ***Figure 5-4***. This connector accommodates either the ExpressCard/34 modules or ExpressCard/54 modules.

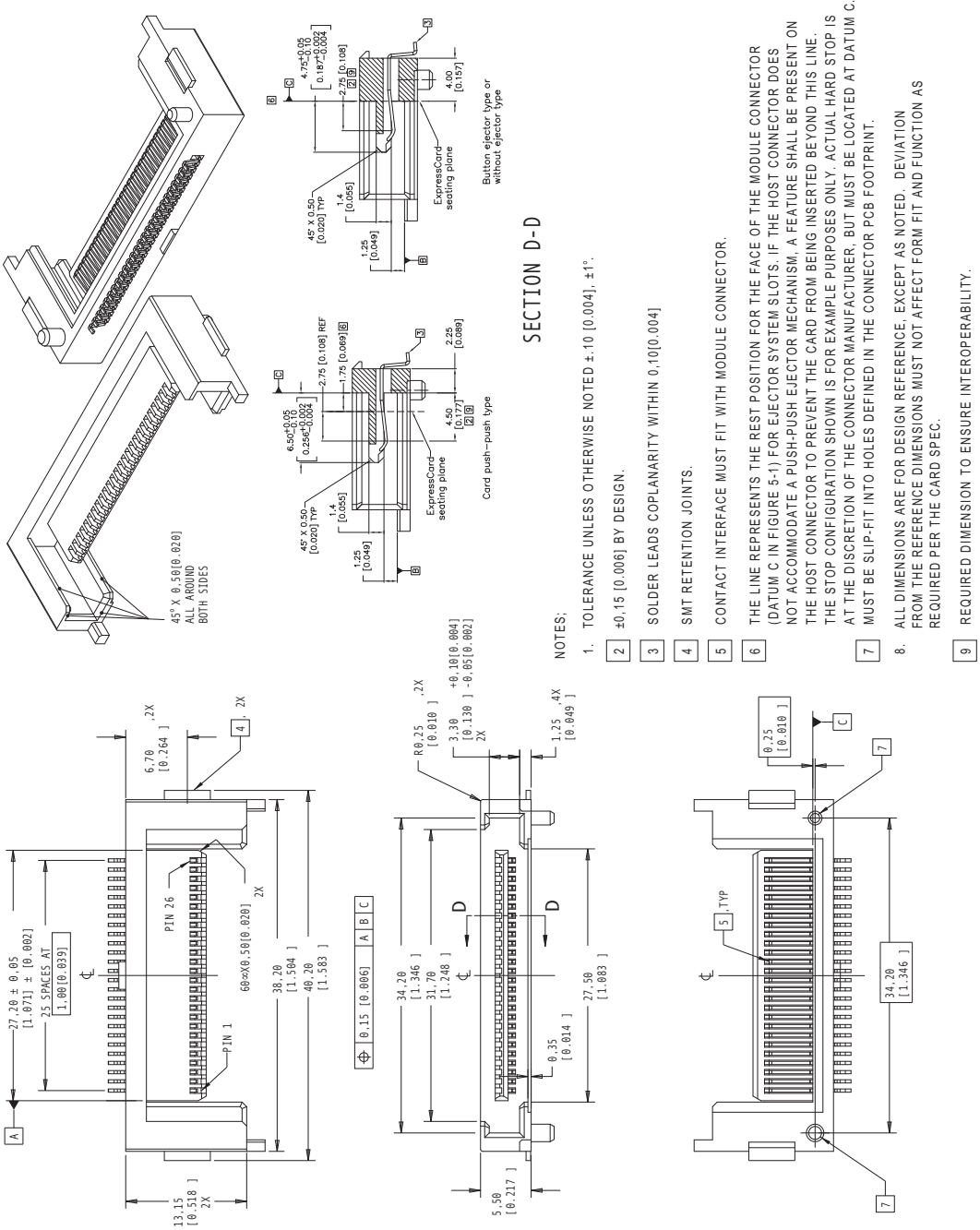


Figure 5-4: Host connector dimensions

The host connector is recommended to be surface-mounted, with footprint shown in ***Figure 5-5***.

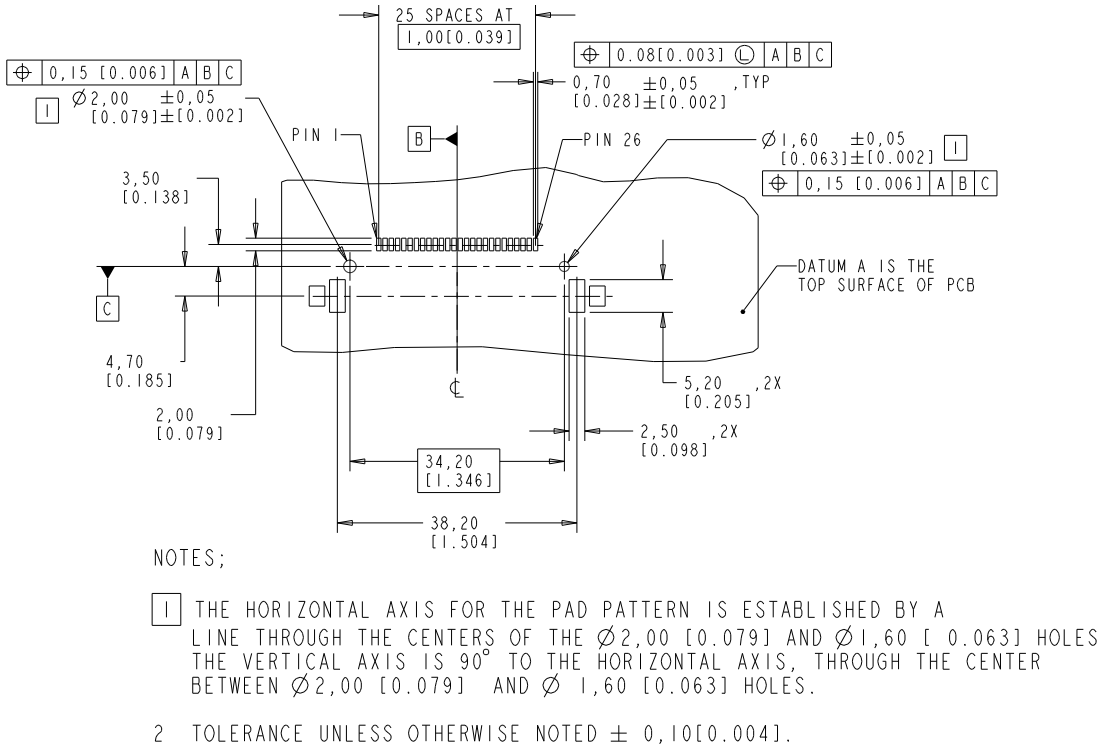


Figure 5-5: Recommended host connector footprint

Mechanical hold-down features are required for the host connector to survive the mating/un-mating forces encountered during module insertion and removal. Although ***Figure 5-5*** illustrates SMT pads as the hold-downs, other features such as screws or through-hole solder joints are also allowed at each system manufacturer's discretion.

5.3 Connector Electrical Requirements

An appropriate electrical test fixture shall be used for evaluating connector signal integrity. The test fixture effects, not including the connector via, are to be de-embedded from measurements. The following are the requirements for the test fixture:

- The test fixture shall be a FR4-based PCB, with microstrip structures. The dielectric thickness between the signaling trace and the reference ground plane, or the stack-up shall be 4 mils.
- The test fixture shall have 6-mil wide 50-Ω single ended traces that must be uncoupled. The impedance variation of those traces shall be controlled within ±5%.
- The ground plane immediately underneath the signal pads of the connector footprint should be removed.
- Unused pins adjacent to the signal pins shall be terminated with 50 _ resistors.

- For the insertion loss and return loss tests, there shall be a 0.75-inch long PCB trace connecting the contact solder pad to the SMA, both on the baseboard and on the insertion module.
- Edge-mounted SMAs are recommended and efforts shall be made to minimize the SMA launch discontinuity.

Only single-ended measurements that are processed to extract the differential characteristics or true differential measurements are allowed. The calibration shall be done to the end of the cables that connects the VNA to the SMA. Therefore, the insertion loss and return loss measurements include 1.5-inch long PCB traces (0.75 inches on the baseboard and 0.75 inches on the insertion module).

Note that the module connector solder pad is not counted as the module PCB trace; it is considered as a part of the connector interface. The 1.5-inch PCB trace included in the connector measurement is a part of the trace length allowed on the host system.

Table 5-1 lists the ExpressCard connector electrical requirements.

Table 5-1: ExpressCard connector electrical requirements

Parameter	Procedure	Requirements
Differential Insertion loss (IL)	EIA 364-101 The measured differential S parameter shall be referenced to an 85 Ω differential impedance.	≥-0.5 dB max up to 2.5 GHz, ≥-[0.8*(f-2.5)+0.5] dB for 2.5 Ghz < f ≤ 5.0 Ghz ≥-[3.0*(f-5)+2.5] dB for 5.0 GHz < f ≤ 7.5 GHz
Differential Return loss (RL)	EIA 364-108 The measured differential S parameter shall be referenced to an 85 Ω differential impedance.	≤-15 dB up to 3.0 GHz, ≤-5 dB up to 5.0 Ghz ≤-1 dB up to 7.5 GHz
Intra-pair skew	Intra-pair skew must be achieved by design; measurement not required.	5 ps max
Differential Crosstalk: NEXT	EIA 364-90 The measured differential S parameter shall be referenced to a 85 Ω differential impedance.	≤-32 dB max up to 2.5 GHz, ≤-26 dB max up to 5.0 Ghz, ≤-20 dB max up to 7.5 GHz
Current rating	EIA 364-70 method 2 1. The sample size is a minimum of three mated connectors. 2. The sample shall be soldered on a PC board with the appropriate footprint. 3. Wire all the voltage pins and all the ground pins in a series circuit. 4. A thermocouple of 30 AWG or less shall be placed to as close to the mating contact as possible. 5. Conduct a temperature rise vs. current test.	0.75 A per pin minimum. The temperature rise above ambient shall not exceed 30 °C. The ambient condition is still air at 25 °C.
Contact Resistance (LLCR)	EIA 364-23B	Initial: 40 mΩ max Final (after stress): 55 mΩ max (allowable resistance change: 15 mΩ)
Withstanding voltage	EIA 364-20 500 Vrms AC for 1 minute	1. No shorting or other damages. 2. Current leakage 1 mA max

5.4 Environmental Requirements

Office environment requirements for the connector are specified in this section. If the intended applications are for environments that differ from the office environment, OEM and module manufacturers can specify additional test requirements to support their intended application environments.

Connector environmental tests shall follow ***EIA-364-1000.01, Environmental Test Methodology for Assessing the Performance of Electrical Connectors and Sockets Used in Business Office Applications***. The test groups/sequences and durations shall be derived from the following requirements:

- Durability (mating/un-mating) rating of 5000 cycles for the host
- Durability (mating/un-mating) rating of 5000 cycles for the module, with an optional rating of 10000 cycles for high-durability modules at module manufacturers' discretion
- Field temperature: 65 ºC
- Field life: 5 years

Since the connector defined has far more than 0.127 mm wipe length, Test Group 6 in ***EIA-364-1000.01*** is not required. The temperature life test duration and the mixed flowing gas test duration values are derived from ***EIA 364-1000.01*** based on the field temperature per the following.

Temperature Life test temperature and duration	105 °C for 120 hours
Temperature Life test temperature and duration for preconditioning	105 °C for 72 hours
Mixed flowing gas test duration	7 days

The pass/fail criteria for the low level contact resistance (LLCR) and the Dielectric Withstanding Voltage are as defined in ***Table 5-1: ExpressCard connector electrical requirements***.

When testing a higher durability module connector (rated for 10000 cycles), the durability test procedure for Test Group 7 in ***EIA 364-1000.01*** shall be modified to reflect the requirement of different durability cycles for the host and module connectors. After 5000 cycles, the LLCR shall be measured. Starting from the 5001-th cycle, a new host connector shall be used to mate with the high-durability module connector.

Test Group 3 in EIA 364-1000.01 shall be modified to include a physical shock test, immediately after the vibration test. The shock test procedure and requirement are described in the table below.

Test description	Procedure	Requirement
Physical shock	EIA 364-27 Acceleration 490 m/s (50G) Standard holding time 11 ms, Semi-sine wave Velocity change 3.44 m/s	No evidence of physical damage

5.5 Mechanical Requirements

Table 5-2 lists mechanical test procedures and requirements for the ExpressCard connector.

Table 5-2: Mechanical test procedures and requirements

Test description	Procedure	Requirements
Insertion force	EIA 364-13 Measure the force necessary to mate the connector assemblies at a maximum rate of 12.5 mm (0.492 inches) per minute.	39 N maximum.
Removal force	EIA 364-13 Measure the force necessary to un-mate the connector assemblies at maximum rate of 12.5 mm (0.492 inches) per minute.	3.7 N min; 18.5 N max

The test sequences are defined in ***Table 5-3***.

Table 5-3: Mechanical test sequence

Test No.	Test Item	Test Sequence
1	LLCR	3, 5
2	Mating force	1
3	Un-mating force	2, 6
4	Temperature life (105ºC for 120 hours)	4

5.6 Additional Requirements

Additional connector requirements are defined in ***Table 5-4***.

Table 5-4: Additional connector requirements

Parameter	Procedure	Requirement
Flammability	UL94V-0 minimum	Material certification or certificate of compliance required with each lot to satisfy the Underwriters Laboratories follow-up service requirements.
Lead-free soldering		Connector must be compatible with lead free soldering process.

This specification does not attempt to define the connector requirements that are considered application-specific. It is up to the users and their connector suppliers to determine if additional requirements shall be added to satisfy the application needs.

6. HOST SYSTEM SPECIFICATION

This chapter describes the host system requirements. Host system ExpressCard electrical and mechanical design guides and design examples are covered in the ***ExpressCard Implementation Guidelines***.

6.1 Slot power control requirements

Power to ExpressCard slots is controlled by implementation-specific hardware within the host system. The module presence pins (**CPPE#** and/or **CPUSB#**) are asserted by the presence of ExpressCard modules inserted into the slot and are intended to enable the power rails to the module so that the module can perform its intended operation.

There are three common system conditions during which the module presence logic should be used by the host system to determine whether or not to provide power to the slot. ***Table 6-1*** summarizes the expected behavior of slot power supplied to the slot based on the state of the host system's power supplies and the module presence state.

Table 6-1: Expected behavior of ExpressCard slot power

System power state		Module presence state[1]	Slot power	
Primary	Auxiliary		Primary (+3.3V and +1.5V)	Auxiliary (+3.3AUX)
OFF	OFF	Don't care	OFF	OFF
ON	ON	De-asserted	OFF	OFF
		Asserted	ON	ON
OFF	ON	De-asserted	OFF	OFF
		Asserted prior to entering this system power state	OFF	ON
		Asserted after entering this system power state	OFF	OFF

1. Module presence state is determined by the combined state of the CPPE# and CPUSB# signals such that if either signal is asserted, then the combined state is also asserted (i.e. logical AND).

As shown in ***Table 6-1***, the system sleep state (primary power OFF, auxiliary power ON) is a special case where the slot power behavior varies depending on whether an ExpressCard module is present in the slot prior to entering the sleep state or inserted after entering the sleep state. The intended operation is defined such that given a module is present prior to entering a system sleep state then the module should be provided auxiliary power to allow for wake circuits to operate. If a module is inserted while the host system is already in a sleep state, then the insertion of the module should not cause auxiliary power to be enabled to the slot and thus the host system will not wake from the sleep state.

6.1.1 USB Specific Requirements

Since the ExpressCard slot does not provide the USB cable bus power ($\mathbf{V_{BUS}}$) as a pin on the interface, USB-based modules require an alternate means for determining $\mathbf{V_{BUS}}$ state in order to

maintain proper USB data line (**USBD+**, **USBD-**) termination. For this purpose, the **+3.3VAUX** power state is deemed to be logically equivalent to $\mathbf{V_{BUS}}$ and the host system shall be able to tolerate active termination on the USB data lines whenever **+3.3VAUX** (or **+3.3V**) is powered.

USB-based ExpressCard modules are specifically reported as self-powered devices. As such, they rely on external power, as opposed to USB $\mathbf{V_{BUS}}$, as their primary source of power. For purposes of an ExpressCard slot implementation, the **+3.3V** and **+1.5V** primary power rails are logically equivalent to external power for USB devices. The host system shall meet all slot behavioral requirements even if a USB-based function removes its USB data line (**USBD+**, **USBD-**) termination as the result of removing primary power from the slot. See also ***Section 3.2.6 USB power control operation*** for more details.

6.2 PCI Express Slot Capabilities Register

The ***PCI Express Base Specification*** defines a slot capabilities register that in an ExpressCard system implementation shall be required for each upstream port associated with an ExpressCard slot. Because of the ExpressCard operational model is hot pluggable and allows surprise insertion/removal of modules, both the Hot-Plug Surprise and Hot-Plug Capable bits shall be hardware initialized to the set state for each ExpressCard slot.

6.3 BIOS ACPI Requirements

This section covers host system requirements related to BIOS ACPI firmware support for ExpressCard module insertion and enumeration.

6.3.1 Supporting Both Interface Options in Legacy Systems

In order to support ExpressCard module implementations on host systems under legacy (non-PCI Express aware) operating systems that feature utilization of both the PCI Express and USB interface being used at the same time, the operating system must be able to determine the dependencies between the two buses. This information is used when an eject request is received. Without understanding the inter-dependencies of the two interfaces, executing a request to turn off one device may cause undesirable effects on the other device.

The mechanism used to define the dependency is an ACPI method and is defined by BIOS as the result of decisions made when the host system is designed. The ACPI method is_OSC, Operating System Capabilities, and is used to convey parent-child type dependencies and relationships.

An example of a _OSC method is shown below. Any host system implementing ExpressCard slots with ports provided by motherboard resident host controllers must implement and support the _OSC ACPI BIOS method.

To support the _OSC method, BIOS first builds a table for each port declaring the PCI Express and USB ports. This is done through a Bus Scope Initialization, _SB.INI. An example of loading the table is:

```
SCOPE (\_SB
    Method (_INI) {
        LoadTable (“OEM1”, “OEMID”, “Table1”, “\\_SB-EXC1”,,)
        LoadTable (“OEM1”, “OEMID”, “Table2”, “\\_SB-EXC2”,,)
        } // end _INI
) // end _SB scope
```

The terms OEM1 and OEMID are ACPI OEM identification terms and are OEM specific. The Table terms define unique tables for each slot. If only one slot is implemented, only one table entry is required. The _SB-EXCx terms create an ACPI device (slot).

Each device has a Hardware ID (_HID) that is system specific. _HIDs are defined within the PCI and ACPI specifications. The _HID must be unique within the ACPI namespace.

Each slot _SB-EXCx method defines the slot’s PCI Express and USB eject dependencies. The USB dependencies must include the Low- and Full-speed and High-speed ports. An _RMV flag is included (and set to “0”) to preclude the operating system from displaying a remove request option when no module is inserted.

The _SB-EXCx example, including the _HID and _EJD declarations, is as follows:

```
Scope(\_SB
{
    Device(\_SB.EXC1)
        {
        Name(HID,("ABC2005"))        // EISA ID of OEM host system
        Method (_STA,0),{…}
        } // end device

    Device(PCI0)
        {
        Device(PCI Express node)
                {
                Name(_ADR,…)      // ACPI path to port
                Name(_EJD,\\_SB.EXC1)
                Name(_RMV,0)
                }
        Device(USB1.1.1 node)
                {                 // example USB legacy host controller, port 1
                Name(_ADR,…)      // ACPI path to low- and full-speed port
                Name(_EJD,\\_SB.EXC1)
                Name(_RMV,0)
                }
        Device(USB2.0.1 node)
                {                 // example USB enhanced host controller, port 2
                Name(_ADR,…)      // ACPI path to USB high-speed port
                Name(_EJD,\\_SB.EXC1)
                Name(_RMV,0)
                }
        }
}
```


This, then, defines for each port used on module slot 1 an eject dependency to only one parent, \SB_EXC1:

```
Device (\_SB.EXC1) {
        Name(_HID, (“ABC2005”))
        ...
        ... PCI Express Function
            Name (_EJD, “\\_SB.EXC1”)
            ...
        ... USB 1.1.1 Function
            Name (_EJD, “\\_SB.EXC1”)
            ...
        ... USB 2.0.1 Function
            Name (_EJD, “\\_SB.EXC1”)
            ...
} // end device
```

A similar device would be implemented for each ExpressCard slot with unique paths, hardware identifications (_HID) and links to each slot and its dependencies:

```
Device (\_SB.EXC2) {
    Name (_HID, (“ABC2006”))
```

The system builder supplies a host system specific INF file that consists of typical INF headers and declares a user-friendly name for each _HID entry:

```
*ABC2005.DeviceDesc = “ExpressCard Slot 1”
*ABC2006.DeviceDesc = “ExpressCard Slot 2”
```

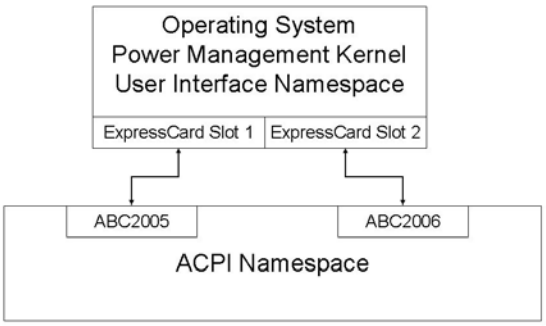


Figure 6-1: System INF-to-ACPI Relationship

The above methods and tables are described in greater detail in all ACPI revisions. They are created and loaded by BIOS by default during POST time. The _OSC method is defined in the ACPI 3 revision and is only implemented in later operating systems. The Operating System Capabilities method is used for several reasons: (1) it enables the unloading of tables if native discovery and handling is done by the operating system, (2) it enables the re-directing of ACPI methods used to detect the insertion and removal of modules by utilizing the Link Detect interrupt re-direct found in port registers.

An example of the _OSC method follows:

```
Device (PCI0) {                                  // root PCI bus
    Name(_HID,EISAID("PNP0A08"))                 // PCI Express root bridge
    Name(_CID,EISAID("PNP0A03"))                 // compatible PCI root bridge
    Name(SUPP,0)                                 // PCI _OSC support field value
    Name(CTRL,0)                                 // PCI _OSC control field value contains
                                                 // bit flags for capabilities supported
    Method(_OSC,4) {                             // check for proper UUID and revision ID
        // disable GPE used to detect insertion / removal if supported in the OS
        If(And(CTRL,0x01))                       // test for native OS support
            Store(0,HPCE)                        // clear hot plug SCI enable bit
            Store(1,HPCS)                        // clear hot plug SCI status bit
            Unload(EXC1)                         // unload methods and tables for non-native
            Unload(EXC2)                         // OS support of insertion / removal
        } // end _OSC method
    } // end PCI0 device
```

How it works

(Note: The following text and figures are conceptual aids only.)

The EXCx status method (_STA) sets or clears a "device present" bit based on the insertion and removal of ExpressCard PCI Express-enabled modules.

BIOS issues a bus check in response to the re-directed PCI Express link detection interrupt. This is the enabler for non-native operating system support.

The bus check causes the operating system to run the PNP enumeration operation which discovers the insertion or removal of the PCI Express function and balances system resources accordingly. When the device is "discovered", the hot-plug tool will contain an entry for the PCI Express function and is appropriate, the USB function.

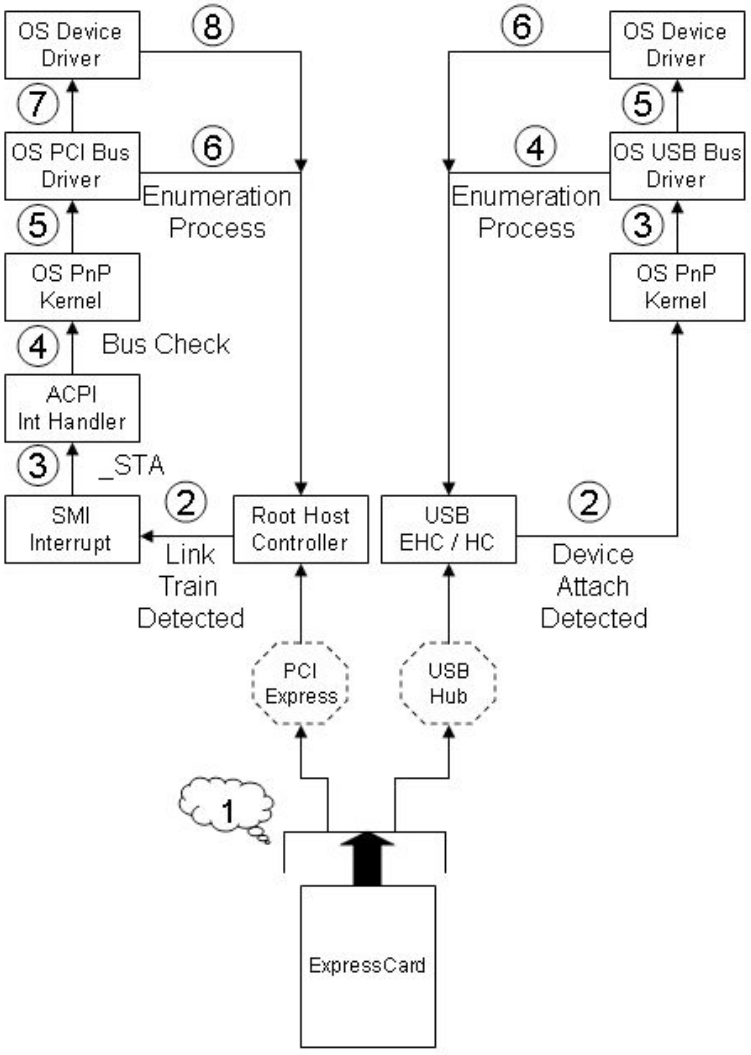


Figure 6-2: ExpressCard Module Insertion Events Within a Non-PCI Express Aware Operating System

USB function discovery is entirely handled by the operating system native USB functionality and is not utilized within the BIOS method except when a device is requested to be removed. The ejection dependency (_EJD) entry will cause the operating system's power management to request the removal of devices present under the USB and PCI hardware trees. Based on the value of _STA, the hot-plug applet will add or remove applet entries.

When a remove request is received (example: PCI Express function), this request is send to the operating system's plug-and-play kernel which then sends a stop request to the operating system power management kernel. Within the power management kernel, a dependency is noted between the port being requested to stop (PCI Express) and the ports (USB 1.1 and USB 2.0) named within the ACPI namespace for that slot (EXC1). Stop requests are then sent to each additional port in the namespace through the appropriate device and bus drivers. When finished, all ports are stopped and any notifications to the user have been processed by the appropriate driver and the "approved" remove request is granted.

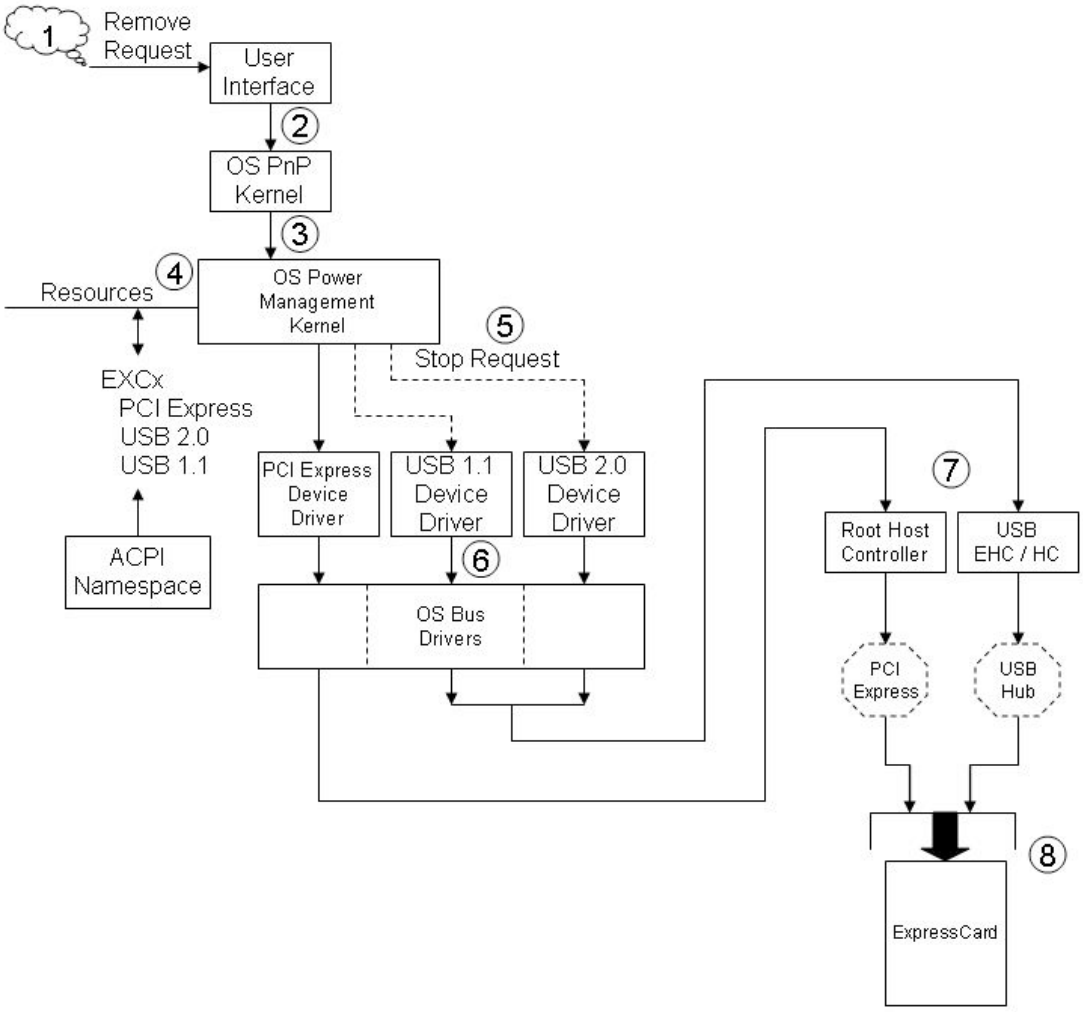


Figure 6-3: ExpressCard Module Removal Events Within a Non-PCI Express Aware Operating System

6.3.1.1 ExpressCard Insertion and Removal Within a PCI Express Aware Operating System

Under a PCI Express aware operating system, the operating system will rely on the mechanisms defined with the PCI Express Base Specification for detecting the insertion and removal of ExpressCard modules. These mechanisms are the hot-plug capabilities bits defined in the Slot Capabilities Register, Hot-Plug Surprise and Hot-Plug Capable.

As indicated in the _OSC method, when the operating system loads, the ACPI tables responsible for discovery will be unloaded and the ACPI interrupt triggered by the link detect interrupt re-direction will be disabled. The insertion / removal events are signaled to the operating system by an in-band PCI Express host controller card present (the Slot Status Register's Presence Detect Changed) interrupt to the bus driver, the plug and play manager and the power manager:

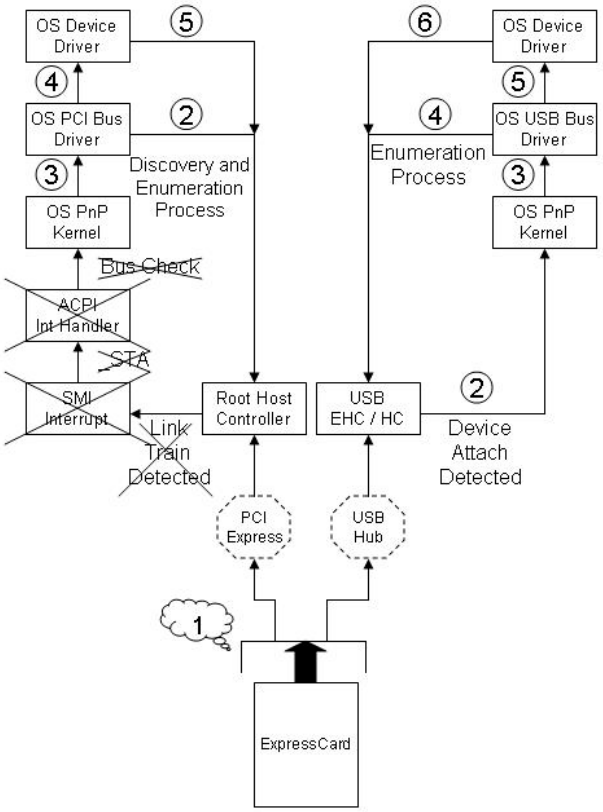


Figure 6-4: ExpressCard Insertion Within A PCI Express Aware Operating System

The removal event following a remove request is similar to the un-aware process except that the stop request handled within the power manager kernel relies on the common serial number provided by the module:

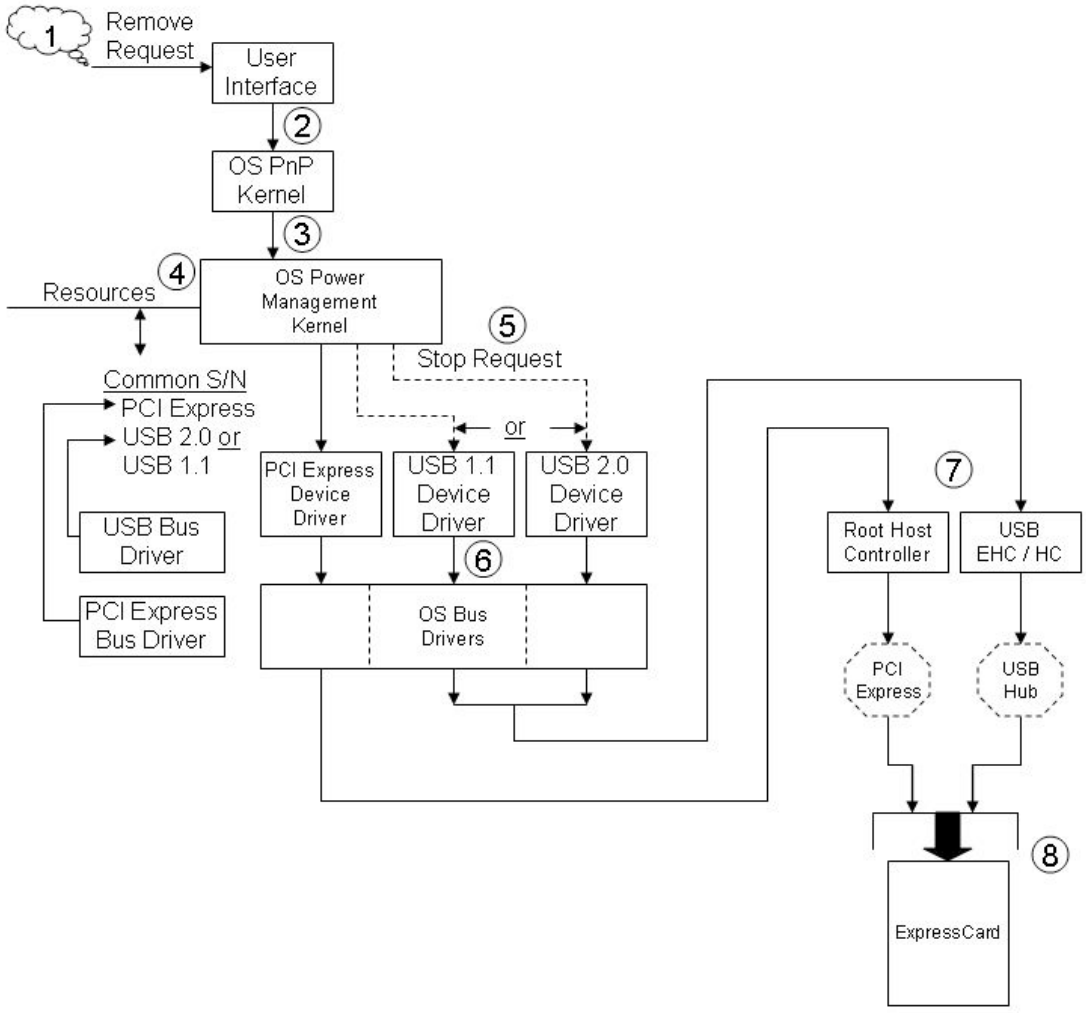


Figure 6-5: ExpressCard Removal Within A PCI Express Aware Operating System

6.3.2 Supporting PCI Bridging on ExpressCard Modules

ExpressCard module implementations are allowed to incorporate PCI-PCI bridges on the module to enable products that reuse existing PCI-based silicon (interconnected using a PCI Express-to-PCI bridge) or to build a multiple function module (interconnected using a PCI Express switch device). Host systems shall be able to recognize and enumerate this module implementation per the resource allocation requirements given herein.

For host systems that rely on legacy (non-PCI Express aware) operating systems, meeting this requirement will require that the BIOS firmware make minimum resource allocations each

ExpressCard slot at system boot time. At boot time, the BIOS shall allocate at least a minimum set of resources to the port that is supporting the slot, independent of if a module is present in the slot or not. Given that a module is present in the slot at boot time, the BIOS shall fully enumerate the module, extending the resources allocations as needed beyond the minimum requirements per the normal PCI enumeration process.

For host systems using PCI Express-aware operating systems, these requirements may be met through the capabilities of the operating system.

Table 6-2 defines minimum resource allocations that the host system shall implement to support PCI bridging on modules. These requirements have been derived from a model based on having up to six (6) PCI end-points implemented on a single module and comprehending the bus architectures necessary to support these end-points whether by a bridge or switch. Modules that require more than these minimum values may have to be present in the slot at boot time in order to ensure the needed resources beyond the minimum allocated.

Table 6-2: ExpressCard Slot Resource Allocations to Support PCI Bridging on Modules

Resource	Minimum per Slot	Comments
Bus numbering	8	One number for the slot plus additional numbers for child buses enumerated on the module
Memory windows	0M (prefetchable)	Devices needing any prefetchable resources will have to be present in the system at boot time; must be specifically programmed.
	32M (non-prefetchable)	Covers collective end-point needs for non-prefetchable memory BARs
I/O range	4K	Covers legacy end-point I/O transaction needs; I/O transactions are currently supported by the ***PCI Express Base Specification, Revision 1.1*** although future revisions of that specification may deprecate this capability.

Figure 6-6 illustrates the bus numbering requirements for a host system which has two ExpressCard slots. Although the illustration shows two slots in sequence with regard to root ports from the host chip set, it is also likely that a system may not contain multiple slots or that multiple slots could be separated by other root ports or even by being on separate PCI Express switches. Independent of the location of a particular slot, the bus numbering allocation requirements shall still apply.

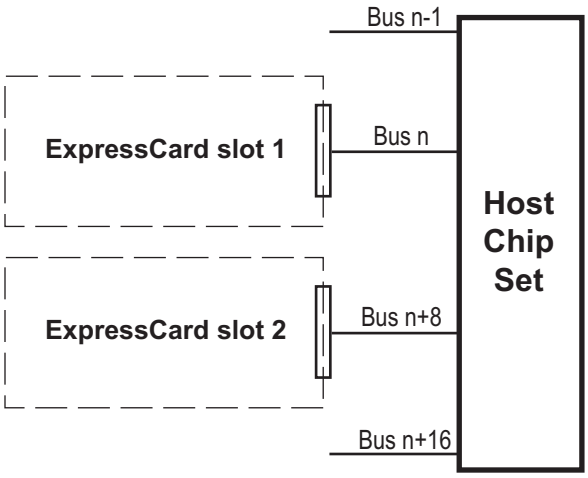


Figure 6-6: ExpressCard Slot Bus Number Allocations for an Example Two-slot System

When assigning resources, legacy operating systems will typically allocate all of the resources that are assigned to the root port to the first PCI-to-PCI Bridge that it finds downstream. This process would repeat for each successive layer of bridges that it finds. Figure 6-7 illustrates this limitation for an example PCI Express switch on a module. This implies that only the simplest of PCI-to-PCI Bridge structures, essentially only those that don't have parallel bridges reporting into a common upstream port will be supported when used with a legacy, pre-PCI Express aware operating system. If a more complex bridge structure is present on the module, then that module may have to be present at boot time in order to ensure that additional bridge resources are set up by the host system.

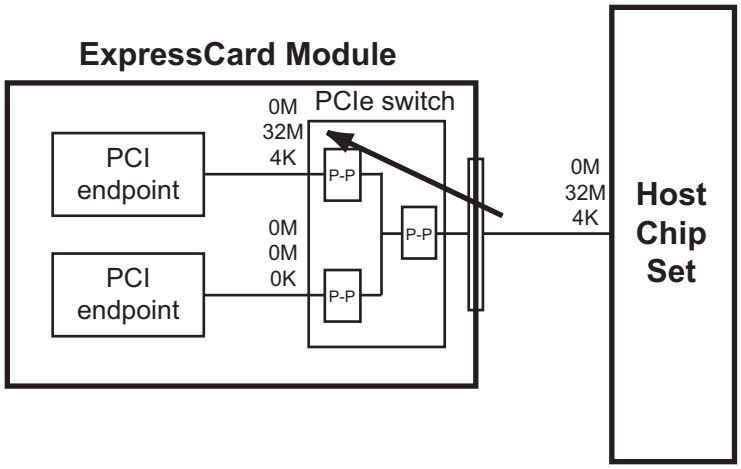


Figure 6-7: Example of Default Resource Allocation under Legacy Operating Systems

In addition to the requirements given above, the assignment of bus numbers along with the allocation of memory windows and I/O ranges shall be done per the requirements of the applicable PCI-related base, firmware and bridge specifications.

6.4 Electromechanical Interlock Requirements

While implementation of an electromechanical interlock to secure an ExpressCard within a slot is optional, the method is not and must conform to the ***PCI Express Base Specification Revision 1.1*** sections ***6.7.1.4 Electromechanical Interlock*** and ***6.7.2.7 Electromechanical Interlock Registers***.

6.5 PCI Express Link Power Management

ExpressCard modules that implement PCI Express-based applications are required to implement link power management including support for both Active State Link PM L0s and L1 states. Likewise, the host system shall implement support for L0s and L1 states in the ExpressCard slot and shall enable the use of each of these states, both in the host system and on the module, by default unless the exit latencies for a given state is unacceptable to the application. The expectation is that, for ExpressCard applications, such unacceptable exit latencies are highly unlikely and that entry into both L0s and L1 state will be enabled.

The responsibility for calculating acceptable exit latencies (if needed) and enabling these states is given to the host system software. For a host system that uses a legacy (non-PCI Express aware) operating system, the enabling responsibility may need to be with the host system BIOS.

Refer to the ***PCI Express Base Specification*** for more information regarding Active State Link PM and the means to determine unacceptable exit latencies.

In addition to Active State Link PM, modules are required to implement dynamic clock control for when in the *L1* state (see section ***3.2.4.1 Dynamic Clock Control***). This feature is intended to help improve power savings for the *L1* state by allowing the reference clock source within the host system to be turned off (parked) and potentially allowing the clock synchronization circuits of the module (PLL, etc.) to also be powered down. The responsibility for enabling this capability lies with the host system software and shall be enabled on all host systems. Once enabled, the module uses the **CLKREQ#** signal for establishing when it is acceptable to have the reference clock off (parked) based on its *L1* entry and exit timing needs.

6.6 USB Power Management

ExpressCard host systems are required to implement the power management features as required for USB compliance.

Refer to the applicable USB specifications for more information regarding implementation requirements for link power management.

