CSE260 Lab Report

Experiment Name:

Familiarization of Fundamental Logic Gates

Submitted by

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Section: 09

Date: Saturday, July 3, 2021

Captain

Date :.....

1. Name of the experiment: Familiarization of Fundamental Logic Gates

2. Objective:

i. To get familiarized with fondamental logic gates and demonstrate the input output relationship of 2-input AND (IC-7408), OR (IC-7432), and NOT (IC-7404) gates by constructing their truth tables.

ii. To get familiarized with other logic gates like NAND (IC-7400), NOR (IC-7402) and XNOR (IC-74266)

3. Required Components and Equipments:

i. For simulation we required Proteus software.

In Proteus we need:

i. Logic probe (BIG)
ii. Logic state
iii. AND
iv. OR
v. NOT
vi. NAND
vii. NOR
viii. XOR

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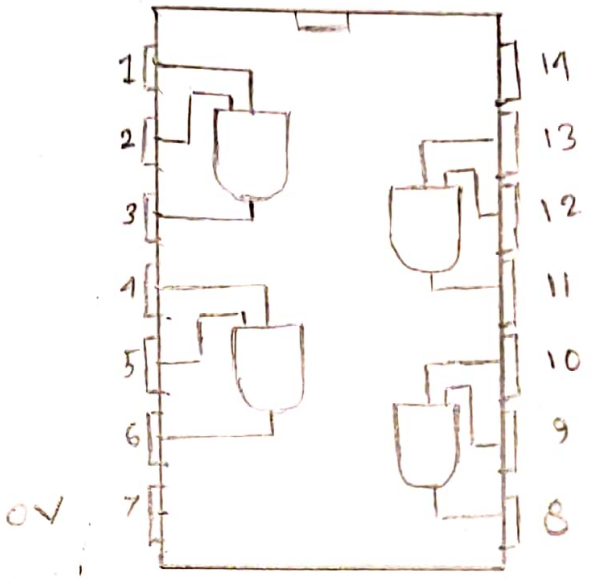
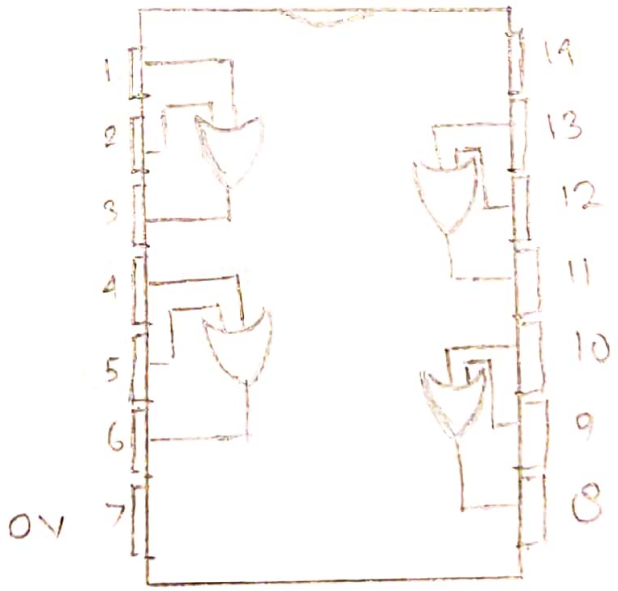
Pin layout of 7408:



Pin layout of 7432:



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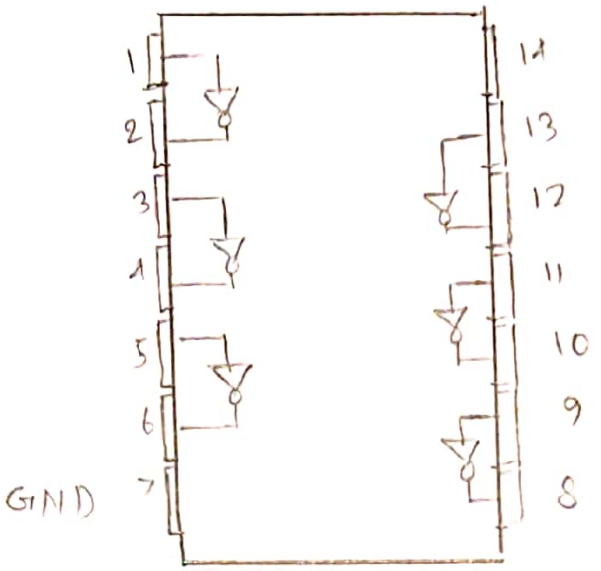
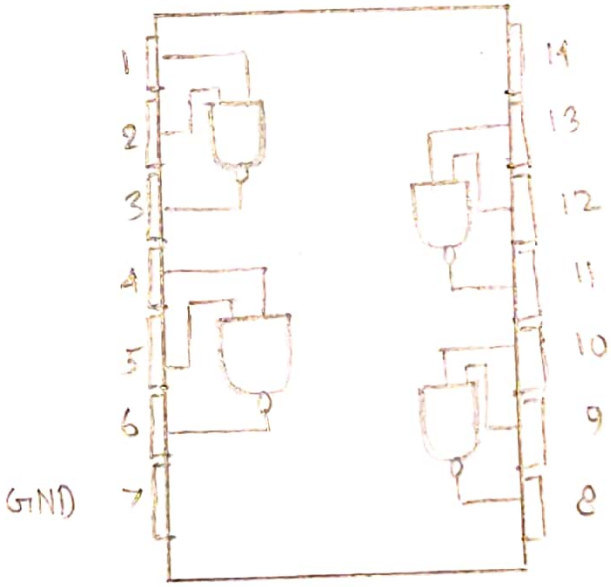
Pin layout of 7404 :



Pin layout of 7400 :



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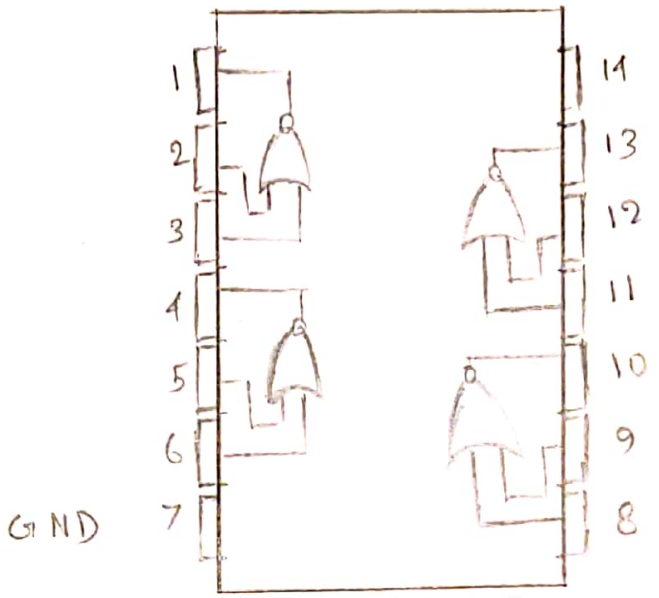
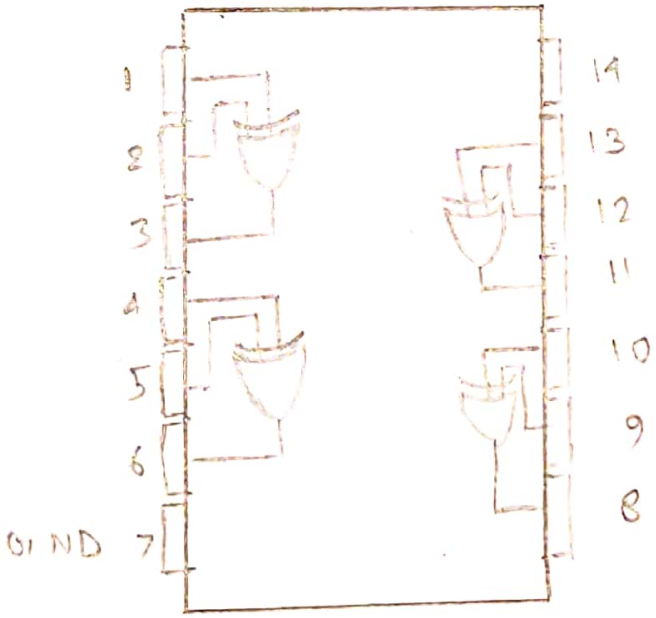
Pin layout of 7402:



Pin layout of 7486:



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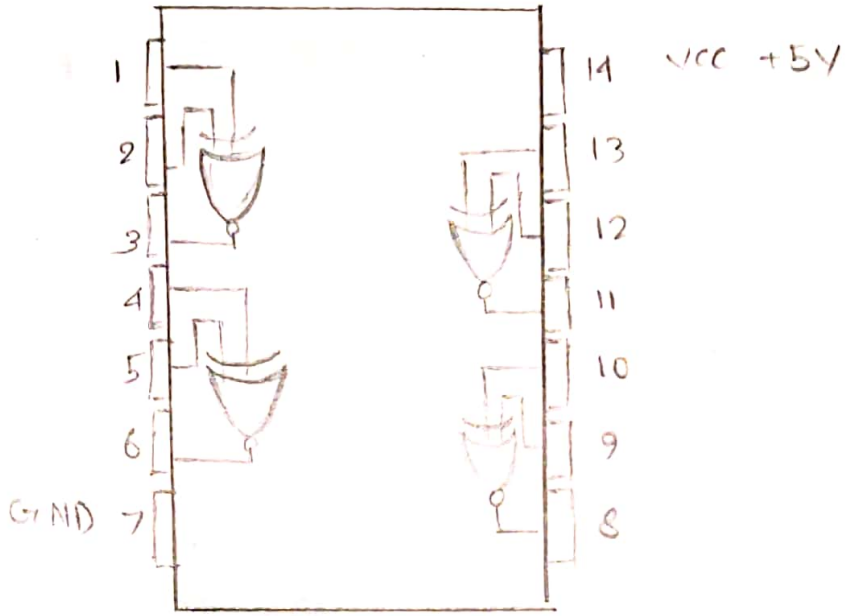
Pin layout of 74266:



5. Truth Table and Discussions:

Truth table of AND gate:

Input		output
A	B	
0	0	0
1	0	0
0	1	0
1	1	1

Truth table of OR gate :

Input		output
A	B	
0	0	0
1	0	1
0	1	1
1	1	1

Truth table of NOT gate:

Input	output
A	
0	1
1	0

Truth table of NAND gate :

Input		output
A	B	
0	0	1
1	0	1
0	1	1
1	1	0

Truth table of NOR gate :

Input		output
A	B	
0	0	1
1	0	0
0	1	0
1	1	0

Truth table of XOR gate:

Input		output
A	B	
0	0	0
1	0	1
0	1	1
1	1	0

Truth table of XNOR gate:

Input		output
A	B	
0	0	1
1	0	0
0	1	0
1	1	1

Discussion:

From this lab we got to know about the fundamental logic gates AND, OR, NOT. AND and OR takes two input and gives one output. If both the inputs are "one" then only the output will be "one". On the other hand, OR gate gives "one" output even if there is one input "one". Lastly, the NOT gives the reversed output.

There are four more gates : NAND, NOR, XNOR and XOR. NAND gate is the combination of AND and Not gate which gives the exact opposite values of AND gate. The same happens with NOR gate, it is the combination of OR and NOT gate. Then, in XOR gate, only if one value of two is "one", it will give output one. Lastly, the XNOR gate is the exact opposite of XOR gate.

Moreover, in the lab we got to learn about different IC constituting these gates and also learned about the simulation in proteus software.