CSE260 Lab Report

Experiment Name:

Parity Generator and Checker

Submitted by

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Section: 09

Date: 18/07/21

Captain

Date :.....

1. Name of the experiment:

Parity Generator and checker

2. Objective:

* To design and implement on Even parity Generator and Even parity checker using XOR gates. (IC-7486)

3. Required Components and Equipment:

i. AT -700 Portable Analog/ Digital Labratory
ii. 7400 x3

In proteus we need:

i. Logic Probe
ii. Logic State
iii. XOR

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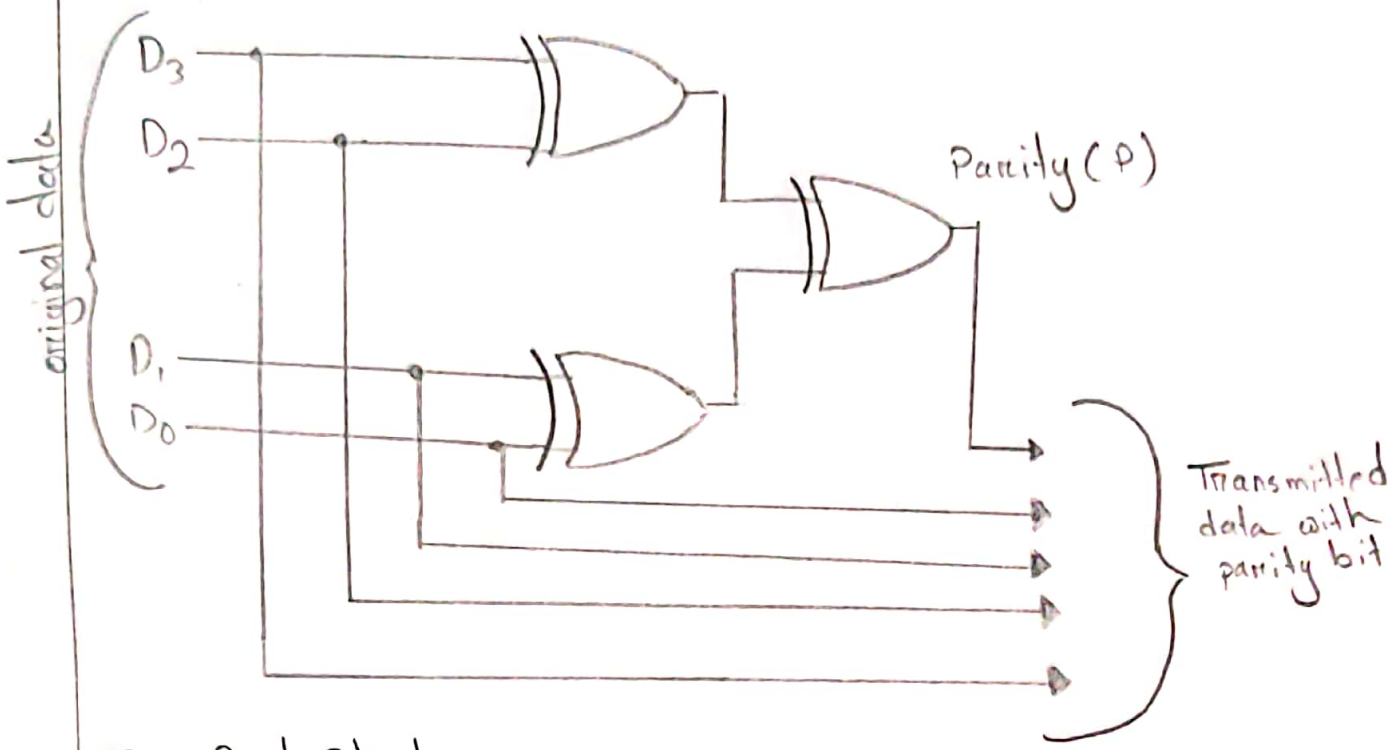
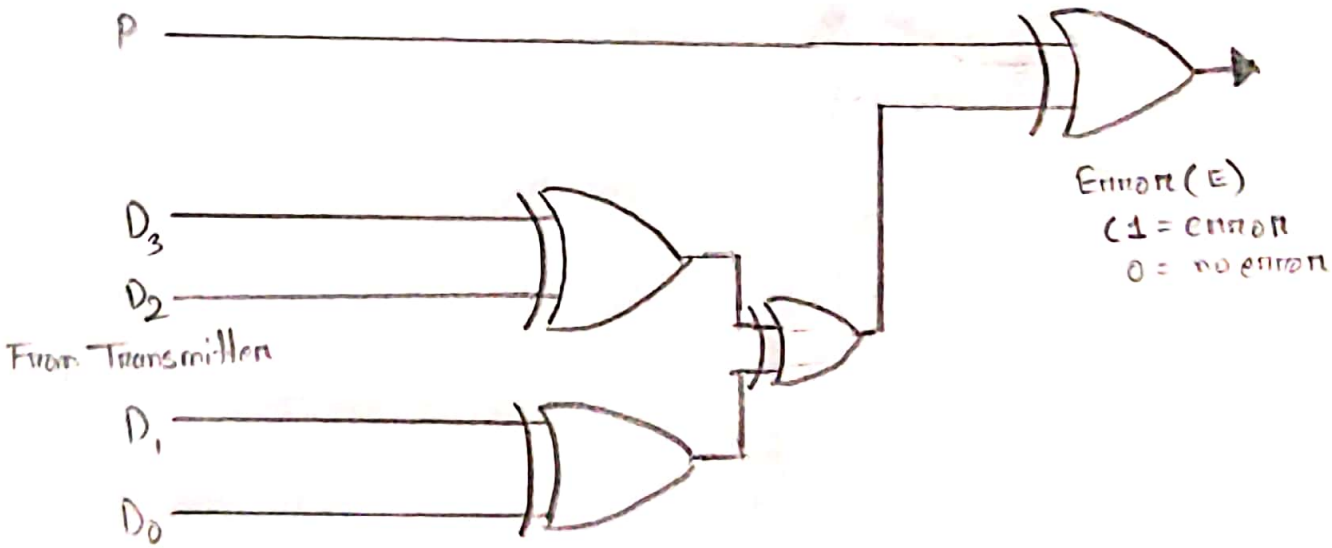
4. Experimental Setup:

Even parity Generator:



Even Parity Checker:



5. Results in Tabular form:

For (a) 0111 (b) 1001 (c) 000 (d) 0100, Parity Generation

P	D_3	D_2	D_1	D_0
1	0	1	1	1
0	1	0	0	1
0	0	0	0	0
1	0	1	0	0

Parity Checker:

P	D_3	D_2	D_1	D_0	Error
0	1	0	1	0	0
1	1	1	1	0	0
1	1	1	1	1	1
1	0	0	0	0	1

Even Parity generator truth table:

D_3	D_2	D_1	D_0	$D_0 \oplus D_1$	$D_2 \oplus D_3$	$(D_0 \oplus D_1) \oplus (D_2 \oplus D_3)$
0	0	0	0	0	0	0
0	0	0	1	1	0	1
0	0	1	0	1	0	1
0	0	1	1	0	0	0
0	1	0	0	0	1	1
0	1	0	1	1	1	0
0	1	1	0	1	1	0
0	1	1	1	0	1	1
1	0	0	0	0	1	1
1	0	0	1	1	1	0
1	0	1	0	1	1	0
1	0	1	1	0	1	1
1	1	0	0	0	0	0
1	1	0	1	1	0	1
1	1	1	0	1	0	1
1	1	1	1	0	0	0

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Even parity checker truth table:

P	D_3	D_2	D_1	D_0	$D_0 \oplus D_1$	$D_2 \oplus D_3$	$P: D_0 \oplus D_1 + D_2 \oplus D_3$	$P' \oplus P$
0	0	0	0	0	0	0	0	0
0	0	0	0	1	1	0	1	1
0	0	0	1	0	1	0	1	1
0	0	0	1	1	0	0	0	0
0	0	1	0	0	0	1	1	1
0	0	1	0	1	1	1	0	0
0	0	1	1	0	1	1	0	0
0	0	1	1	1	0	1	1	1
0	1	0	0	0	0	1	1	1
0	1	0	0	1	1	1	0	0
0	1	0	1	0	1	1	0	1
0	1	0	1	1	0	1	1	0
0	1	1	0	0	0	0	0	1
0	1	1	0	1	1	0	1	1
0	1	1	1	0	1	0	1	0
0	1	1	1	1	0	0	0	1
1	0	0	0	0	0	0	0	0
1	0	0	0	1	1	0	1	0
1	0	0	1	0	1	0	1	1
1	0	0	1	1	0	0	0	0
1	0	1	0	0	0	1	1	1
1	0	1	0	1	1	1	0	1
1	0	1	1	0	1	1	0	1
1	0	1	1	1	0	1	1	0
1	1	0	0	0	0	1	1	0
1	1	0	0	1	1	1	0	1
1	1	0	1	0	1	1	0	1
1	1	0	1	1	0	1	1	0
1	1	1	0	0	0	0	0	1
1	1	1	0	1	1	0	1	0
1	1	1	1	0	1	0	1	0
1	1	1	1	1	0	0	0	1

Discussion :

we know, XOR gate will give output "0" if both the inputs are same. If they are diffrent, the output will be "1". From the truth table of parity generator we can see if the number of "1"s are even output is 0. If we look at the parity checker truth table, if the parity bit matches from the received inputs with its checker, error is "0" else is "1". Thus XOR gates are used to get to the conclusion of error detection.