CSE260 Lab Report

Experiment Name: Design and Implementation of 4-bit Parallel Binary Adder

Submitted by

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Section: 09

Date: 15/8/2021

Captain

Date :

Name of the experiment: Design and implementation of 4-bit Parallel Binary Adder.

objective :

i. To understand how addition occurs in digital device

ii. To implement adders which adds up to 4-bit binary

Required components

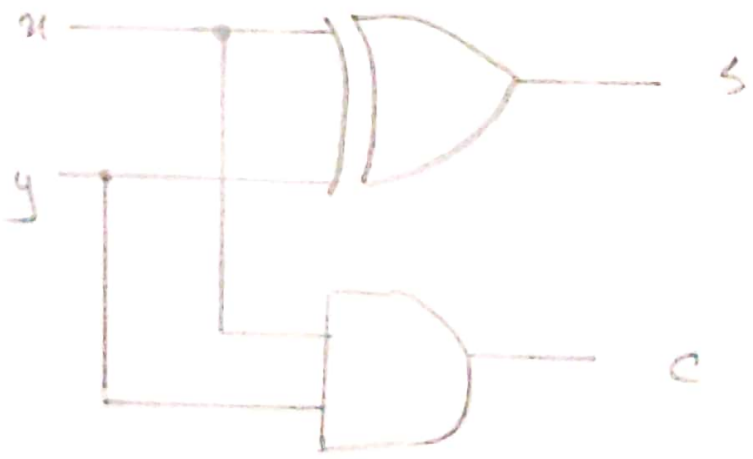
i. AT-700 portable Analog / Digital laboratory

ii. XOR, AND gate

iii. IC 74283

Experimental setup:

Half Adder Circuit :



$s = x \oplus y$

$c = xy$

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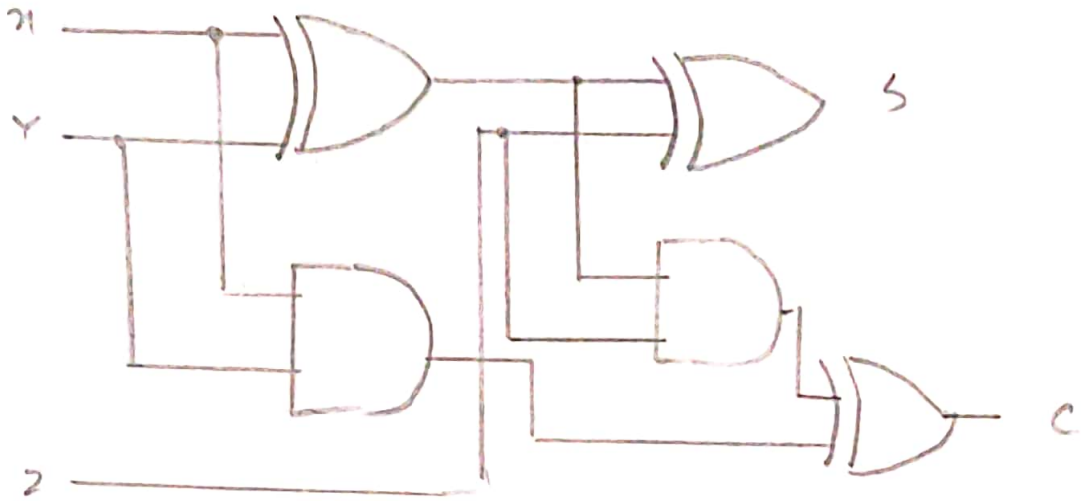
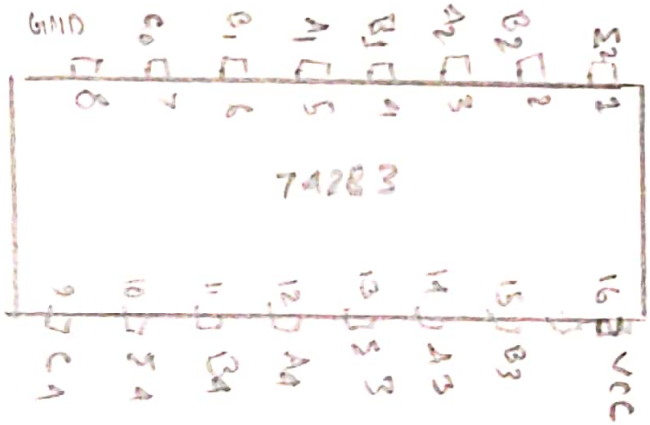
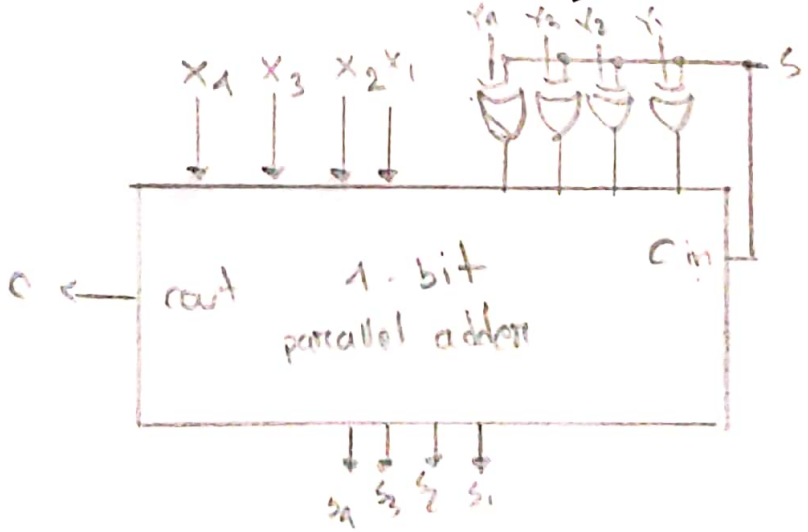
Full Adder :



4 bit Parallel adder



4 bit full adder cum subtractor :



Result:

Truth table of half adder:

x	y	c	s
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Truth table of full adder:

x	y	z	c	s
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

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Discussion :

* A half adder perfoms addition of two bits,

$c = zy$ and $s = z \oplus Y$

* For full adder, c = carry out, z = carry in

Like,

```
  ①①   Carry
  0 1 1 1
  1 0 1 1
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1 0 0 1 0
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* For positive bit addition s is initially 0 but in addition of negative number s is 1 initially. XOR with every single bit will give us negative of that positive number. Also in the 4 bit add cum substract we can add two negative numbers by doing XOR.