

HardRingCorrectness \triangleq

$$\begin{aligned} & \wedge \forall t \in TaskSet : \wedge \square (Len(TaskState[taskId(t)].msg) \leq 3) \\ & \quad \wedge \square \Diamond ENABLED SendElem(t) \\ & \wedge \square (ENABLED NextChip \Rightarrow History.elem = Shared.chipCount) \end{aligned}$$

ReservationSafety \triangleq

$$\begin{aligned} & \square \forall chip, j \in Task : \wedge ENABLED SendRese(T[j]) \\ & \quad \wedge Shared.chipCount = chip \\ & \Rightarrow \wedge TaskState[j].res[chip] = j \\ & \quad \wedge \forall i \in Task \setminus \{j\} : TaskState[i].res[chip] \in \{j, -1\} \end{aligned}$$

SoftRingFairness \triangleq

$$\begin{aligned} & \wedge \forall i \in Proc : \square (\text{IF } i \in Shared.proc \\ & \quad \text{THEN } ProcState[i].list \neq \langle \rangle \Rightarrow \Diamond (i = ProcState[i].token) \\ & \quad \text{ELSE TRUE}) \\ & \wedge \square \Diamond (\forall i \in Proc \setminus Failed : \text{IF } i \in Shared.proc \\ & \quad \text{THEN } Len(ProcState[i].list) = 0 \\ & \quad \text{ELSE TRUE}) \end{aligned}$$