Voltage and energy in Charge Redistribution DACs used in SAR ADCs

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Abstract

This document describes the development of a simplified and a general models for calculation of voltage and energy in capacitive DAC topologies used in Charge Redistribution (CR) Successive Approximation Register(SAR) ADCs..

1 Models for voltage and energy in CR ADCs

We consider that the comparator inputs present infinite impedance and therefore drain no current from the DAC outputs. Following this assumption, the comparator is removed from the analysis, without compromising the accuracy of the models. Most of the switching schemes use only two voltage levels as reference voltages in the DAC arrangement, namely ground and V_{REF}. For these topologies, we may rely on a simplified model to compute the DAC output voltage and the energy. Some other switching schemes, on the other hand, use another intermediate reference voltage, such as V_{CM}. For the latter, we devise a general model that support an arbitrary number of references and concurrent switching of multiple capacitors.

2 Simplified voltage model for CR DACs

Since the CR DACs are based on switched capacitors, they do not present static power consumption. Therefore, we are only interested in the power consumtion that takes place in the transistions between states. The circuit in Figure 1 provides a good representation of a CR DAC transistioning between abitrary states. In the diagram, C_{T} represents the sum of capacitances that has the bottom plate connected to V_{REF} and remain in this condition during the transistion. The capacitor C_{B} represents the sum of capacitances with bottom plates connected to ground that are left unchanged during the transition. The remaining capacitor, C_{X}, represents the capacitance being switched. The switch S_1 is initially connected to ground and is switched to V_{REF} at time $t = 0$. All the voltages and currents on the circuit totally settle at time t_s. We can discretize

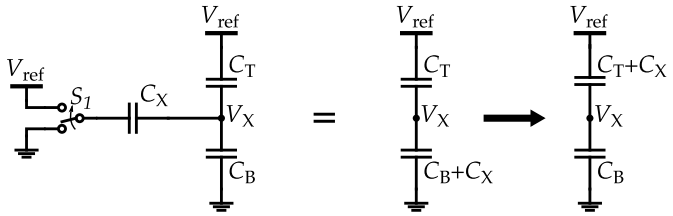

Figure 1: Circuit representation of a CR DAC transistioning between abitrary states.

the time domain and define $V_{\mathrm{X}}(0) \equiv V_{\mathrm{X}}[i-1]$ and $V_{\mathrm{X}}(t_s) \equiv V_{\mathrm{X}}[i]$. Since there is no current path for the top plates of the capacitors, the charge at the node V_{X} is conserved.

$$Q_X[0] = Q_X[1] \tag{1}$$

The equation (1) can be rewritten as follows:

$$C_{\mathrm{X}}V_{\mathrm{X}}[i-1]+C_{\mathrm{T}}\left(V_{\mathrm{X}}[i-1]-V_{\mathrm{REF}}\right)+C_{\mathrm{B}}V_{\mathrm{X}}[i-1] = C_{\mathrm{X}}\left(V_{\mathrm{X}}[i]-V_{\mathrm{REF}}\right)+C_{\mathrm{T}}\left(V_{\mathrm{X}}[i]-V_{\mathrm{REF}}\right)+C_{\mathrm{B}}V_{\mathrm{X}}[i] \tag{2}$$

Solving (2) for $V_{\mathrm{X}}[i]$ leads to

$$V_{\mathrm{X}}[i] = V_{\mathrm{X}}[i-1] + \frac{C_{\mathrm{X}}}{C_{\mathrm{X}}+C_{\mathrm{T}}+C_{\mathrm{B}}}V_{\mathrm{REF}}. \tag{3}$$

Similarly, if C_{X} is switched from V_{REF} to ground, (3) becomes

$$V_{\mathrm{X}}[i] = V_{\mathrm{X}}[i-1] - \frac{C_{\mathrm{X}}}{C_{\mathrm{X}}+C_{\mathrm{T}}+C_{\mathrm{B}}}V_{\mathrm{REF}}. \tag{4}$$

To quantify the energy consumed from the reference source when S_1 switches ground to V_{REF}, let us again consider the simple circuit of Figure 1, assuming that at the instant $t = 0$, V_{X} is equal to $V_{\mathrm{X}}(0)$ and S_1 is disconnected from ground and connected to V_{REF}. The energy spent to switch the bottom plate of C_{X} to V_{REF} is given in (5), considering that V_{REF} is a dc voltage source and the current flowing through its terminals is I_{REF}.

$$E_{\mathrm{REF}} = V_{\mathrm{REF}} \int_0^{t_s} I_{\mathrm{REF}}\, dt \tag{5}$$

The current I_{REF} can be described in terms of the charge drainded to the capacitors connected to V_{REF}. This is seen in (6), where $Q_{C_{\mathrm{X}}}$ and $Q_{C_{\mathrm{T}}}$ are the charges stored in C_{X} and C_{T}, respectively.

$$I_{\mathrm{REF}}(t) = -\left(\frac{\mathrm{d}Q_{C_{\mathrm{X}}}}{\mathrm{d}t} + \frac{\mathrm{d}Q_{C_{\mathrm{T}}}}{\mathrm{d}t}\right) \tag{6}$$

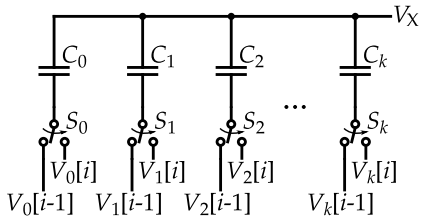

Figure 2: Circuit used to develop the general voltage model for CR DACs.

Rewriting (5) in terms of (6) yields in

$$E_{\mathrm{REF}}[i] = -V_{\mathrm{REF}} \int_0^{t_s} \left(\frac{\mathrm{d}Q_{C_{\mathrm{X}}}}{\mathrm{d}t} + \frac{\mathrm{d}Q_{C_{\mathrm{T}}}}{\mathrm{d}t} \right) \mathrm{d}t \tag{7}$$

$$= -V_{\mathrm{REF}} \left(\int_{Q_{C_{\mathrm{X}}}(0)}^{Q_{C_{\mathrm{X}}}(t_s)} \mathrm{d}Q_{C_{\mathrm{X}}} + \int_{Q_{C_{\mathrm{T}}}(0)}^{Q_{C_{\mathrm{T}}}(t_s)} \mathrm{d}Q_{C_{\mathrm{T}}} \right) \tag{8}$$

Integrating, we arrive at

$$E_{\mathrm{REF}}[i] = -V_{\mathrm{REF}} \left[(Q_{C_{\mathrm{X}}}[i] - Q_{C_{\mathrm{X}}}[i-1]) + (Q_{C_{\mathrm{T}}}[i] - Q_{C_{\mathrm{T}}}[i-1]) \right] \tag{9}$$

$$= -V_{\mathrm{REF}} C_{\mathrm{X}} \left[(V_{\mathrm{X}}(t_s) - V_{\mathrm{REF}}) - (V_{\mathrm{X}}[i-1]) \right] - V_{\mathrm{REF}} C_{\mathrm{T}} \left[(V_{\mathrm{X}}[i] - V_{\mathrm{REF}}) - (V_{\mathrm{X}}[i-1] - V_{\mathrm{REF}}) \right]. \tag{10}$$

Solving (10) leads to

$$E_{\mathrm{REF}}[i] = V_{\mathrm{REF}} C_{\mathrm{X}} \left(V_{\mathrm{REF}} + V_{\mathrm{X}}[i-1] - V_{\mathrm{X}}[i] \right) + V_{\mathrm{REF}} C_{\mathrm{T}} \left(V_{\mathrm{X}}[i-1] - V_{\mathrm{X}}[i] \right). \tag{11}$$

Plugging (3) into (11) yields in

$$E_{\mathrm{REF}}[i] = \frac{C_{\mathrm{B}} C_{\mathrm{X}}}{C_{\mathrm{B}} + C_{\mathrm{T}} + C_{\mathrm{X}}} V_{\mathrm{REF}}^2. \tag{12}$$

Equations (3) and (12) may be readily used to calculate the top-plate voltage and the energy in the DAC topologies based on the principle of charge redistribution, respectively, if only V_{REF} and ground are employed as references. Additionally, the model is only valid if only one capacitor is switched at each transition.

3 General voltage model for CR DACs

In order to develop a broader model, consider the capacitive array in Figure 2, where the bottom plates of k capacitors are switched at the same time from their initial voltages $V_0[i-1], V_1[i-1] ... V_k[i-1]$ to arbitrary voltage levels $V_0[i], V_1[i] ... V_k[i]$. Again, the principle of charge conservation holds, and the charge of the i-th cycle is the same as the previous cycle:

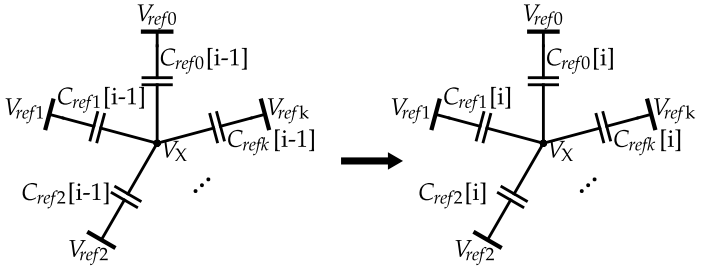

Figure 3: Circuit used to develop the general energy model for CR DACs.

$$Q_X[i] = Q_X[i-1]. \tag{13}$$

By expanding (13) similarly as in (1) and solving for $V_{\mathrm{X}}[i]$, we arrive at (14).

$$V_{\mathrm{X}}[i] = \frac{C_0\left(V_0[i] - V_0[i-1] + V_{\mathrm{X}}[i-1]\right) + \ldots + C_k\left(V_k[i] - V_k[i-1] + V_{\mathrm{X}}[i-1]\right)}{C_0 + C_1 + \ldots + C_k} \tag{14}$$

By collecting the similar terms together, (14) may be rewritten as (15), wheren N indicates the total number of reference sources employed.

$$V_{\mathrm{X}}[i] = \frac{\sum_{j=0}^{N-1} C_j(V_{\mathrm{X}}[i-1] + V_j[i] - V_j[i-1])}{\sum_{j=0}^{N-1} C_j} \tag{15}$$

In order to compute the energy, we assume that the only voltage levels allowed on the bottom plates of the capacitors are the reference voltages. This simplification does not pose any limitation on the analysis, as this happens naturally in a charge-redistribution DAC. These voltages may comprehend any finite number of voltage sources $V_{\mathrm{REF0}}, V_{\mathrm{REF1}} ... V_{\mathrm{REF},k}$, even though practical implementations of charge-redistribution DACs use 2 or 3 (i.e. V_{DD}, ground and the common-mode voltage V_{CM}). In the model for voltage in the DAC, we considered that the capacitances are fixed and that the voltages on their bottom plates vary in time. On the other hand, for the energy model, we will use the assumption of fixed and known voltage levels and compute the variation of the capacitance connected to each one of those voltage sources. This analogy is depicted in Figure 3 and simplifies the calculation of energy when multiple references or capacitors are switched concurrently. Also, this change of standpoint is not harmful to the analysis because we care most about the amount of energy that is spent from V_{REF}, and have limited interest on the distribution of currents among the capacitors.

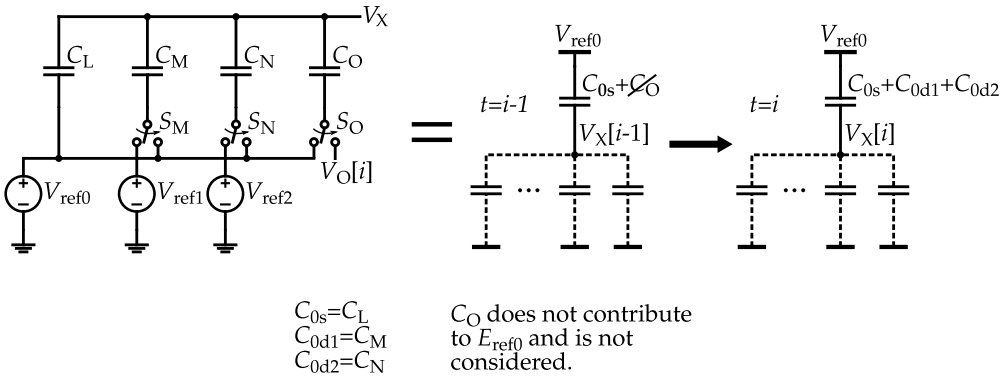

Figure 4: Example of capacitance values assignment for V_{REF0}.

For every state transistion in the DAC, the capacitance connected to a given voltage source $V_{\mathrm{REF},j}$ can be split up into 2 components: $C_{j,\mathrm{s}}$, which is the capacitance that was maintained static since the previous cycle; and $C_{j,\mathrm{d}}$, which is the capacitance that was just connected to the reference voltage in the current cycle. Additionally, $C_{j,\mathrm{d}}$ is further subdivided according to the voltage that was previously applied to the bottom plate of these capacitors, so that $C_{j,\mathrm{d1}}$ corresponds to all the capacitors previously connected to V_{REF1}, $C_{j,\mathrm{d2}}$ corresponds to all the capacitors previously connected to V_{REF2} and so on. Note that if a capacitor is disconnected from the voltage source in the transition of states, it does not contribute to its energy consumption. The assignment of capacitance values is exemplified for V_{REF0} in Figure 4.

At each cycle, the energy drawn from $V_{\mathrm{REF},j}$ is the sum of the energies spent to charge $C_{j,\mathrm{s}}$ and $C_{j,\mathrm{d0}}, C_{j,\mathrm{d1}} ... C_{j,\mathrm{d},k}$. Thus, the energy consumed in the i-th cycle is given by:

$$E_{\mathrm{REF},j}[i] = E_{j,\mathrm{s}}[i] + \sum_{k=0}^{N-1} E_{j,\mathrm{d},k}[i] \tag{16}$$

Following a similar reasoning to that presented in Section 2, (16) may be rewritten as

$$E_{\mathrm{REF},j}[i] = -V_{\mathrm{REF},j} \left(\int_{Q_{C_{j,\mathrm{s}}}[i-1]}^{Q_{C_{j,s}}[i]} \mathrm{d}Q_{C_{j,s}} + \sum_{k=0}^{N-1} \int_{Q_{C_{j,\mathrm{d},k}}[i-1]}^{Q_{C_{j,\mathrm{d},k}}[i]} \mathrm{d}Q_{C_{j,\mathrm{d},k}} \right). \tag{17}$$

By solving and simplifying, we arrive at

$$E_{\mathrm{REF},j}[i] = -V_{\mathrm{REF},j} \left(C_{j,\mathrm{s}} \left(V_{\mathrm{X}}[i-1] - V_{\mathrm{X}}[i] \right) + \sum_{k=0}^{N-1} C_{j,\mathrm{d},k} \left(V_{j,\mathrm{d},k}[i-1] + V_{\mathrm{X}}[i] - V_{\mathrm{X}}[i-1] - V_{\mathrm{REF},j} \right) \right) \tag{18}$$

The total energy consumed during a transition is found summing the contribution of all the reference sources.

$$E_{\text{total}} = \sum_{j=0}^{N-1} E_{\text{REF},j} \tag{19}$$

Therefore, (15), (18) and (19) can be employed in order to find the total energy consumption and the contribution of all the reference sources in the ADC.

The general model requires solving slightly more complicated equations than the proposed simplified model to compute the energy of switching schemes. On the other hand, this general model is easier to be implemented algorithmically on a computer, which makes it a good alternative to automate the computations. One of the advantages of automating the calculations is that it makes easier to extend the analysis to new switching schemes as they appear.