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| Taylor Eby | |
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# Education

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| **BEng, Electrical Engineering**  University of Victoria | September 2012 – August 2017 |
| Took specialization courses in digital signal processing and embedded systems. Graded Strongly in Math courses. Participated in aeronautical engineering student club.  **GPA: 7.09/9.00 (A- equivalent)** | |

# Technologies

**Languages**: C++; C; MATLAB; SQL; bash; Python; Assembly; VHDL

**Simulators**: Altium Designer, KiCad, LTSpice

**Operating Systems**: UNIX, OS X, Windows

**Certifications**: Standard First Aid, Canadian Advanced Amateur Radio Operator License (callsign VE7 JUC)

# Technical Experience

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| **Senior Design Project AutoPot** | May 2017 – August 2017 |
| Automated planter pot to monitor environmental conditions and regulate nutrients, water and light for basil plants. Implemented with an Arduino with C, SQL and Javascript/Perl webpage. | |

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| **Embedded Frequency Counter** | September 2016 – December 2016 |
| Designed a ARM microcontroller to adjust and sample a 555 timer waveform generator and display the measured frequency on LCD screen. Wrote an SPI driver for the LCD screen and configured a DAC and ADC, all in C. | |

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| **Phase Vocoder Application** | May 2016 – August 2016 |
| Phase vocoding application that performed audio effects by processing windowed FFTs of input signal data. Implemented with C++ using JUCE libraries; used Git for version control. | |

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| **Signal Resampling Application** | May 2016 – August 2016 |
| Signal resampling using efficient decimation and interpolation with the ability to multiplex/demultiplex several signals. Implemented with C++ and tested using .wav files. | |

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| **3D Mesh Viewer with Iterative Subdivision** | May 2016 – August 2016 |
| Mesh viewer for Object File Format (OFF) files capable of performing mesh refinement subdivision iteratively. Implemented with C++ using CGAL and OpenGL libraries. | |

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| **Pseudo-Random Number Generator** | May 2015 – August 2015 |
| PRNG for cryptography using hardware division based on Park and Miller algorithm. Implemented with VHDL on Spartan 3E FPGA. | |

# Work Experience

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| **Hardware Designer Co-op**  Nokia | January 2017 – April 2017 |
| * Performed electrical and optical hardware testing and verification for Nokia products with laboratory equipment (i.e. high frequency and bandwidth oscilloscope, multimeter, soldering iron, traffic generator). * Verified I2C, SPI, UART communication protocols. * Gained experience with Linux, Python and TCL. * Performed hardware jitter analysis testing to meet industry ITU-T OTU2e requirements. | |

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| **Client Support Technician Co-op**  Canada’s Michael Smith Genome Sciences Centre | September 2014 – April 2015 |
| * Provided first tier support and systems administration for an organization of ~300 employees primarily using JIRA ticket management. * Researched mass virtualization solutions to preserve legacy software for microbiology lab machines. * Gained experience with command-line UNIX and bash. * Tracked and organized logistics of organization wide OS update. | |

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| **Electrical Co-op Student**  UVic Aero | January 2014 – May 2014 |
| * Worked with an undergraduate team in a trainee role to continue work on an existing unmanned aerial vehicle, which won 3rd place at the Unmanned Systems Canada competition in 2014. * Transcribed a PCB design from a blueprint using Altium Designer, which was used in the avionics system. * Assisted with setup of omnidirectional and directional tracking antennas. | |