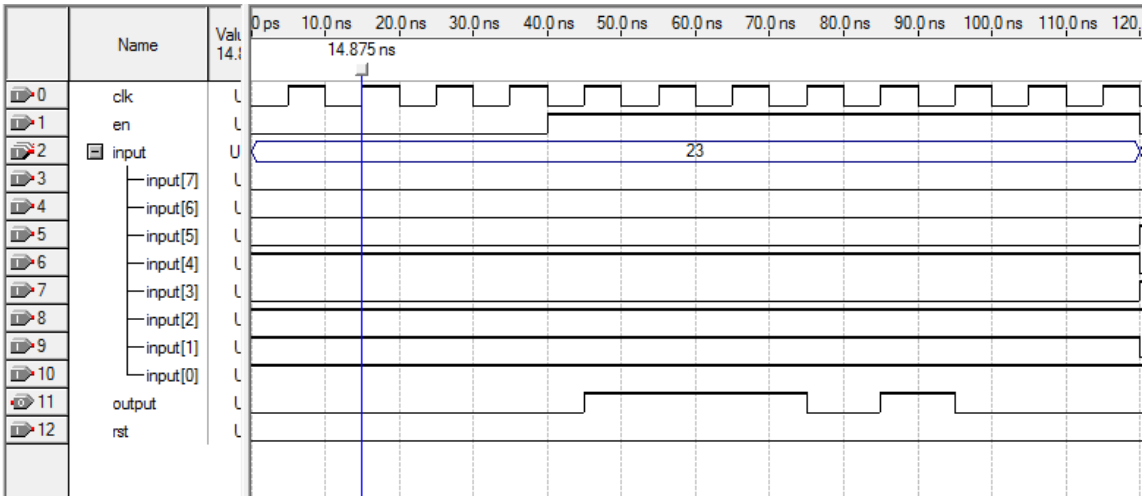
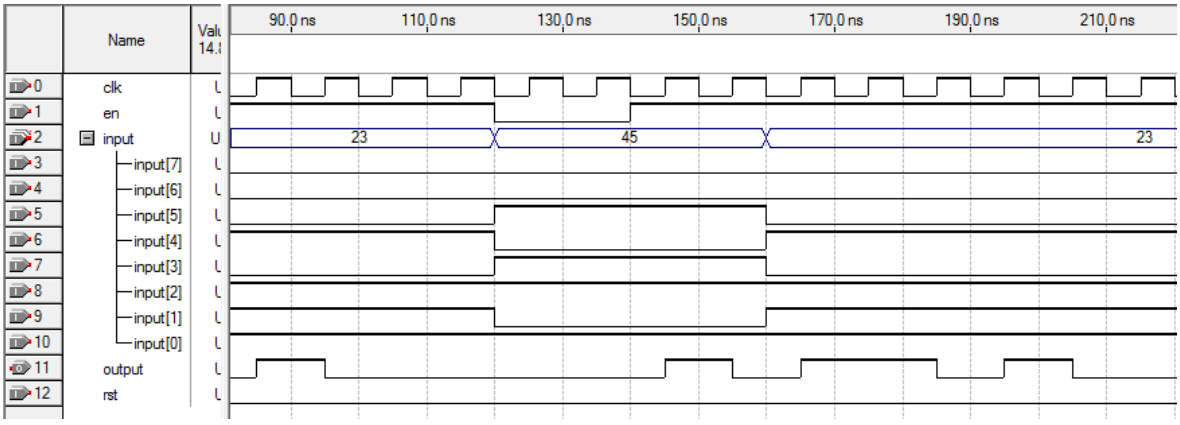
After running some tests on the parallel to serial shift register, I believe the entity is working like it should be. On a rising clock edge, if the enable is false, the entity takes and clocks in the input. If the enable is true, the entity begins shifting the loaded data down 1 bit and the output takes in the 0^{th} bit of that data every time.

Now, there is no counter to keep track of when this data is finished being transferred. So its possible that the data is being corrupted by our python code, or other glue logic in the design. So I'd have to do more tests to give a definitive answer.

I've attached some screenshots below of the parallel to serial shift register working properly.



In this screenshot, the enable is false for 4 clock cycles to show the data in this case (23) is being loaded. The output starts to appear on the 5^{th} rising clock edge after the enable goes true. The output appears as all bits appearing backwards from the original data since it is capturing the 0^{th} bit after each right shift.



In the above example, I have changed the input to 45 and the same behavior is exhibited.

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