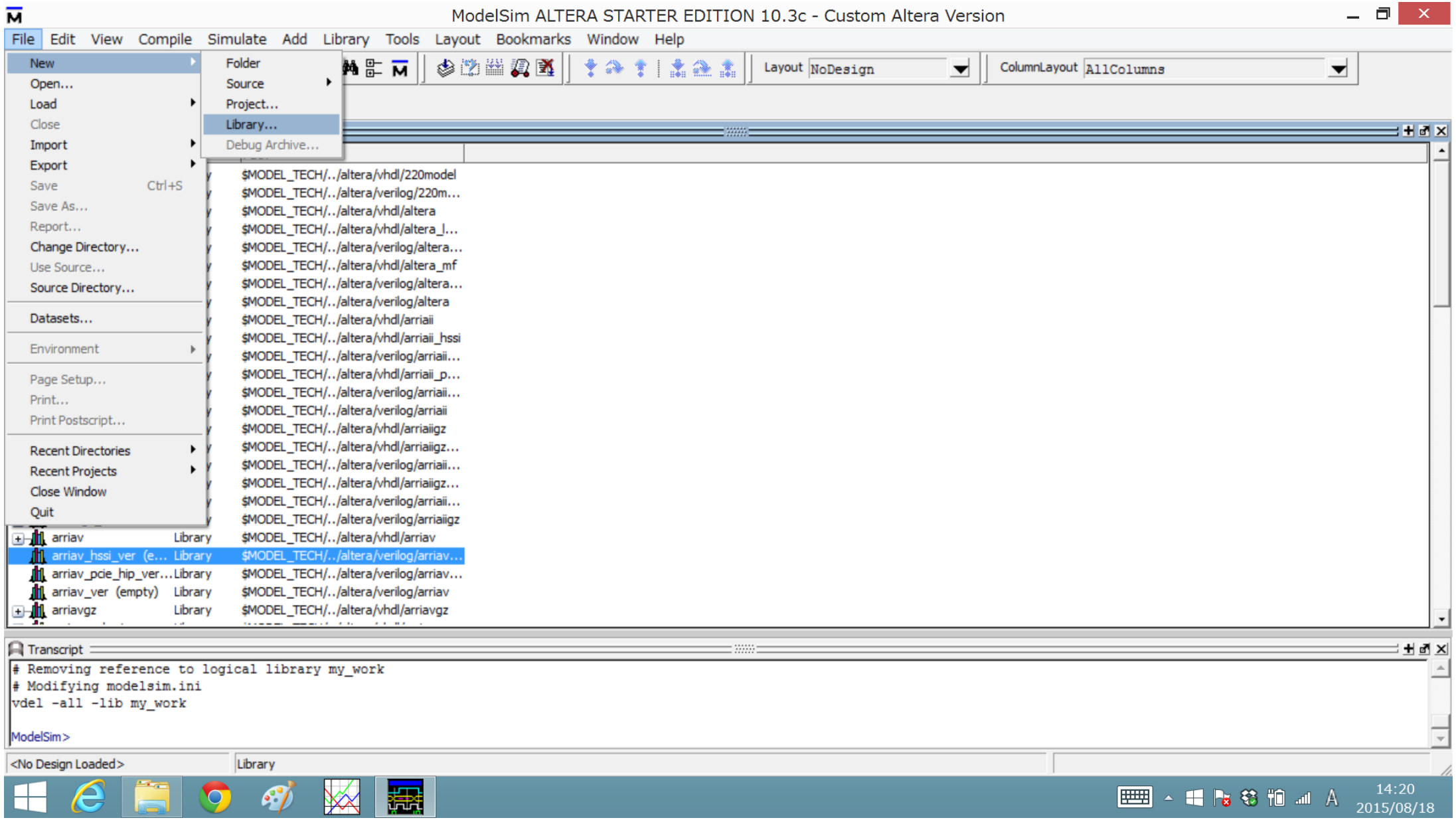
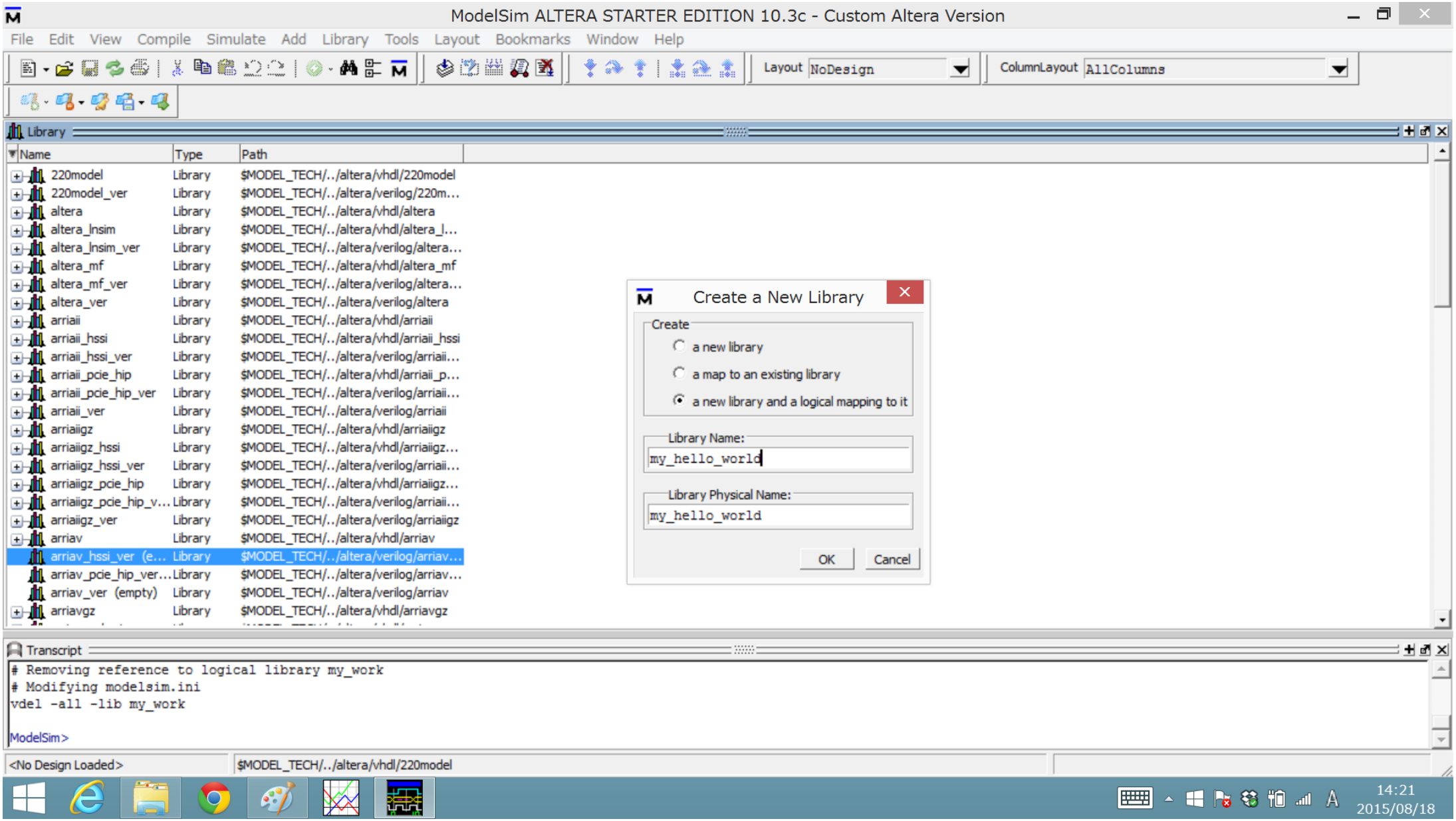
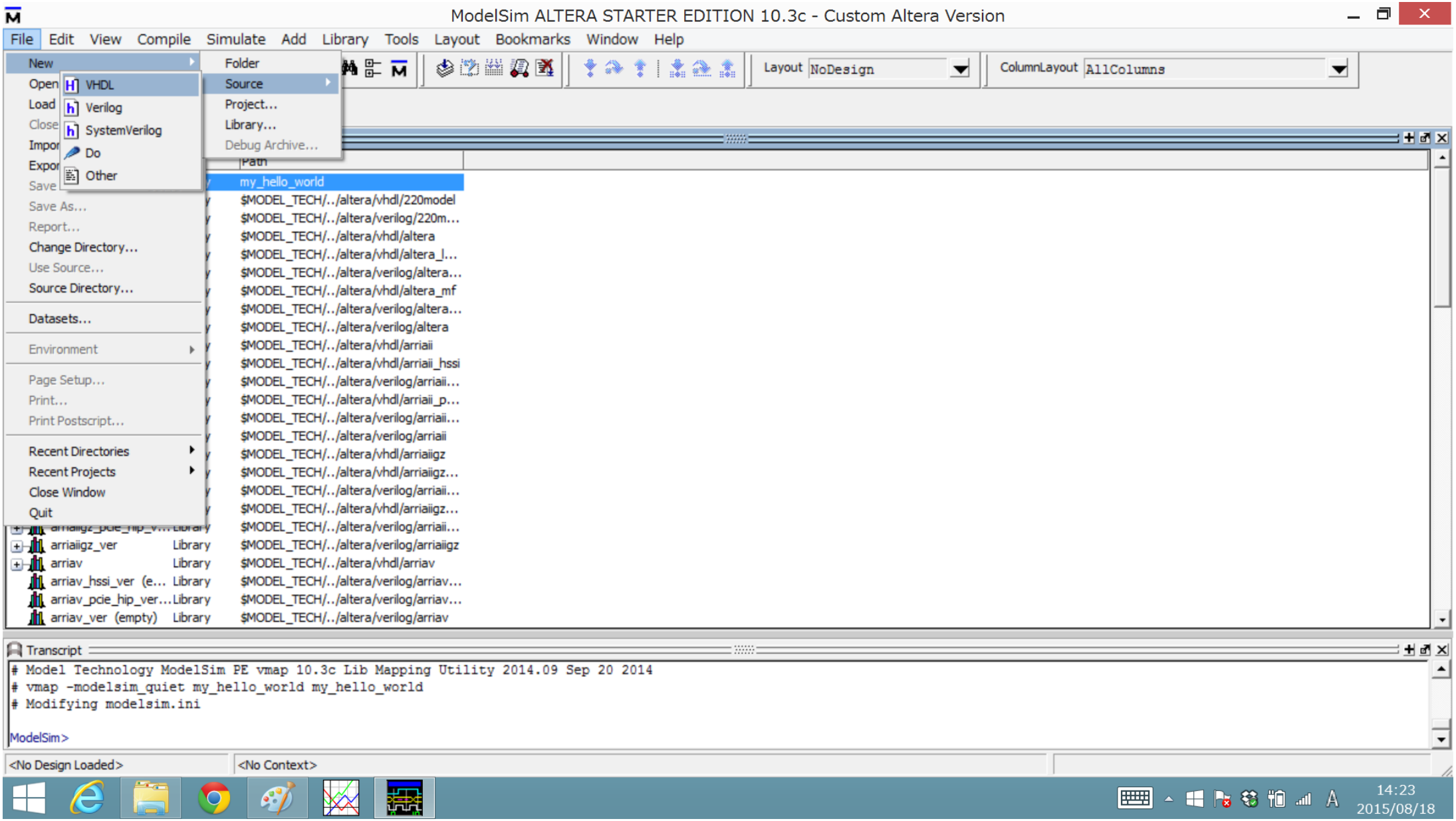
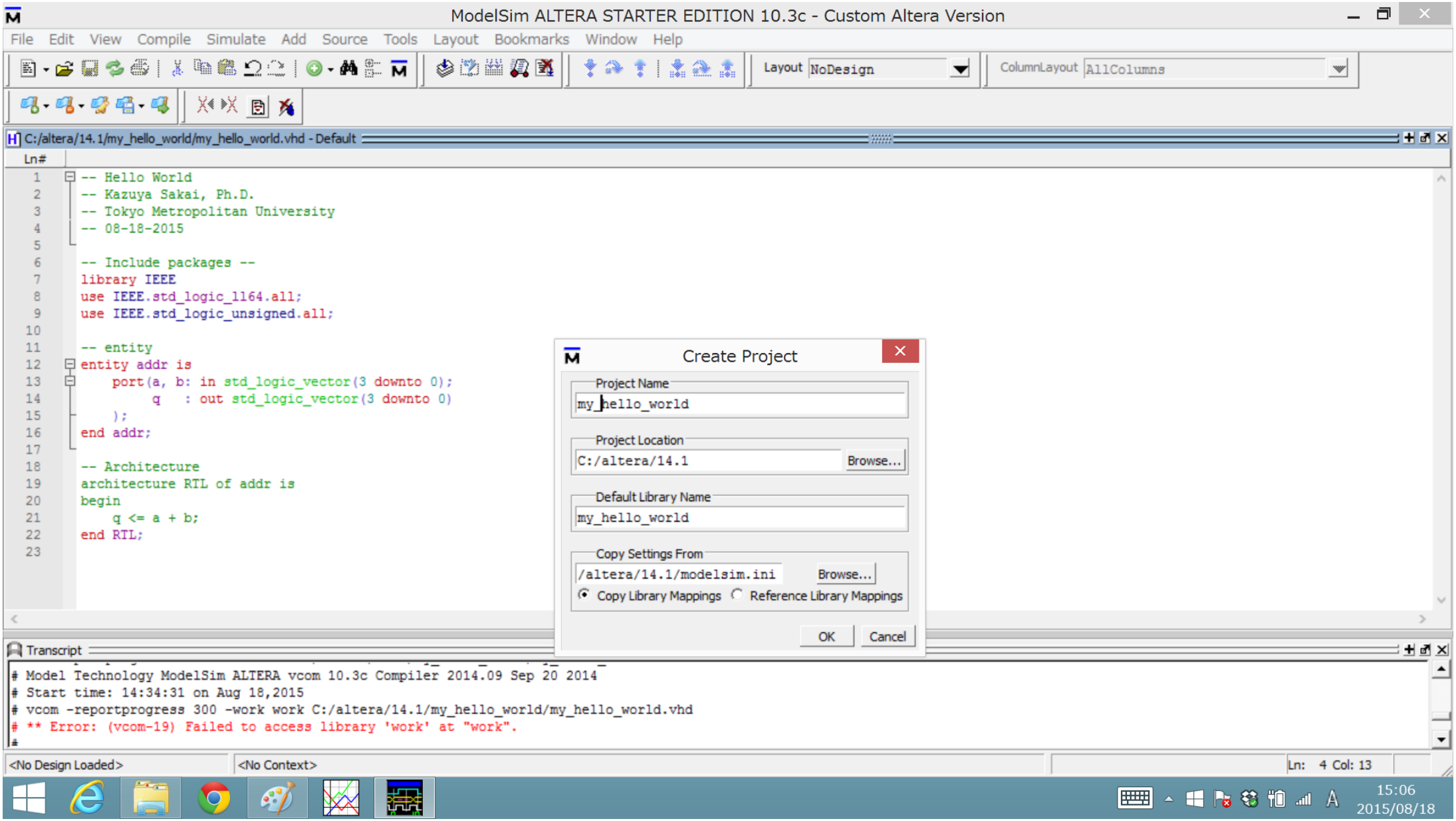
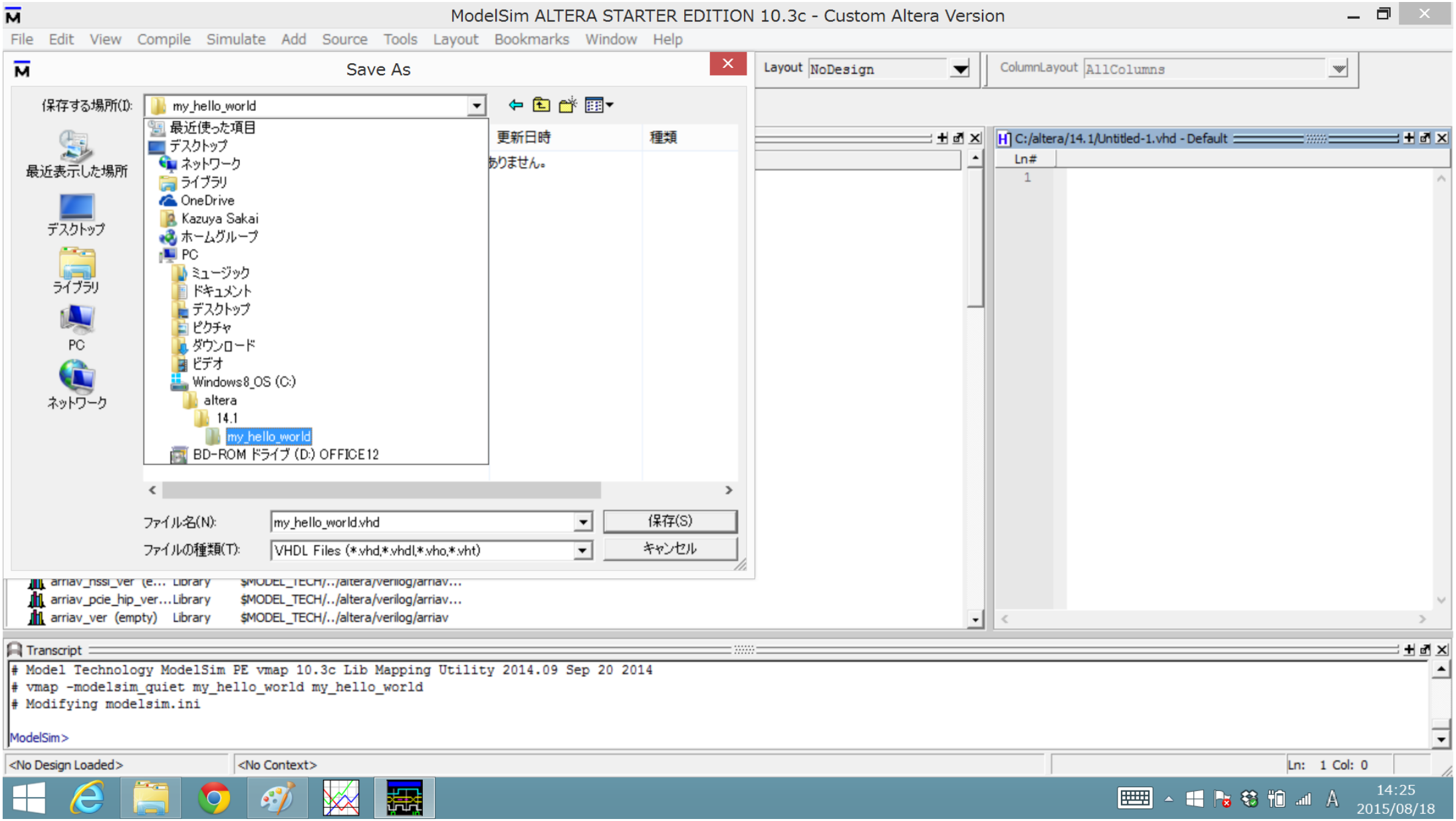
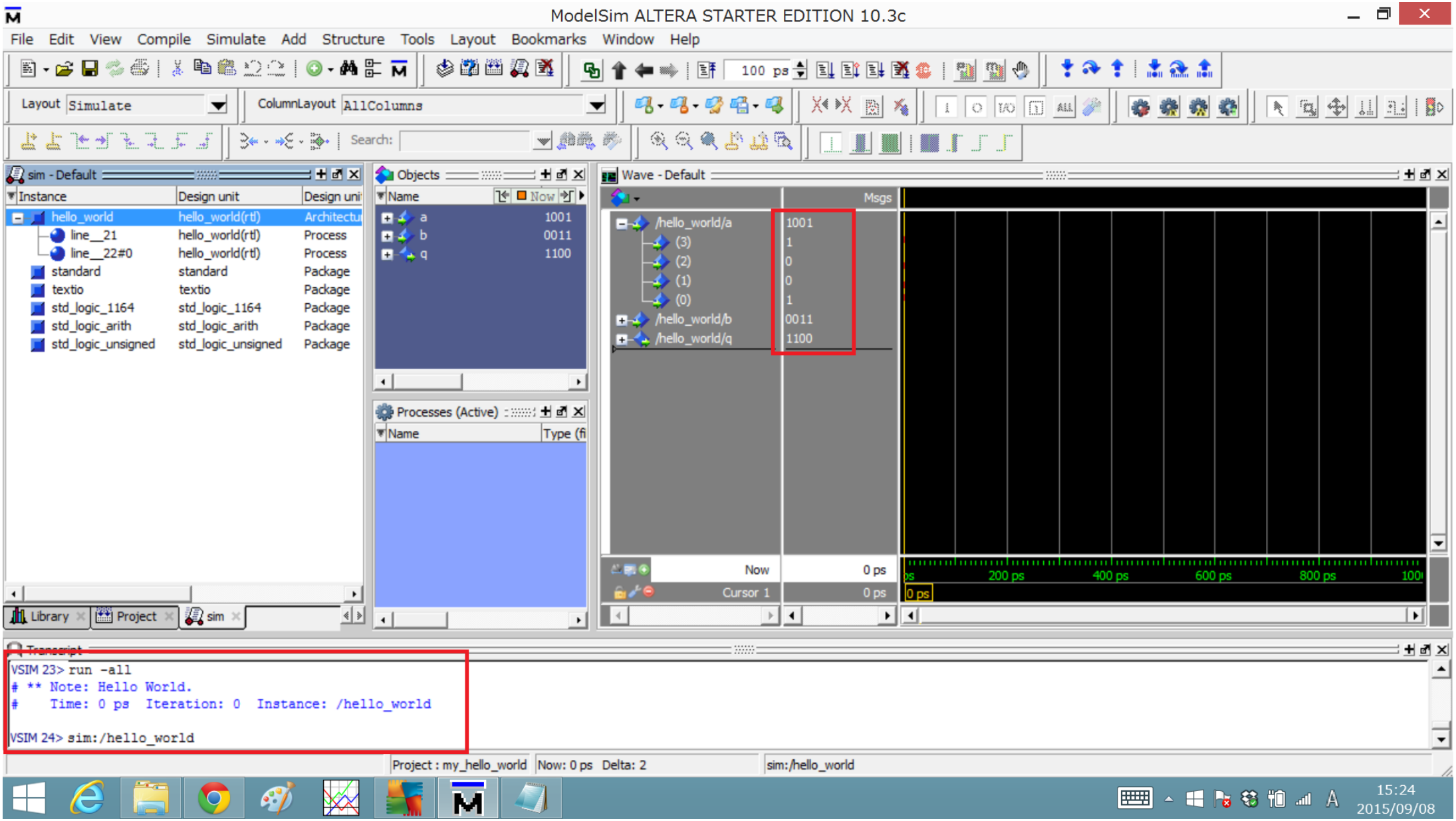

ModelSim ALTERA STARTER EDITION 10.3c - Custom Altera Version
File Edit View Compile Simulate Add Library Tools Layout Bookmarks Window Help
New
Open...
Load
Close
Import
Export
Save Ctrl+S
Save As...
Report...
Change Directory...
Use Source...
Source Directory...
Datasets...
Environment
Page Setup...
Print...
Print Postscript...
Recent Directories
Recent Projects
Close Window
Quit
Folder
Source
Project...
Library...
Debug Archive...
Layout NoDesign
ColumnLayout AllColumns
$MODEL_TECH/../altera/vhdl/220model
$MODEL_TECH/../altera/verilog/220m...
$MODEL_TECH/../altera/vhdl/altera
$MODEL_TECH/../altera/vhdl/altera_l...
$MODEL_TECH/../altera/verilog/altera...
$MODEL_TECH/../altera/vhdl/altera_mf
$MODEL_TECH/../altera/verilog/altera...
$MODEL_TECH/../altera/verilog/altera
$MODEL_TECH/../altera/vhdl/arriaii
$MODEL_TECH/../altera/vhdl/arriaii_hssi
$MODEL_TECH/../altera/verilog/arriaii...
$MODEL_TECH/../altera/vhdl/arriaii_p...
$MODEL_TECH/../altera/verilog/arriaii...
$MODEL_TECH/../altera/verilog/arriaii
$MODEL_TECH/../altera/vhdl/arriaiigz
$MODEL_TECH/../altera/vhdl/arriaiigz...
$MODEL_TECH/../altera/verilog/arriaii...
$MODEL_TECH/../altera/vhdl/arriaiigz...
$MODEL_TECH/../altera/verilog/arriaii...
$MODEL_TECH/../altera/verilog/arriaiigz
arriav Library $MODEL_TECH/../altera/vhdl/arriav
arriav_hssi_ver (e... Library $MODEL_TECH/../altera/verilog/arriav...
arriav_pcie_hip_ver... Library $MODEL_TECH/../altera/verilog/arriav...
arriav_ver (empty) Library $MODEL_TECH/../altera/verilog/arriav
arriavgz Library $MODEL_TECH/../altera/vhdl/arriavgz
Transcript
Removing reference to logical library my_work
Modifying modelsim.ini
vdel -all -lib my_work
ModelSim>
<No Design Loaded>
Library
14:20
2015/08/18


ModelSim ALTERA STARTER EDITION 10.3c - Custom Altera Version
File Edit View Compile Simulate Add Library Tools Layout Bookmarks Window Help
Layout NoDesign
ColumnLayout AllColumns
Library
Name Type Path
220model Library $MODEL_TECH/../altera/vhdl/220model
220model_ver Library $MODEL_TECH/../altera/verilog/220m...
altera Library $MODEL_TECH/../altera/vhdl/altera
altera_lnsim Library $MODEL_TECH/../altera/vhdl/altera_l...
altera_lnsim_ver Library $MODEL_TECH/../altera/verilog/altera...
altera_mf Library $MODEL_TECH/../altera/vhdl/altera_mf
altera_mf_ver Library $MODEL_TECH/../altera/verilog/altera...
altera_ver Library $MODEL_TECH/../altera/verilog/altera
arriaii Library $MODEL_TECH/../altera/vhdl/arriaii
arriaii_hssi Library $MODEL_TECH/../altera/vhdl/arriaii_hssi
arriaii_hssi_ver Library $MODEL_TECH/../altera/verilog/arriaii...
arriaii_pcie_hip Library $MODEL_TECH/../altera/vhdl/arriaii_p...
arriaii_pcie_hip_ver Library $MODEL_TECH/../altera/verilog/arriaii...
arriaii_ver Library $MODEL_TECH/../altera/verilog/arriaii
arriaiigz Library $MODEL_TECH/../altera/vhdl/arriaiigz
arriaiigz_hssi Library $MODEL_TECH/../altera/vhdl/arriaiigz...
arriaiigz_hssi_ver Library $MODEL_TECH/../altera/verilog/arriaii...
arriaiigz_pcie_hip Library $MODEL_TECH/../altera/vhdl/arriaiigz...
arriaiigz_pcie_hip_v... Library $MODEL_TECH/../altera/verilog/arriaii...
arriaiigz_ver Library $MODEL_TECH/../altera/verilog/arriaiigz
arriav Library $MODEL_TECH/../altera/vhdl/arriav
arriav_hssi_ver (e... Library $MODEL_TECH/../altera/verilog/arriav...
arriav_pcie_hip_ver... Library $MODEL_TECH/../altera/verilog/arriav...
arriav_ver (empty) Library $MODEL_TECH/../altera/verilog/arriav
arriavgz Library $MODEL_TECH/../altera/vhdl/arriavgz
Create a New Library
Create
a new library
a map to an existing library
a new library and a logical mapping to it
Library Name:
my_hello_world
Library Physical Name:
my_hello_world
OK
Cancel
Transcript
Removing reference to logical library my_work
Modifying modelsim.ini
vdel -all -lib my_work
ModelSim>
<No Design Loaded>
$MODEL_TECH/../altera/vhdl/220model
14:21
2015/08/18


ModelSim ALTERA STARTER EDITION 10.3c - Custom Altera Version
File Edit View Compile Simulate Add Library Tools Layout Bookmarks Window Help
New
Open
Load
Close
Impor
Expor
Save
Save As...
Report...
Change Directory...
Use Source...
Source Directory...
Datasets...
Environment
Page Setup...
Print...
Print Postscript...
Recent Directories
Recent Projects
Close Window
Quit
VHDL
Verilog
SystemVerilog
Do
Other
Folder
Source
Project...
Library...
Debug Archive...
Layout NoDesign
ColumnLayout AllColumns
Path
my_hello_world
$MODEL_TECH/../altera/vhdl/220model
$MODEL_TECH/../altera/verilog/220m...
$MODEL_TECH/../altera/vhdl/altera
$MODEL_TECH/../altera/vhdl/altera_l...
$MODEL_TECH/../altera/verilog/altera...
$MODEL_TECH/../altera/vhdl/altera_mf
$MODEL_TECH/../altera/verilog/altera...
$MODEL_TECH/../altera/verilog/altera
$MODEL_TECH/../altera/vhdl/arriaii
$MODEL_TECH/../altera/vhdl/arriaii_hssi
$MODEL_TECH/../altera/verilog/arriaii...
$MODEL_TECH/../altera/vhdl/arriaii_p...
$MODEL_TECH/../altera/verilog/arriaii...
$MODEL_TECH/../altera/verilog/arriaii
$MODEL_TECH/../altera/vhdl/arriaiigz
$MODEL_TECH/../altera/vhdl/arriaiigz...
$MODEL_TECH/../altera/verilog/arriaii...
$MODEL_TECH/../altera/vhdl/arriaiigz...
$MODEL_TECH/../altera/verilog/arriaii...
arriaiigz_ver Library $MODEL_TECH/../altera/verilog/arriaiigz
arriav Library $MODEL_TECH/../altera/vhdl/arriav
arriav_hssi_ver (e... Library $MODEL_TECH/../altera/verilog/arriav...
arriav_pcie_hip_ver... Library $MODEL_TECH/../altera/verilog/arriav...
arriav_ver (empty) Library $MODEL_TECH/../altera/verilog/arriav
Transcript
Model Technology ModelSim PE vmap 10.3c Lib Mapping Utility 2014.09 Sep 20 2014
vmap -modelsim_quiet my_hello_world my_hello_world
Modifying modelsim.ini
ModelSim>
<No Design Loaded>
<No Context>
14:23
2015/08/18


ModelSim ALTERA STARTER EDITION 10.3c - Custom Altera Version
File Edit View Compile Simulate Add Source Tools Layout Bookmarks Window Help
Layout NoDesign
ColumnLayout AllColumns
C:/altera/14.1/my_hello_world/my_hello_world.vhd - Default
Ln#
1 -- Hello World
2 -- Kazuya Sakai, Ph.D.
3 -- Tokyo Metropolitan University
4 -- 08-18-2015
5
6 -- Include packages --
7 library IEEE
8 use IEEE.std_logic_1164.all;
9 use IEEE.std_logic_unsigned.all;
10
11 -- entity
12 entity addr is
13 port(a, b: in std_logic_vector(3 downto 0);
14 q : out std_logic_vector(3 downto 0)
15);
16 end addr;
17
18 -- Architecture
19 architecture RTL of addr is
20 begin
21 q <= a + b;
22 end RTL;
23
Create Project
Project Name
my_hello_world
Project Location
C:/altera/14.1
Browse...
Default Library Name
my_hello_world
Copy Settings From
/altera/14.1/modelsim.ini
Browse...
Copy Library Mappings
Reference Library Mappings
OK
Cancel
Transcript
Model Technology ModelSim ALTERA vcom 10.3c Compiler 2014.09 Sep 20 2014
Start time: 14:34:31 on Aug 18,2015
vcom -reportprogress 300 -work work C:/altera/14.1/my_hello_world/my_hello_world.vhd
** Error: (vcom-19) Failed to access library 'work' at "work".
#
<No Design Loaded>
<No Context>
Ln: 4 Col: 13
15:06
2015/08/18


ModelSim ALTERA STARTER EDITION 10.3c - Custom Altera Version
File Edit View Compile Simulate Add Source Tools Layout Bookmarks Window Help
Save As
保存する場所(I):
my_hello_world
最近使った項目
デスクトップ
ネットワーク
ライブラリ
OneDrive
Kazuya Sakai
ホームグループ
PC
ミュージック
ドキュメント
デスクトップ
ピクチャ
ダウンロード
ビデオ
Windows8_OS (C:)
altera
14.1
my_hello_world
BD-ROM ドライブ (D:) OFFICE12
最近表示した場所
デスクトップ
ライブラリ
PC
ネットワーク
更新日時
種類
ありません。
ファイル名(N):
my_hello_world.vhd
保存(S)
ファイルの種類(T):
VHDL Files (*.vhd,*.vhdl,*.vho,*.vht)
キャンセル
Layout NoDesign
ColumnLayout AllColumns
C:/altera/14.1/Untitled-1.vhd - Default
Ln#
1
arriav_pcie_hip_ver... Library $MODEL_TECH/../altera/verilog/arriav...
arriav_ver (empty) Library $MODEL_TECH/../altera/verilog/arriav
Transcript
Model Technology ModelSim PE vmap 10.3c Lib Mapping Utility 2014.09 Sep 20 2014
vmap -modelsim_quiet my_hello_world my_hello_world
Modifying modelsim.ini
ModelSim>
<No Design Loaded>
<No Context>
Ln: 1 Col: 0
14:25
2015/08/18


ModelSim ALTERA STARTER EDITION 10.3c
File Edit View Compile Simulate Add Structure Tools Layout Bookmarks Window Help
sim - Default
Instance Design unit Design uni
hello_world hello_world(rtl) Architectu
line__21 hello_world(rtl) Process
line__22#0 hello_world(rtl) Process
standard standard Package
textio textio Package
std_logic_1164 std_logic_1164 Package
std_logic_arith std_logic_arith Package
std_logic_unsigned std_logic_unsigned Package
Objects
Name
a 1001
b 0011
q 1100
Processes (Active)
Name Type (fi
Wave - Default
Msgs
/hello_world/a 1001
(3) 1
(2) 0
(1) 0
(0) 1
/hello_world/b 0011
/hello_world/q 1100
Now 0 ps
Cursor 1 0 ps
200 ps 400 ps 600 ps 800 ps
0 ps
Library Project sim
Transcript
VSIM 23> run -all
** Note: Hello World.
Time: 0 ps Iteration: 0 Instance: /hello_world
VSIM 24> sim:/hello_world
Project : my_hello_world Now: 0 ps Delta: 2 sim:/hello_world
15:24
2015/09/08