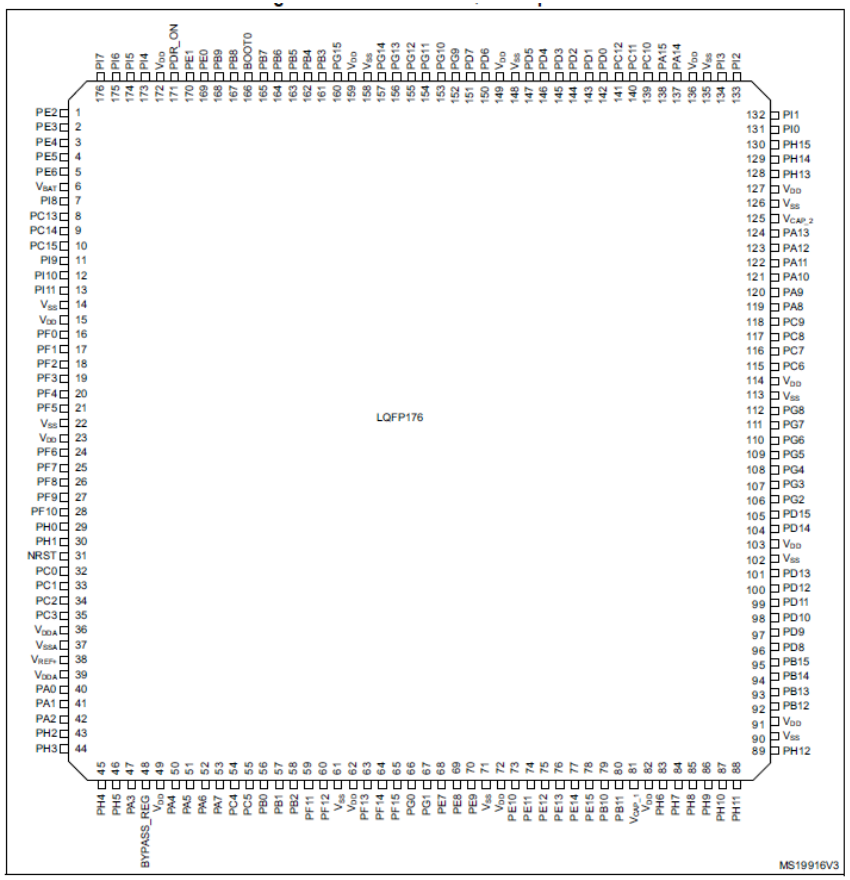
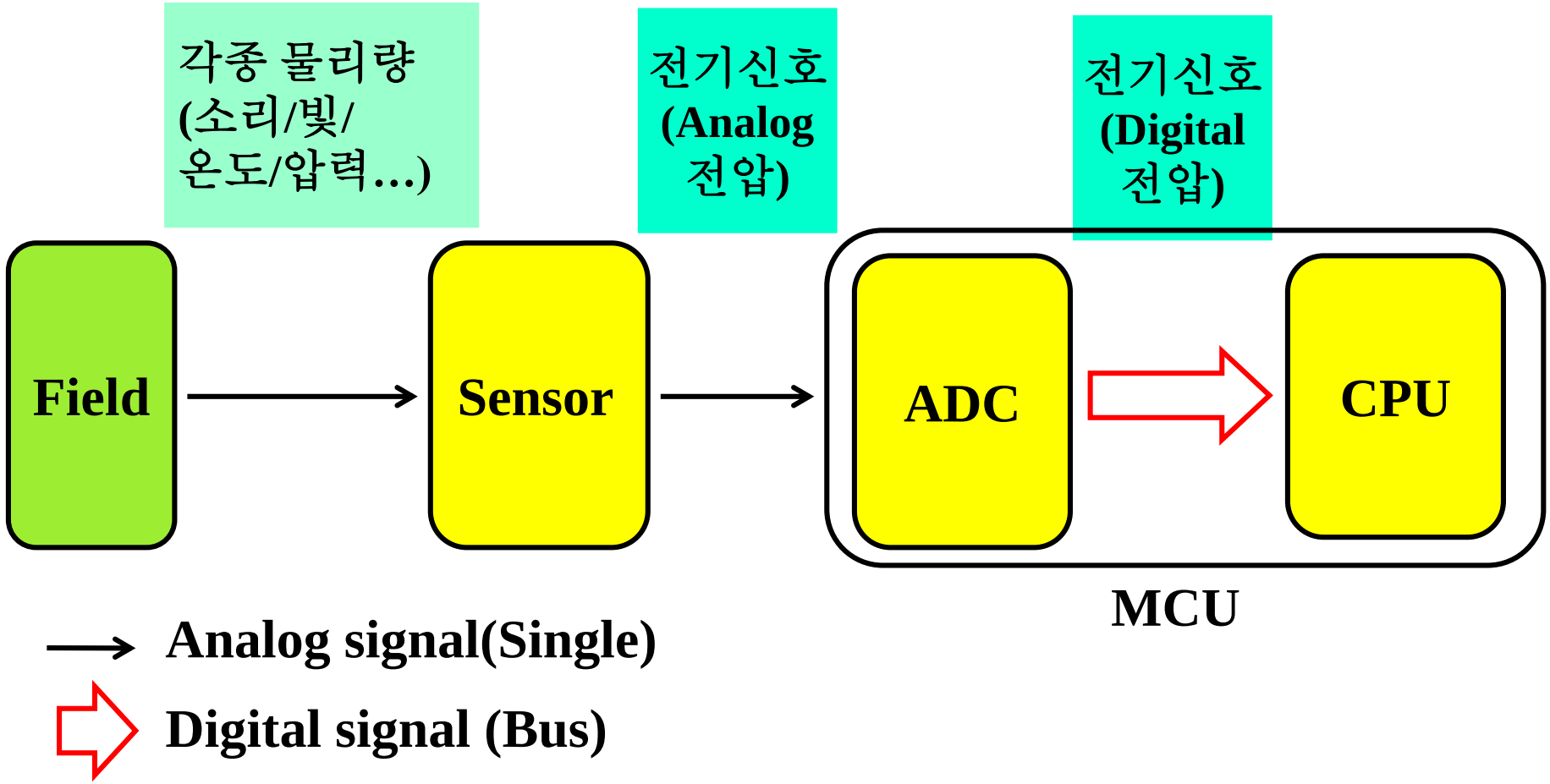
STM32F407 ADC



한국산업기술대학교 메카트로닉스공학과
마이크로컴퓨터응용
담당교수: 남윤석

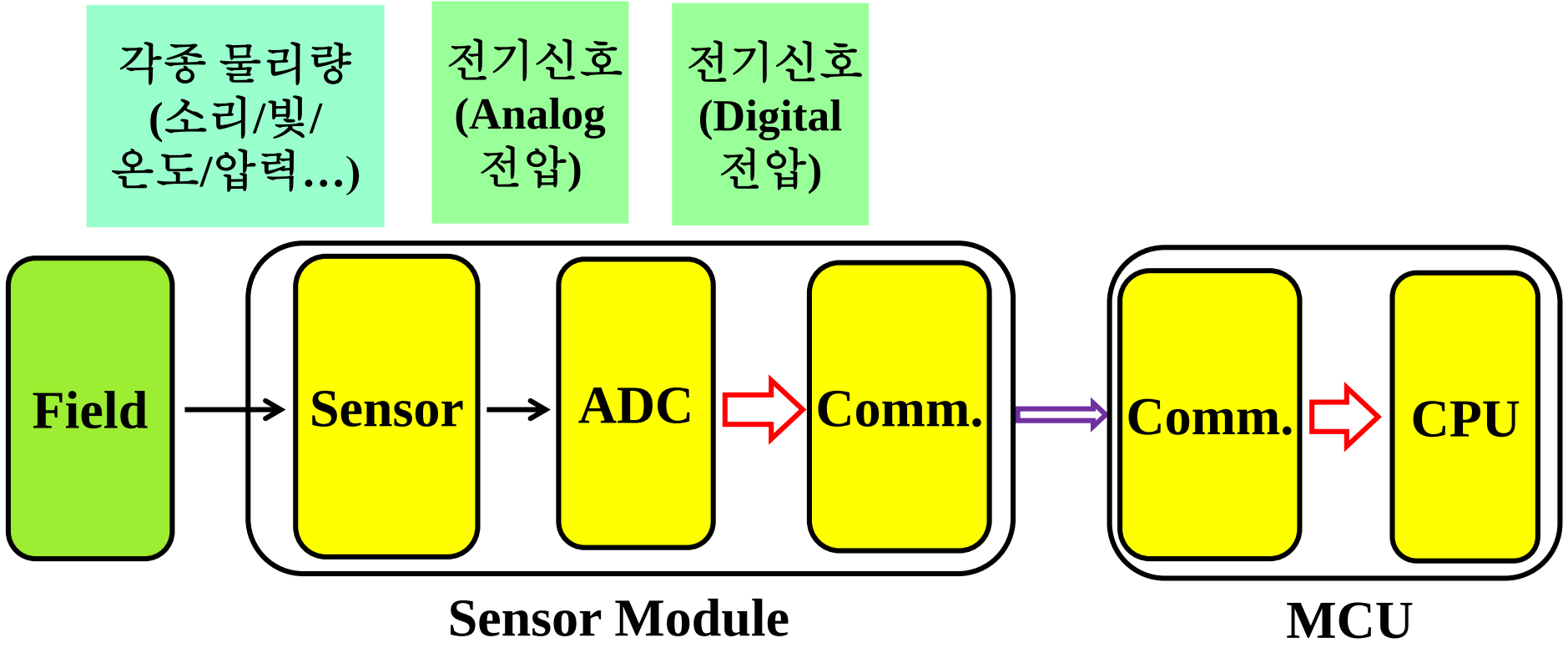
0.1 Sensor Interface 구조

(1) Sensor-ADC 이용



0.1 Sensor Interface 구조

(2) Communication 이용



Analog signal(Single)

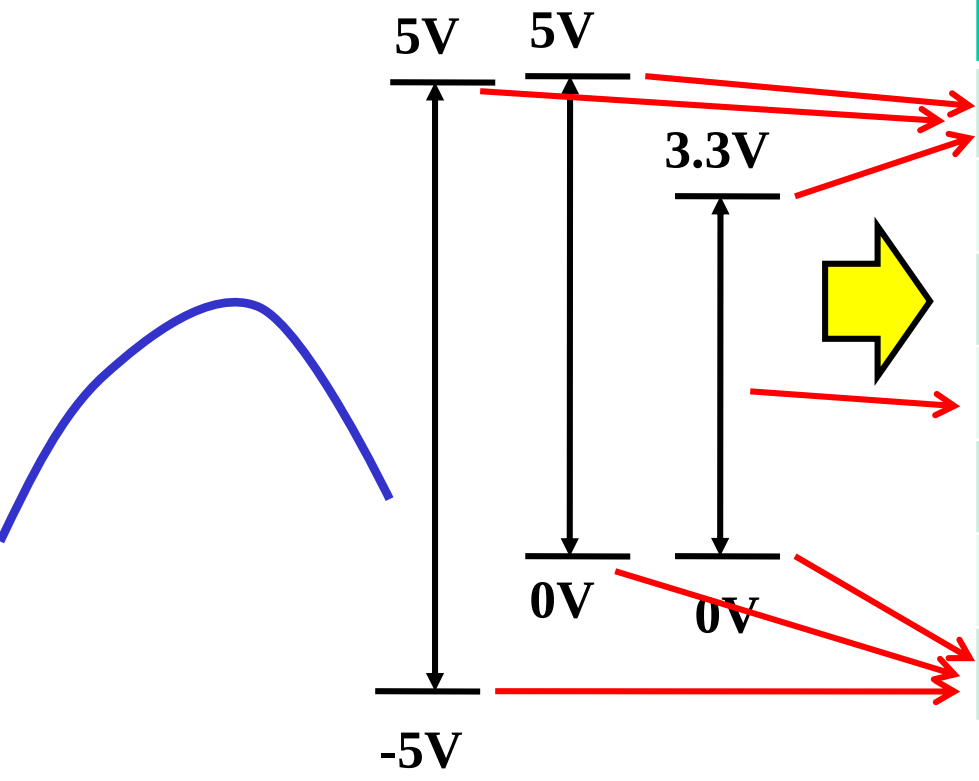
Serial Communication(I2C, SPI, USART)

Digital signal (Bus)

0.2 A/D 컨버터(converter) 정의

- 정의: **Analog signal**을 **Digital signal**로 **Conversion**(변환)하는 회로(모듈)
- 변환시 고려해야할 요소

  : **Analog** 신호전압범위, 디지털신호표현크기(bit 수)



8bit	10bit	12bit
0b11111111	0b1111111111	0b111111111111
0b11111110	0b1111111110	0b111111111110
0b11111101	0b1111111101	0b111111111101
……	……..	……..
0b00000010	0b0000000010	0b000000000010
0b00000001	0b0000000001	0b000000000001
0b00000000	0b0000000000	0b000000000000

0.3 ADC(A/D converter) 와 DAC(D/A converter)

- ADC

- DAC

0.4 A/D 컨버터(converter) 주요 용어

- **A/D 컨버터 중요 용어: 입력전압 범위, 분해능**

- 입력전압 범위: 0~5V, 0~12V, -5~+5V 등

- 분해능 : 8 bit, 10bit, 12bit, 14bit, 16bit 등

*** 분해능이란? 입력값을 얼마나 세밀하게 변환할 수 있는가를 나타내는 수치**

예)입력 전압 범위가 0~5V이고, 분해능이 10bit 이면 최소 변환 전압 값은?

입력전압 영역(5=5-0)을 210 = 1024 로 나눈 값**

5/1024 = 0.005V

- **A/D 컨버터 과정**

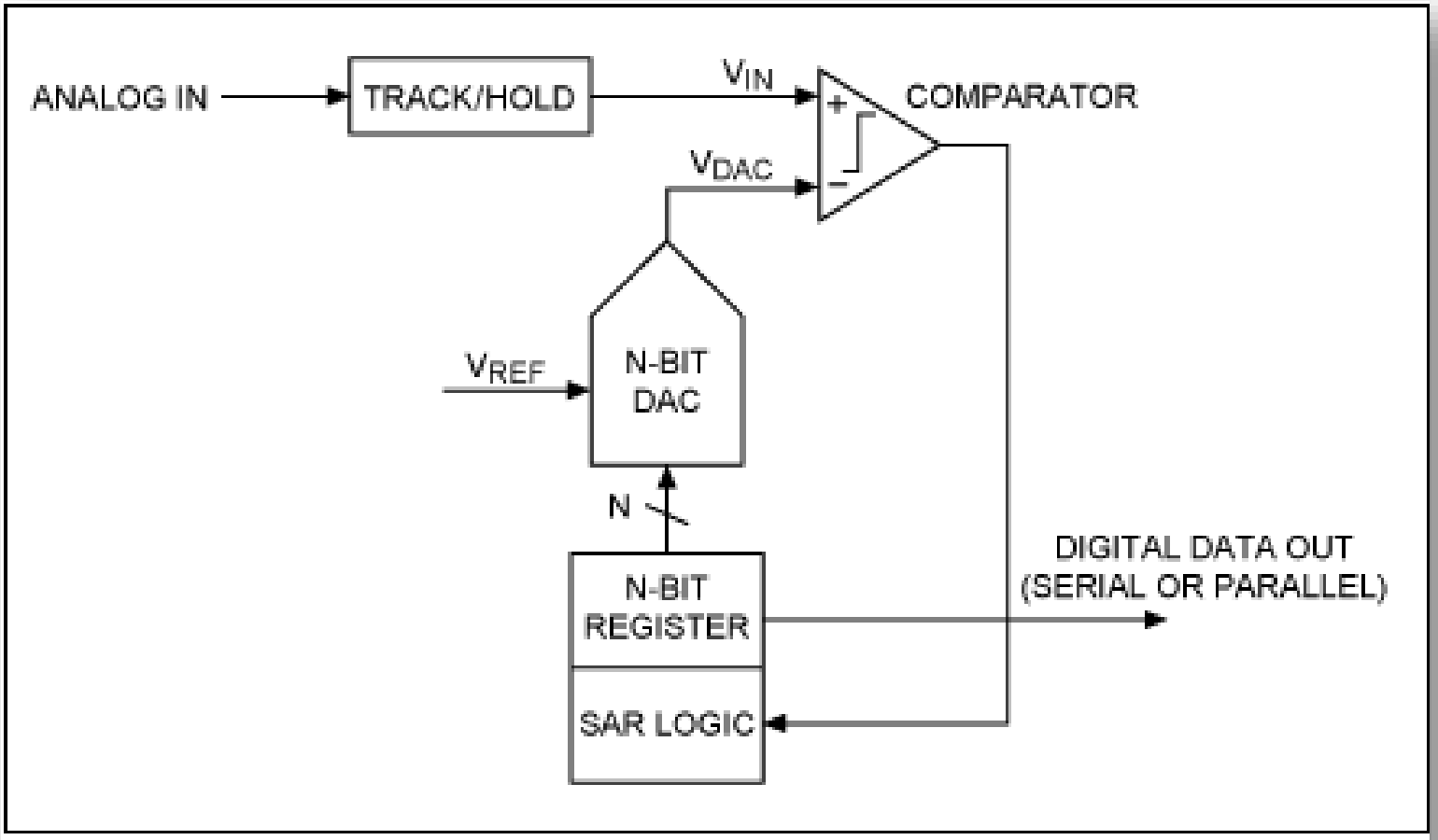
(예1) 0~5V(입력전압범위) 아날로그 신호 입력 : 2비트(분해능) 디지털 값으로 변환

0V : 00B
5 x (1/3)V : 01B
5 x (2/3)V : 10B
5V : 11B

(예2) 0~5V (입력전압범위) 아날로그 신호 입력 : 8비트 (분해능) 디지털 값으로 변환

0V : 0000 0000B
1.25V : 0011 1111B
2.5V : 0111 1111B
3.75V : 1011 1111B
5V : 1111 1111B

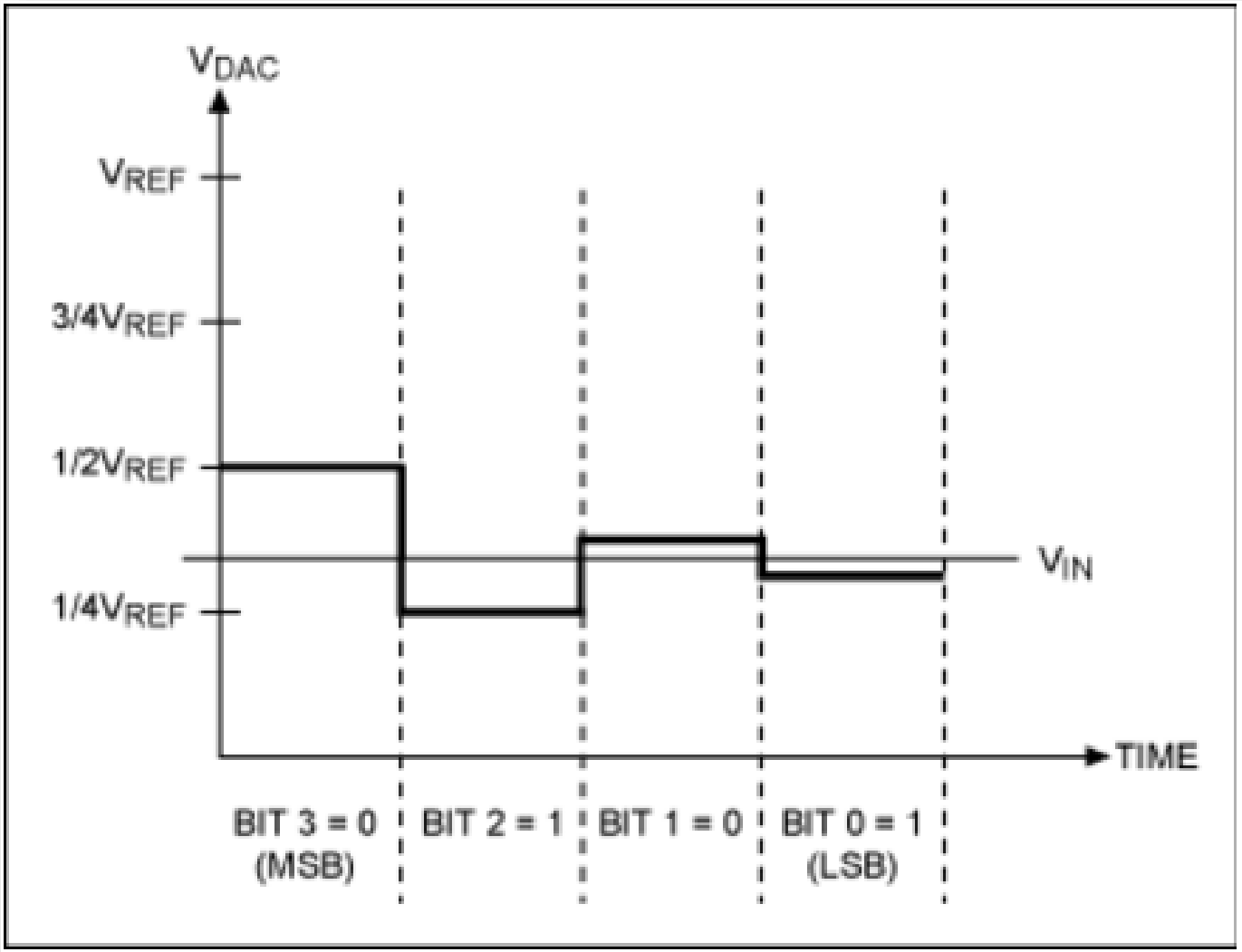
1. STM32F407 ADC 개요



Simplified N-bit SAR ADC architecture.

- **SAR(Successive-approximation-register) ADC Architecture**
- **12 bit Resolution**
- **Ref 전압 Max 3.3V**

* SAR type ADC의 동작 예

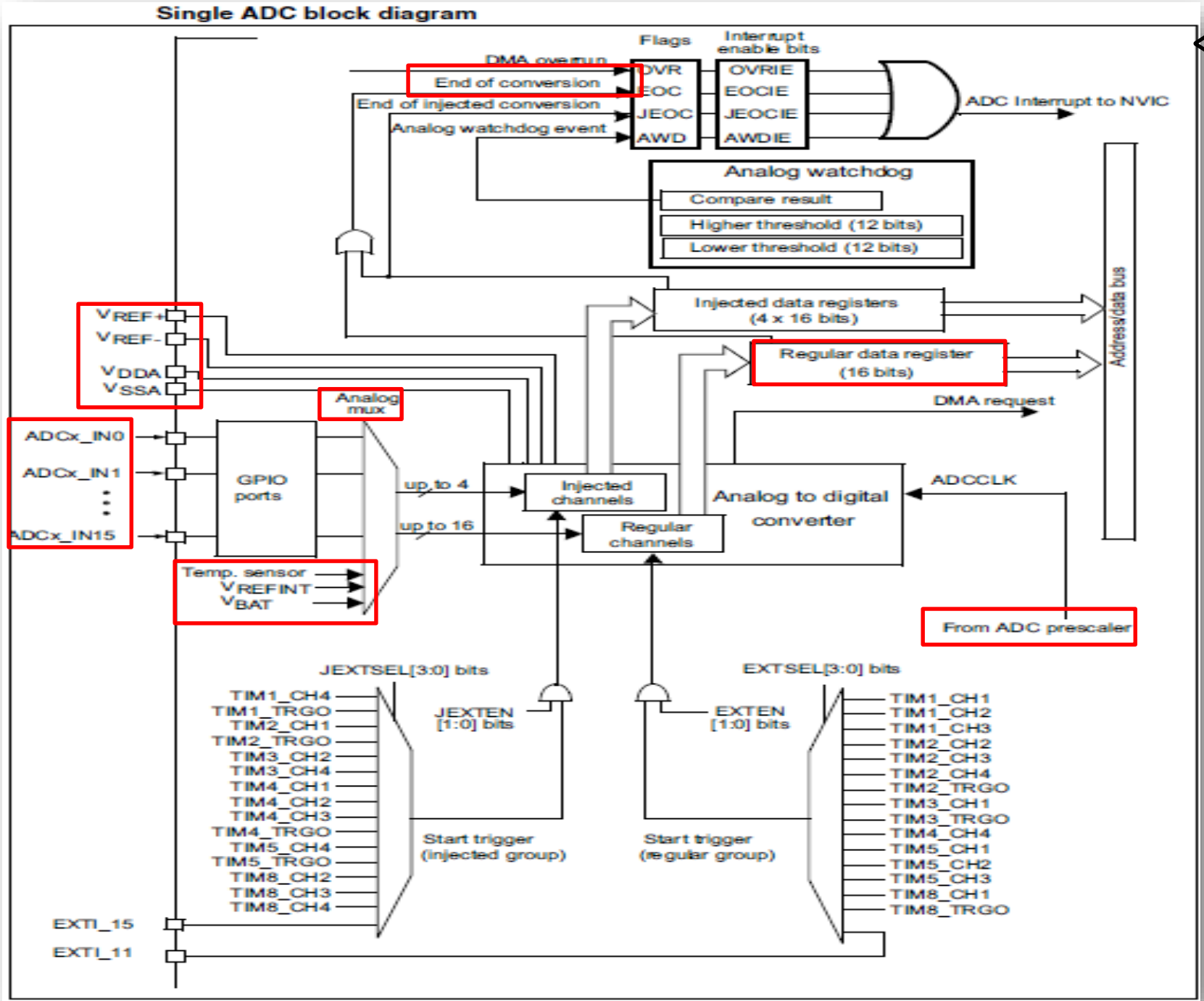


SAR operation (4-bit ADC example).

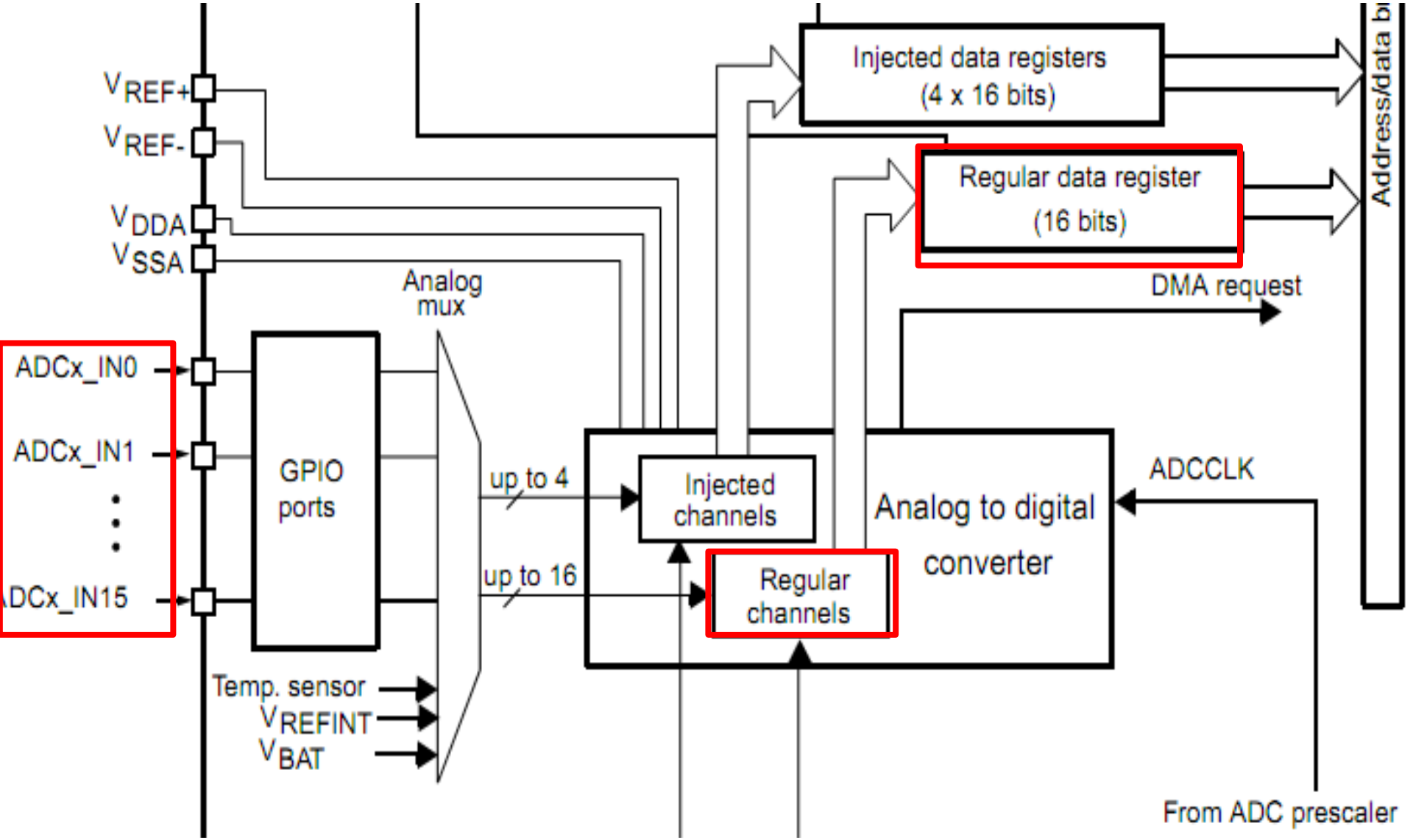
- 총 **19**개 아날로그 신호 입력채널**:**
  - 외부입력 **16**개
  - 내부입력 **3**개**(Vbat, VrefInt, TempSensor)**
- 변환 종료시 또는 아날로그 워치독 이벤트 발생시 인터럽트 발생
- 여러 변환 모드 제공**:** 단일**(single),** 연속**(continuous),** 스캔**(scan),** 불연속**(discontinuous)** 변환 모드
- 변환결과값 저장**:** left or right-aligned 16-bit data register
- **ADC** 공급 전압 요구사항 **: Full speed** 상황에서 **2.4V ~ 3.6V, Slow speed** 상황에서 **1.8V** 이하
- **ADC input** 범위 **: Vref-(Vssa**에 연결됨**) ~ Vref+(Vdda**에 연결됨**)**
  즉**,** 측정하고자 하는 입력신호의 범위는 **ADC** 기준전압범위**(Vref- ~ Vref+)**에 의해 결정

2. STM32F407 ADC 구성

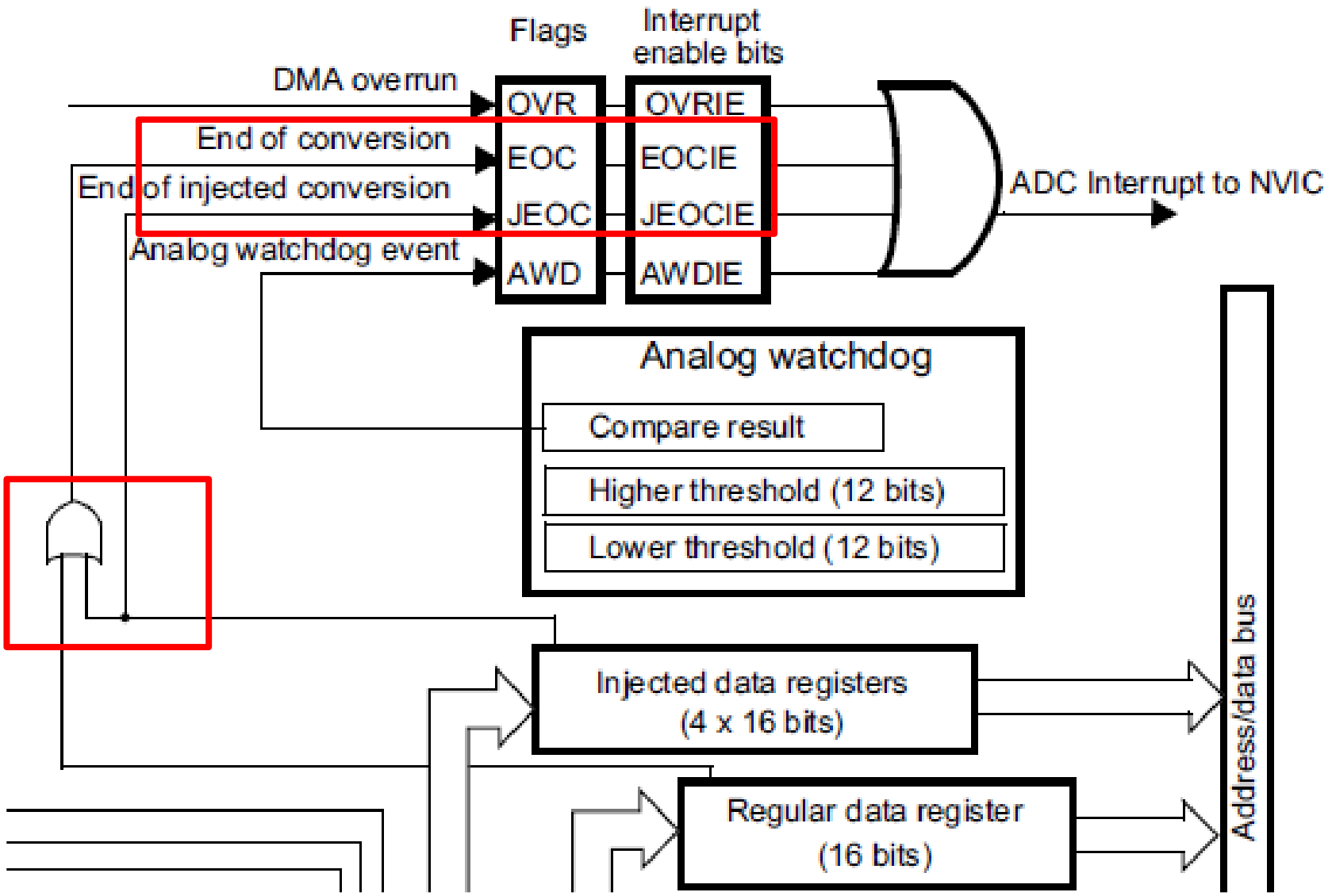
- 총 3개의 ADC 모듈(ADC1, ADC2, ADC3) 장착
- 각 ADCx 내부의 AD 변환모듈: 2개 채널(Regular channel, Injected channel)
- AD 변환된 데이터 저장: 2개의 16비트 데이터 레지스터(Regular data register, Injected data register)에 각각 저장되어 MCU로 전달
- 외부의 아날로그 입력: ADCx_IN0 ~ ADCx_IN15의 16개 핀을 통해 입력
- 내부의 아날로그 입력
  ADCx_IN16(내부) : Temperature Sensor 온도 측정용
  ADCx_IN17(내부) : Internal Reference voltage 측정용
  ADCx_IN18(내부) : V_{BAT} 전압 측정용
- AD 변환 시작용 트리거 신호의 입력
  - 기본: ADCx→CR2. SWSTART 비트를 ON
  - 외부: 외부인터럽트 입력 EXTI_11과 EXTI_15
  - 내부: Timer



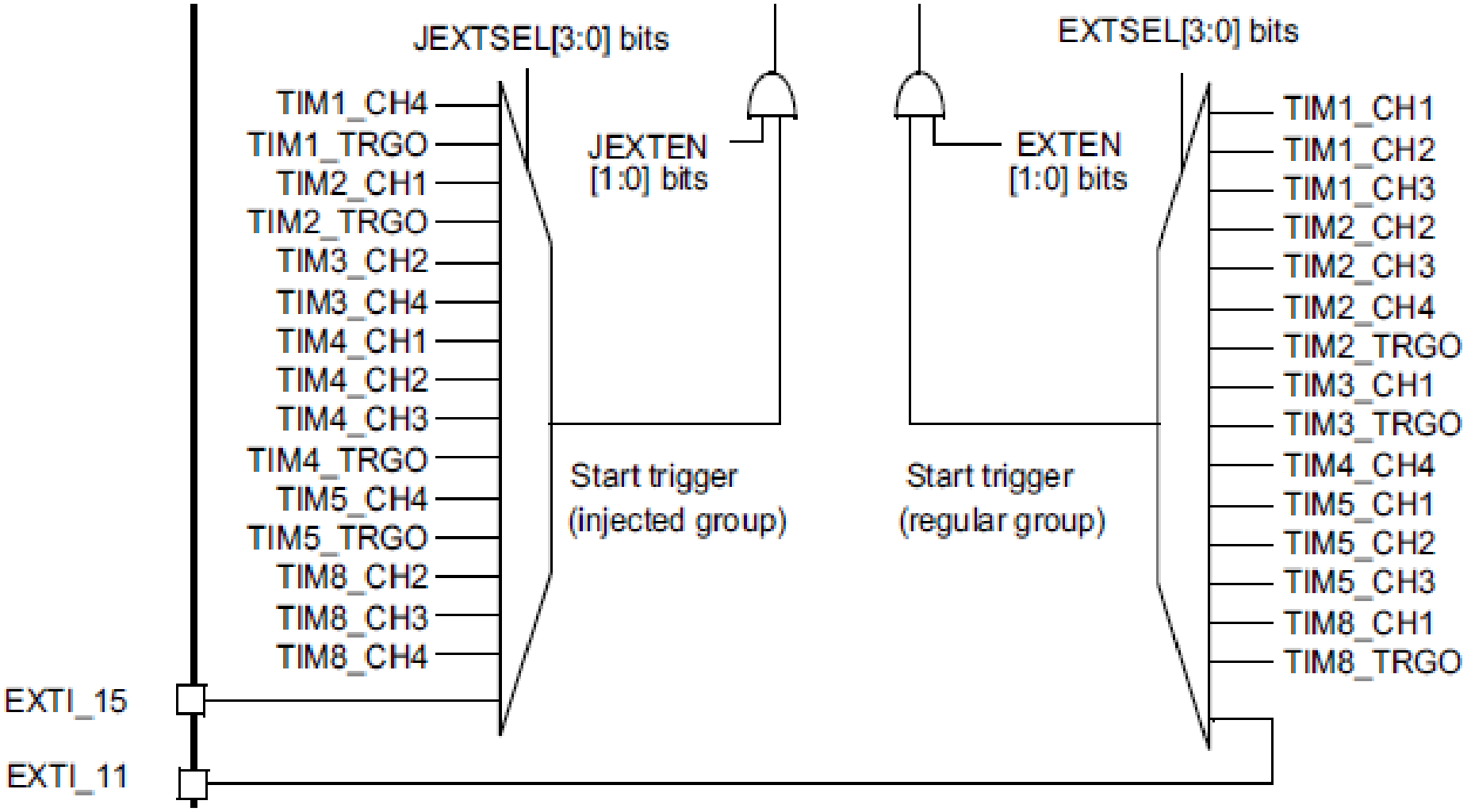
<그림1>
ADC
구성도
(전체)



<그림2> ADC 구성도(ADC 및 Data Register 부분)



<그림 3> ADC 구성도(Interrupt 신호발생 부분)

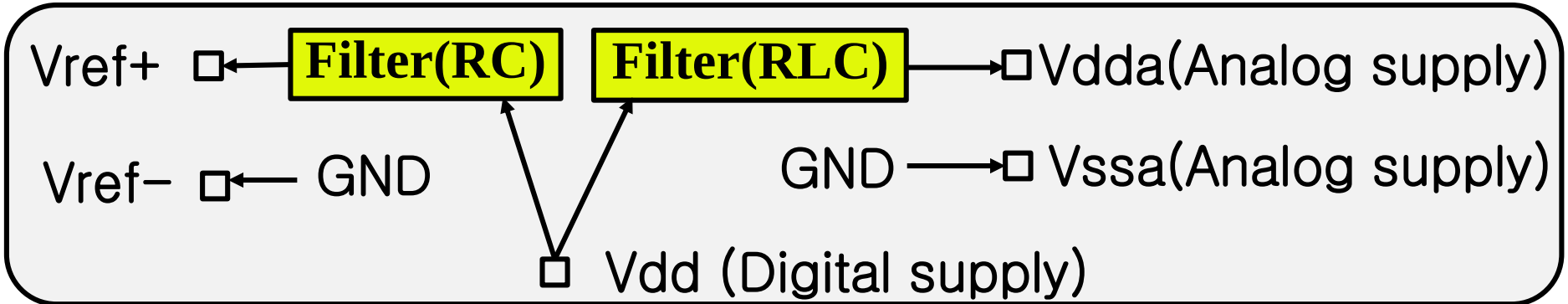


<그림 4> ADC 구성도(ADC start Trigger 신호발생 부분)

- **ADC 관련된 pins**

Name	Signal type	Remarks
V_{REF+}	Input, analog reference positive	The higher/positive reference voltage for the ADC, $1.8\ V \le V_{REF+} \le V_{DDA}$
V_{DDA}	Input, analog supply	Analog power supply equal to V_{DD} and $2.4\ V \le V_{DDA} \le V_{DD}$ (3.6 V) for full speed $1.8\ V \le V_{DDA} \le V_{DD}$ (3.6 V) for reduced speed
V_{REF-}	Input, analog reference negative	The lower/negative reference voltage for the ADC, $V_{REF-} = V_{SSA}$
V_{SSA}	Input, analog supply ground	Ground for analog power supply equal to V_{SS}
ADCx_IN[15:0]	Analog input signals	16 analog input channels

- 표준 연결 방법



• ADC 모듈의 입력 채널(총24ch)(PA[0:7],PB[0:1],PC[0:5],PF[3:10])

ADC1		ADC2		ADC3	
채널 이름	관련GPIO 핀	채널 이름	관련GPIO 핀	채널 이름	관련GPIO 핀
ADC1_IN0	PA0	ADC2_IN0	PA0	ADC3_IN0	PA0
ADC1_IN1	PA1	ADC2_IN1	PA1	ADC3_IN1	PA1
ADC1_IN2	PA2	ADC2_IN2	PA2	ADC3_IN2	PA2
ADC1_IN3	PA3	ADC2_IN3	PA3	ADC3_IN3	PA3
ADC1_IN4	PA4	ADC2_IN4	PA4	ADC3_IN4	PF6
ADC1_IN5	PA5	ADC2_IN5	PA5	ADC3_IN5	PF7
ADC1_IN6	PA6	ADC2_IN6	PA6	ADC3_IN6	PF8
ADC1_IN7	PA7	ADC2_IN7	PA7	ADC3_IN7	PF9
ADC1_IN8	PB0	ADC2_IN8	PB0	ADC3_IN8	PF10
ADC1_IN9	PB1	ADC2_IN9	PB1	ADC3_IN9	PF3
ADC1_IN10	PC0	ADC2_IN10	PC0	ADC3_IN10	PC0
ADC1_IN11	PC1	ADC2_IN11	PC1	ADC3_IN11	PC1
ADC1_IN12	PC2	ADC2_IN12	PC2	ADC3_IN12	PC2
ADC1_IN13	PC3	ADC2_IN13	PC3	ADC3_IN13	PC3
ADC1_IN14	PC4	ADC2_IN14	PC4	ADC3_IN14	PF4
ADC1_IN15	PC5	ADC2_IN15	PC5	ADC3_IN15	PF5

• 각 모듈(ADCx)의 입력 채널 선택 과정

(1) ADCx 모듈의 채널을 선택하고, 관련 GPIO clock enable,
(예) ADC1의 CH0을 선택하고자 하면, Port A에 clock enable 함.
(2) GPIOx → MODER 를 Analog IN으로 설정
(예) ADC1의 CH0(PA0)을 선택하였다면, GPIOA→MODER의 1,0 bit를 '11'로 set .
(3) ADCx clock enable (APB2ENR)

- (1)선택시 주의사항

: 같은 pin는 중복으로 서로 다른 모듈에 속할 수 없음. 예를 들면,
- ADC1이 CH4(PA4)을 사용할 경우, ADC2는 CH4을 사용할 수 없음(PA4이 양쪽에 관련되어 있으므로)
- 그러나, ADC1이 CH4(PA4)을 사용할 경우, ADC3도 CH4(PF6)를 사용할 수 있음

3. STM32F407 ADC 주요 기능

3.1 ADC on-off control

- **ADC Power On: ADCx→CR2.ADON=1**
- **Conversion Start: ADCx→CR2. SWSTART**

  or ADCx→CR2. JSWSTART=1
- **Conversion Stop and ADC Power Down : ADCx→CR2.ADON=0**

3.2 ADC clock

- **Analog 회로용 clock: ADCCLK(ADC1,2,3)**
  - **APB2 clock으로부터 분주되어 제공(fPCLK2/2, /4, /6 or /8)**
- **Digital 회로용 clock(레지스터 R/W access용)**
  - **APB2 clock(Max 84MHz)**
  - **RCC→APB2ENR에서 Enable 설정**

3.3 Channel selection

: 외부입력을 받는 16개 채널중 변환할 채널 선택과 변환순서를 지정하기 위한 방법

- **레귤러 그룹(Regular group)을 이용 : ADCx→SQRx 레지스터를 이용하여 채널의 변환순서를 16개까지 지정 가능(주로 이 방법이 사용)**
  -ADCx→SQR1.L[3:0] bits : 변환채널수 설정
  -ADCx→SQRy. SQz[4:0] bits : 변환순서 설정(y=1~3, z=1~16)

- **인젝티드 그룹(Injected group)을 이용 : ADC_JSQR 레지스터를 이용하여 채널의 변환순서를 4개까지 지정 가능(레귤러 그룹보다는 우선순위가 높음, 즉 우선 처리해야할 입력신호는 인젝티드 그룹 이용하는 것이 유리함)**
  -ADCx→JSQR.JL[1:0] bits : 변환채널수 설정
  -ADCx→JSQR. JSQy[4:0] bits : 변환순서 설정(y=1~4)

3.4 단일(Single) 변환 모드 (Regular Group 경우)

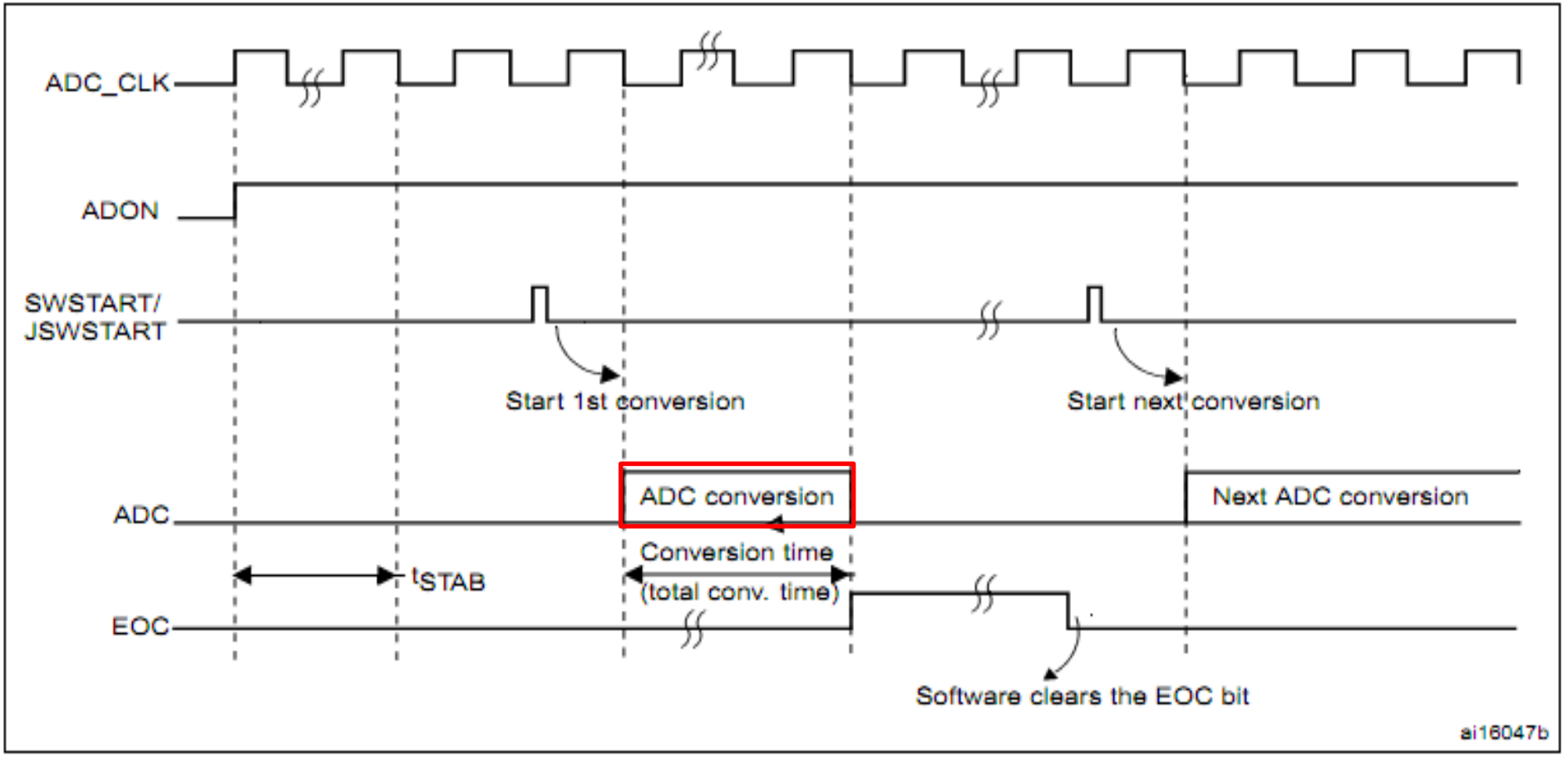
- ADC는 변환을 1번만 수행
- 단일 변환 모드 설정: ADCx→CR2.CONT 비트=0
- 단일 변환 시작: ADCx→CR2.SWSTART 비트=1 또는 외부 트리거 입력 인가
- 단일 변환 종료후:
  - 변환결과값 저장: 16-bit ADCx→DR register
  - EOC (end of conversion) flag = 1
  - Interrupt 발생 (if EOCIE bit = 1)

3.5 연속(Continuous) 변환 모드(Regular Group 경우)

- 연속으로 AD변환을 실행케 하는 모드
- 하나의 변환이 완료되면 바로 다음의 변환 시작
- 연속 변환 모드 설정: ADCx→CR2.CONT 비트=1
- 연속 변환 시작: ADCx→CR2.SWSTART 비트=1 또는 외부 트리거 입력이 인가 (반드시 EOCS = 0)
- 각 변환 종료후: 변환결과값 저장: ADCx→DR register
  - EOC flag = 1, Interrupt 발생 (if EOCIE bit = 1)

3.6 동작 타이밍 선도

- AD 변환기는 전원 공급 후 제대로 동작하기 위해서는 t_{STAB} 만큼의 안정화(stabilization) 시간이 필요
- 변환 시작 신호가 주어진 후 15클럭 사이클이 지나면 변환 완료



<그림 5> ADC의 동작 타이밍 선도

3.7 스캔(Scan) 모드

- 채널 그룹 내의 모든 채널들을 **ADCx→SQRx** 레지스터에 지정된 순서대로 스캔하여 변환하는 모드
- 스캔 모드 설정 : **ADCx→CR1.SCAN** 비트=1
- 연속 변환 모드인 경우는 스캔 모드의 동작이 연속적으로 일어남

3.8 불연속(Discontinuous) 모드

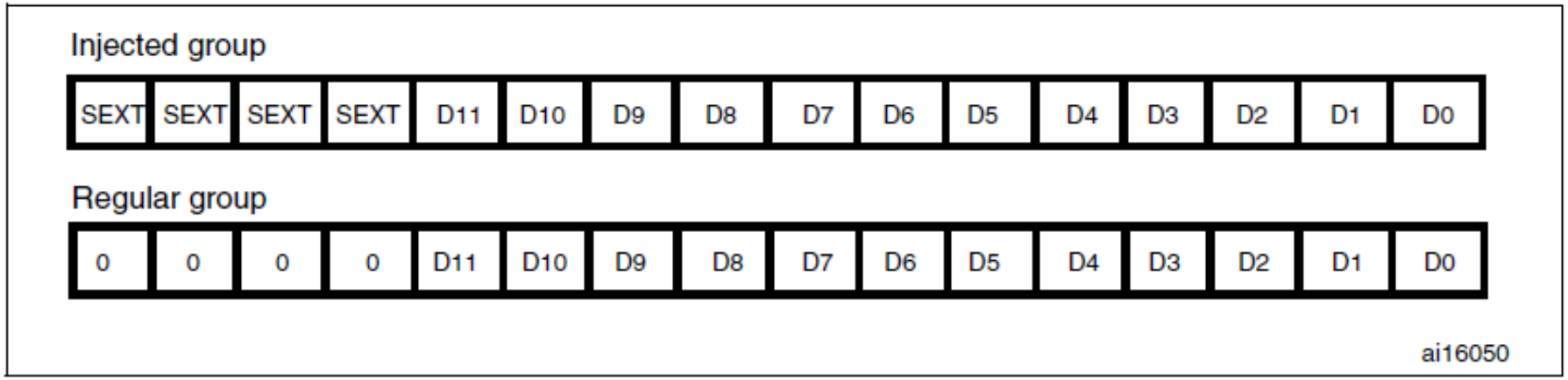
- 채널 그룹 내의 일부 채널을 미리 정해진 순서대로 변환하는 모드
- 외부 트리거 신호가 입력되면 **n**개**(n<=8)** 채널의 변환만 이루어짐. 다시 외부 트리거 신호가 입력되면 다음의 **n**개 변환, **n**개가 되지 않더라도 정해진 변환 순서의 끝이 되면 그대로 종료

(변환 예) n=3이고, 채널의 변환 순서 = **0, 1, 2, 3, 6, 7, 9, 10** 일 경우

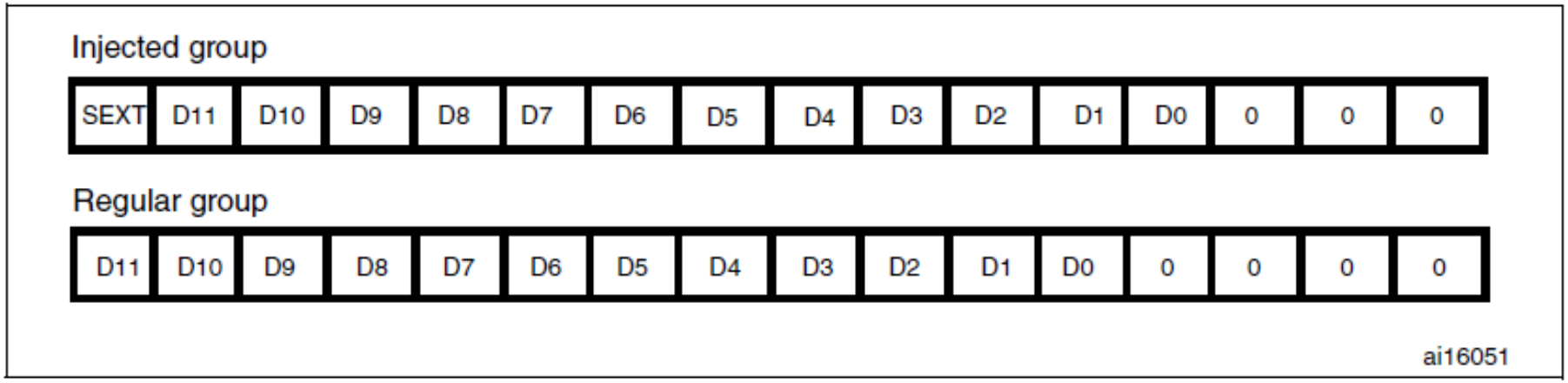
- **1**번째 트리거 입력 : 채널 **0, 1, 2** 가 변환됨
- **2**번째 트리거 입력 : 채널 **3, 6, 7** 이 변환됨
- **3**번째 트리거 입력 : 채널 **9, 10** 이 변환되고 **EOC** 이벤트 발생
- **4**번째 트리거 입력 : 다시 채널 **0, 1, 2** 가 변환됨
- 이 후는 동일한 방식의 동작이 반복됨

3.9 데이터 정렬

• 데이터 레지스터에 변환결과를 저장하는 방식; 오른쪽 정렬(Right aligned)(reset 값)과 왼쪽 정렬(Left aligned) 방식



(a) 오른쪽 정렬



(b) 왼쪽 정렬

3.10 외부 트리거에 의한 변환 시작(레귤러 그룹 경우)

- **ADCx→CR2.EXTSEL[3:0] 비트 설정: 레귤러 채널에 대하여 외부 트리거 신호(timer capture or EXTI line)를 선택**

Source	Type	EXTSEL[3:0]
TIM1_CH1 event	Internal signal from on-chip timers	0000
TIM1_CH2 event		0001
TIM1_CH3 event		0010
TIM2_CH2 event		0011
TIM2_CH3 event		0100
TIM2_CH4 event		0101
TIM2_TRGO event		0110
TIM3_CH1 event		0111
TIM3_TRGO event		1000
TIM4_CH4 event		1001
TIM5_CH1 event		1010
TIM5_CH2 event		1011
TIM5_CH3 event		1100
TIM8_CH1 event		1101
TIM8_TRGO event		1110
EXTI line11	External pin	1111

• **ADC_CR2.EXTEN[1:0] 비트 설정: 레귤러 채널에 대하여 External trigger Enable (polarity 도 지정)**

Source	EXTEN[1:0] / JEXTEN[1:0]
Trigger detection disabled	00
Detection on the rising edge	01
Detection on the falling edge	10
Detection on both the rising and falling edges	11

3.11 ADC 인터럽트

• **AD 변환이 완료된 경우: 인터럽트 발생 가능**

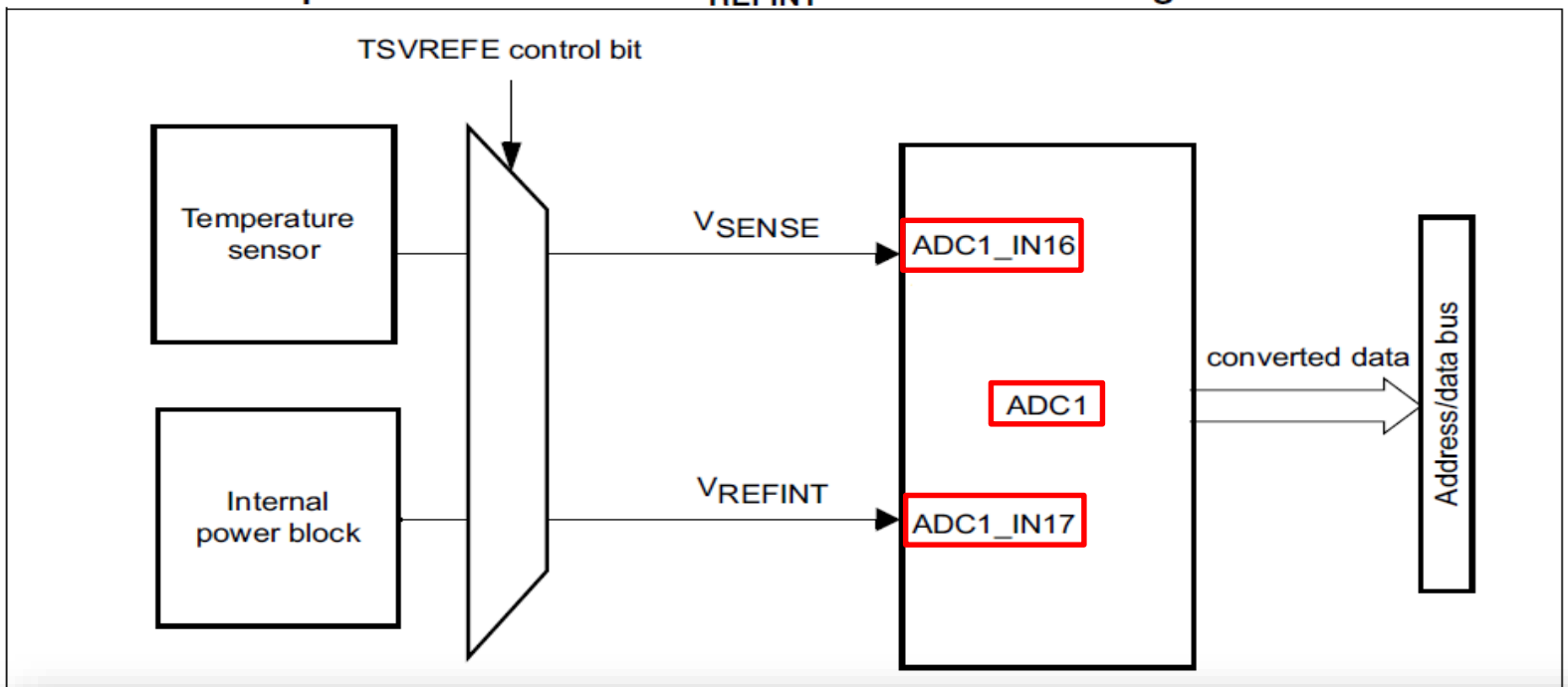
• **ADC1, ADC2, ADC3 인터럽트: 동일한 인터럽트 벡터(18번)**

•**인터럽트 핸들러 루틴: ADC_IRQHandler(void)**

Interrupt event	Event flag	Enable control bit
End of conversion of a regular group	EOC	EOCIE
End of conversion of an injected group	JEOC	JEOCIE
Analog watchdog status bit is set	AWD	AWDIE
Overrun	OVR	OVRIE

3.12 Temperature sensor

Temperature sensor and V_{REFINT} channel block diagram



Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40 °C < T_A < +105 °C	1.18	1.21	1.24	V

Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L (1)	V_{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope (1)	Average slope	-	2.5		mV/°C
V_{25} (1)	Voltage at 25 °C	-	0.76		V

Calculate the temperature using the following formula:

$$\text{Temperature (in °C)} = \{(V_{SENSE} - V_{25}) / \text{Avg\_Slope}\} + 25$$

- **Reading the temperature**

1. Select ADCx→IN16 or ADCx→IN18 input channel.
2. Select a sampling time greater than the minimum sampling time specified in the datasheet.
3. ADC→CCR. TSVREFE bit =1 to wake up the temperature sensor from power down mode
4. Start the ADC conversion by ADCx→CR2.SWSTART bit=1(or by external trigger)
5. Read the resulting VSENSE data in the ADC data register
6. Calculate the temperature using the following formula:
Temperature (in ˚C) = {(VSENSE – V25) / Avg_Slope} + 25
Where:
-V25 = VSENSE value for 25˚ C
- Avg_Slope = average slope of the temperature vs. VSENSE curve (given in mV/˚C or µV/˚C)
*** Refer to the datasheet's electrical characteristics section for the actual values of V25 and Avg_Slope.**

4. ADC 레지스터

4.1 Register Map

Table 54. ADC global register map

Offset	Register
0x000 - 0x04C	ADC1
0x050 - 0x0FC	Reserved
0x100 - 0x14C	ADC2
0x118 - 0x1FC	Reserved
0x200 - 0x24C	ADC3
0x250 - 0x2FC	Reserved
0x300 - 0x308	Common registers

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	ADC_SR	Reserved																										OVR	STRT	JSTRT	JEOC	EOC	AWD
	Reset value																											0	0	0	0	0	0
0x04	ADC_CR1	Reserved					OVRIE	RES[1:0]		AWDEN	JAWDEN	Reserved						DISC NUM [2:0]			JDISCEN	DISCEN	JAUTO	AWD SGL	SCAN	JEOCIE	AWDIE	EOCIE	AWDCH[4:0]					
	Reset value						0	0	0	0	0							0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x08	ADC_CR2	Reserved	SWSTART	EXTEN[1:0]		EXTSEL [3:0]				Reserved	JSWSTART	JEXTEN[1:0]		JEXTSEL [3:0]				Reserved				ALIGN	EOCS	DDS	DMA	Reserved						CONT	ADON
	Reset value		0	0	0	0	0	0	0		0	0	0	0	0	0	0					0	0		0							0	0
0x0C	ADC_SMPR1	Sample time bits SMPx_x																															
	Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x10	ADC_SMPR2	Sample time bits SMPx_x																															
	Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x14	ADC_JOFR1	Reserved																				JOFFSET1[11:0]											
	Reset value																					0	0	0	0	0	0	0	0	0	0	0	0
0x18	ADC_JOFR2	Reserved																				JOFFSET2[11:0]											
	Reset value																					0	0	0	0	0	0	0	0	0	0	0	0
0x1C	ADC_JOFR3	Reserved																				JOFFSET3[11:0]											
	Reset value																					0	0	0	0	0	0	0	0	0	0	0	0
0x20	ADC_JOFR4	Reserved																				JOFFSET4[11:0]											
	Reset value																					0	0	0	0	0	0	0	0	0	0	0	0

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x24	ADC_HTR	Reserved																				HT[11:0]											
	Reset value																					1	1	1	1	1	1	1	1	1	1	1	1
0x28	ADC_LTR	Reserved																				LT[11:0]											
	Reset value																					0	0	0	0	0	0	0	0	0	0	0	0
0x2C	ADC_SQR1	Reserved								L[3:0]				Regular channel sequence SQx_x bits																			
	Reset value									0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x30	ADC_SQR2	Reserved	Reserved	Regular channel sequence SQx_x bits																													
	Reset value			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x34	ADC_SQR3	Reserved	Regular channel sequence SQx_x bits																														
	Reset value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x38	ADC_JSQR	Reserved										JL[1:0]		Injected channel sequence JSQx_x bits																			
	Reset value											0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x3C	ADC_JDR1	Reserved																JDATA[15:0]															
	Reset value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x40	ADC_JDR2	Reserved																JDATA[15:0]															
	Reset value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x44	ADC_JDR3	Reserved																JDATA[15:0]															
	Reset value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x48	ADC_JDR4	Reserved																JDATA[15:0]															
	Reset value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x4C	ADC_DR	Reserved																Regular DATA[15:0]															
	Reset value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	ADC_CSR	Reserved										OVR	STRT	JSTRT	JEOC	EOC	AWD	Reserved		OVR	STRT	JSTRT	JEOC	EOC	AWD	Reserved		OVR	STRT	JSTRT	JEOC	EOC	AWD
	Reset value											0	0	0	0	0	0			0	0	0	0	0	0			0	0	0	0	0	0
												ADC3								ADC2								ADC1					
0x04	ADC_CCR	Reserved								TSVREFE	VBATE	Reserved				ADCPRE[1:0]		DMA[1:0]		DDS	Reserved	DELAY [3:0]				Reserved		MULTI [4:0]					
	Reset value									0	0					0	0	0	0	0		0	0	0	0			0	0	0	0	0	0
0x08	ADC_CDR	Regular DATA2[15:0]																Regular DATA1[15:0]															
	Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

5. ADC 주요 레지스터

- **ADC status register (ADC_SR)**

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										OVR	STRT	JSTRT	JEOC	EOC	AWD
										rc_w0	rc_w0	rc_w0	rc_w0	rc_w0	rc_w0

- **Bit 1 EOC: Regular channel end of conversion**

This bit is set by hardware at the end of the conversion of a regular group of channels. It is cleared by software or by reading the ADC_DR register.

0: Conversion not complete (EOCS=0), or sequence of conversions not complete (EOCS=1)

1: Conversion complete (EOCS=0), or sequence of conversions complete (EOCS=1)

- **ADC control register 1 (ADC_CR1)**

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved					OVRIE	RES		AWDEN	JAWDEN	Reserved					
					rw	rw	rw	rw	rw						

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DISCNUM[2:0]			JDISCEN	DISCEN	JAUTO	AWDSGL	SCAN	JEOCIE	AWDIE	EOCIE	AWDCH[4:0]				
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

- **Bits 25:24 RES[1:0]: Resolution of the conversion**

00: 12-bit (15 ADCCLK cycles) 01: 10-bit (13 ADCCLK cycles)

10: 8-bit (11 ADCCLK cycles)11: 6-bit (9 ADCCLK cycles)

- **Bit 8 SCAN: Scan mode**

In Scan mode, the inputs selected through the ADC_SQRx or ADC_JSQRx registers are converted.

0: Scan mode disabled 1: Scan mode enabled

Note: An EOC interrupt is generated if the EOCIE bit is set:

– At the end of each regular group sequence if the EOCS bit is cleared to 0

– At the end of each regular channel conversion if the EOCS bit is set to 1

Note: A JEOC interrupt is generated only on the end of conversion of the last channel if JEOCIE =1.

- **Bit 5 EOCIE: Interrupt enable for EOC**

0: EOC interrupt disabled

1: EOC interrupt enabled. An interrupt is generated when the EOC bit is set.

- **ADC control register 2 (ADC_CR2)**

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
reserved	SWSTART	EXTEN		EXTSEL[3:0]				reserved	JSWSTART	JEXTEN		JEXTSEL[3:0]			
	rw	rw	rw	rw	rw	rw	rw		rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved				ALIGN	EOCS	DDS	DMA	Reserved						CONT	ADON
				rw	rw	rw	rw							rw	rw

- **Bit 30 SWSTART: Start conversion of regular channels**

This bit is set by software to start conversion and cleared as soon as the conversion starts.

0: Reset state 1: Starts conversion of regular channels

- **Bits 29:28 EXTEN: External trigger enable for regular channels**

These bits are set and cleared by software to select the external trigger polarity and enable the trigger of a regular group.

00: Trigger detection disabled

01: Trigger detection on the rising edge

10: Trigger detection on the falling edge

11: Trigger detection on both the rising and falling edges

- **Bits 27:24 EXTSEL[3:0]: External event select for regular group**

These bits select the external event used to trigger the start of conversion of a regular group:

0000: Timer 1 CC1 event **0001: Timer 1 CC2 event**
0010: Timer 1 CC3 event **0011: Timer 2 CC2 event**
0100: Timer 2 CC3 event **0101: Timer 2 CC4 event**
0110: Timer 2 TRGO event **0111: Timer 3 CC1 event**
1000: Timer 3 TRGO event **1001: Timer 4 CC4 event**
1010: Timer 5 CC1 event **1011: Timer 5 CC2 event**
1100: Timer 5 CC3 event **1101: Timer 8 CC1 event**
1110: Timer 8 TRGO event **1111: EXTI line11**

- **Bit 11 ALIGN: Data alignment**

0: Right alignment **1: Left alignment**

- **Bit 10 EOCS: End of conversion selection**

0: The EOC bit is set at the end of each sequence of regular conversions. Overrun detection is enabled only if DMA=1.
1: The EOC bit is set at the end of each regular conversion. Overrun detection is enabled.

- **Bit 1 CONT: Continuous conversion**

This bit is set and cleared by software. If it is set, conversion takes place continuously until it is cleared.
0: Single conversion mode
1: Continuous conversion mode

- **Bit 0 ADON: A/D Converter ON / OFF**

0: ***Disable ADC conversion and go to power down mode***
1: Enable ADC

- **ADC sample time register 1 (ADC_SMPR1)**

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved					SMP18[2:0]			SMP17[2:0]			SMP16[2:0]			SMP15[2:1]	
					rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SMP15_0	SMP14[2:0]			SMP13[2:0]			SMP12[2:0]			SMP11[2:0]			SMP10[2:0]		
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

- **ADC sample time register 2 (ADC_SMPR2)**

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		SMP9[2:0]			SMP8[2:0]			SMP7[2:0]			SMP6[2:0]			SMP5[2:1]	
		rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SMP 5_0	SMP4[2:0]			SMP3[2:0]			SMP2[2:0]			SMP1[2:0]			SMP0[2:0]		
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

- **Bits 26:0 SMPx[2:0]: Channel x sampling time selection**

During sampling cycles, the channel selection bits must remain unchanged.

Note: 000: 3 cycles **001: 15 cycles** **010: 28 cycles**

011: 56 cycles **100: 84 cycles** **101: 112 cycles**

110: 144 cycles **111: 480 cycles**

- **ADC regular sequence register 1 (ADC_SQR1)**

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								L[3:0]				SQ16[4:1]			
								rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SQ16_0	SQ15[4:0]					SQ14[4:0]					SQ13[4:0]				
rw	rw	rw	rw	rw	rw	rw	rw				rw	rw	rw	rw	rw

- **Bits 23:20 L[3:0]: Regular channel sequence length**

0000: 1 conversion 0001: 2 conversions

...

1111: 16 conversions

- **Bits 19:15 SQ16[4:0]: 16th conversion in regular sequence**

These bits are written by software with the channel number (0..18) assigned as the 16th in the conversion sequence.

Bits 14:10 SQ15[4:0]: 15th conversion in regular sequence

Bits 9:5 SQ14[4:0]: 14th conversion in regular sequence

Bits 4:0 SQ13[4:0]: 13th conversion in regular sequence

- **ADC regular sequence register 2 (ADC_SQR2)**

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		SQ12[4:0]					SQ11[4:0]					SQ10[4:1]			
		rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SQ10_0	SQ9[4:0]					SQ8[4:0]					SQ7[4:0]				
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

- **Bits 29:26 SQ12[4:0]: 12th conversion in regular sequence**

These bits are written by software with the channel number (0..18) assigned as the 12th in the sequence to be converted.

Bits 24:20 SQ11[4:0]: 11th conversion in regular sequence

Bits 19:15 SQ10[4:0]: 10th conversion in regular sequence

Bits 14:10 SQ9[4:0]: 9th conversion in regular sequence

Bits 9:5 SQ8[4:0]: 8th conversion in regular sequence

Bits 4:0 SQ7[4:0]: 7th conversion in regular sequence

- **ADC regular sequence register 3 (ADC_SQR3)**

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		SQ6[4:0]					SQ5[4:0]					SQ4[4:1]			
		rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SQ4_0		SQ3[4:0]					SQ2[4:0]					SQ1[4:0]			
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

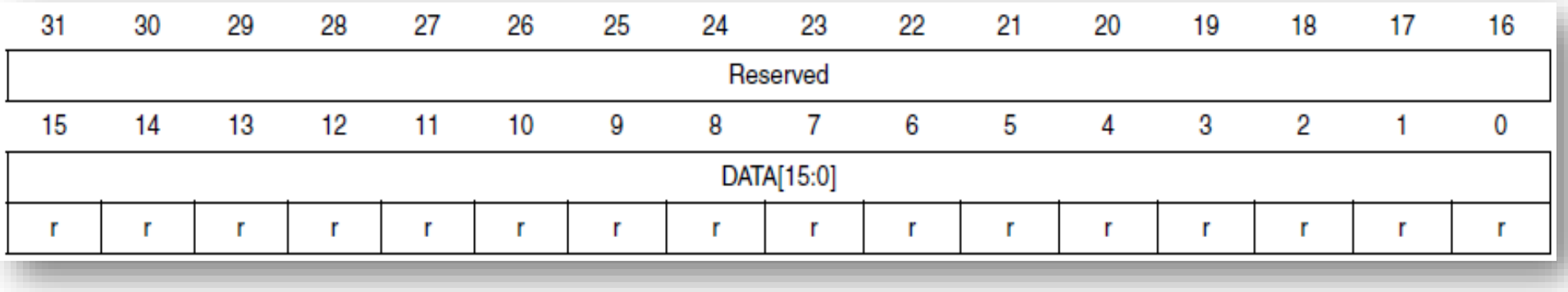
- **Bits 29:25 SQ6[4:0]: 6th conversion in regular sequence**

These bits are written by software with the channel number (0..18) assigned as the 6th in the sequence to be converted.

- **Bits 24:20 SQ5[4:0]: 5th conversion in regular sequence**
- **Bits 19:15 SQ4[4:0]: 4th conversion in regular sequence**
- **Bits 14:10 SQ3[4:0]: 3rd conversion in regular sequence**
- **Bits 9:5 SQ2[4:0]: 2nd conversion in regular sequence**
- **Bits 4:0 SQ1[4:0]: 1st conversion in regular sequence**

- **ADC regular data register (ADC_DR)**

Reset value: 0x0000 0000



31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA[15:0]															
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

Bits 15:0 DATA[15:0]: Regular data

These bits are read-only. They contain the conversion result from the regular channels.

ADC common control register (ADC_CCR)

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								TSVREFE	VBATE	Reserved				ADCPRE	
								rw	rw					rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA[1:0]		DDS	Res.	DELAY[3:0]				Reserved			MULTI[4:0]				
rw	rw	rw		rw	rw	rw	rw				rw	rw	rw	rw	rw

- **Bit 23 TSVREFE: Temperature sensor and VREFINT enable**

This bit is set and cleared by software to enable/disable the temperature sensor and the VREFINT channel.

0: Temperature sensor and VREFINT channel disabled

1: Temperature sensor and VREFINT channel enabled

- **Bits 17:16 ADCPRE: ADC prescaler**

Set and cleared by software to select the frequency of the clock to the ADC. The clock is common for all the ADCs.

Note: 00: PCLK2 divided by 2

01: PCLK2 divided by 4

10: PCLK2 divided by 6

11: PCLK2 divided by 8

Bits 4:0 **MULTI[4:0]:** Multi ADC mode selection

These bits are written by software to select the operating mode.

– All the ADCs independent:
00000: Independent mode

– 00001 to 01001: Dual mode, ADC1 and ADC2 working together, ADC3 is independent
00001: Combined regular simultaneous + injected simultaneous mode
00010: Combined regular simultaneous + alternate trigger mode
00011: Reserved
00101: Injected simultaneous mode only
00110: Regular simultaneous mode only
00111: interleaved mode only
01001: Alternate trigger mode only

– 10001 to 11001: Triple mode: ADC1, 2 and 3 working together
10001: Combined regular simultaneous + injected simultaneous mode
10010: Combined regular simultaneous + alternate trigger mode
10011: Reserved
10101: Injected simultaneous mode only
10110: Regular simultaneous mode only
10111: interleaved mode only
11001: Alternate trigger mode only
All other combinations are reserved and must not be programmed

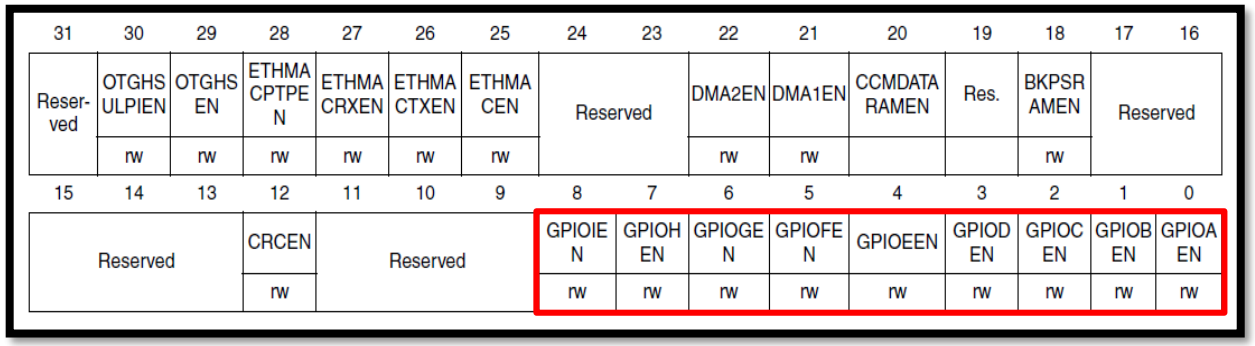
STM32F407 ADC의 주요 전기적 특징

Table 67. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply		1.8(1)	-	3.6	V
V_{REF+}	Positive reference voltage		1.8(1)(2)(3)	-	V_{DDA}	V
f_{ADC}	ADC clock frequency	V_{DDA} = 1.8(1)(3) to 2.4 V	0.6	15	18	MHz
		V_{DDA} = 2.4 to 3.6 V(3)	0.6	30	36	MHz
t_S(4)	Sampling time	f_{ADC} = 30 MHz	0.100	-	16	µs
			3	-	480	$1/f_{ADC}$
t_{CONV}(4)	Total conversion time (including sampling time)	f_{ADC} = 30 MHz 12-bit resolution	0.50	-	16.40	µs
		f_{ADC} = 30 MHz 10-bit resolution	0.43	-	16.34	µs
		f_{ADC} = 30 MHz 8-bit resolution	0.37	-	16.27	µs

RCC clock enable 레지스터 구조

•RCC_AHB1ENR

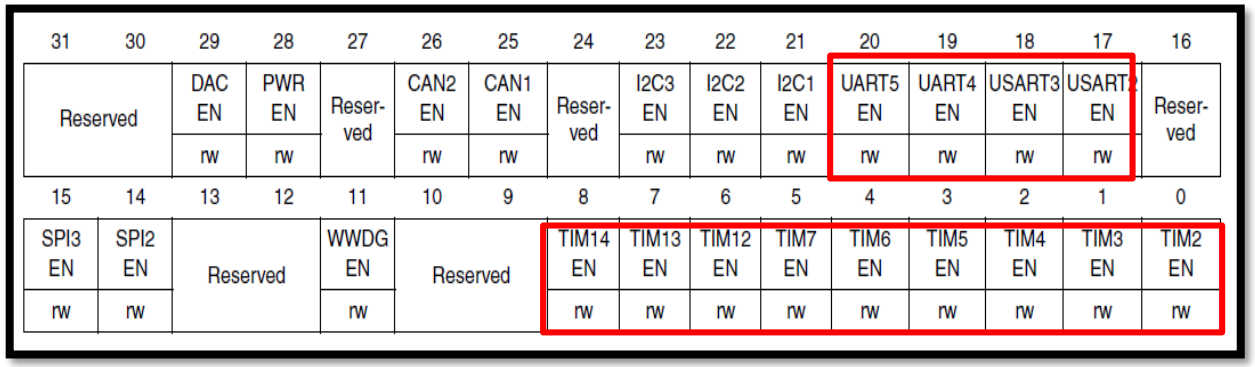


31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reser-ved	OTGHS ULPIEN	OTGHS EN	ETHMA CPTPE N	ETHMA CRXEN	ETHMA CTXEN	ETHMA CEN	Reserved		DMA2EN	DMA1EN	CCMDATA RAMEN	Res.	BKPSR AMEN	Reserved	
	rw	rw	rw	rw	rw	rw			rw	rw			rw		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			CRCEN	Reserved			GPIOIE N	GPIOH EN	GPIOGE N	GPIOFE N	GPIOEEN	GPIOD EN	GPIOC EN	GPIOB EN	GPIOA EN
			rw				rw	rw	rw	rw	rw	rw	rw	rw	rw

GPIO

•RCC_APB1ENR



31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		DAC EN	PWR EN	Reser-ved	CAN2 EN	CAN1 EN	Reser-ved	I2C3 EN	I2C2 EN	I2C1 EN	UART5 EN	UART4 EN	USART3 EN	USART2 EN	Reser-ved
		rw	rw		rw	rw		rw	rw	rw	rw	rw	rw	rw	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI3 EN	SPI2 EN	Reserved		WWDG EN	Reserved		TIM14 EN	TIM13 EN	TIM12 EN	TIM7 EN	TIM6 EN	TIM5 EN	TIM4 EN	TIM3 EN	TIM2 EN
rw	rw			rw			rw	rw	rw	rw	rw	rw	rw	rw	rw

USART:2~5

Timer:2~7, 12~14

•RCC_APB2ENR

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved													TIM11 EN	TIM10 EN	TIM9 EN
													rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reser-ved	SYSCF G EN	Reser-ved	SPI1 EN	SDIO EN	ADC3 EN	ADC2 EN	ADC1 EN	Reserved		USART6 EN	USART1 EN	Reserved		TIM8 EN	TIM1 EN
	rw		rw	rw	rw	rw	rw			rw	rw			rw	rw

Timer:9~11

Timer:1,8

SYSCFG _EN

SPI1

ADC

USART:1,6

●인터럽트 벡터 테이블(총82개)- Interrupts (0~15)

0	7	settable	WWDG	Window Watchdog interrupt	0x0000 0040
1	8	settable	PVD	PVD through EXTI line detection interrupt	0x0000 0044
2	9	settable	TAMP_STAMP	Tamper and TimeStamp interrupts through the EXTI line	0x0000 0048
3	10	settable	RTC_WKUP	RTC Wakeup interrupt through the EXTI line	0x0000 004C
4	11	settable	FLASH	Flash global interrupt	0x0000 0050
5	12	settable	RCC	RCC global interrupt	0x0000 0054
6	13	settable	EXTI0	EXTI Line0 interrupt	0x0000 0058
7	14	settable	EXTI1	EXTI Line1 interrupt	0x0000 005C
8	15	settable	EXTI2	EXTI Line2 interrupt	0x0000 0060
9	16	settable	EXTI3	EXTI Line3 interrupt	0x0000 0064
10	17	settable	EXTI4	EXTI Line4 interrupt	0x0000 0068
11	18	settable	DMA1_Stream0	DMA1 Stream0 global interrupt	0x0000 006C
12	19	settable	DMA1_Stream1	DMA1 Stream1 global interrupt	0x0000 0070
13	20	settable	DMA1_Stream2	DMA1 Stream2 global interrupt	0x0000 0074
14	21	settable	DMA1_Stream3	DMA1 Stream3 global interrupt	0x0000 0078
15	22	settable	DMA1_Stream4	DMA1 Stream4 global interrupt	0x0000 007C

●인터럽트 벡터 테이블- Interrupts (16~28)

Position	Priority	Type of priority	Acronym	Description	Offset
16	23	settable	DMA1_Stream5	DMA1 Stream5 global interrupt	0x0000 0080
17	24	settable	DMA1_Stream6	DMA1 Stream6 global interrupt	0x0000 0084
18	25	settable	ADC	ADC1, ADC2 and ADC3 global interrupts	0x0000 0088
19	26	settable	CAN1_TX	CAN1 TX interrupts	0x0000 008C
20	27	settable	CAN1_RX0	CAN1 RX0 interrupts	0x0000 0090
21	28	settable	CAN1_RX1	CAN1 RX1 interrupt	0x0000 0094
22	29	settable	CAN1_SCE	CAN1 SCE interrupt	0x0000 0098
23	30	settable	EXTI9_5	EXTI Line[9:5] interrupts	0x0000 009C
24	31	settable	TIM1_BRK_TIM9	TIM1 Break interrupt and TIM9 global interrupt	0x0000 00A0
25	32	settable	TIM1_UP_TIM10	TIM1 Update interrupt and TIM10 global interrupt	0x0000 00A4
26	33	settable	TIM1_TRG_COM_TIM11	TIM1 Trigger and Commutation interrupts and TIM11 global interrupt	0x0000 00A8
27	34	settable	TIM1_CC	TIM1 Capture Compare interrupt	0x0000 00AC
28	35	settable	TIM2	TIM2 global interrupt	0x0000 00B0

●인터럽트 벡터 테이블- Interrupts (29~43)

29	36	settable	TIM3	TIM3 global interrupt	0x0000 00B4
30	37	settable	TIM4	TIM4 global interrupt	0x0000 00B8
31	38	settable	I2C1_EV	I^2C1 event interrupt	0x0000 00BC
32	39	settable	I2C1_ER	I^2C1 error interrupt	0x0000 00C0
33	40	settable	I2C2_EV	I^2C2 event interrupt	0x0000 00C4
34	41	settable	I2C2_ER	I^2C2 error interrupt	0x0000 00C8
35	42	settable	SPI1	SPI1 global interrupt	0x0000 00CC
36	43	settable	SPI2	SPI2 global interrupt	0x0000 00D0
37	44	settable	USART1	USART1 global interrupt	0x0000 00D4
38	45	settable	USART2	USART2 global interrupt	0x0000 00D8
39	46	settable	USART3	USART3 global interrupt	0x0000 00DC
40	47	settable	EXTI15_10	EXTI Line[15:10] interrupts	0x0000 00E0
41	48	settable	RTC_Alarm	RTC Alarms (A and B) through EXTI line interrupt	0x0000 00E4
42	49	settable	OTG_FS WKUP	USB On-The-Go FS Wakeup through EXTI line interrupt	0x0000 00E8
43	50	settable	TIM8_BRK_TIM12	TIM8 Break interrupt and TIM12 global interrupt	0x0000 00EC

●인터럽트 벡터 테이블- Interrupts (44~56)

Position	Priority	Type of priority	Acronym	Description	Offset
44	51	settable	TIM8_UP_TIM13	TIM8 Update interrupt and TIM13 global interrupt	0x0000 00F0
45	52	settable	TIM8_TRG_COM_TIM14	TIM8 Trigger and Commutation interrupts and TIM14 global interrupt	0x0000 00F4
46	53	settable	TIM8_CC	TIM8 Capture Compare interrupt	0x0000 00F8
47	54	settable	DMA1_Stream7	DMA1 Stream7 global interrupt	0x0000 00FC
48	55	settable	FSMC	FSMC global interrupt	0x0000 0100
49	56	settable	SDIO	SDIO global interrupt	0x0000 0104
50	57	settable	TIM5	TIM5 global interrupt	0x0000 0108
51	58	settable	SPI3	SPI3 global interrupt	0x0000 010C
52	59	settable	UART4	UART4 global interrupt	0x0000 0110
53	60	settable	UART5	UART5 global interrupt	0x0000 0114
54	61	settable	TIM6_DAC	TIM6 global interrupt, DAC1 and DAC2 underrun error interrupts	0x0000 0118
55	62	settable	TIM7	TIM7 global interrupt	0x0000 011C
56	63	settable	DMA2_Stream0	DMA2 Stream0 global interrupt	0x0000 0120

7. STM32F407의 ADC 프로그래밍 실습

7.1 프로그램에서의 ADCx set-up 과정 및 레지스터 설정

RCC 설정

- RCC→AHB1ENR(GPIOy Clock Enable)
- RCC→APB2ENR(ADCx Clock Enable)

INT Enable

- GPIOy→MODER , Analog input
- NVIC→ISER[ ] (ADC Interrupt 사용 경우)

ADCx 초기 설정

- ADC→CCR(Mode, Clock)
- ADCx→CR1/2, ADCx→ SQR1/2/3(Mode, Trigger, Resolution, Data_Align, Regular channel sequence length)
- ADCx→SMPR1/2

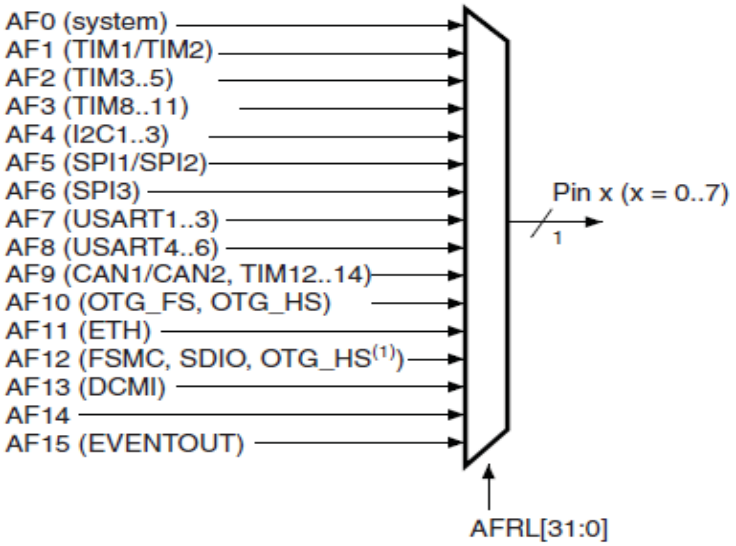
Int Handler 설정

- ADC_IRQHandler()

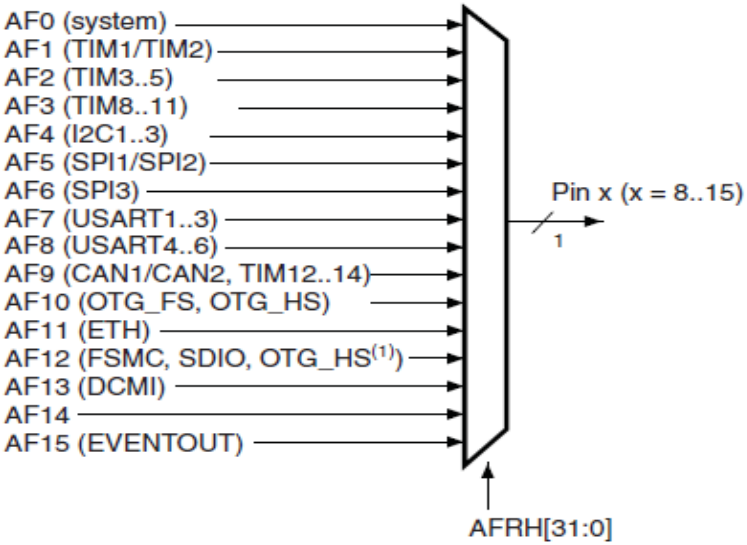
• Selecting an Alternate function

Selecting an alternate function on STM32F405xx/07xx and STM32F415xx/17xx

For pins 0 to 7, the GPIOx_AFRL[31:0] register selects the dedicated alternate function



For pins 8 to 15, the GPIOx_AFRH[31:0] register selects the dedicated alternate function



7.2 STM32F407의 ADC의 Address(Memory map)

Bus	Boundary address	Peripheral
APB2	0x4001 4C00 - 0x4001 57FF	Reserved
	0x4001 4800 - 0x4001 4BFF	TIM11
	0x4001 4400 - 0x4001 47FF	TIM10
	0x4001 4000 - 0x4001 43FF	TIM9
	0x4001 3C00 - 0x4001 3FFF	EXTI
	0x4001 3800 - 0x4001 3BFF	SYSCFG
	0x4001 3400 - 0x4001 37FF	Reserved
	0x4001 3000 - 0x4001 33FF	SPI1
	0x4001 2C00 - 0x4001 2FFF	SDIO
	0x4001 2400 - 0x4001 2BFF	Reserved
	0x4001 2000 - 0x4001 23FF	ADC1 - ADC2 - ADC3
	0x4001 1800 - 0x4001 1FFF	Reserved
	0x4001 1400 - 0x4001 17FF	USART6
	0x4001 1000 - 0x4001 13FF	USART1
	0x4001 0800 - 0x4001 0FFF	Reserved
	0x4001 0400 - 0x4001 07FF	TIM8
	0x4001 0000 - 0x4001 03FF	TIM1
	0x4000 7800- 0x4000 FFFF	Reserved

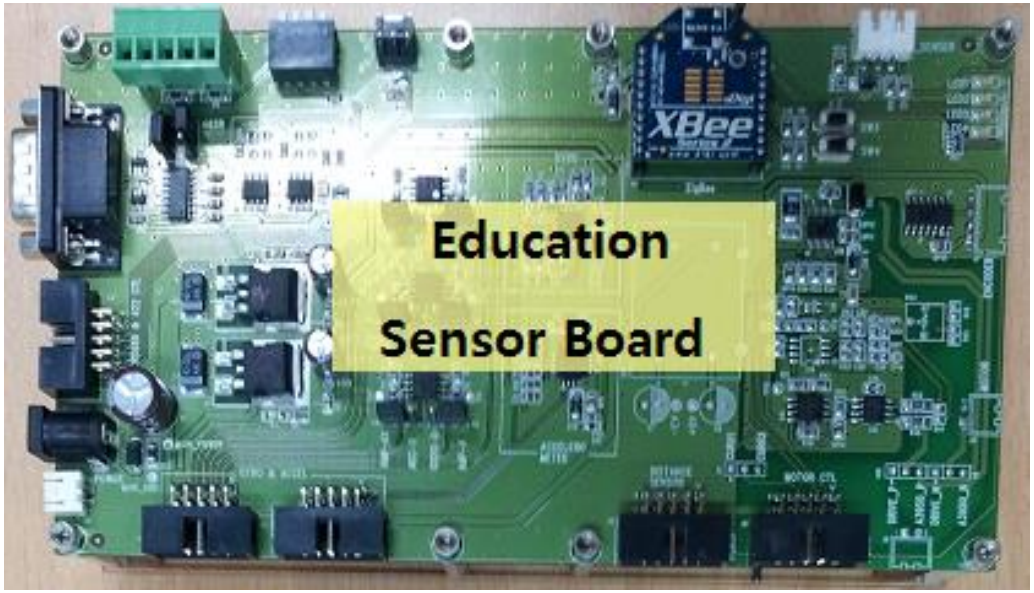
7.3 STM32F407의 ADC관련 header file(stm32f4xx.h)주요 부분

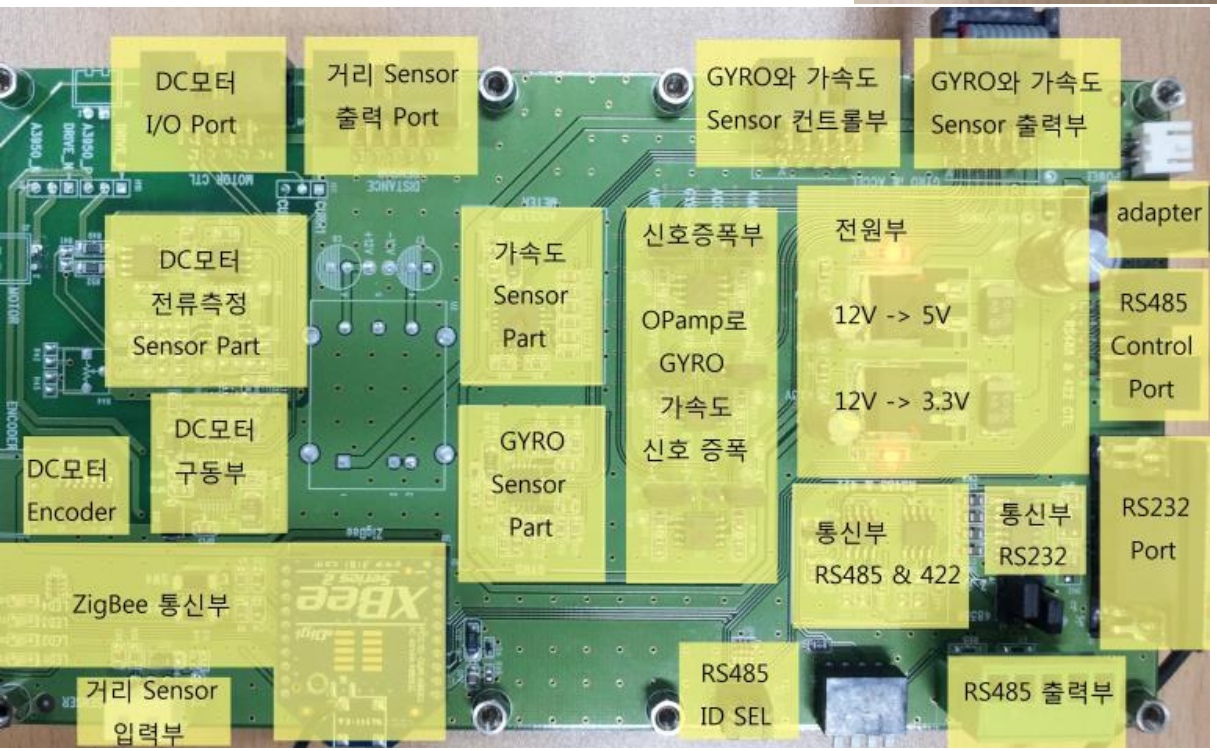
```
/* Peripheral memory map */
#define PERIPH_BASE    ((uint32_t)0x40000000) /* Peripheral base address */
#define APB1PERIPH_BASE      PERIPH_BASE
#define APB2PERIPH_BASE      (PERIPH_BASE + 0x00010000)

 /* APB2 peripherals */
 #define ADC1_BASE           (APB2PERIPH_BASE + 0x2000)
 #define ADC2_BASE           (APB2PERIPH_BASE + 0x2100)
 #define ADC3_BASE           (APB2PERIPH_BASE + 0x2200)
 #define ADC_BASE            (APB2PERIPH_BASE + 0x2300)

 #define ADC                 ((ADC_Common_TypeDef *) ADC_BASE)
 #define ADC1                ((ADC_TypeDef *) ADC1_BASE)
 #define ADC2                ((ADC_TypeDef *) ADC2_BASE)
 #define ADC3                ((ADC_TypeDef *) ADC3_BASE)

typedef struct
{  __IO uint32_t CSR; //ADC Common status register, offset:ADC1_BASE + 0x300
  __IO uint32_t CCR; //ADC common control register, offset:ADC1_BASE + 0x304
  __IO uint32_t CDR;  //ADC common regular data register for dual
                      AND triple modes, offset: ADC1 base address + 0x308
} ADC_Common_TypeDef;
```

```
typedef struct
{
  __IO uint32_t SR;     // ADC status register, Address offset: 0x00
  __IO uint32_t CR1;  // ADC control register 1, Address offset: 0x04
  __IO uint32_t CR2; //ADC control register 2, Address offset: 0x08
  __IO uint32_t SMPR1; //ADC sample time register 1, Address offset: 0x0C
  __IO uint32_t SMPR2; //ADC sample time register 2, Address offset: 0x10
  __IO uint32_t JOFR1;  //ADC injected channel data offset register 1, offset: 0x14
  __IO uint32_t JOFR2;  // ADC injected channel data offset register 2, offset: 0x18
  __IO uint32_t JOFR3;//ADC injected channel data offset register 3, offset: 0x1C
  __IO uint32_t JOFR4;  //ADC injected channel data offset register 4, offset: 0x20
  __IO uint32_t HTR; //ADC watchdog higher threshold register, offset: 0x24
  __IO uint32_t LTR; //ADC watchdog lower threshold register, offset: 0x28
  __IO uint32_t SQR1; //ADC regular sequence register 1, offset: 0x2C
  __IO uint32_t SQR2;//ADC regular sequence register 2, offset: 0x30
  __IO uint32_t SQR3;//ADC regular sequence register 3,  offset: 0x34
  __IO uint32_t JSQR; //ADC injected sequence register, offset: 0x38
  __IO uint32_t JDR1;  //ADC injected data register 1, offset: 0x3C
  __IO uint32_t JDR2;  //ADC injected data register 2, Address offset: 0x40
  __IO uint32_t JDR3;  //ADC injected data register 3, Address offset: 0x44
  __IO uint32_t JDR4; //ADC injected data register 4, Address offset: 0x48
  __IO uint32_t DR; //ADC regular data register,  Address offset: 0x4C
} ADC_TypeDef;
```

부록 : ADC Application (Sensor Interface)

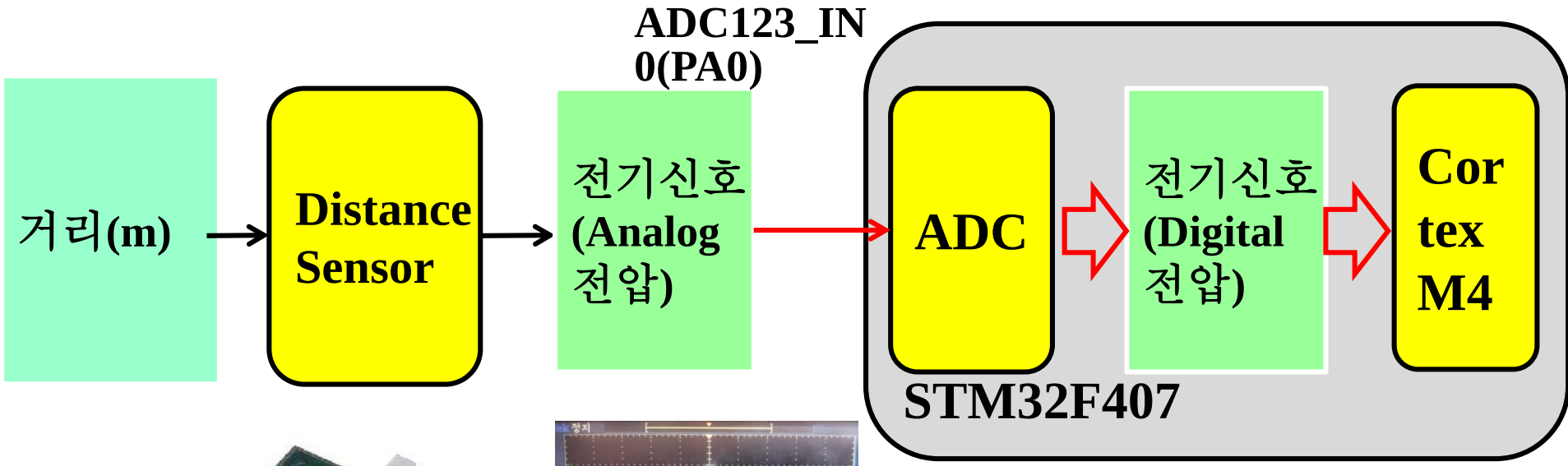
센서 실습 보드

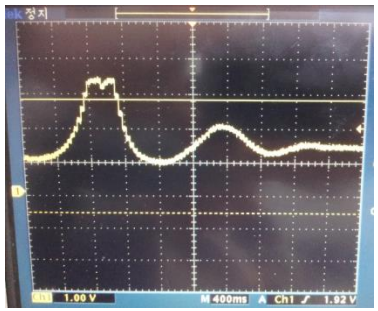

Education
Sensor Board


DC모터
I/O Port
거리 Sensor
출력 Port
GYRO와 가속도
Sensor 컨트롤부
GYRO와 가속도
Sensor 출력부
adapter
DC모터
전류측정
Sensor Part
가속도
Sensor
Part
신호증폭부
OPamp로
GYRO
가속도
신호 증폭
전원부
12V -> 5V
12V -> 3.3V
RS485
Control
Port
DC모터
구동부
DC모터
Encoder
GYRO
Sensor
Part
통신부
RS485 & 422
통신부
RS232
RS232
Port
ZigBee 통신부
RS485
ID SEL
RS485 출력부
거리 Sensor
입력부

센서 실습 보드 인터페이스

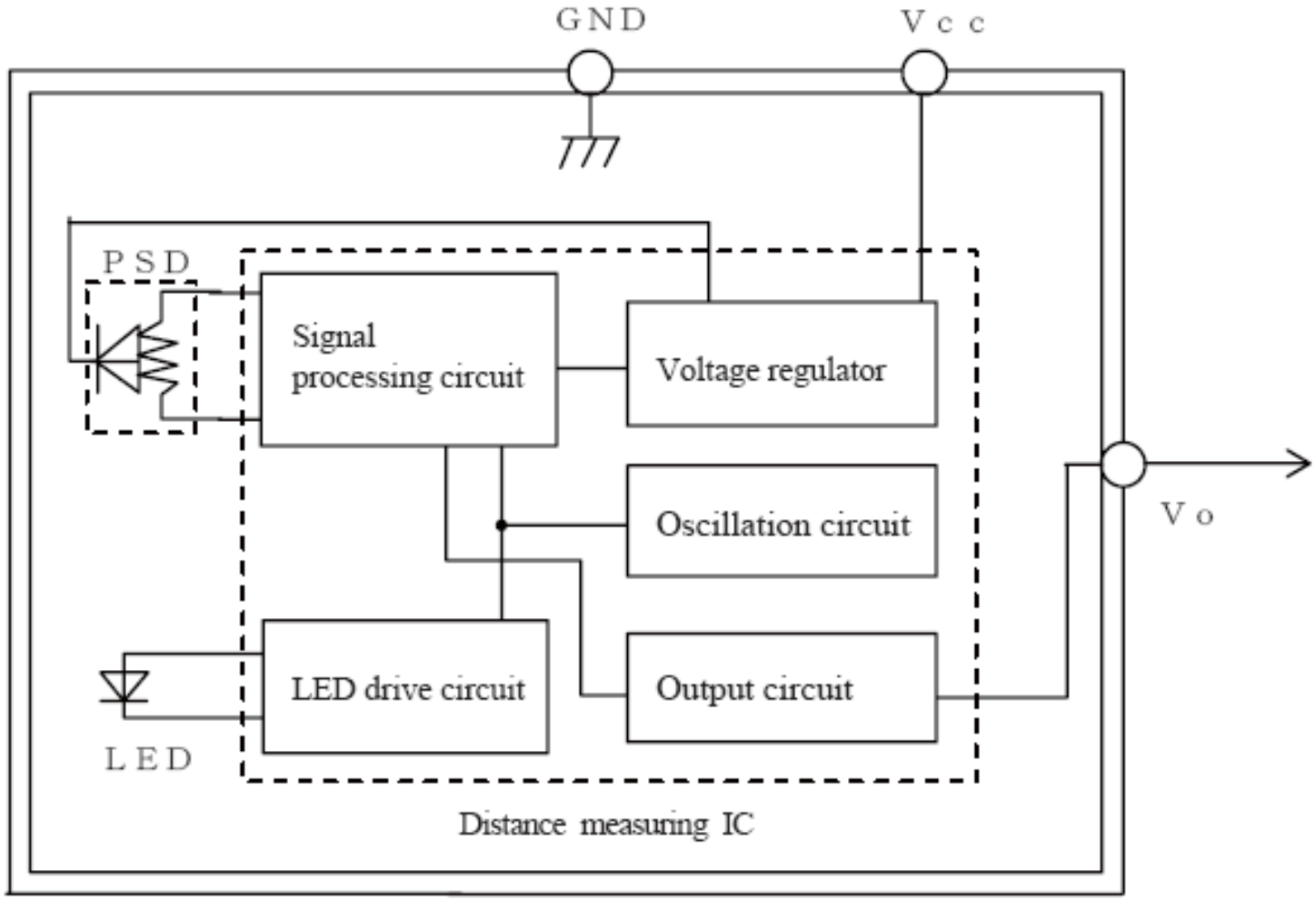
1. Distance Sensor Interface



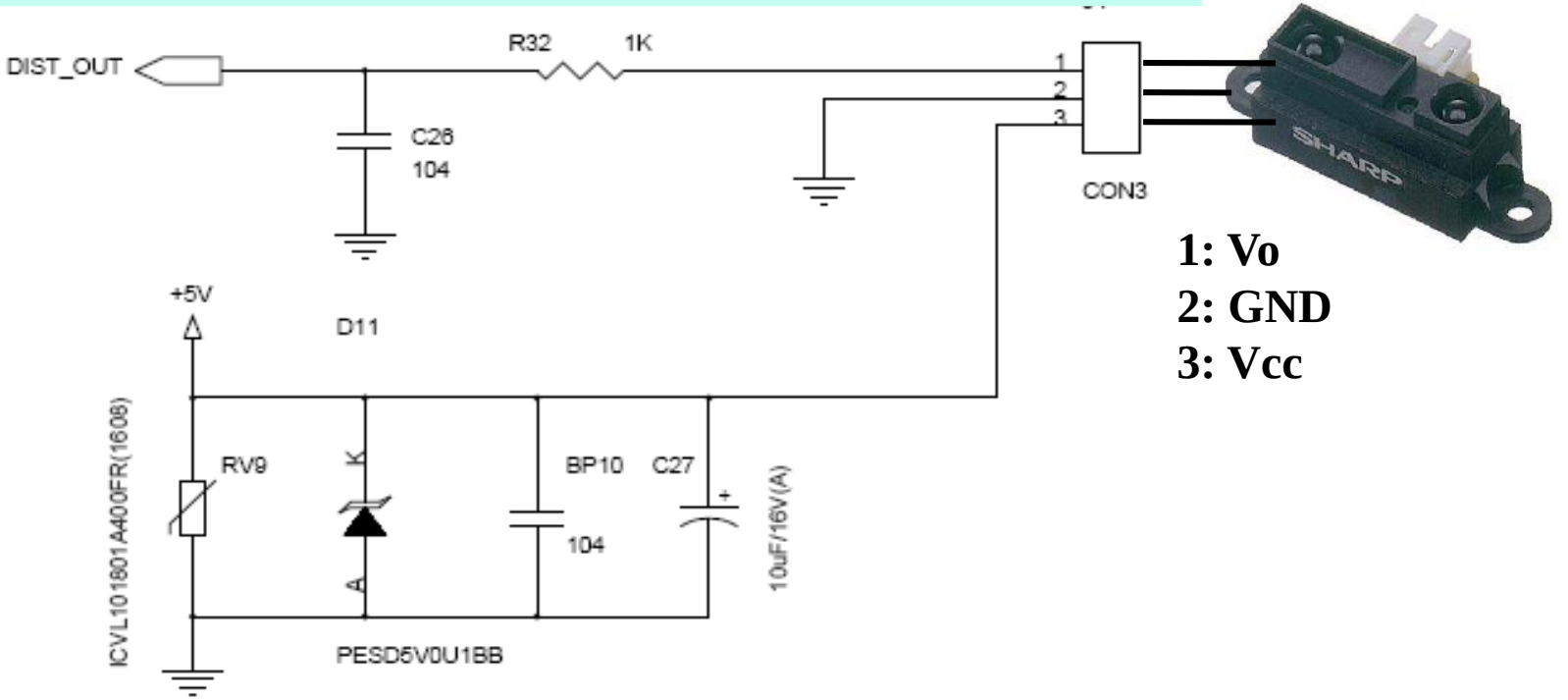


적외선 거리
측정 Sensor
(GP2Y0A21YK0F)

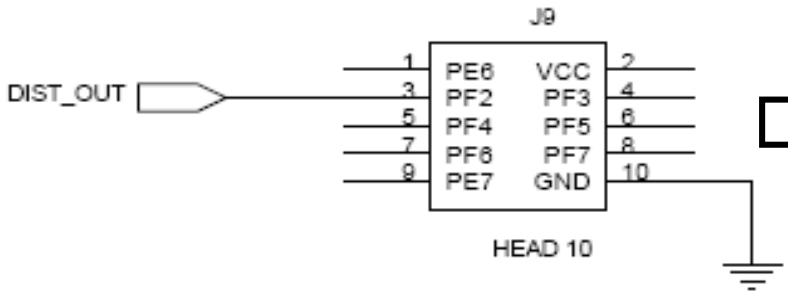
■Block diagram



거리 Sensor 인터페이스 회로(with u-processor)

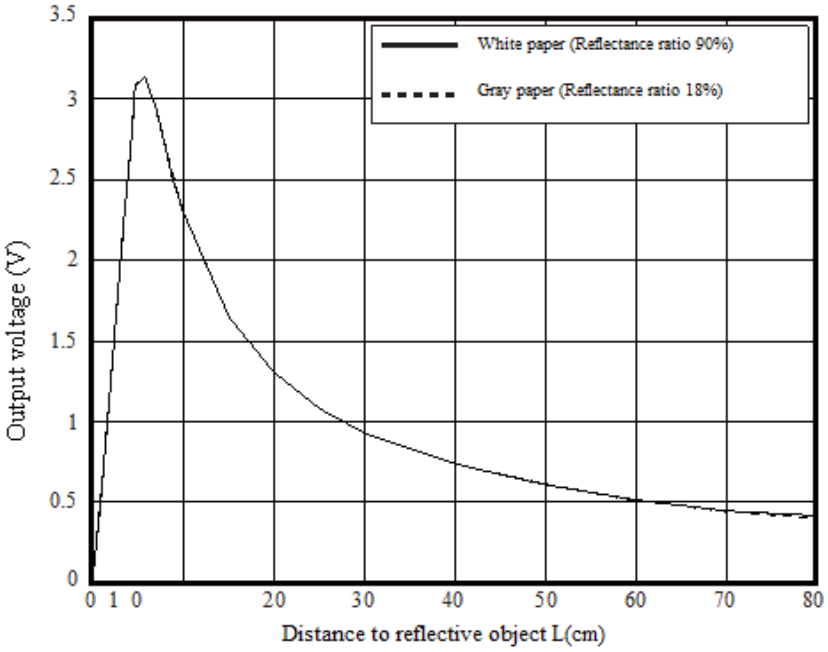


1: Vo
2: GND
3: Vcc

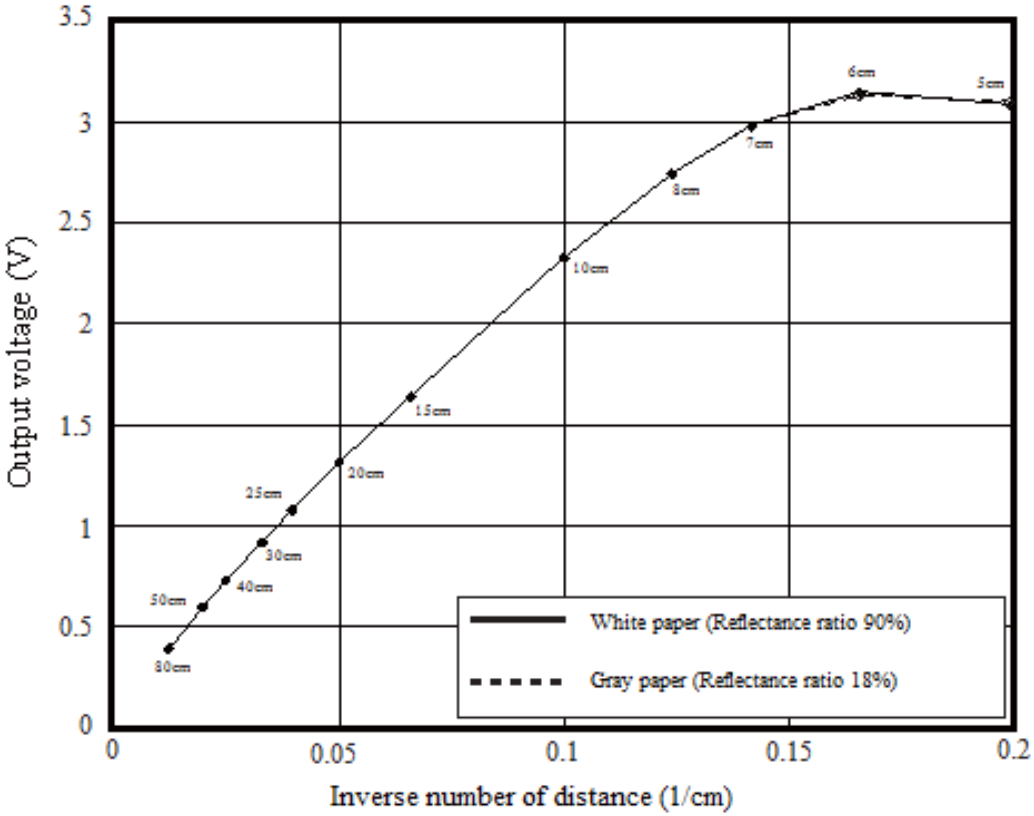


STM32F407(J2-ADC123_IN0(PA0))

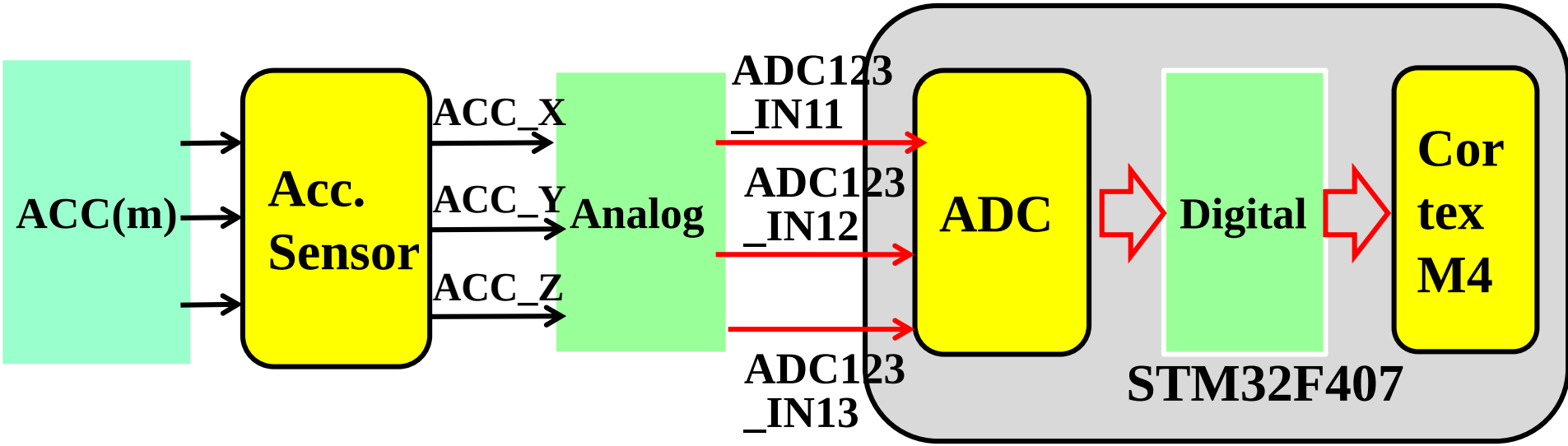
거리와 전압 사이 관계



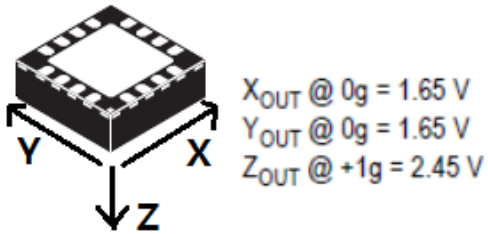
거리 측정범위: **10㎝~80㎝**



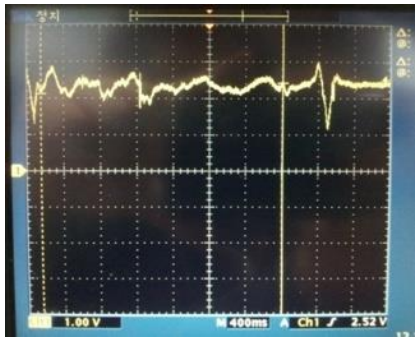
2. Acceleration Sensor Interface



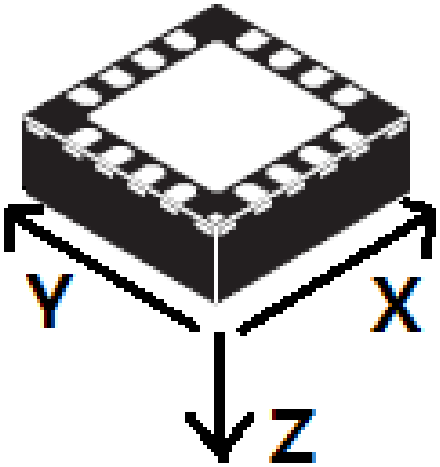
- ADC123_IN11 = PC1
- ADC123_IN12 = PC2
- ADC123_IN13 = PC3



가속도 측정 Sensor
(MMA7260QT)



Characteristic	Symbo	Min	Typ	Max	Unit
Output Signal Zero g (T_A = 25°C, V_{DD} = 3.3 V)(5)	V_{OFF}	1.485	1.65	1.815	V



X_{OUT} @ 0g = 1.65 V
Y_{OUT} @ 0g = 1.65 V
Z_{OUT} @ +1g = 2.45 V

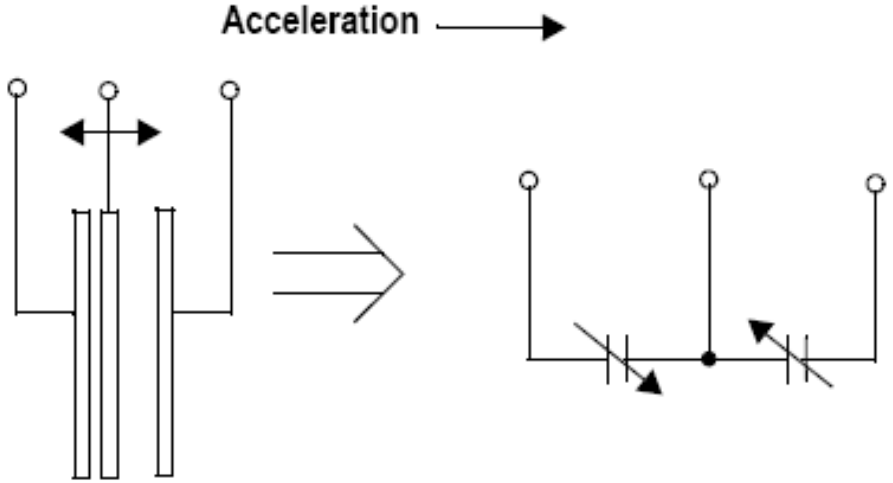
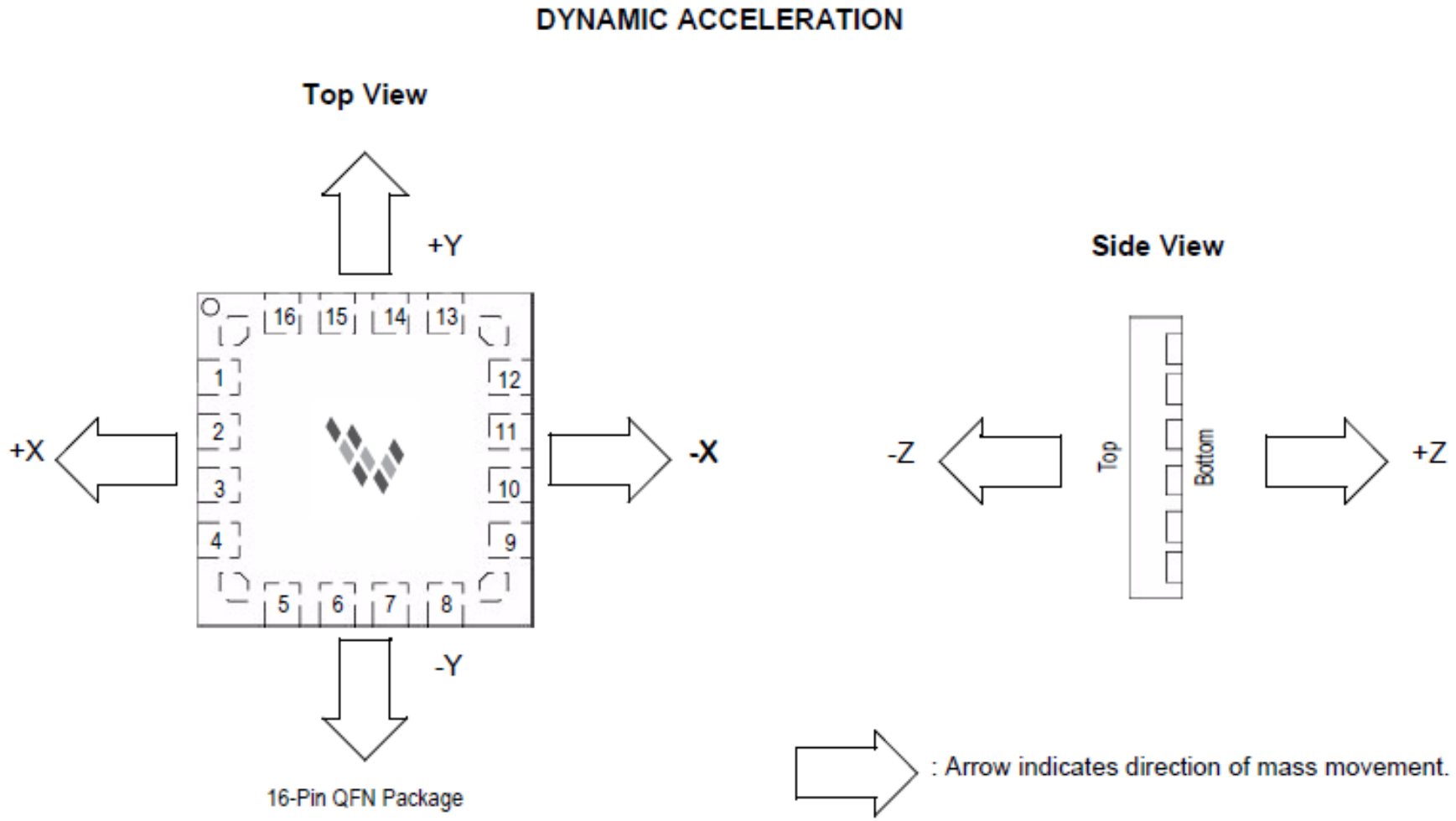
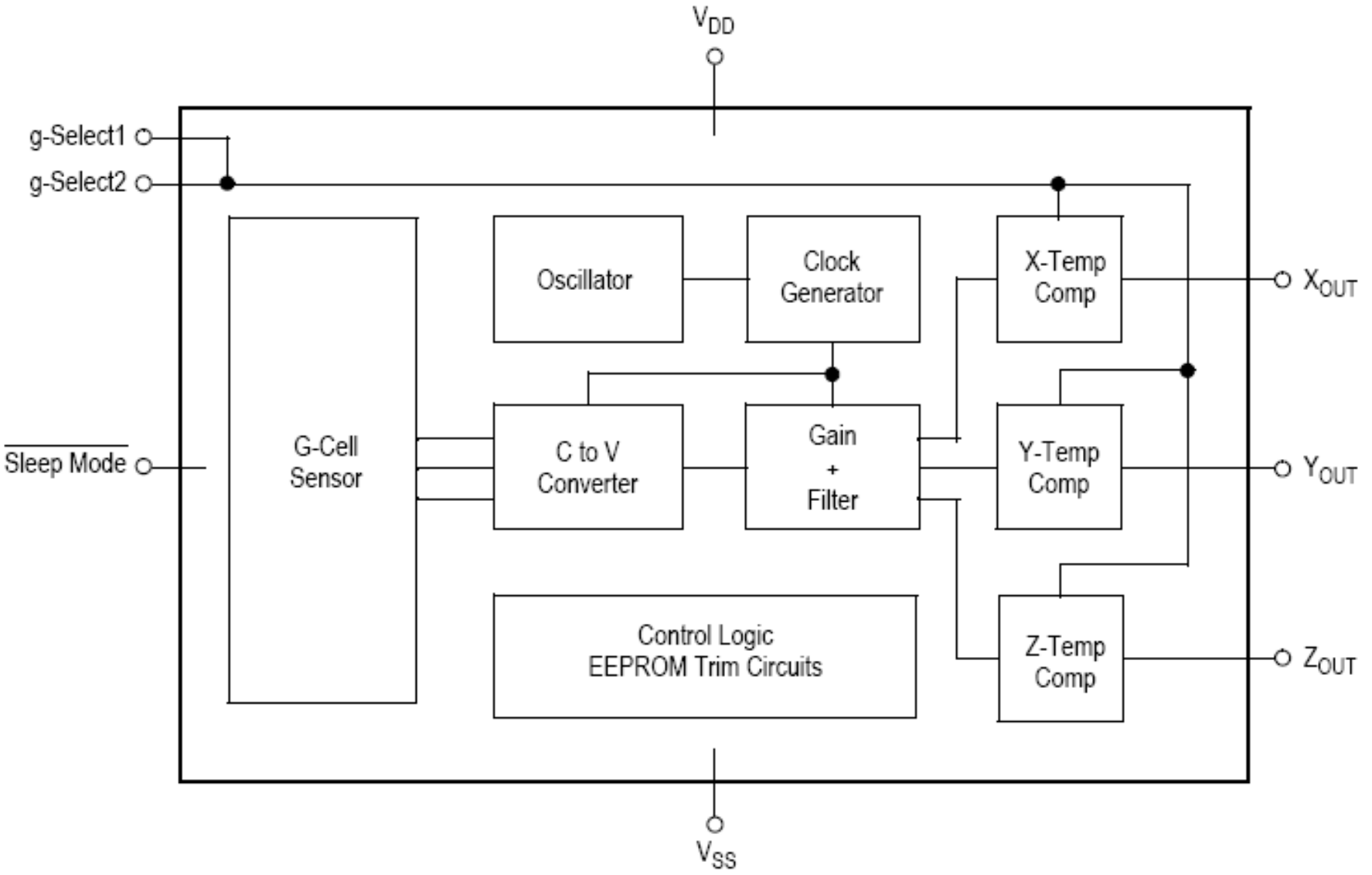


Figure 3. Simplified Transducer Physical Model

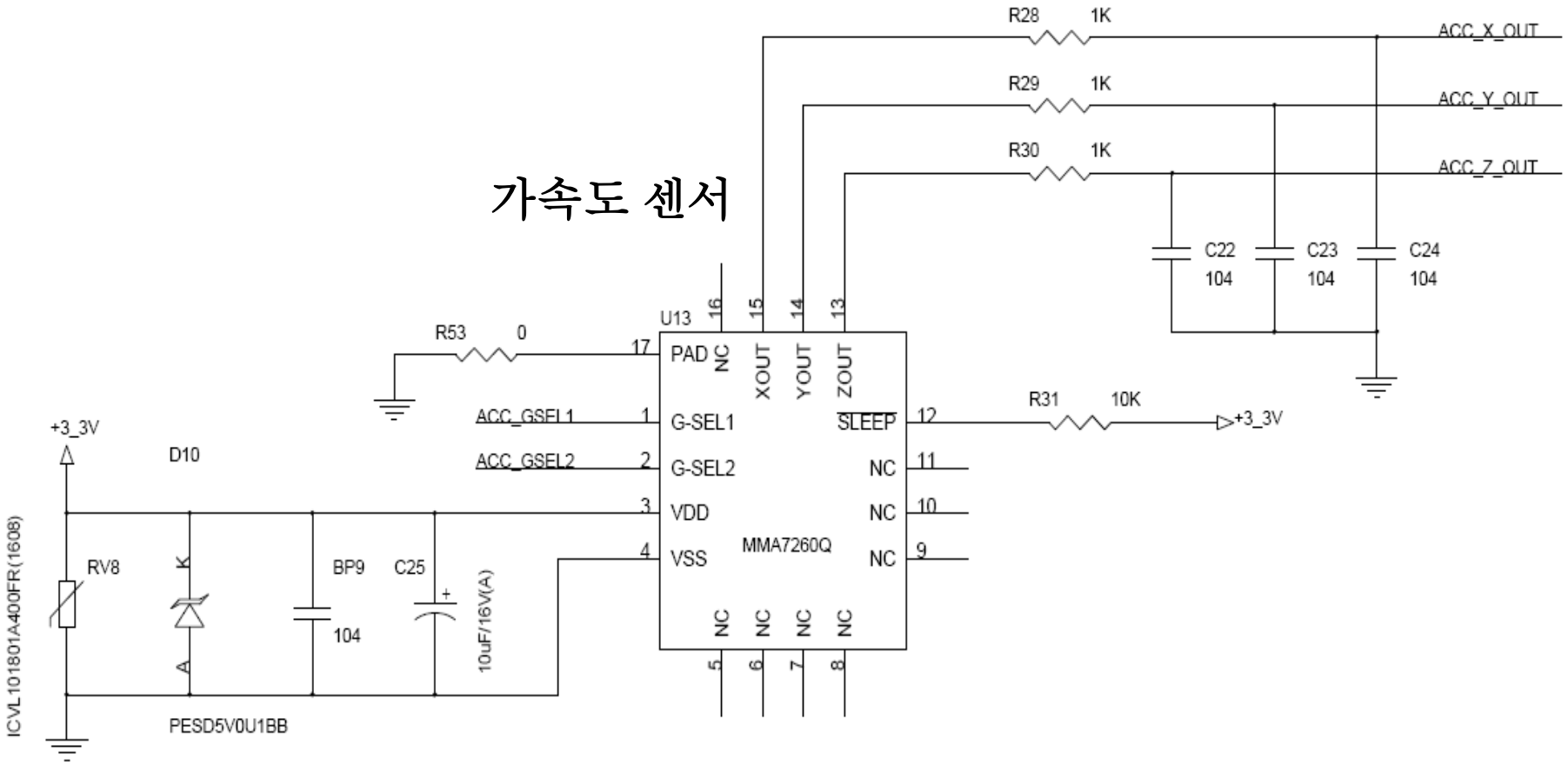
가속도 측정 Sensor (MMA7260QT) 가속도 축



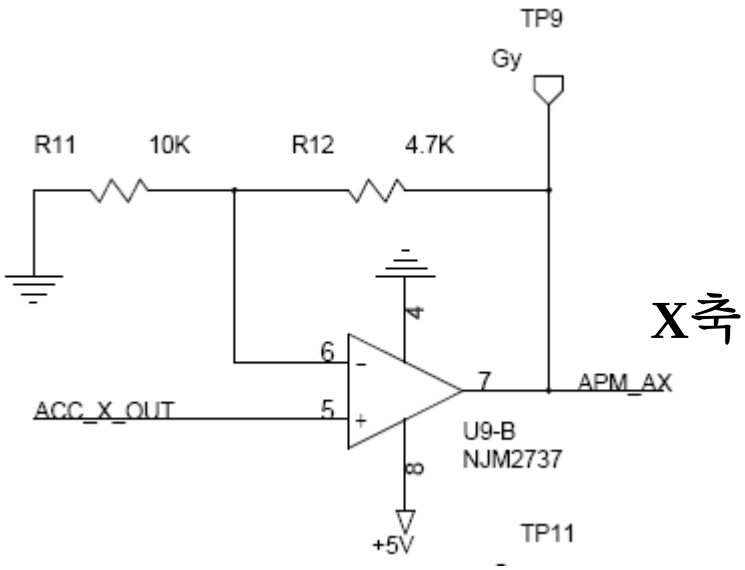
가속도 측정 Sensor (MMA7260QT) 내부 구성도

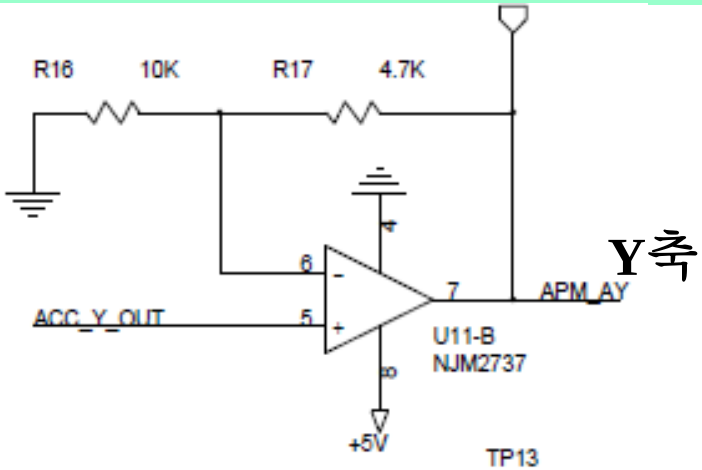


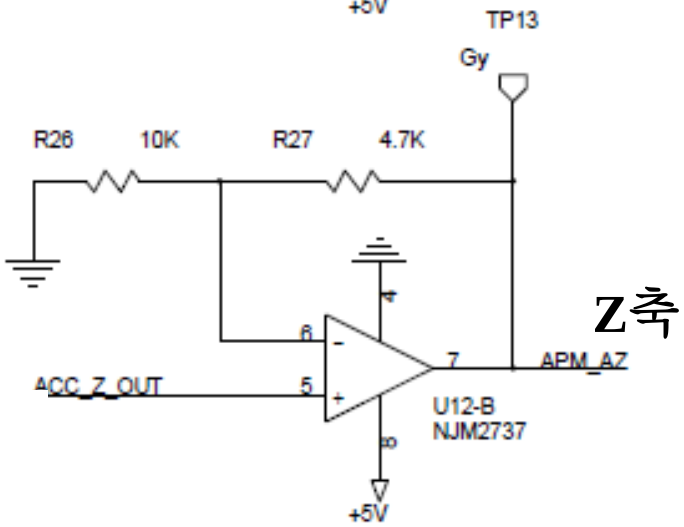
가속도 측정 Sensor 인터페이스 회로(with u-processor)



가속도 측정 Sensor 인터페이스 회로(with u-processor)

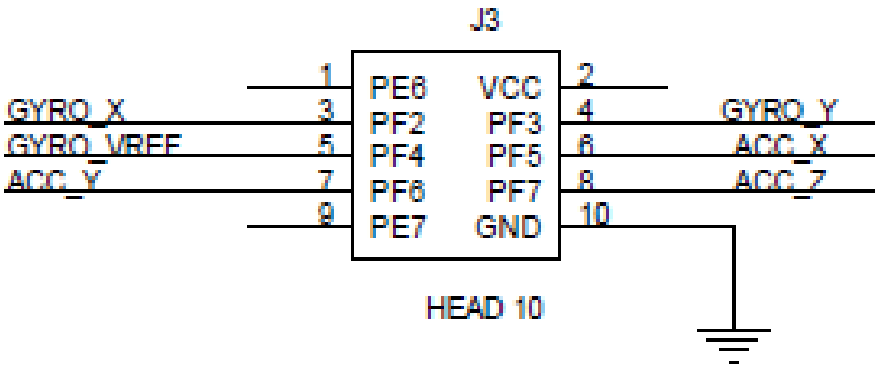






센서출력 증폭회로

증폭율: 1+ 4.7K/10K= 1.47



STM32F407 (PC1~3):
ADC123_IN11,12,13 (J2)