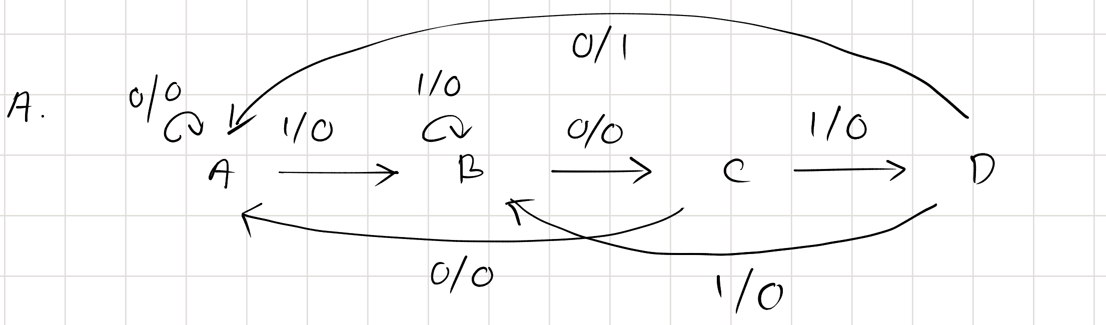
1.	Implement a sequence recognizer using T or J-K flip-flops that can detect the "1010" subsequences, while overlap will be supported between detected subsequences. For this design: A. Draw the state diagram by using gray code for assigning state. B. Draw the state table with output and Flip Flop inputs. C. Minimize the functions of output and Flip Flop inputs. D. Draw the circuit diagram using the block diagram of Flip Flops and basic gates. E. For an input bit sequence of x= "**101010001101001010**", what will be the output bit sequence?	 [1.5] [2] [2] [1.5] [1]

Disclaime: Benzir's brain can only consider overlap of a single bit. therefore no overlap in 1010.

A.



	next state		output	
	$x=0$	$x=1$	$x=0$	$x=1$
A (00)	A	B	0	0
B (01)	C	B	0	0
C (11)	A	D	0	0
D (10)	A	B	1	0

B.

Q_1	Q_0	x	Q_1	Q_0	y	T_1	T_0
0	0	0	0	0	0	0	0
0	0	1	0	1	0	0	1
0	1	0	1	1	0	1	0
0	1	1	0	1	0	0	0
1	0	0	0	0	1	1	0
1	0	1	0	1	0	1	1
1	1	0	0	0	0	1	1
1	1	1	1	0	0	0	1

C.

$$T_1 = Q_1\bar{Q}_0 + Q_0\bar{x}$$

$Q_1 \backslash Q_0x$	00	01	11	10
0				1
1	1	1		1

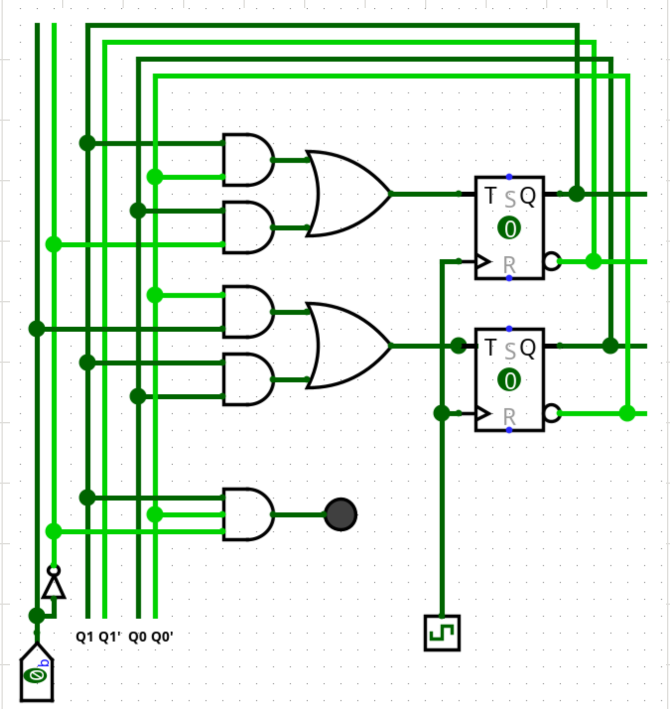
$$T_0 = \bar{Q}_0x + Q_1Q_0$$

$Q_1 \backslash Q_0x$	00	01	11	10
0		1	1	1
1		1		

$$y = Q_1\bar{Q}_0\bar{x}$$

$Q_1 \backslash Q_0x$	00	01	11	10
0				
1	1			

D.



E. input : 1 0 1 0 1 0 0 0 1 1 0 1 0 0 1 0 1 0

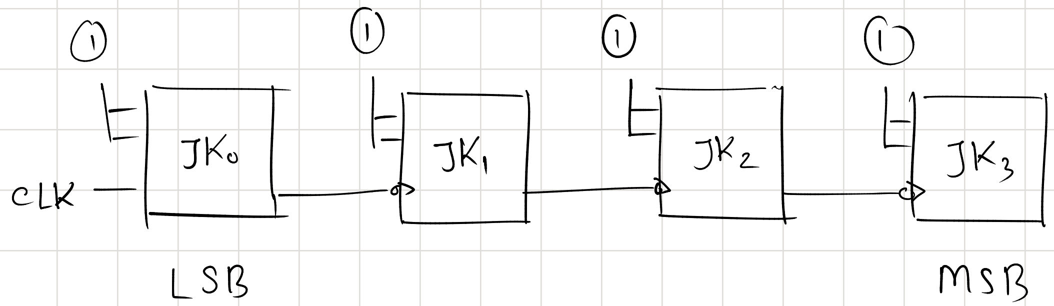
output : 0 0 0 1 0 0 0 0 0 0 0 0 1 0 0 0 0 1

2. A. Design a 3-bit universal shift register with the functions given in the function table below. Here two control bits X and Y determine the mode of operation. Use D Flip Flops for your design. [6]

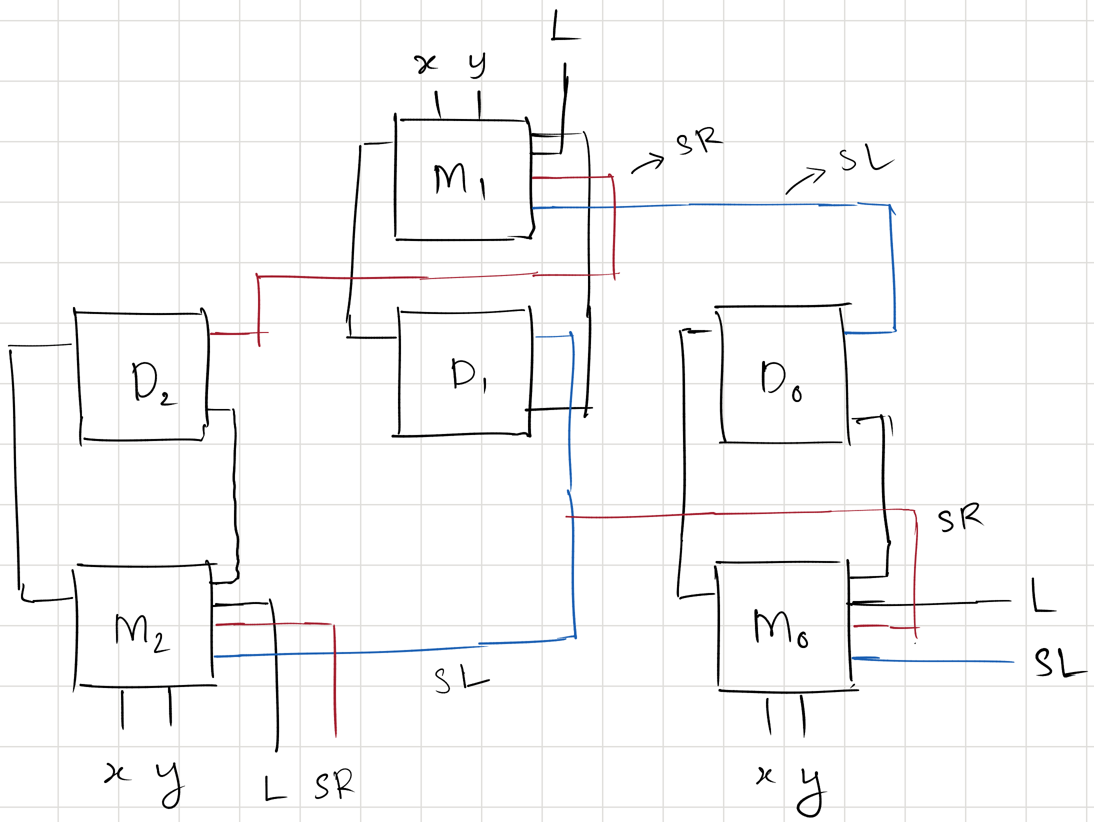
X	Y	Operation
0	0	Toggle
0	1	Parallel Load
1	0	Shift Right
1	1	Shift Left

B. Design a 4-bit asynchronous Downward Ripple Counter using negative edge J-K Flip Flops. [2]

B.



A.



3. A sequential circuit has two D flip flops, one input X, and one output y is specified by the following input equations:

$$A(t+1) = Ax \oplus B'x'$$
$$B(t+1) = (A' + B)x$$
$$y(t+1) = Ax' + (B' \oplus x)$$

A. Draw the logic diagram of the circuit. [2.5]
B. Derive the state table. [3]
C. Derive the state diagram. [2.5]

B. $A = Ax \oplus \bar{B}\bar{x}$

$= \overline{Ax}\,\bar{B}\bar{x} + Ax\,\overline{\bar{B}\bar{x}}$

$= (\bar{A} + \bar{x})\bar{B}\bar{x} + Ax(B + x)$

$= \bar{A}\bar{B}\bar{x} + \bar{B}\bar{x} + ABx + Ax$

$= \bar{A}\bar{B}\bar{x} + A\bar{B}\bar{x} + \bar{A}\bar{B}\bar{x} + ABx + ABx + A\bar{B}x$

$= \bar{A}\bar{B}\bar{x} + A\bar{B}\bar{x} + ABx + A\bar{B}x$

$= \Sigma m(0, 4, 5, 7)$

$B = (\bar{A} + B)x$

$= \bar{A}x + Bx$

$= \bar{A}Bx + \bar{A}\bar{B}x + ABx + \bar{A}Bx$

$= \bar{A}\bar{B}x + \bar{A}Bx + ABx$

$= \Sigma m(1, 3, 7)$

$y = A\bar{x} + (\bar{B} \oplus x)$

$= AB\bar{x} + A\bar{B}\bar{x} + Bx + \bar{B}\bar{x}$

$= AB\bar{x} + A\bar{B}\bar{x} + ABx + \bar{A}Bx + A\bar{B}\bar{x} + \bar{A}\bar{B}\bar{x}$

$= AB\bar{x} + A\bar{B}\bar{x} + ABx + \bar{A}Bx + \bar{A}\bar{B}\bar{x}$

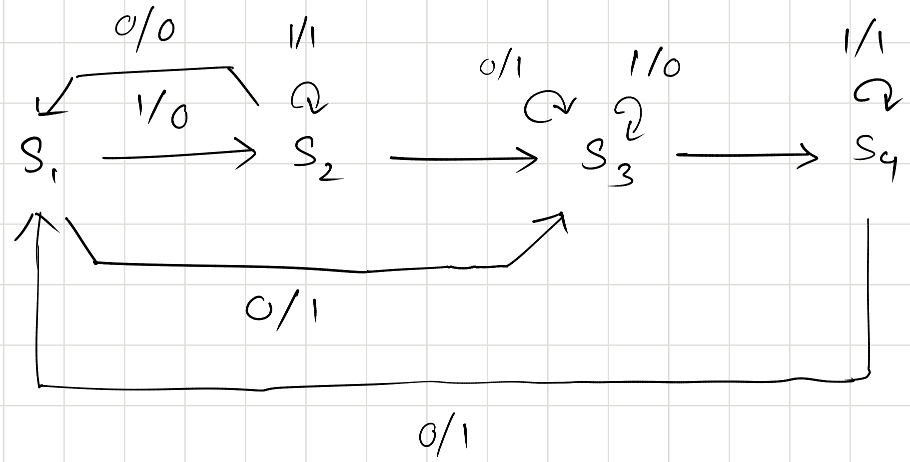
$= \Sigma m(6, 4, 7, 3, 0)$

$= \Sigma m(0, 3, 4, 6, 7)$

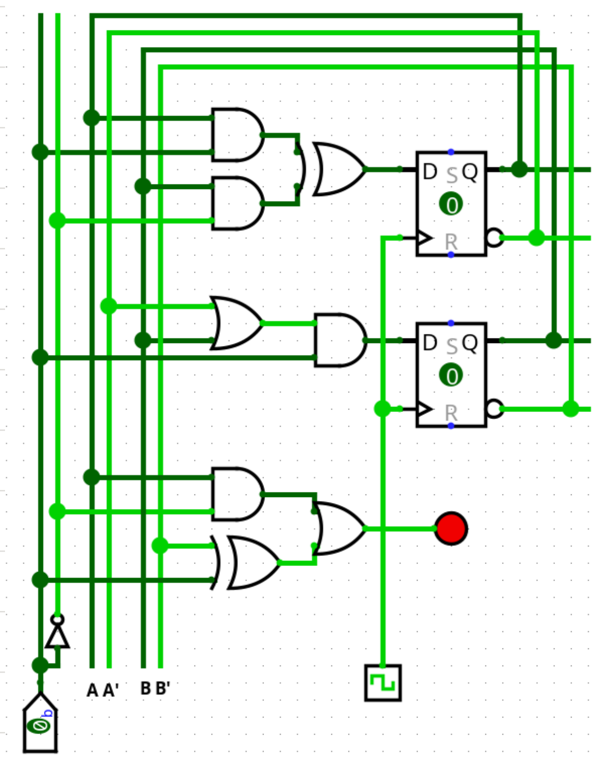
A	B	x	A	B	y
0	0	0	1	0	1
0	0	1	0	1	0
0	1	0	0	0	0
0	1	1	0	1	1
1	0	0	1	0	1
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	1	1	1

C.

	next state		output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
S_1 (00)	S_3	S_2	1	0
S_2 (01)	S_1	S_2	0	1
S_3 (10)	S_3	S_3	1	0
S_4 (11)	S_1	S_4	1	1



A.



4.	You are tasked with designing an alarm system for a security application. The system has multiple sensors: Door Sensor, Window Sensor, Motion Sensor, and Fire Sensor. Design a priority encoder circuit that detects the highest priority event among these sensors. Assume that Fire Sensor has the highest priority, followed by Motion Sensor, Door Sensor, and Window Sensor.	[4]

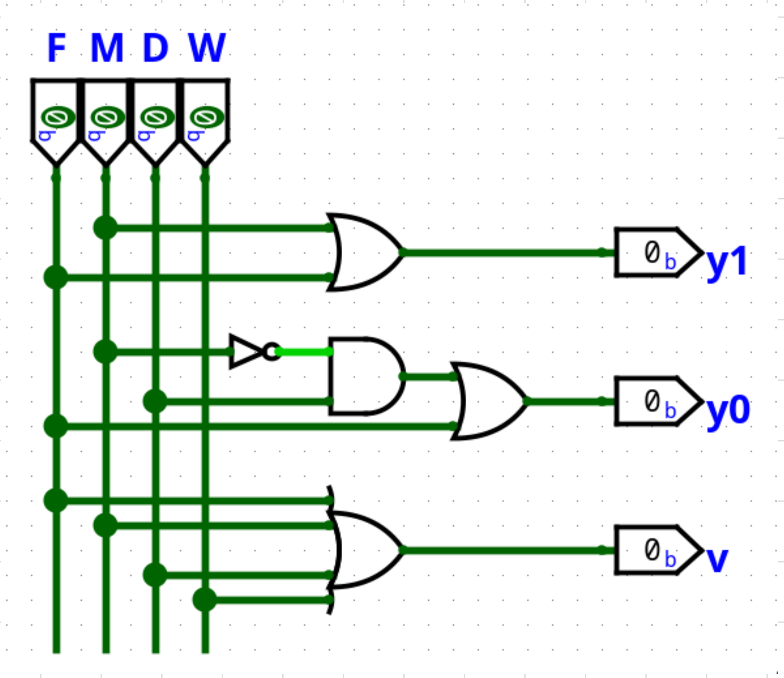
F	M	D	W	Y_1	Y_0	V
0	0	0	0	x	x	0
0	0	0	1	0	0	1
0	0	1	x	0	1	1
0	1	x	x	1	0	1
1	x	x	x	1	1	1

$Y_1 = M + F$

FM \ DW	00	01	11	10
00	x			
01	1	1	1	1
11	1	1	1	1
10	1	1	1	1

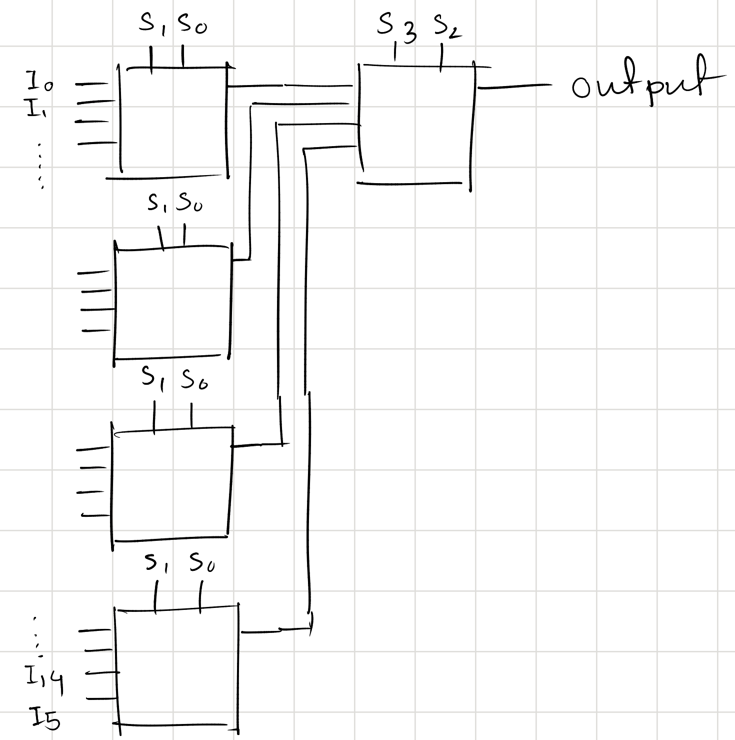
$Y_0 = \bar{M}D + F$

FM \ DW	00	01	11	10
00	x		1	1
01				
11	1	1	1	1
10	1	1	1	1



5.	Design a 16:1 MUX using 4:1 MUX (as many as you require) only.	[4]

inputs: $I_0 - I_{15}$ selects: $S_0 - S_3$



6.	Design an Octal to Binary Encoder. A. Draw the function table B. Write the equations for the output of your encoder. C. Draw the logic diagram of the encoder.	[4]

A.

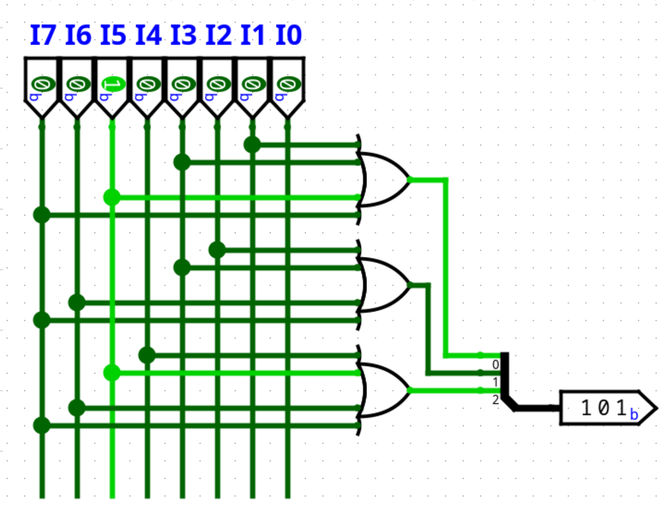
I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	Y_2	Y_1	Y_0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	1	0	0	0	1	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	1	0	1
0	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1

B. $Y_0 = I_1 + I_3 + I_5 + I_7$

$Y_1 = I_2 + I_3 + I_6 + I_7$

$Y_2 = I_4 + I_5 + I_6 + I_7$

C.



7.	Implement the following functions using a decoder and OR gates only. $F(X, Y, Z) = \prod M(0,3,5,6)$	[4]

$$F(x, y, z) = \prod M(0,3,5,6) = \sum m(1,2,4,7)$$