Machine Model

••

Java Virtual Machine

C

Operating System

Memory Hierarchy

Instruction Set Architecture

Hardware

Machine Model

Java Virtual Machine

C

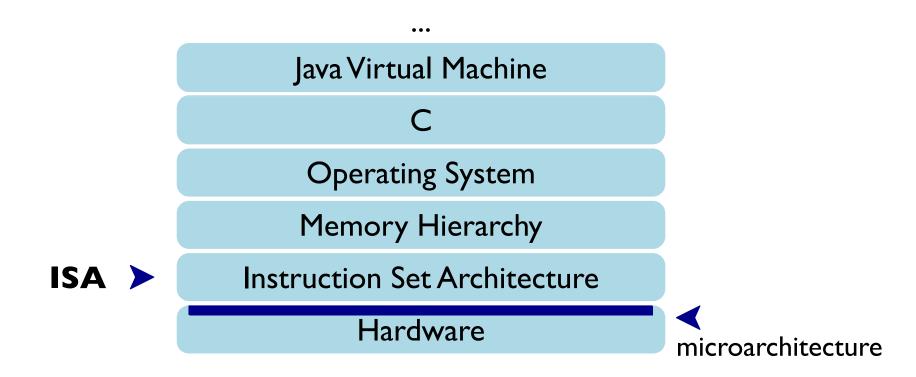
Operating System

Memory Hierarchy

ISA Instruction Set Architecture

Hardware

Machine Model



Instructions

```
pushq %rbx
movq %rdx, %rbx
call mult2
movq %rax, (%rbx)
popq %rbx
ret
```

Instructions

Assembly instructions

```
pushq %rbx
movq %rdx, %rbx
call mult2
movq %rax, (%rbx)
popq %rbx
ret
```

Instructions

Assembly instructions

```
pushq %rbx
movq %rdx, %rbx
call mult2
movq %rax, (%rbx)
popq %rbx
ret
```

Machine instructions

```
53
48 89 d3
e8 00 00 00 00
48 89 03
5b
c3
```

Example ISAs

x86 and x86-64 — desktop and server

ARM — mobile

IA64 (Itanium)

SPARC

POWER (PowerPC)

HPPA

680x0 (Motorola) 6502 (Motorola)

x86-64 Family History

1978: Intel 8086 and 80286

• 16-bit words

1980s: Intel 80386 and 486

• 32-bit words

1990s: Intel Pentium, AMD K5 and K6

• Still 32-bit words

2000s: AMD Athlon 64, Intel Core

• 64-bit words

Backward compatibility maintained for nearly 40 years!

CISC

complex instruction set

- Directly provide common operations
- Mixed instruction sizes;
 common things are compact

x86

RISC

reduced instruction set

- Provide simple and uniform primitives
- Similarly simple and uniform encoding

SPARC

MPIS

POWER

ARM

CISC

complex instruction set

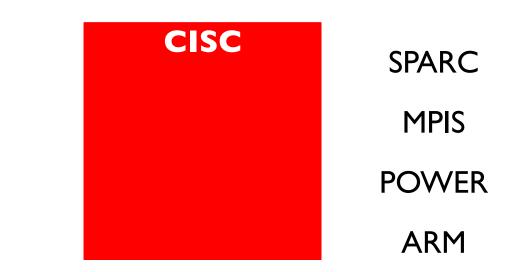
- Directly provide common operations
- Mixed instruction sizes;
 common things are compact

x86

RISC

reduced instruction set

- Provide simple and uniform primitives
- Similarly simple and uniform encoding



CISC

complex instruction set

- Directly provide common operations
- Mixed instruction sizes;
 common things are compact

RISC

reduced instruction set

- Provide simple and uniform primitives
- Similarly simple and uniform encoding

x86



SPARC

MPIS

POWER

ARM

CISC

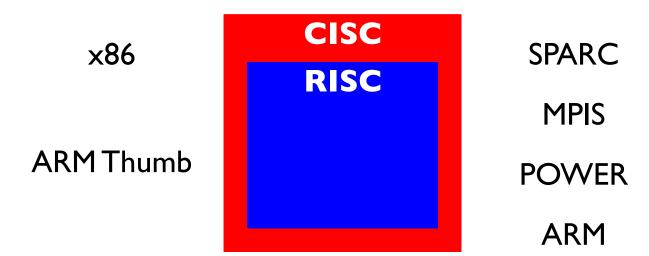
complex instruction set

- Directly provide common operations
- Mixed instruction sizes;
 common things are compact

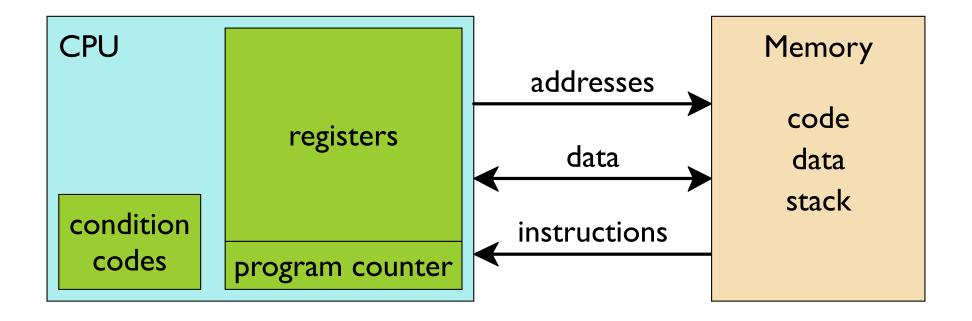
RISC

reduced instruction set

- Provide simple and uniform primitives
- Similarly simple and uniform encoding



Machine Code View



CPU

registers

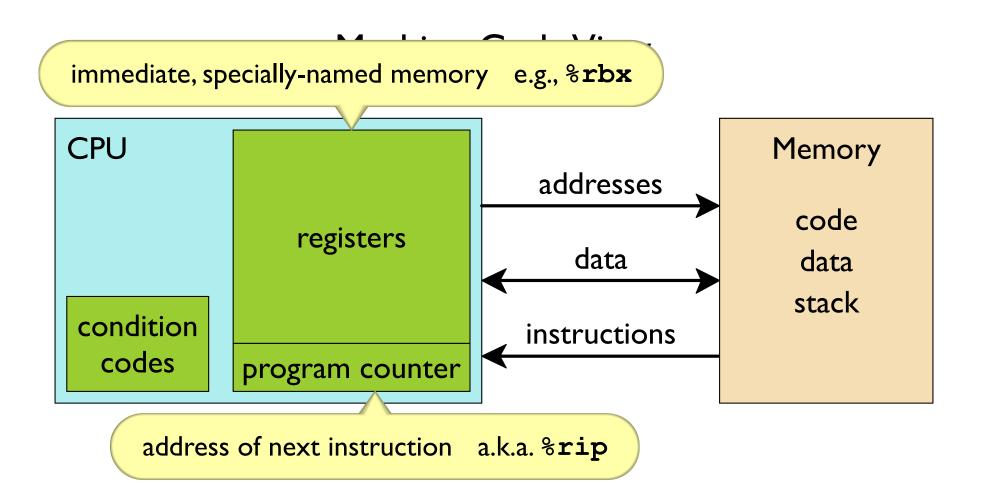
condition
codes

rogram counter

registers

e.g., % rbx

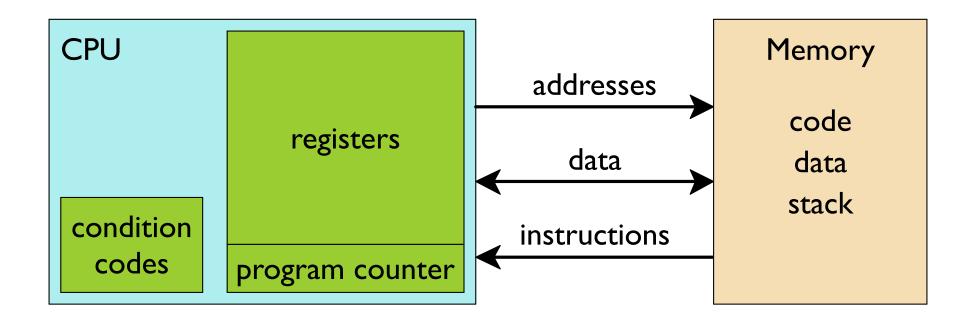
Memory
addresses
code
data
stack



immediate, specially-named memory e.g., %rbx **CPU** Memory addresses code registers data data stack condition instructions codes program counter address of next instruction a.k.a. %rip status of recent arithmetic or comparison e.g., cmpq \$0x5,%rdi

immediate, specially-named memory e.g., %rbx **CPU** Memory addresses code registers data data stack condition instructions codes program counter address of next instruction a.k.a. %rip byte-addressable status of recent arithmetic or comparison e.g., cmpq \$0x5,%rdi

Machine Code View



Instruction categories:

- Arithmetic: perform arithmetic on register or memory
- Data: transfer data between memory and registers
- Control: make program counter jump, (un)conditionally

Turning C into Machine Code

```
$ gcc -Og p1.c p2.c -lc -o p
$ ./p
```

text C: p1.c and p2.c

♣ compiler: gcc -0g -S

text Assembly: p1.s and p2.s

assembler: gcc or as

binary Object: p1.0 and p2.0

Library: libc.a

🦊 linker: gcc or ld 🔺

binary executable: p

C-to-Machine Example

```
long mult2(long a, long b);

void multstore(long x, long y, long *dest) {
  long t = mult2(x, y);
  *dest = t;
}
```

\$ gcc -S -Og multstore.c

```
pushq %rbx
movq %rdx, %rbx
call mult2
movq %rax, (%rbx)
popq %rbx
ret
```

```
53
48 89 d3
e8 00 00 00 00
48 89 03
5b
c3
```

\$ gcc -c multstore.s or gcc -c -Og multstore.c
\$ objdump -d multstore.o

Link

```
#include <stdio.h>
void multstore(long x, long y, long *dest);
long mult2(long a, long b) {
  return a*b;
}
int main() {
  long r;
  multstore(2, 3, &r);
  printf("%ld\n", r);
  return 0;
                                           Сору
```

```
$ gcc -c -Og main.c
$ gcc -o m main.o multstore.o
$ ./m
$ objdump -d m
```

Data Formats

An assembly instruction's suffix indicates the size of the operand Example: movq moves a "quad" word

Because x86 started as a 16-bit architecture:

```
b "byte" 8 bits char
w "word" 16 bits short
1 "long word" 32 bits int
q "quad word" 64 bits long
```

Floating-point operations:

```
s "single precision" 32 bits float1 "double precision" 64 bits double
```

No aggregate types, such as arrays and structures. Those are generated by the compiler from these primitive formats.

Register Names

63	32	16	8 0
%rax	%eax	%ax	%al
%rbx	%ebx	%bx	%bl
%rcx	%ecx	%CX	%cl
%rdx	%edx	%dx	%dl
%rsi	%esi	%si	%sil
%rdi	%edi	%di	%dil
%rbp	%ebp	%bp	%bpl
%rsp	%esp	%sp	%spl
%r8	%r8d	%r8w	%r8b

%r15

%r15d

%r15w %r15b

Operand Examples

M[addr] = the value stored at addr in memory

R[reg] = the value stored in the register named reg

%eax	register	R[%eax]
\$0x2a3 0x2a3	literal absolute	0x2a3 M[0x2a3]
(%eax) 7 (%edx)	indirect base + displacement	M[R[\$eax]] M[7 + R[\$edx]]
(%eax,%ecx) 7(%eax,%ecx)	indexed indexed	M[R[\$eax] + R[\$ecx]] M[7 + R[\$eax] + R[\$ecx]]
<pre>(,%eax,4) 7(,%eax,4) (%eax,%ecx,4) 7(%eax,%ecx,4)</pre>	scaled indexed scaled indexed scaled indexed scaled indexed	$M[R[\$eax] \times 4]$ $M[7 + R[\$eax] \times 4]$ $M[R[\$eax] + R[\$ecx] \times 4]$ $M[7 + R[\$eax] + R[\$ecx] \times 4]$

CPU

register value %eax 0x200 %ecx 0x41 %edx 0x4

Memory

address value
0x200 0x12
0x204 0x2a
0x208 0xd4
0x20c 0xfd

operand meaning value

\$0x204

%eax

(%eax)

0x208

(%edx,%ecx,8)

0x1f8(,%edx,4)

CPU

register	value
%eax %ecx	0x200 0x41
%edx	0 x 4

Memory

value
0x12
0x2a
0xd4
0xfd

```
operand
                    meaning
                    0x204
```

\$0x204

%eax

(%eax)

0x208

(%edx, %ecx, 8)

0x1f8(,%edx,4)

value

CPU

register value %eax 0x200 %ecx 0x41 %edx 0x4

Memory

address value
0x200 0x12
0x204 0x2a
0x208 0xd4
0x20c 0xfd

operand \$0x204

meaning 0x204

value 0x204 = 516

%eax

(%eax)

0x208

(%edx,%ecx,8)

0x1f8(,%edx,4)

CPU

register value %eax 0x200 %ecx 0x41 %edx 0x4

meaning

R[%eax]

0x204

Memory

address value
0x200 0x12
0x204 0x2a
0x208 0xd4
0x20c 0xfd

operand

\$0x204

%eax

(%eax)

0x208

(%edx, %ecx, 8)

0x1f8(,%edx,4)

value

0x204 = 516

CPU

register	value
%eax	0x200
%ecx	0x41
%edx	0x4

meaning

R[%eax]

0x204

Memory

address value
0x200 0x12
0x204 0x2a
0x208 0xd4
0x20c 0xfd

operand

\$0x204

%eax

(%eax)

0x208

(%edx, %ecx, 8)

0x1f8(,%edx,4)

value

0x204 = 516

0x200 = 512

CPU

register value %eax 0x200 %ecx 0x41 %edx 0x4

Memory

address value
0x200 0x12
0x204 0x2a
0x208 0xd4
0x20c 0xfd

operand

\$0x204

%eax

(%eax)

meaning

0x204

R[%eax]

M[R[\$eax]] = M[0x200]

g value

0x204 = 516

0x200 = 512

0x208

(%edx,%ecx,8)

0x1f8(,%edx,4)

CPU

register value 0x200%eax %ecx 0x41%edx 0x4 Memory

address value 0x200 0x120x204 0x2a 0x208 0xd40x20c 0xfd

operand meaning \$0x204 0x204

%eax

(%eax)

0x208

R[%eax]

M[R[\$eax]] = M[0x200]

value

0x204 = 516

0x200 = 512

0x12 = 18

0x1f8(,%edx,4)

(%edx, %ecx, 8)

CPU

register value %eax 0x200 %ecx 0x41 %edx 0x4

Memory

address value
0x200 0x12
0x204 0x2a
0x208 0xd4
0x20c 0xfd

operand meaning

\$0**x204** 0x204

R[\$eax]

(%eax) M[R[%eax]] = M[0x200]

0x208 M[0x208]

(%edx,%ecx,8)

0x1f8(,%edx,4)

value

0x204 = 516

0x200 = 512

0x12 = 18

CPU

register value %eax 0x200 %ecx 0x41 %edx 0x4

Memory

address value
0x200 0x12
0x204 0x2a
0x208 0xd4
0x20c 0xfd

operand meaning \$0x204 0x204

%eax

(%eax)

0x208

(%edx,%ecx,8)

meaning value

0x204

R[\$eax] 0x200 = 512

M[R[\$eax]] = M[0x200] 0x12 = 18

M[0x208]

0xd4 = 212

0x204 = 516

0x1f8(,%edx,4)

CPU

register value %eax 0x200 %ecx 0x41 %edx 0x4

Memory

address value
0x200 0x12
0x204 0x2a
0x208 0xd4
0x20c 0xfd

operand	meaning	value
\$0x204	0x204	0x204 = 516
%eax	R[%eax]	0x200 = 512
(%eax)	M[R[\$eax]] = M[0x200]	0x12 = 18
0x208	M[0x208]	0xd4 = 212
(%edx,%ecx,8)	$M[R[%edx]+R[%ecx]\times 8]$	

 $= M[0x4+0x41\times8] = M[0x20c]$

0x1f8(,%edx,4)

CPU

register	value
%eax	0 x 200
%ecx	0x41
%edx	0 x 4

0x1f8(,%edx,4)

Memory

address value
0x200 0x12
0x204 0x2a
0x208 0xd4
0x20c 0xfd

operand	meaning	value
\$0x204	0x204	0x204 = 516
%eax	R[%eax]	0x200 = 512
(%eax)	M[R[\$eax]] = M[0x200]	0x12 = 18
0x208	M[0x208]	0xd4 = 212
(%edx,%ecx,8)	$M[R[\$edx]+R[\$ecx]\times 8]$	0xfd = 253
	$= M[0x4+0x41\times8] = M[0x20c]$	
	- M[OR HOR HNO] - M[OR200]	

CPU

register value %eax 0x200 %ecx 0x41 %edx 0x4

Memory

address value
0x200 0x12
0x204 0x2a
0x208 0xd4
0x20c 0xfd

valua

operand	meaning	value
\$0x204	0x204	0x204 = 516
%eax	R[%eax]	0x200 = 512
(%eax)	M[R[\$eax]] = M[0x200]	0x12 = 18
0x208	M[0x208]	0xd4 = 212
(%edx,%ecx,8)	$M[R[%edx]+R[%ecx]\times 8]$	0xfd = 253
	$= M[0x4+0x41\times8] = M[0x20c]$	
0x1f8(,%edx,4)	$M[0x1f8+0+R[%edx]\times4]$	
	$= M[0x1f8+0+0x4\times4] = M[0x208]$	

Operand Practice

CPU

register value %eax 0x200 %ecx 0x41 %edx 0x4

Memory

address value
0x200 0x12
0x204 0x2a
0x208 0xd4
0x20c 0xfd

operand	meaning	value
\$0x204	0x204	0x204 = 516
%eax	R[%eax]	0x200 = 512
(%eax)	M[R[\$eax]] = M[0x200]	0x12 = 18
0x208	M[0x208]	0xd4 = 212
(%edx,%ecx,8)	$M[R[\$edx]+R[\$ecx]\times 8]$	0xfd = 253
	$= M[0x4+0x41\times8] = M[0x20c]$	
0x1f8(,%edx,4)	$M[0x1f8+0+R[%edx]\times4]$	0xd4 = 212
	$= M[0x1f8+0+0x4\times4] = M[0x208]$	

Copying Data

```
movx source, dest
```

Example:

```
movb $0xF, (%rbx)
```

 $movb \Rightarrow copy a byte$

 $\$0xF \Rightarrow copy$ the literal value 0xF

 $(%rbx) \Rightarrow copy it to the memory pointed at by %rbx$

Copying Data

```
movx source, dest
```

Example:

```
movw %ax, (%rsp)
```

movw ⇒ copy two bytes

%ax ⇒ copy it from the register %ax

(%rsp) \Rightarrow copy it to the current stack

Stack Shortcuts

pushx source

popx dest

Combines an adjustment of %rsp with a copy to/from memory it points to (i.e., the stack)

The stack grows ``down"

Example:

pushl %ebp

push1 ⇒ copy four bytes

push1 ⇒ decrement %rsp by four bytes

%ebp ⇒ copy four bytes from **%ebp** to memory now pointed at by **%rsp**

Stack Shortcuts

pushx source

popx dest

Combines an adjustment of %rsp with a copy to/from memory it points to (i.e., the stack)

The stack grows ``down"

Example:

popq %rax

popq ⇒ copy eight bytes

%rax ⇒ copy eight bytes from memory now pointed at by %rsp to %rax

popq ⇒ increment %rsp by eight bytes

```
int exchange(int *xp, int y) {
  int x = *xp;
  *xp = y;
  return x;
}
```

movq -0x18(%rbp),%rax
movl -0x1c(%rbp),%edx
movl (%rax),%ecx
movl %edx,(%rax)
movl %ecx,%eax
...

```
int exchange(int *xp, int y) {
  int x = *xp;
  *xp = y;
  return x;
```

```
without –Og, roughly
   movq -0x18(%rbp),%rax %rax = xp
   movl -0x1c(%rbp),%edx
   movl (%rax), %ecx
   movl %edx, (%rax)
   movl %ecx, %eax
```

```
int exchange(int *xp, int y) {
  int x = *xp;
  *xp = y;
  return x;
}
```

```
movq -0x18(%rbp),%rax
movl -0x1c(%rbp),%edx
movl (%rax),%ecx
movl %edx,(%rax)
movl %ecx,%eax
...
```

```
%rax = xp
%edx = y
```

```
int exchange(int *xp, int y) {
  int x = *xp;
  *xp = y;
  return x;
}
```

```
movq -0x18(%rbp),%rax
movl -0x1c(%rbp),%edx
movl (%rax),%ecx
movl %edx,(%rax)
movl %ecx,%eax
```

```
%rax = xp
%edx = y
%ecx = *xp
```

```
int exchange(int *xp, int y) {
  int x = *xp;
  *xp = y;
  return x;
}
```

```
movq -0x18(%rbp),%rax
movl -0x1c(%rbp),%edx
movl (%rax),%ecx
movl %edx,(%rax)
movl %ecx,%eax
```

```
%rax = xp
%edx = y
%ecx = *xp
put y in *xp
```

```
int exchange(int *xp, int y) {
  int x = *xp;
  *xp = y;
  return x;
```

without –Og, roughly

```
movq -0x18(%rbp),%rax
movl -0x1c(%rbp), %edx
movl (%rax),%ecx
movl %edx, (%rax)
movl %ecx, %eax
```

```
%rax = xp
%edx = y
ecx = *xp
put y in *xp
%eax = old *xp
```

```
void decode1(int *xp, int *yp, int *zp) {
}
```

```
movq 8(%rbp),%rdi
movq 16(%rbp),%rbx
movq 24(%rbp),%rsi
movl (%rdi),%eax
movl (%rbx),%edx
movl (%rsi),%ecx
movl %eax,(%rbx)
movl %edx,(%rsi)
movl %ecx,(%rdi)
```

```
void decode1(int *xp, int *yp, int *zp) {
}
```

```
movq 8(%rbp),%rdi
movq 16(%rbp),%rbx
movq 24(%rbp),%rsi
movl (%rdi),%eax
movl (%rbx),%edx
movl (%rsi),%ecx
movl %eax,(%rbx)
movl %edx,(%rsi)
movl %ecx,(%rdi)
```

%rdi = xp

```
void decode1(int *xp, int *yp, int *zp) {
}
```

```
movq 8(%rbp),%rdi
movq 16(%rbp),%rbx
movq 24(%rbp),%rsi
movl (%rdi),%eax
movl (%rbx),%edx
movl (%rsi),%ecx
movl %eax,(%rbx)
movl %edx,(%rsi)
movl %ecx,(%rdi)
```

```
%rdi = xp
%rbx = yp
```

```
void decode1(int *xp, int *yp, int *zp) {
}
```

```
movq 8(%rbp),%rdi
movq 16(%rbp),%rbx
movq 24(%rbp),%rsi
movl (%rdi),%eax
movl (%rbx),%edx
movl (%rsi),%ecx
movl %eax,(%rbx)
movl %edx,(%rsi)
movl %ecx,(%rdi)
```

```
%rdi = xp
%rbx = yp
%rsi = zp
```

```
void decode1(int *xp, int *yp, int *zp) {
}
```

```
movq 8(%rbp),%rdi
movq 16(%rbp),%rbx
movq 24(%rbp),%rsi
movl (%rdi),%eax
movl (%rbx),%edx
movl (%rsi),%ecx
movl %eax,(%rbx)
movl %edx,(%rsi)
movl %ecx,(%rdi)
```

```
%rdi = xp
%rbx = yp
%rsi = zp
%eax = *xp
```

```
void decode1(int *xp, int *yp, int *zp) {
}
```

```
movq 8(%rbp),%rdi
movq 16(%rbp),%rbx
movq 24(%rbp),%rsi
movl (%rdi),%eax
movl (%rbx),%edx
movl (%rsi),%ecx
movl %eax,(%rbx)
movl %edx,(%rsi)
movl %ecx,(%rdi)
```

```
void decode1(int *xp, int *yp, int *zp) {
}
```

```
movq 8(%rbp),%rdi
movq 16(%rbp),%rbx
movq 24(%rbp),%rsi
movl (%rdi),%eax
movl (%rbx),%edx
movl (%rsi),%ecx
movl %eax,(%rbx)
movl %edx,(%rsi)
movl %ecx,(%rdi)
```

```
%rdi = xp
%rbx = yp
%rsi = zp
%eax = *xp
%edx = *yp
%ecx = *zp
```

```
void decode1(int *xp, int *yp, int *zp) {
}
```

```
movq 8(%rbp),%rdi
movq 16(%rbp),%rbx
movq 24(%rbp),%rsi
movl (%rdi),%eax
movl (%rbx),%edx
movl (%rsi),%ecx
movl %eax,(%rbx)
movl %edx,(%rsi)
movl %ecx,(%rdi)
```

```
%rdi = xp
%rbx = yp
%rsi = zp
%eax = *xp
%edx = *yp
%ecx = *zp
put *xp in *yp
```

```
void decode1(int *xp, int *yp, int *zp) {

}
```

```
movq 8(%rbp),%rdi
movq 16(%rbp),%rbx
movq 24(%rbp),%rsi
movl (%rdi),%eax
movl (%rbx),%edx
movl (%rsi),%ecx
movl %eax,(%rbx)
movl %edx,(%rsi)
movl %ecx,(%rdi)
```

```
%rdi = xp
%rbx = yp
%rsi = zp
%eax = *xp
%edx = *yp
%ecx = *zp
put *xp in *yp
put old *yp in *zp
```

```
void decode1(int *xp, int *yp, int *zp) {
}
```

```
movq 8(%rbp),%rdi
movq 16(%rbp),%rbx
movq 24(%rbp),%rsi
movl (%rdi),%eax
movl (%rbx),%edx
movl (%rsi),%ecx
movl %eax,(%rbx)
movl %edx,(%rsi)
movl %ecx,(%rdi)
```

```
%rdi = xp
%rbx = yp
%rsi = zp
%eax = *xp
%edx = *yp
%ecx = *zp
put *xp in *yp
put old *yp in *zp
put old *zp in *xp
```

```
void decode1(int *xp, int *yp, int *zp) {
  int old_y = *yp, old_z = *zp;
  *yp = *xp;
  *zp = old_y;
  *xp = old_z;
}
```

```
movq 8(%rbp),%rdi
movq 16(%rbp),%rbx
movq 24(%rbp),%rsi
movl (%rdi),%eax
movl (%rbx),%edx
movl (%rsi),%ecx
movl %eax,(%rbx)
movl %edx,(%rsi)
movl %ecx,(%rdi)
```

```
%rdi = xp
%rbx = yp
%rsi = zp
%eax = *xp
%edx = *yp
%ecx = *zp
put *xp in *yp
put old *yp in *zp
put old *zp in *xp
```

Arithmetic Operations

addx source, dest	dest = dest + source
subx source, dest	dest = dest - source
imulx source, dest	dest = dest * source
salx source, dest	signed dest = dest << source
sarx source, dest	signed dest = dest >> source
shlx source, dest	unsigned dest = dest << source
shrx source, dest	unsigned dest = dest >> source
xor x source, dest	dest = dest ^ source
andx source, dest	dest = dest & source
orx source, dest	dest = dest source

Shortcuts: Simple Arithmetic

incx dest	dest = dest + I
decx dest	dest = dest - I
negx dest	dest = - dest
notx dest	dest = ∼ dest

Shortcut: Computing Addresses

leax source, destRegister

Like movx, but only computes an address that contains a value; the destination is always a regsiter

The same effect could be achieved with arithmetic operations

Example:

leaq ⇒ compute address as eight bytes

4 (%rbx, %rsp) \Rightarrow add %rbx and %rsp and 4

%rax ⇒ put that address in %rax

Shortcut: Computing Addresses

leax source, destRegister

Like movx, but only computes an address that contains a value; the destination is always a regsiter

The same effect could be achieved with arithmetic operations

Example:

leaq ⇒ compute address as eight bytes

 $(%rsp) \Rightarrow use the address in the register %rsp$

%rax ⇒ put that same address in %rax

```
long arith(long x, long y, long z) {
  long t1 = x+y;
  long t2 = z+t1;
  long t3 = x+4;
  long t4 = y * 48;
  long t5 = t3 + t4;
  long rval = t2 * t5;
  return rval;
```

```
leaq (%rdi,%rsi), %rax
addq %rdx, %rax
leaq (%rsi,%rsi,2), %rdx
salq $4, %rdx
leaq 4(%rdi,%rdx), %rcx
imulq %rcx, %rax
ret
```

```
long arith(long x, long y, long z) {
  long t1 = x+y;
  long t2 = z+t1;
  long t3 = x+4;
  long t4 = y * 48;
  long t5 = t3 + t4;
  long rval = t2 * t5;
  return rval;
```

```
leaq (%rdi,%rsi), %rax
addq %rdx, %rax
leaq (%rsi,%rsi,2), %rdx
salq $4, %rdx
leaq 4(%rdi,%rdx), %rcx
imulq %rcx, %rax
ret
```

```
long arith(long x, long y, long z) {
  long t1 = x+y;
  long t2 = z+t1;
  long t3 = x+4;
  long t4 = y * 48;
  long t5 = t3 + t4;
  long rval = t2 * t5;
  return rval;
```

```
leaq (%rdi,%rsi), %rax
addq %rdx, %rax
leaq (%rsi,%rsi,2), %rdx
salq $4, %rdx
leaq 4(%rdi,%rdx), %rcx
imulq %rcx, %rax
ret
```

```
%rax = t1 = x+y
%rax = t2 = z+t1
```

```
long arith(long x, long y, long z) {
  long t1 = x+y;
  long t2 = z+t1;
  long t3 = x+4;
  long t4 = y * 48;
  long t5 = t3 + t4;
  long rval = t2 * t5;
  return rval;
```

```
leaq (%rdi,%rsi), %rax
addq %rdx, %rax
leaq (%rsi,%rsi,2), %rdx
salq $4, %rdx
leaq 4(%rdi,%rdx), %rcx
imulq %rcx, %rax
ret
```

```
%rax = t1 = x+y
%rax = t2 = z+t1
%rdx = y*3
```

```
long arith(long x, long y, long z) {
  long t1 = x+y;
  long t2 = z+t1;
  long t3 = x+4;
  long t4 = y * 48;
  long t5 = t3 + t4;
  long rval = t2 * t5;
  return rval;
```

```
leaq (%rdi,%rsi), %rax
addq %rdx, %rax
leaq (%rsi,%rsi,2), %rdx
salq $4, %rdx
leaq 4(%rdi,%rdx), %rcx
imulq %rcx, %rax
ret
```

```
%rax = t1 = x+y
%rax = t2 = z+t1
%rdx = y*3
%rdx = y*48
```

```
long arith(long x, long y, long z) {
  long t1 = x+y;
  long t2 = z+t1;
  long t3 = x+4;
  long t4 = y * 48;
  long t5 = t3 + t4;
  long rval = t2 * t5;
  return rval;
```

```
leaq (%rdi,%rsi), %rax
addq %rdx, %rax
leaq (%rsi,%rsi,2), %rdx
salq $4, %rdx
leaq 4(%rdi,%rdx), %rcx
imulq %rcx, %rax
ret
```

```
%rax = t1 = x+y
%rax = t2 = z+t1
%rdx = y*3
%rdx = y*48
%rcx = t5 = x+4+y*48
```

```
long arith(long x, long y, long z) {
  long t1 = x+y;
  long t2 = z+t1;
  long t3 = x+4;
  long t4 = y * 48;
  long t5 = t3 + t4;
  long rval = t2 * t5;
  return rval;
```

```
leaq (%rdi,%rsi), %rax
addq %rdx, %rax
leaq (%rsi,%rsi,2), %rdx
salq $4, %rdx
leaq 4(%rdi,%rdx), %rcx
imulq %rcx, %rax
ret
```

```
%rax = t1 = x+y
%rax = t2 = z+t1
%rdx = y*3
%rdx = y*48
%rcx = t5 = x+4+y*48
%rax = t2*t5
```