02155 Computer Architecture and Engineering Fall 2019

Assignment 2

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This report contains "5" pages

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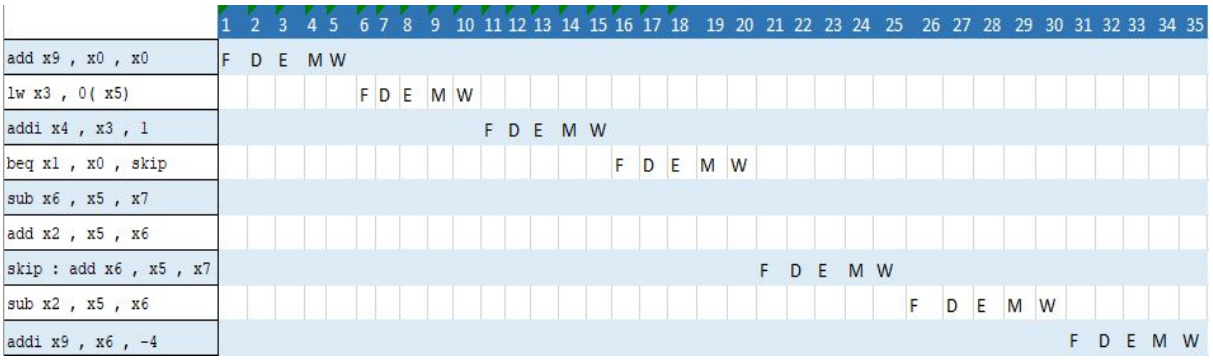
Exercise A2.1 - Exam problem (fall 2009)

1.A

P1 single cycle RISC-V processor (each instruction is executed in one clock cycle) with T_{clock} =5 ns.

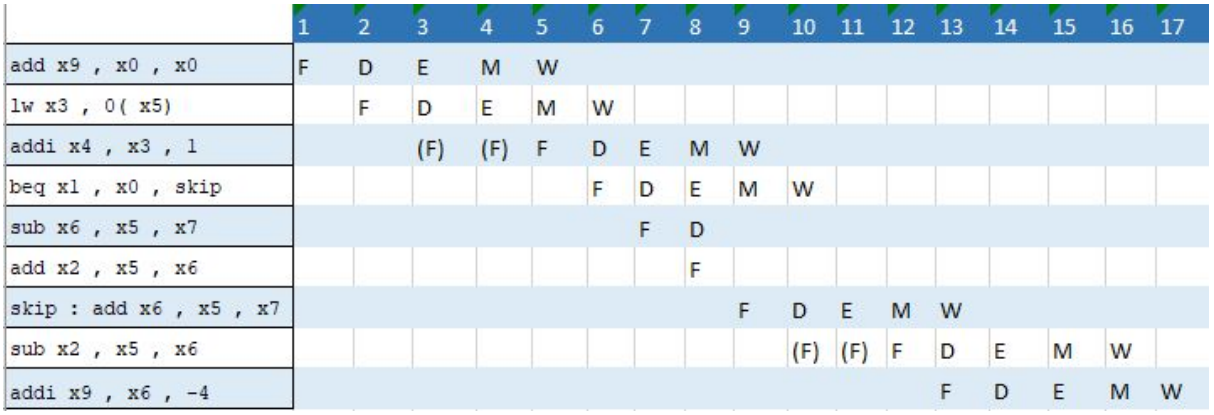


	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35
add x9 , x0 , x0	F	D	E	M	W																														
lw x3 , 0(x5)						F	D	E	M	W																									
addi x4 , x3 , 1											F	D	E	M	W																			
beq x1 , x0 , skip																F	D	E	M	W														
sub x6 , x5 , x7																																			
add x2 , x5 , x6																																			
skip : add x6 , x5 , x7																				F	D	E	M	W											
sub x2 , x5 , x6																									F	D	E	M	W						
addi x9 , x6 , -4																														F	D	E	M	W	

The execution of

$P_1 = T_{clock} \times \ clock\ cycle \ = 5ns \times 7 \ = 35ns$ as also seen from the diagram

P2: 5-stage pipelined RISC-V processor without data-forwarding, with Tclock = 1 ns
Branches are assumed not-taken.



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
add x9 , x0 , x0	F	D	E	M	W												
lw x3 , 0(x5)		F	D	E	M	W											
addi x4 , x3 , 1			(F)	(F)	F	D	E	M	W								
beq x1 , x0 , skip						F	D	E	M	W							
sub x6 , x5 , x7							F	D									
add x2 , x5 , x6								F									
skip : add x6 , x5 , x7									F	D	E	M	W				
sub x2 , x5 , x6										(F)	(F)	F	D	E	M	W	
addi x9 , x6 , -4													F	D	E	M	W

The execution of

$P_2 = T_{clock} \times \ clock\ cycle \ = 1ns \times 17 \ = 17ns$ as also seen from the diagram

P3: as P2, but with data-forwarding implemented.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
add x9 , x0 , x0	F	D	E	M	W									
lw x3 , 0(x5)		F	D	E	M	W								
addi x4 , x3 , 1			(F)	F	D	E	M	W						
beq x1 , x0 , skip					F	D	E	M	W					
sub x6 , x5 , x7						F	D							
add x2 , x5 , x6							F							
skip : add x6 , x5 , x7								F	D	E	M	W		
sub x2 , x5 , x6									F	D	E	M	W	
addi x9 , x6 , -4										F	D	E	M	W

The execution of $P_3 = T_{clock} \times clock\ cycle = 1ns \times 14 = 14\ ns$ as also seen from the diagram

1.B

Speed-up

$$\frac{P_1}{P_3} = \frac{35}{14} = 2.5$$

$$\frac{P_2}{P_3} = \frac{17}{14} = 1.2$$

We can conclude that P_3 is 2.5 faster than P_1 and 1.2 faster than P_2

Exercise A2.2 - Exam problem (fall 2011)

2.A

P1 5-stage pipelined RISC-V processor (stages: F, D, E, M, W) without data-forwarding, with T_{clock} =1 ns.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
add x5 , x0 , x0	F	D	E	M	W										
lw x4 , 0(x3)		F	D	E	M	W									
add x5 , x5 , x4			(F)	(F)	F	D	E	M	W						
lw x6 , 4(x3)						F	D	E	M	W					
add x5 , x5 , x6							(F)	(F)	F	D	E	M	W		
sw x5 , 8(x3)										(F)	(F)	F	D	E	M

W

The execution of

$P_1 = T_{clock} \times clock\ cycle = 1ns \times 16 = 16ns$ as also seen from the diagram

P2: as P1, but with data-forwarding implemented.

	1	2	3	4	5	6	7	8	9	10	11	12	13
add x5 , x0 , x0	F	D	E	M	W								
lw x4 , 0(x3)		F	D	E	M	W							
add x5 , x5 , x4			(F)	F	D	E	M	W					
lw x6 , 4(x3)					F	D	E	M	W				
add x5 , x5 , x6						(F)	F	D	E	M	W		
sw x5 , 8(x3)								(F)	F	D	E	M	W

The execution of

$P_2 = T_{clock} \times clock\ cycle = 1ns \times 13 = 13ns$ as also seen from the diagram

P1R: as P1, but with a compiler that can re-arrange instructions to reduce stalls.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
add x5 , x0 , x0	F	D	E	M	W										
lw x4 , 0(x3)		F	D	E	M	W									
lw x6 , 4(x3)			F	D	E	M	W								
add x5 , x5 , x4				(F)	F	D	E	M	W						
add x5 , x5 , x6							(F)	F	D	E	M	W			
sw x5 , 8(x3)									(F)	(F)	F	D	E	M	W

The execution of $P_{1R} = T_{clock} \times clock\ cycle = 1ns \times 15 = 15\ ns$ as also seen from the diagram

P2R: as P2, but with a compiler that can re-arrange instructions to reduce stalls.

	1	2	3	4	5	6	7	8	9	10
lw x4 , 0(x3)	F	D	E	M	W					
lw x6 , 4(x3)		F	D	E	M	W				
add x5 , x0 , x0			F	D	E	M	W			
add x5 , x5 , x4				F	D	E	M	W		
add x5 , x5 , x6					F	D	E	M	W	
sw x5 , 8(x3)						F	D	E	M	W

The execution of $P_{1R} = T_{clock} \times clock\ cycle = 1ns \times 10 = 10\ ns$ as also seen from the diagram

2.B

Speed-up

$$\frac{P_1}{P_{2R}} = \frac{16}{10} = 1.6$$

$$\frac{P_2}{P_{2R}} = \frac{13}{10} = 1.3$$

We can conclude that P_{2R} is 1.6 faster than P_1 and 1.3 faster than P_2

Exercise A2.3 - Exam problem (fall 2012)

A

To find the execution time when the clock rate is 2.0GHz we need to apply the formula of

CPU time = $\frac{CPUclockcycles}{clockrate}$

on the c program when execution time and clock rate are given, thereby we isolate the clock to use later.

$clockcyles = clockrate \cdot CPUtime$

$clockcyles = 2.4 * 10^9 \cdot 52*10^{(-3)} = 1.248000000 * 10^8$

now we apply the first formula to find out the execution time is when the clock rate is 2.0GHz

CPU time = $\frac{1.248000000*10^8}{2.0*10^9} = 0.06240000000s * 10^3 = 62.40000000ms$

finally the speed-up is

$\frac{CPU_{old}}{CPU_{time}} = \frac{52ms}{62.4ms} = 0.8333$

B

To find the clock rate in GHz we do $Hz = \frac{10^{12}}{600} = 1.666666667 * 10^9 Hz$

CPU time = $\frac{CPUclockcycles}{clockrate}$

CPU time = $\frac{1.248*10^8}{1.6*10^9} = 0.06240000000s * 10^3 = 62.40000000ms$

C

CPI = $\frac{CPUclockcycles}{Instructionscount}$

CPI = $\frac{1.248*10^8}{83.2*10^6} = 1.5$

D

To find the clock rate, we need to find what the clock cycle is.

clock cycle= CPI $\cdot Instrcutioncount 82\% = 1.5 \cdot \frac{100-18}{100} \cdot 83.2 \cdot 10^6$ which equals to $1.2 * 10^8$

clock rate=$\frac{clockcycle}{CPUtime}$ = $\frac{1.2*10^8}{52*10^{(-3)}}$= $1.9 * 10^8$=2.0GHz