THE CURIOUS CASE OF SR830:

MYSTERIOUS OSCILLATIONS OF THE LOCK-IN AMPLIFIER OUTPUT

by

Talha Jawad Ansari

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ABSTRACT

We document the oscillatory deviations of the SR830 lock-in amplifier output from a Butterworth-filter based theoretical model. A LabVIEW program is developed for experiment control and data acquisition. We obtain resonance response plots at the reference frequency of 32 765.00 Hz at time constants of 1 s, 10 s, and 30 s and filter roll-off settings of 6, 12, 18, and 24 dB/octave. Results show strong evidence of non-mitigating oscillations at 30 s time constant and 24 dB/octave filter roll-off. A discrete Fourier transform suggested that the oscillations comprised of several frequencies close to the harmonics of the reference and the lock-in input frequency.

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"The most beautiful thing we can experience is the mysterious. It is the source of all true art and true science."- Albert Einstein

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1. INTRODUCTION

1.1 Background

The Stanford Research System (SRS) SR830 DSP Lock in Amplifier has an important role in scientific and technical applications today. The digital nature of SR830 allows it to process signals and produce output that is remarkably close to a lock-in amplifier's theoretical model. However, during an experiment carried out at Middlebury College, the lock-in output showed evidence of non-mitigating oscillations, resulting in seemingly random deviations from its theoretical model. The results can be seen in Fig. 1.1.[1] These observations motivated an effort for a deeper understanding of the principles governing the SR830; and the pursuit of answers became an inspiration behind this project.

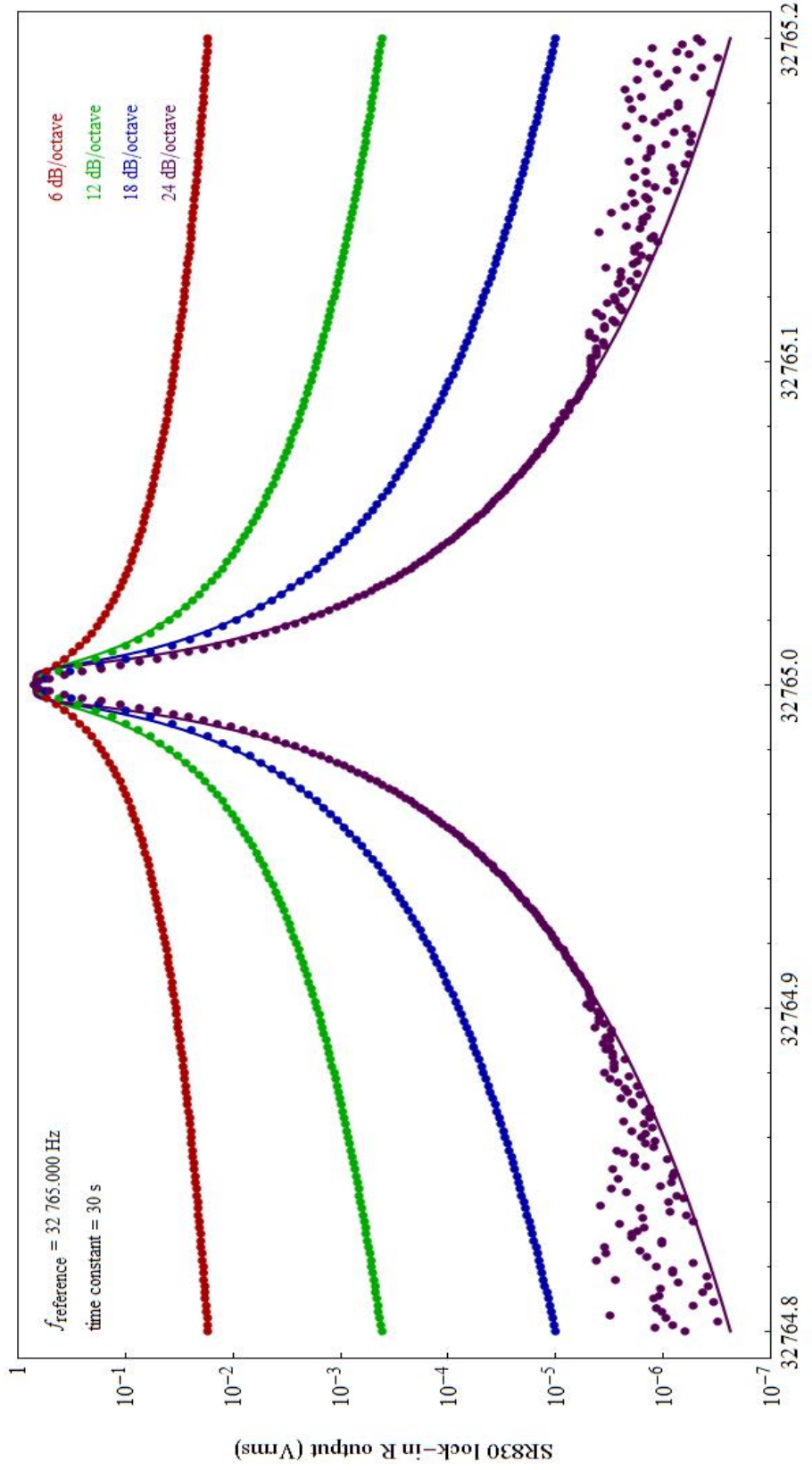


FIG. 1.1. Previously obtained resonance response plots (dots) of the SR830 lock-in amplifier showing deviations from the theoretical model (solid line).

1.2 What is a lock-in amplifier?

Since the start of the electronic age, one of the biggest challenges engineers have faced has been coping with the presence of noise in signals. In the field of noise reduction, Robert H. Dicke's discovery of a phase sensitive detection in 1960's was a major breakthrough.[2] A lock-in amplifier uses the phase sensitive detection to measure the amplitude and phase of signals of a known frequency in high noise environments, even when noise is thousand times larger.[3] The use of lock-in amplifiers is so widespread in the scientific industry today that it will be unrealistic to summarize it within the scope of this project.

Lock-in amplifiers function on the principle of phase-sensitive-detection (PSD). The input to the lock-in, which contains the signal and the noise, is multiplied by a reference wave of frequency equal to that of the input signal. This converts all the waves in the input with frequency at the reference frequency to DC, while everything else, including the noise, remains at a non-zero frequency. Passing the signal through a high-quality low-pass filter rejects the waves with non-zero frequencies, producing a DC output with amplitude which is proportional to the amplitude of the input signal.

The process of-noise reduction in a lock-in amplifier is achieved through its four main components: AC amplifier or band filter, voltage-controlled-oscillator (VCO), phase-sensitive-detector or multiplier, and low-pass filter. Figure 1.2 shows a schematic diagram of a basic lock-in with its main components.

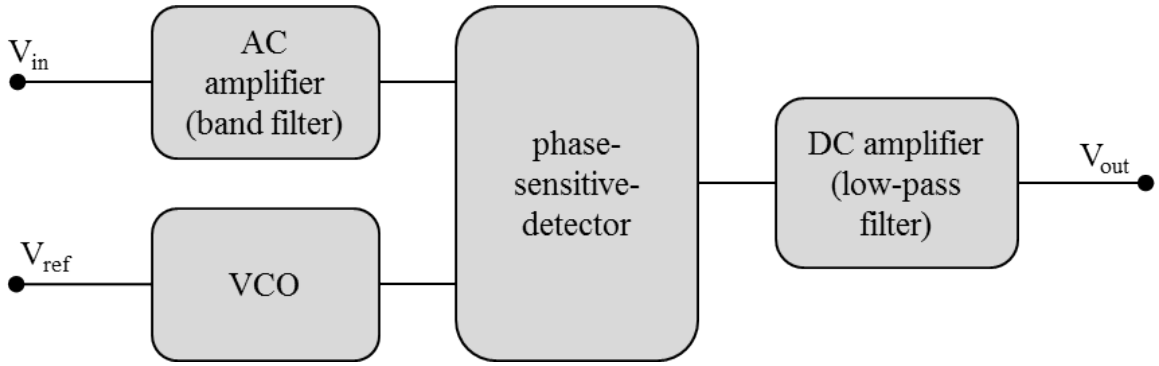


FIG. 1.2. Schematic diagram of a basic lock-in amplifier.

1.3 Mathematical foundations of a lock-in amplifier

Signal processing in a lock-in amplifier can be described mathematically. Assume that the input to the lock-in, V_{in}, consists of two parts, the signal V_{sig} and the noise V_{noise}. In this case, the signal can be a sine wave,

$$V_{sig}(t) = V_{sig_0} \sin(\omega_{sig} t + \theta_{sig}), \tag{1}$$

where V_{sig_0} represents the amplitude of $V_{sig}(t)$. The other part, noise, can potentially be made up of signals of many frequencies. Thus, V_{noise} is represented by a Fourier superposition of the form

$$V_{noise}(t) = \sum_n V_{noise_{n0}} \sin(\omega_{noise_n} t + \theta_{noise_n}), \tag{2}$$

where $V_{noise_{n0}}$ is the amplitude of the n^{th} term of the noise. In both Eqs. (1), and (2), ω is the angular frequency, related to the frequency by $\omega = 2\pi f$, and θ is the phase of the sinusoidal wave. The total input to the lock-in is thus of the form

$$V_{in}^*(t) = V_{sig_0} \sin(\omega_{sig} t + \theta_{sig}) + \sum_n V_{noise_{n0}} \sin(\omega_{noise_n} t + \theta_{noise_n}). \tag{3}$$

For explanatory purposes, we can simplify the sum in Eq. (3) to a single term, since it is possible to expand our analysis to the other terms as all terms in the end. A simplified version of Eq. (3) then becomes

$$V_{in}(t) = V_{sig_0} \sin(\omega_{sig} t + \theta_{sig}) + V_{noise_0} \sin(\omega_{noise} t + \theta_{noise}). \quad (4)$$

AC amplifier

The first main component of a lock-in, the AC amplifier, has two basic functions: it acts as a band-pass to reject noise at frequencies distant from ω_{ref}, and amplifies the band-pass output to enhance the waves with frequencies closer to ω_{ref}. The power-gain of the AC amplifier is referred to as the sensitivity of the lock-in. Assuming bandwidth of 100 Hz and a gain of *G*, the output from the AC amplifier becomes

$$V_{AC}(t) = G \left[V_{sig_0} \sin(\omega_{sig} t + \theta_{sig}) + V_{noise_0} \sin(\omega_{noise} t + \theta_{noise}) \right], \quad (5)$$

where the noise frequency, $2\pi\omega_{noise}$, is assumed to be within the bandwidth of the band-pass.

Voltage controlled oscillator (VCO)

A reference signal is an oscillating wave generated in the VCO, which is essentially a function generator with sine and TTL outputs. A reference signal is generated internally by the lock-in amplifier, and its frequency is determined either through the lock-in front panel, or through an external signal. The reference frequency, ω_{ref}, is the frequency at which the lock-in measures the input amplitude. In this case, $\omega_{ref} = \omega_{sig}$. Modern lock-in amplifiers, also called *dual-phase*, produce two reference signals at a phase difference of 90^{o} from eachother. The two sinusoidal reference signals with phase differences of $\theta_{ref}$and $\theta_{ref} + 90^{o}$ are then represented by

$$V_{ref1}(t) = V_{ref_0} \sin(\omega_{ref} t + \theta_{ref}), \tag{6}$$

and

$$V_{ref2}(t) = V_{ref_0} \cos(\omega_{ref} t + \theta_{ref}). \tag{7}$$

The 90^{o} phase shift for $V_{ref2}(t)$ has been incorporated in the change of sine wave into cosine. The reference signals $V_{ref}(t)$ are then passed to the phase-sensitive-detector (PSD) as one of its two multiplicands.

Phase-Sensitive-Detector (PSD)

The core of a lock-in amplifier is the PSD. A PSD multiplies $V_{AC}(t)$ with $V_{ref}(t)$. In the case of V_{ref1}, the output of a PSD becomes

$$V_{PSD1} = GV_{ref_0} \Big[V_{sig_0} \sin(\omega_{sig} t + \theta_{sig}) \sin(\omega_{ref} t + \theta_{ref}) + V_{noise_0} \sin(\omega_{noise} t + \theta_{noise}) \sin(\omega_{ref} t + \theta_{ref}) \Big]. \tag{8}$$

Expanding and using the double angle formula,[4]

$$\sin(A)\sin(B) = \frac{1}{2}[\cos(A - B) - \cos(A + B)],$$

on Eq. (8) gives

$$V_{PSD1}(t) = \frac{1}{2} G V_{sig_0} V_{ref_0} \Big[\cos\Big((\omega_{sig} - \omega_{ref})t + \theta_{sig} - \theta_{ref}\Big) - \cos\Big((\omega_{sig} + \omega_{ref})t + \theta_{sig} + \theta_{ref}\Big)\Big] + \frac{1}{2} G V_{noise} \;\; V_{ref_0}\big[\cos\big((\omega_{noise} - \omega_{ref})t + \theta_{noise} - \theta_{ref}\big) - \cos\big((\omega_{noise} + \omega_{ref})t + \theta_{noise} + \theta_{ref}\big)\big]. \quad (9)$$

Invoking the relationship $\omega_{ref} = \omega_{sig}$, and defining $\alpha_{\pm} = \omega_{noise} \pm \omega_{ref}$ and $\theta_{\pm} = \theta_{sig} \pm \theta_{ref}$, we obtain the final output of phase-sensitive-multiplication of V_{sig} by V_{ref1}

$$V_{PSD1}(t) = \frac{1}{2} G V_{sig_0} V_{ref_0}\big[\cos(\theta_{-}) - \cos\big(2\omega_{ref}t + \theta_{+}\big)\big] + \frac{1}{2} G V_{noise} \;\; V_{ref_0}\big[\cos\big(\alpha_{-}t + \theta_{noise} - \theta_{ref}\big) - \cos\big(\alpha_{+}t + \theta_{noise} + \theta_{ref}\big)\big]. \quad (10)$$

Repeating the same multiplication by V_{ref2} in Eq. (7) and using the double angle formula[5]

$$\sin(A)\cos(B) = \frac{1}{2}[\sin(A + B) + \sin(A - B)],$$

we obtain the second output of the PSD

$$V_{PSD2}(t) = \frac{1}{2} G V_{sig_0} V_{ref_0} \left[\sin\left(2\omega_{ref} t + \theta_+\right) + \sin(\theta_-)\right] + \frac{1}{2} G V_{noise_0} V_{ref_0} \left[\sin\left(\alpha_+ t + \theta_{noise} + \theta_{ref}\right) + \sin\left(\alpha_- t + \theta_{noise} - \theta_{ref}\right)\right]. \quad (11)$$

As can be seen in Eqs. (10), and (11), there are two distinct types of terms, or sums of terms, present in $V_{PSD}(t)$: a zero frequency DC wave and oscillating AC waves. Interestingly, the zero frequency term is also proportional to the amplitude of $V_{sig}(t)$, the signal we want to measure. Finally the output from the PSD is fed to the last component of a lock-in, a low-pass filter.

Low-pass filter

As a last step in the process, the low-pass filter rejects, at least theoretically, all the signals in the input that have non-zero frequencies. This leaves only the DC term from Eqs. (10)**,** and (11)**.** Practically, this is achieved by attenuating the AC parts of the waveform to zero over a set time constant. The time constant setting of the lock-in determines the steepness of the low-pass filter and essentially the ability of a lock-in to reject signals with a frequency other than the frequency of the signal. The DC output from the filter is adjusted for the factor of V_{ref_0}, G, and 1/2 to produce the two DC outputs of a lock-in,

$$X = V_{sig_0} \cos(\theta), \quad (12)$$

and

$$Y = V_{sig_0} \sin(\theta). \tag{13}$$

Where we have made the substitution $\theta \equiv \theta_{-}$ is made. Referring back to the simplification made for the expression of V_{noise} in Eq. (2), it can now be seen that all the terms of the noise sum of the Eq. (2) will be attenuated to zero by the low-pass filter – thus justifying our treatment of a single term as representative of the entire noise sum. As a the final step, the *X* and *Y* outputs may be converted to the more meaningful polar coordinates, as magnitude *R* and the phase θ, where

$$R = \sqrt{X^2 + Y^2} = V_{sig_0}, \tag{14}$$

and

$$\theta = \tan^{-1}\frac{Y}{X} = \theta_{sig} - \theta_{ref}. \tag{15}$$

As a convention, lock-in amplifiers give out the voltage output as root-mean-squared (rms) instead of the amplitude, in which case $R_{rms} = \frac{\sqrt{2}}{2} R$.

1.4 Model SR830 DSP Lock-in Amplifier

The goal of this senior project is to study the performance of the SR830 DSP Lock-in Amplifier by Stanford Research Systems (SRS), hereby referred to as the SR830. A picture of the front panel of the SR830, taken in Dunham Lab, is shown in Fig. 1.3. Instead of processing $V_{in}(t)$ in analog, as was the case in the previous SRS models, the SR830 converts the analog input into binary digits using a 16-bit A/D convertor sampling at 256 kHz. Thus, instead of the physical components of a lock-in described in the previous section, a digital lock-in processes a signal computationally in a digital signal processing unit (DSPU). The digital output is converted back to an analog before being transmitted at the BNC output connectors of the SR830 front panel.

FIG. 1.3. Front panel and the user interface of the SR830 lock-in amplifier.

The SR830 uses a low-power Motorola 24-bit DSP56001 for its computations. This digital signal processing unit (DSPU), based on a 33-MHz clock, is capable of executing a 1024-point complex Fast Fourier Transform in 1.98 milliseconds.[6] In order to

permit convenient loading of user programs onto the chip, the DSP56001 features 512 words of full-speed, on-chip program RAM memory, two 256-word data RAMs, two preprogrammed data ROMs, and special on-chip bootstrap hardware.

Digital lock-in amplifiers vs. the analog

One of the main ways in which a digital lock-in like the SR830 improves over their traditional analog versions, like the SR530, is in the attenuation of internal noise. In a digital lock-in, the only internal source of error is before the digitization process. Once the input is processed through the A/D convertor, no further error is introduced. This allows the lock-in to perform its computations efficiently. The robustness of a digital PSD in rejecting harmonics, output offsets, and AC-amplifier gain errors is particularly noteworthy. In addition, the 20-bit accuracy of the reference signal produced by the SR830 further lowers the harmonic content.[7]

In contrast to an analog low-pass filter, which has space and resource limitations and offers up to 6 dB/octave and 12 dB/octave roll-off settings, the digital nature of SR830 allows for an even higher roll off settings, such as 18 db/octave and 24 dB/octave. Greater roll-off compensates for lower time constants when dealing with a very high-noise signal, thus making the process more time-efficient. However, it will be worth studying why the SR830 allows for only four filter stages when a digital algorithm can theoretically allow for an even higher roll-off setting.

Despite the improvements, digital lock-in amplifiers have disadvantages. Firstly, as digital filters use a sampling process and discrete-time processing, they experience latency i.e. the difference in time between the input and the response. Furthermore, due to

the sampling nature of A/D convertor, the quality of a signal is reduced. This is particularly problematic for high frequency signals, reducing the dynamic range for the lock-in.

1.5 Butterworth filter in a lock-in amplifier

An ideal electrical filter should not only have a zero sensitivity in the 'stop' region but also uniform sensitivity in the 'pass' region.[8] Butterworth offered a theoretical model for a perfect filter by showing that any number of basic RLC elementary pairs of resistors, capacitors, and inductors can be combined to approach closer and closer to an ideal filter.[9] Figure 1.4 shows the schematic design of a generalized 3-stage Butterworth low-pass filter.

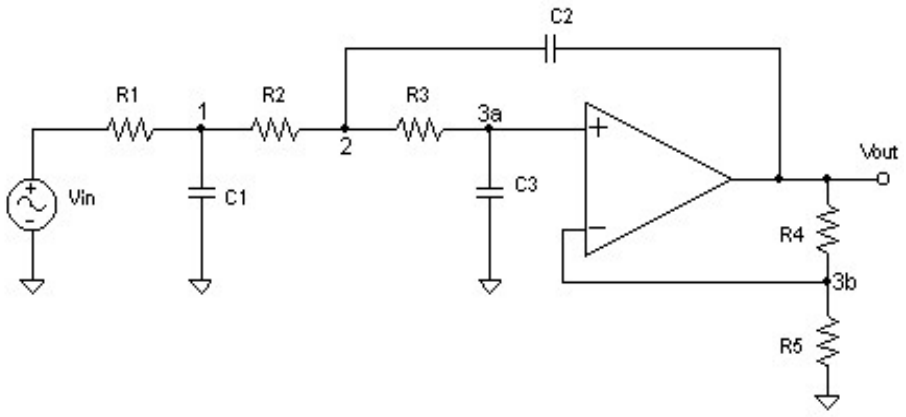


FIG. 1.4. Schematic design of an analog 3-stage Butterworth filter.[10]

With an input signal of V_{sig}, the output R_{rms} of a low-pass Butterworth filter for a lock-in amplifier is derived as [11]

$$R_{rms} = V_{sig_{rms}} \frac{1}{\sqrt{1 + \left[\frac{2\pi\left(f_{sig} - f_{ref}\right)}{\omega_B}\right]^{2m}}}, \tag{16}$$

where $\omega_B = 1/\tau$, f_{sig} and f_{ref} are the frequencies of the input and the reference signal, related to the angular frequencies ω_{sig} and ω_{ref} by the relation $\omega = 2\pi f$, and m is the number of stages of a Butterworth filter, also called the filter pole value. In our experiment, we assumed that the filter pole values of m = 1, 2, 3, and 4 corresponded to the filter roll off settings of 6, 12, 18, and 24 dB/octave respectively. Essentially, Eq. (16) represents the theoretical model for the SR830 output.

It is worth mentioning that, according to the SR830 specifications,[12] a single RC filter requires time of about five time constants to settle to its final value. Additionally, a low pass filter, with time constant of 1s, takes the value of previous four to five seconds and averages them.

2. EXPERIMENTAL PROCEDURE

2.1 Apparatus design

The apparatus for the experiment was set up as shown in Fig. 2.1**.** The time bases of two Agilent function generators of model 33220A were synchronized by connecting the 10-MHz back-panel output of the clock of one Agilent, hereby referred to as the *master*, to the 10-MHz back-panel input of the clock of other Agilent, hereby referred to as *slave*. The sync of the master Agilent was connected to the reference frequency input of SRS Model SR830 DSP Lock-in Amplifier and the slave Agilent was used to produce the input signal for the SR830. All three instruments were connected to a Dell OptiPlex 780 Windows PC through the General Purpose Interface Bus (GPIB). Equipment control and data acquisition were carried out through an internally developed LabVIEW program. The SR830 unit, S/N 76741**,** which was used while developing and testing the program, was replaced by S/N 76606 due to a reference frequency malfunction. The experimental apparatus was set up in the Dunham Lab, in basement of a six-floor concrete-walled building. The lack of electromagnetic signals present in the basement reduced ambient noise in the data. A picture of the apparatus during an experiment is shown in Fig. 2.2.

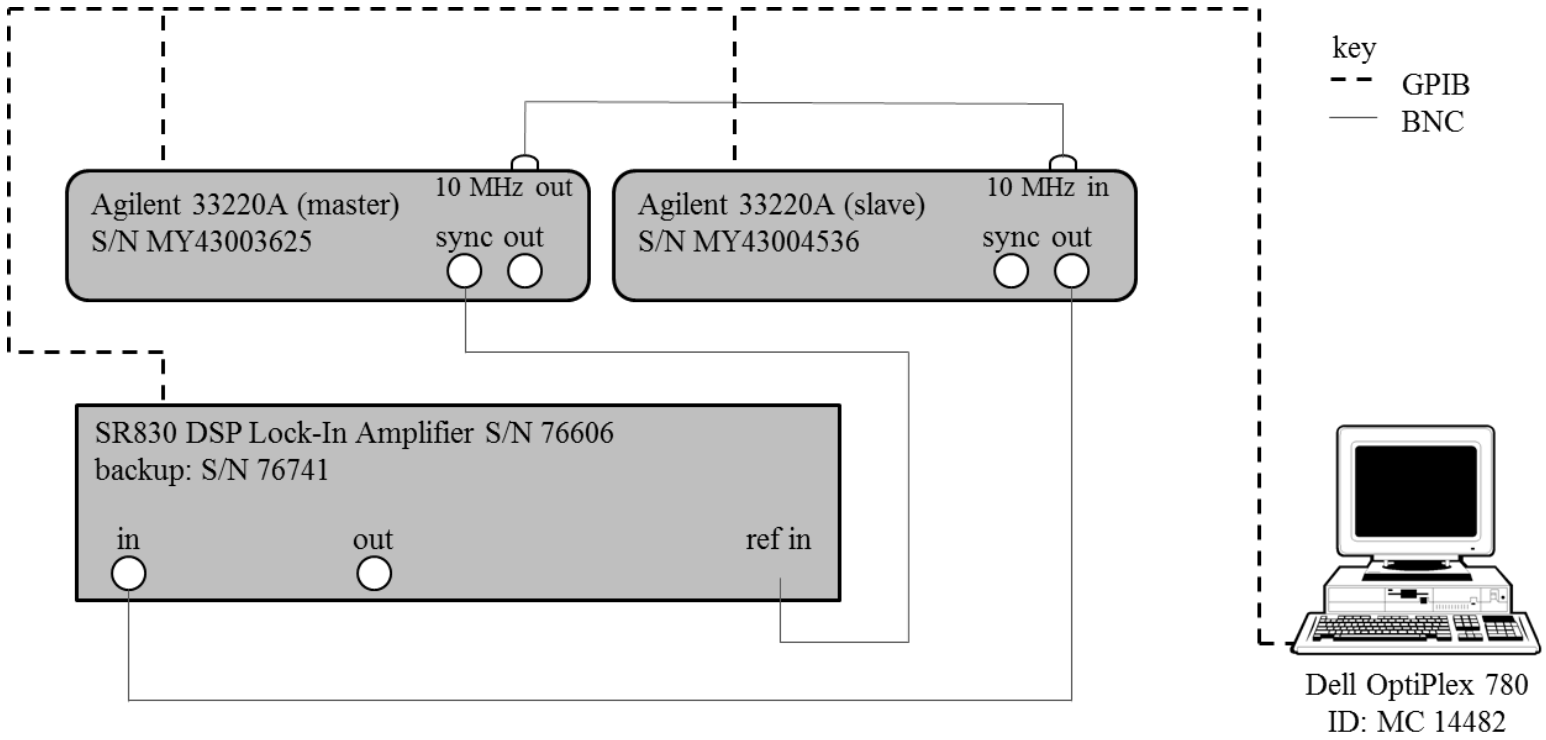


FIG. 2.1. Apparatus design used in the experiment. Solid grey lines represent BNC connections between the instruments and the broken weighted line shows the GPIB connections with the Dell PC.

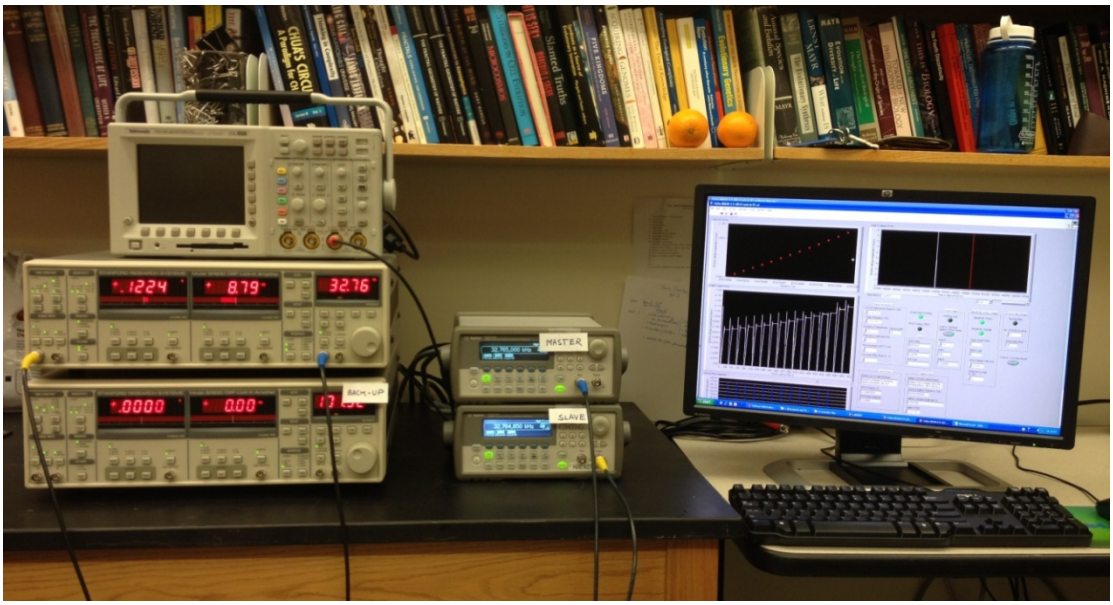
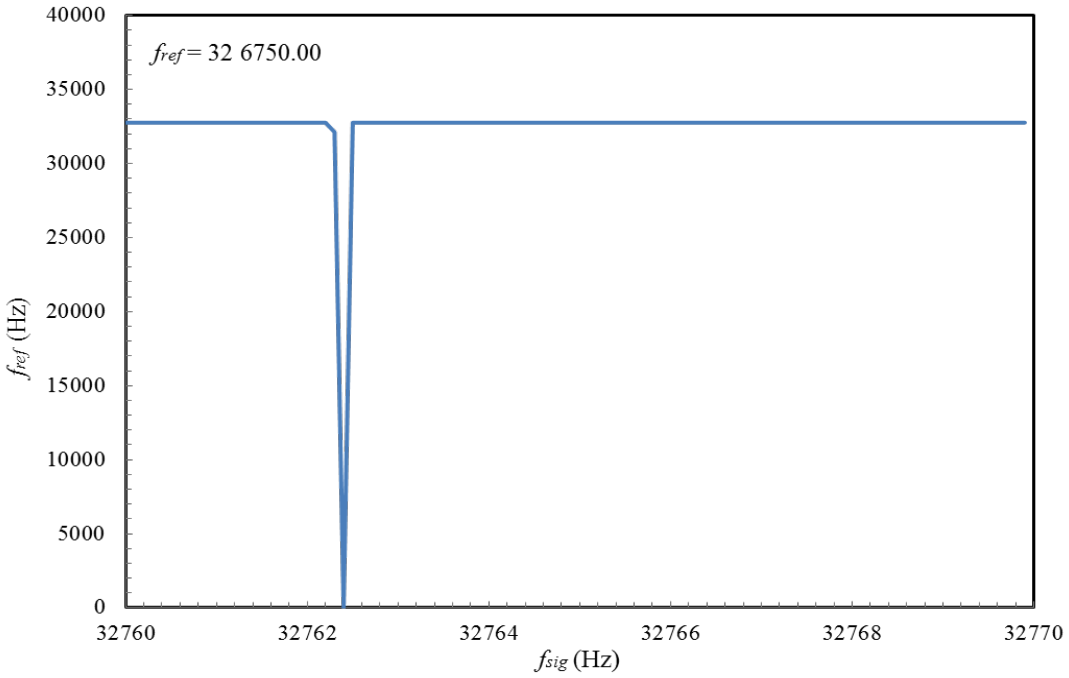


FIG. 2.2. A picture of the experimental apparatus during a running experiment.

One of the issues encountered while testing the apparatus was the SR830's sporadic disconnection from the external reference signal. During this event, the lock-in was found to lose the trigger from the master Agilent for about a minute and thus shifted to its internal reference frequency. The sudden change in reference frequency away from f_{sig} forced the SR830 output to zero. One such event which was recorded is shown in Fig. 2.3. Although the exact cause of the malfunction was not discovered, changing the SR830 unit fixed the issue. A different SR830, S/N 76606, was then used for the remaining of the project.

(a)



(b)

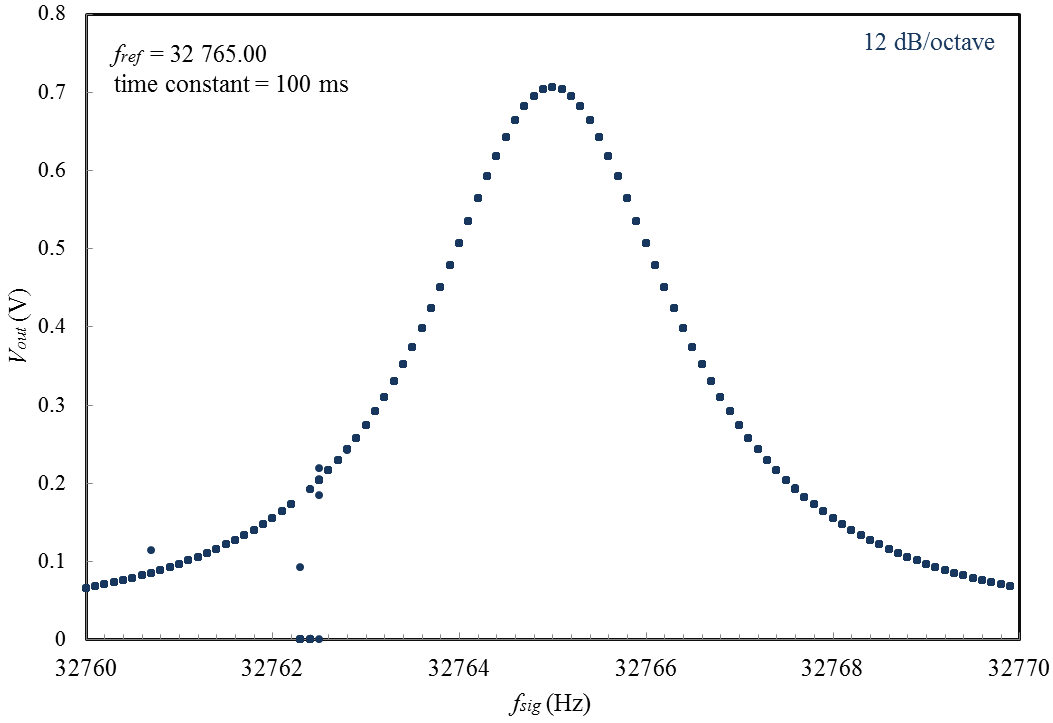


FIG. 2.3. Results of a preliminary experiment showing the reference frequency malfunction. (a) Reference frequency, f_{ref} is plotted against f_{sig}. Sudden drop in f_{ref} around $f_{sig} = 32\ 762.50$ Hz can be seen. (b) Resonance response of the SR830 showing the V_{out} drop to zero during the malfunction.

2.2 LabVIEW for experiment control

A program was designed and developed in the LabVIEW 2011 environment for experiment control and data acquisition. A flowchart diagram of the program, with its main structures and methods, is shown in Fig. 2.4. The program was made robust enough to detect and solve for common connectivity and instrument failures, and had a friendly graphical user-interface (GUI).

The program had several features, including a waiting period for the lock-in response to stabilize after a frequency change, an intelligent sensitivity setting selection depending on the value of the SR830 output, and a gradual increase in the SR830 input amplitude during the frequency-change-stabilization period in an attempt to mitigate the sudden spikes in output after a frequency change. A softcopy of the complete LabVIEW program is provided in the CD in Appendix A**.**

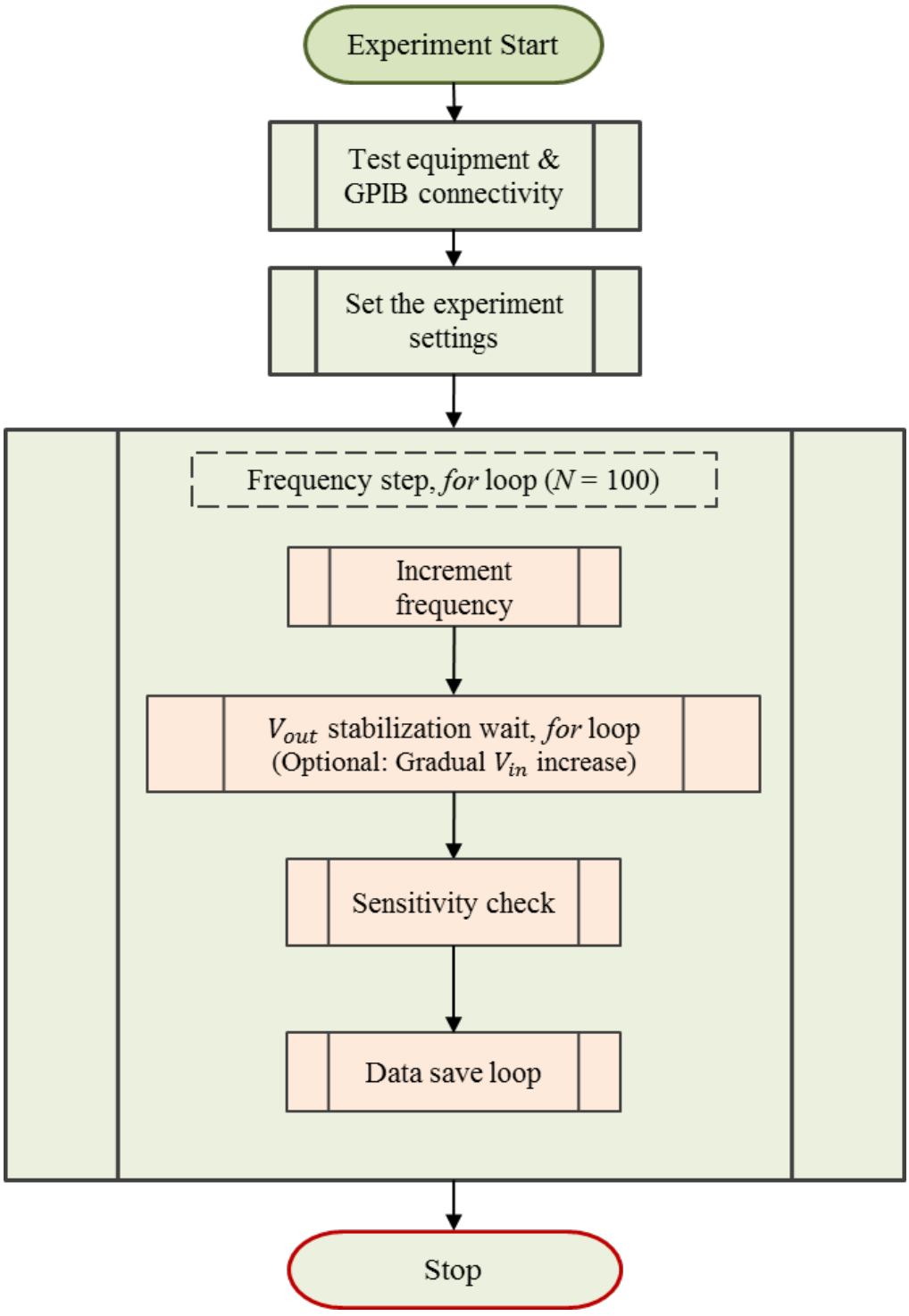


FIG. 2.4. A basic flowchart diagram showing the functions and operational structure of the LabVIEW program used for experiment control and data acquisition.

Graphical user interface (GUI)

The front panel of the LabVIEW program was designed with three basic objectives: (1) to give the user the flexibility in setting the experiment conditions, (2) to offer an insight into the performance of the program while an experiment is in progress, and (3) to provide a graphical representation of the data acquired in the experiment. A screenshot of the front panel of the program is shown in Fig. 2.5. The section *Input Parameters* allows the user to choose the experiment settings, such as f_{ref}, initial f_{sig}, step size, time constant, and filter roll-off. The sections *Stabilization Wait*, *Sensitivity Check* and *Data Save* represent the three main stages of the program. LED lights in each of their boxes indicate when the program is passing through that stage. Settings specific to these stages can also be altered through the GUI. The graph pane in the upper right displays the output R_{rms} on a real-time basis, regardless of the program stage. The lower left graph also displays R_{rms} against time, but is limited to the *Wait Stage* only. The upper left graph logarithmically displays the SR830 output values acquired in the *Data Save* stage.

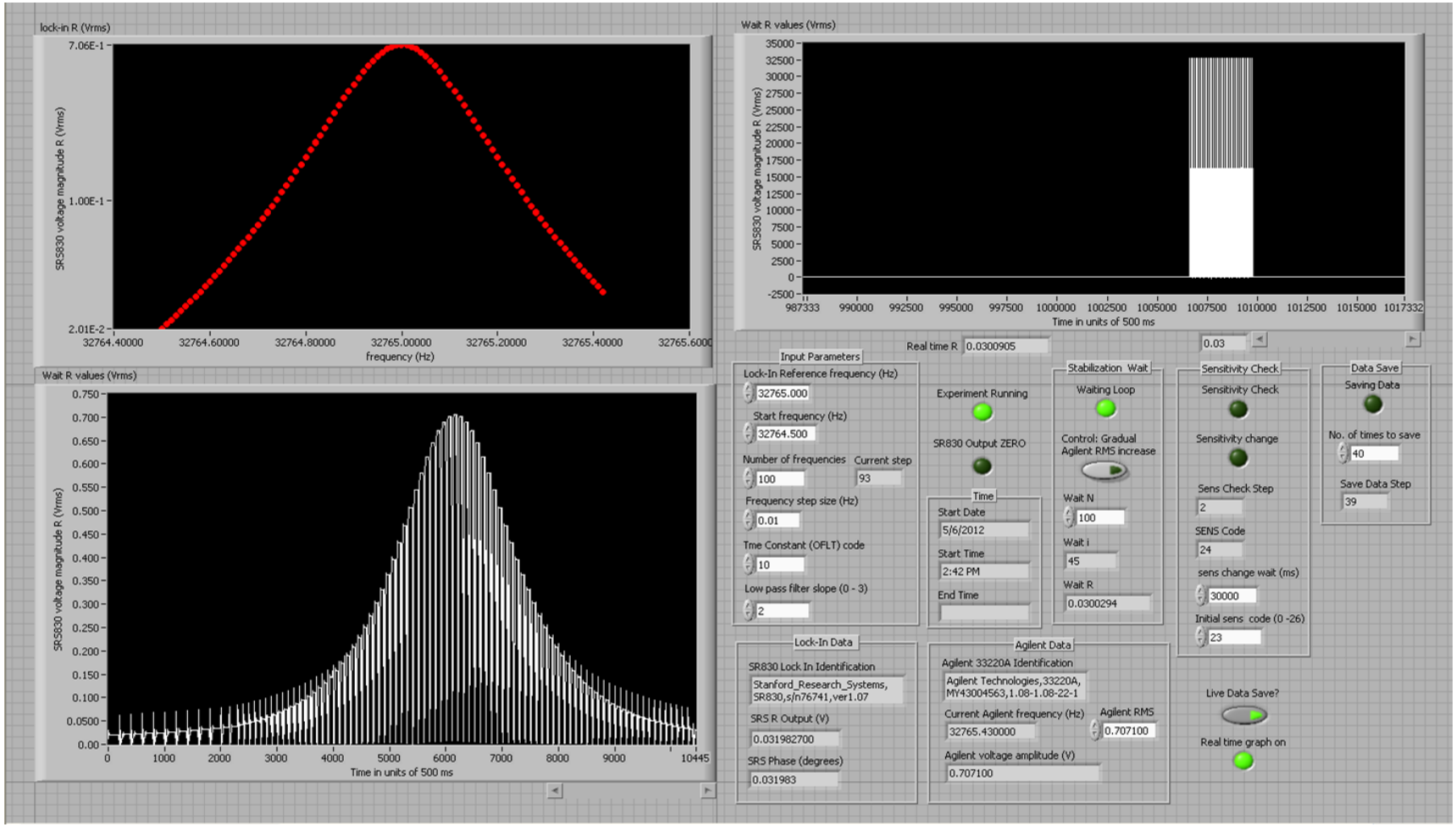


FIG. 2.5. Front panel of the LabVIEW program used for experiment control and data acquisition. The interface provides user-friendly selection of experiment conditions, insight into the internal process of the program, and a real-time graphical display of the relevant data.

GPIB communication error

During the initial experiment tests, we noticed sporadic errors in the GPIB communication with the SR830. It was discovered that under certain circumstances, contrary to the claim by Stanford Research Systems, the SR830 could not handle multiple GPIB commands at once. A basic interaction with an instrument using GPIB, when a particular setting or value from the instrument is read, involved two stages: (1) GPIB *write* which sends the command to the instrument, (2) GPIB *read* which reads the response of the instrument to the *write* command. During the experiment, we noticed that if the experiment was stopped while a GPIB command was in process, the SR830 saved the response to the command in its buffer. During the next experiment, when a new *write* command was sent, the SR830 first returned the response to the command from the previous experiment, which is already saved in its buffer. This created a gap between the GPIB commands sent and the lock-in responses received.

In order to detect this GPIB communication error, the following strategy was employed: a particular parameter, say time constant of 10 s, was set on the SR830 using the GPIB *write* command. The same parameter was read off from the lock-in immediately afterwards. If the value of the parameter that was set initially did not match the value read, a GPIB communication error had occurred. In this case, the experiment was stopped. Manually restarting the lock-in corrected for this error. However, late in the project, the GPIB *clear* function in the LabVIEW was discovered, which provided an easy way to clear the GPIB buffers and solve for the malfunction automatically without requiring stopping the program.

R_{rms} stabilization wait

During the frequency loop, a change in f_{sig} after each iteration resulted in an offshoot in the SR830 output. This offshoot had to be stabilized before R_{rms} data could be recorded. A *for* loop with time delay frames, where *N* is proportional to the waiting time, was used to provide a waiting period for the output to stabilize. Each iteration through the loop corresponded to a wait period of approximately 200 to 500 ms.

Gradual SR830 input amplitude rise

One strategy utilized to mitigate the offshoot in the lock-in output from a change in frequency was to instantaneously lower the amplitude of the input from the Agilent slave prior to changing the frequency, and then gradually increase it to the standard rms value of 0.7071 V. In order to do this, the waiting period for R_{rms} stabilization was divided into five equal-length periods. During the first period, the amplitude of the lock-in input was kept at the minimum possible value of 0.0071 V. The amplitude was gradually increased during the next two periods. Each iteration through the *for* loop incremented the amplitude by $0.7/(2N/5)$ V, where *N* is the number of iterations, until, the input reached 0.7071 V. During the remaining two periods, the SR830 was allowed to stabilize before proceeding to the sensitivity check phase. A sample of the SR830 output during the frequency-change stabilization loop is shown in Fig. 2.6. The R_{rms} value during stabilization wait was recorded during each experiment to so that the user could ensure that the output had stabilized before the program went on to the next stage.

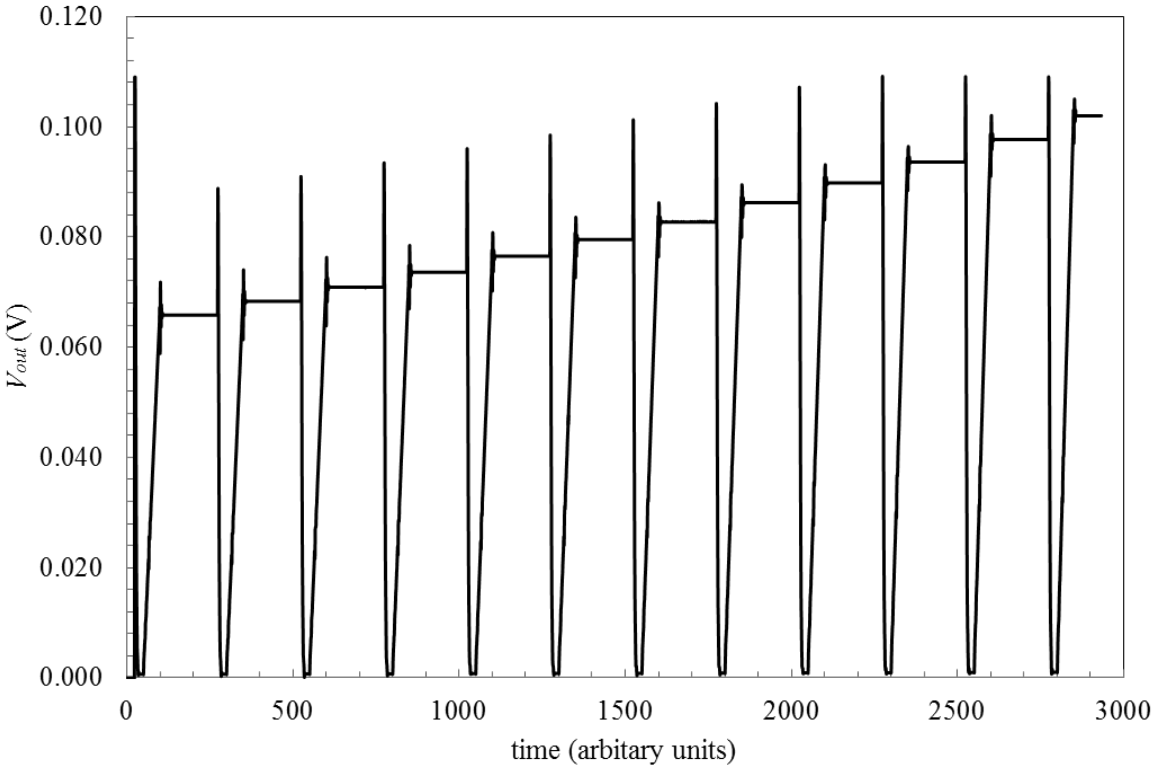


FIG. 2.6. The lock-in output during the frequency-change stabilization wait. The initial voltage drop during each resulted from the V_{in} amplitude being decreased to zero. Spikes seen are due to the SR830 response to the frequency change.

Sensitivity check

During the experiment, we obtained the resonance response plots by incrementally increasing the frequency of the SR830 input, f_{sig}, by the frequency step size. However, as f_{sig} closed in on the reference frequency f_{ref}, the SR830 output increased significantly. This required an intelligent SR830 sensitivity selection to prevent an output overload. On the other hand, if the output got too low, the sensitivity had to be decreased accordingly to maintain the precision of the data.

One way to ensure appropriate sensitivity was to use the SR830 *Auto-Gain* function on the stabilized output. However, the *Auto-Gain* was only available for time constants of less than 3 s. For greater time constants, a separate algorithm was developed which compared V_{out} to voltage ranges appropriate for the different sensitivity settings. Table I shows the sensitivity selection criteria used in the algorithm. In order to ensure a perfect sensitivity selection, the check was performed twice for each frequency. Additionally, to reduce the chances of basing the choice of sensitivity setting on an outlier output, the SR830 output used in the sensitivity check was the average of three output values recorded 1 s apart. If, during this stage, the sensitivity of the SR830 had to be altered, the SR830 output was made to wait for further 300 s so it could stabilize.

TABLE I. Criteria used in the LabVIEW program to make the appropriate sensitivity choice.

SR830 output range (V)	Sensitivity code	Sensitivity
1 to 0.1	26	1 V / μA
0.1 to 0.001	23	100 mV / nA
0.001 to 0.0001	20	10 mV / nA
0.0001 to 1×10^{-6}	17	1 mV / nA
1×10^{-6} to 1×10^{-8}	14	100 μV / pA
1×10^{-8} to 0	11	10 μV / pA

Real-time SR830 output

In order to give the user a better insight into the performance of the lock-in, we included a real-time graphical display of the R_{rms}. This was essentially a *while* loop with conditions designed to have it operate continuously throughout the experiment, as long as the user wished. The structure of the program required the *while* loop to be run parallel to the frequency loop. The real-time R_{rms} data, which included the output for the entire experiment, was saved in a separate *.lvm* file.

2.3 Experiment parameters

In our research, we studied the performance of an SR830 DSP lock-in amplifier at various time constant and filter roll-off settings. Specifically, with the rms amplitude of the SR830 input held constant at 0.7071 V, we incremented the input frequency f_{sig} by the frequency step-size and studied the response of the rms output R_{rms}. The reference frequency, f_{ref}, was standardized at 32 765.00 Hz. However, the f_{sig} range and the step size had to be adjusted depending on the time constant. Other settings, like DC/AC coupling, notch filter and reserve, had little effect on the resonance response curve, and were manually controlled. Moreover, the theoretical model derived for the SR830 assuming a Butterworth filter (see Sect. 1.5) was also independent of these settings.

The SR830 offers fourteen time constant values, ranging from 10 μs to 30 s. Higher time constants up to 30 ks are available for very low reference frequencies.[13] A complete list of time constant values can be found in the SR830 user manual. For the roll-off settings for its low-pass filter, the SR830 allows 6 dB/ octave, 12 dB/octave, 18 dB/octave, and 24 dB/octave. Generally, a longer time constant and a greater filter roll-off translate into better noise rejection by the low-pass filter. However, these were exactly the settings that gave peculiar results in the experiment.

2.4 Data acquisition and formatting

Once the SR830 output, R_{rms}, had stabilized and a sensitivity check had been performed, R_{rms} was saved a tabular form in a *.lvm* file alongside other relevant experimental data. For each value of the input frequency, f_{sig}, forty R_{rms} data points each about a second apart were recorded. A complete list of the all the parameters, including the SR830 and Agilent function generator settings, which were recorded in the experiment is provided in Table II. The first column of the data file contained an unidentified variable, which was assumed to be a proxy for time and was ignored. A tabular view of a sample data file is attached in Appendix 2**.**

TABLE I. List of the variables and experiment parameters recorded during the experiment. The order of the list corresponds to the column number in the tabular file. Column 1 contained an unidentified variable and was ignored during analysis.

Column	Variable	Units	Expected range or value
2	f_{sig}	Hz	32764.50 to 32765.50
3	V_{out} (R-RMS)	V	0.00 to 0.7071
4	phase, ϑ	deg	0 to 180
5	sensitivity	-	1 to 26
6	filter roll off	-	0 to 3
7	time constant	-	1 to 13
8	f_{ref} (measured by the SR830)	Hz	32765.00
9	SR830 input config V_{in} (A, B)	-	0 or 1
10	float(0), ground(1)	-	0 or 1
11	coupling: AC(0), DC(1)	-	0 or 1
12	notch filter: no filter(0), line(1), 2xline(2)	-	0 to 2
13	reserve: high(0), normal(1), low noise(2)	-	0 to 2
14	Sync filter: off(0), on(1)	-	0 or 1
15	V_{in} (measured by the slave Agilent)	V	0.00 to 0.7071
16	f_{ref} (measured by the Agilent)	Hz	32765
17	f_{ref} (measured by the standby SR830)	Hz	32765
18	gradual Vin increase: no(0), yes(1)	-	0 or 1
19	Comments: identification for SR830, Agilent 'slave', Agilent 'master'	-	-

3. RESULTS & ANALYSIS

3.1 Resonance response plots

We obtained resonance response plots of R_{rms} by varying f_{sig} at time constants τ = 100 ms, 1 s, 10 s, and 30 s respectively. For each τ, all four filter roll-off settings were used, corresponding to a Butterworth filter pole values of m = 1, 2, 3, and 4. The R_{rms} stabilization wait in the LabVIEW program was adjusted according to these parameters. Generally, higher τ and m required a longer stabilization wait.

This section presents the results of our experiment. Resonance response plots for τ = 1 s, 10 s, and 30 s are shown in Figs. 3.1 – 3.4. Plots for all four roll-off settings are shown in a single chart, except for the 30 s time constant 24 dB/octave chart, which is shown separately to prevent an overlap of data points with plots of other roll-off settings. Plots have been color coded by their roll-off setting. Discrete data points on the graph refer to the actual R_{rms} data obtained. For each of the filter roll off settings, f_{sig} was increased from 32764.5 Hz to 32765.5 Hz with a step size of 0.01 Hz. The theoretical curve, which was represented by the solid line, has been obtained using the Butterworth frequency response function given in Eq. (16).

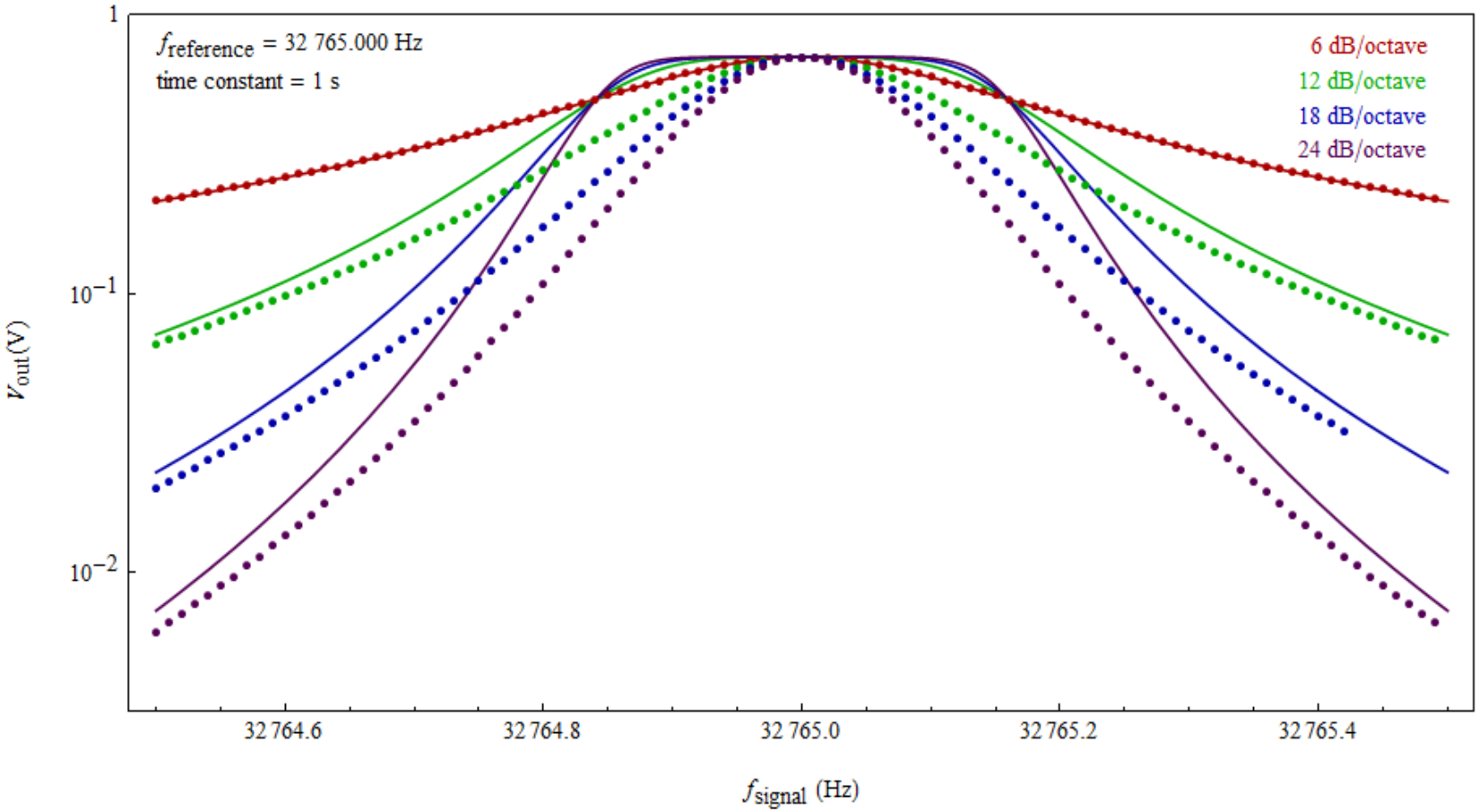


FIG. 3.1. Resonance response plots for a time constant of 1 s.

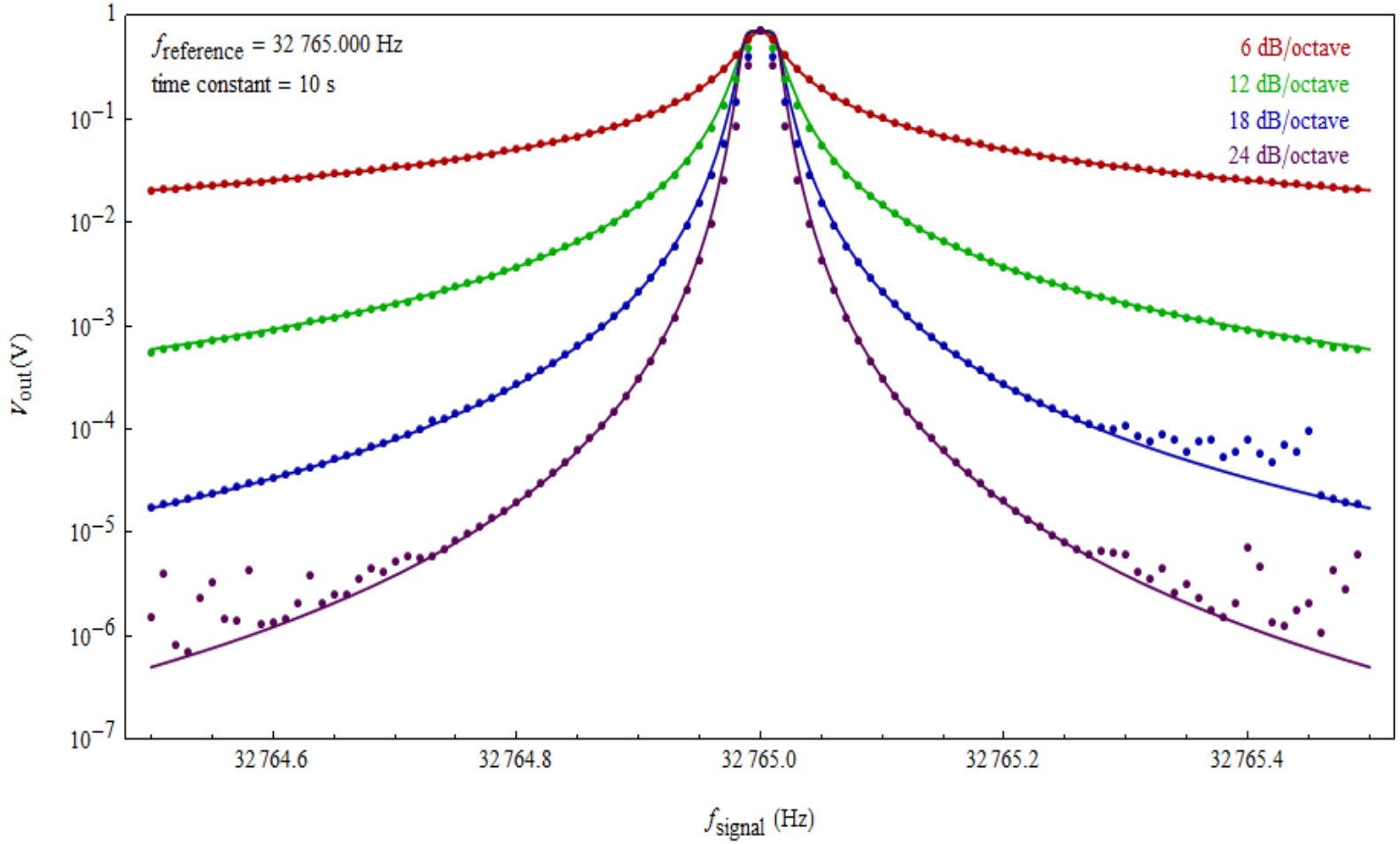


FIG. 3.2. Resonance response plots for a time constant of 10 s. At roll-off setting of 18 dB/octave and 24 dB/octave, seemingly random deviations of the SR830 output from the theoretical model can be observed.

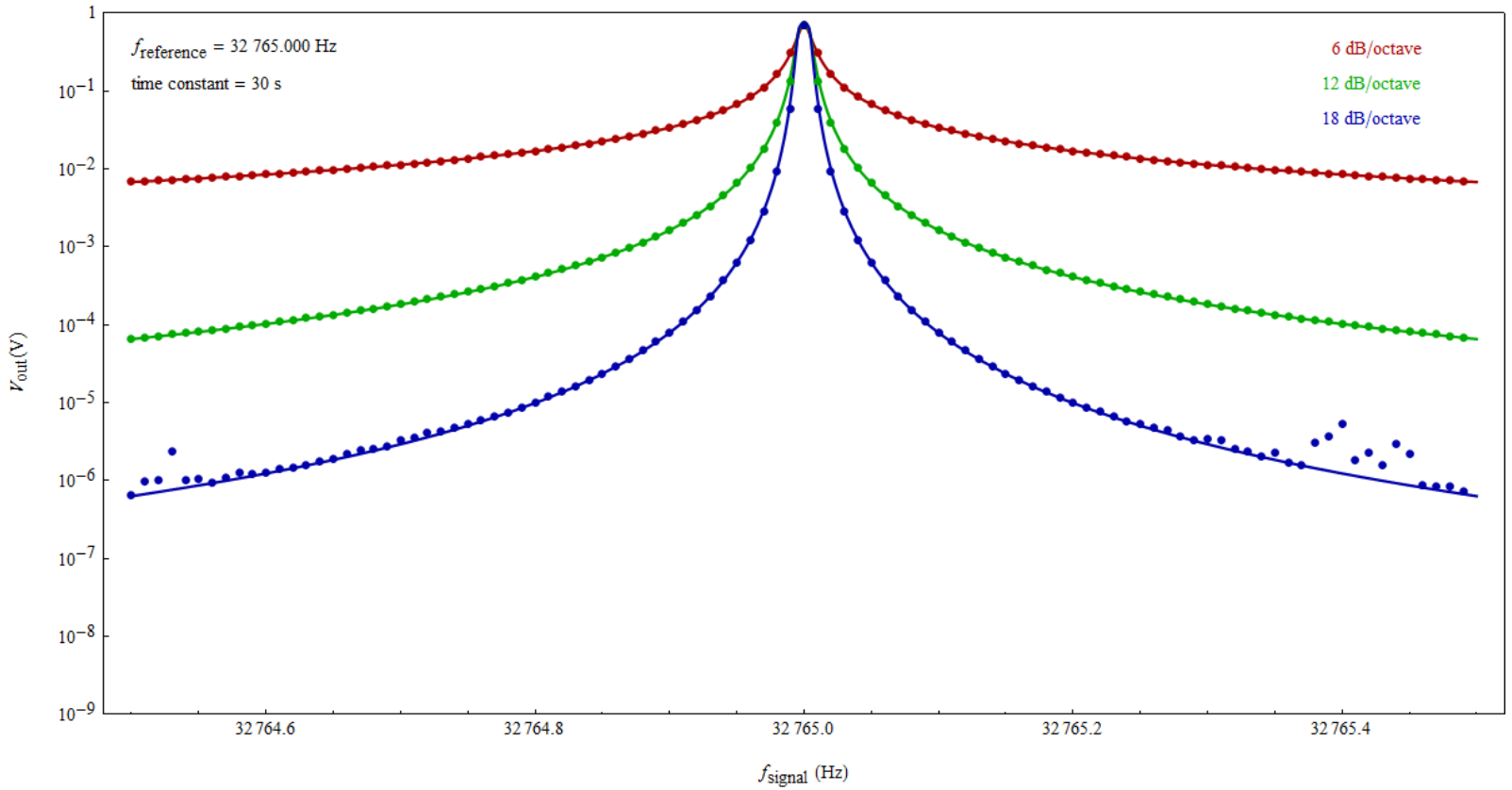


FIG. 3.3. Resonance response plots for 30 s time constant at 6 dB/octave, 12 dB/octave, and 18 dB/octave roll-off settings. At18 dB/octave, seemingly random deviations of the SR830 output from the theoretical curve can be observed.

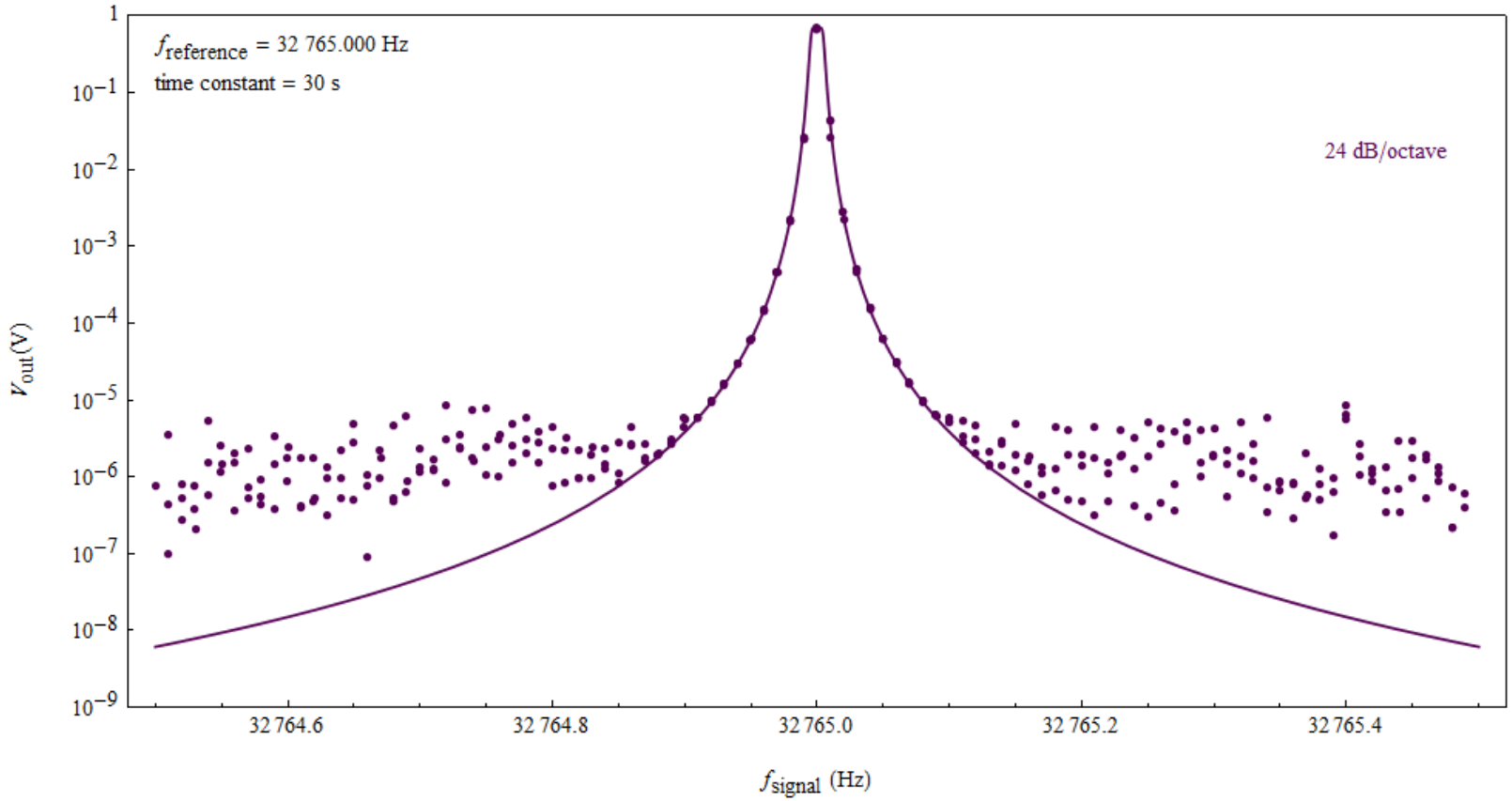


FIG. 3.4. Resonance response plots for a 30 s time constant at 24 dB/octave filter roll-off. Deviations of the SR830 output from the theoretical model can be observed.

3.2 Oscillations in the SR830 output

The digital nature of the SR830 ensures that, once the input is digitized, no further error is introduced. However, the results shown in Section 3 show considerable deviations from the theoretical model of a lock-in amplifier for time constants of 10 s and 30 s, at roll-off settings of 18 dB/octave and 24 dB/octave. Closer observation at these settings showed evidence for non-mitigating oscillations in the R_{rms}, in contrast to the expected stable output. This was considered to be the explanation behind the deviations in the resonance response plots. Therefore, our analysis was focused on studying these oscillations.

Observing the waveform in real time indicated that these oscillations corresponded to more than one frequency, perhaps a Fourier superposition of many frequencies. Data for the SR830 output with $f_{sig} = 32675.49$ exhibiting the oscillations was acquired at 10 s time constant and a 24 dB/octave roll-off. Figure 3.5 plots a section of output against time and shows these oscillations. Each time unit is 0.015625 ms. A zoomed-in version of the same plot, which is shown in Fig. 3.6 shows the oscillations at smaller level. The data were recorded over four hours, but there was no evidence to suggest that the oscillations were dying off.

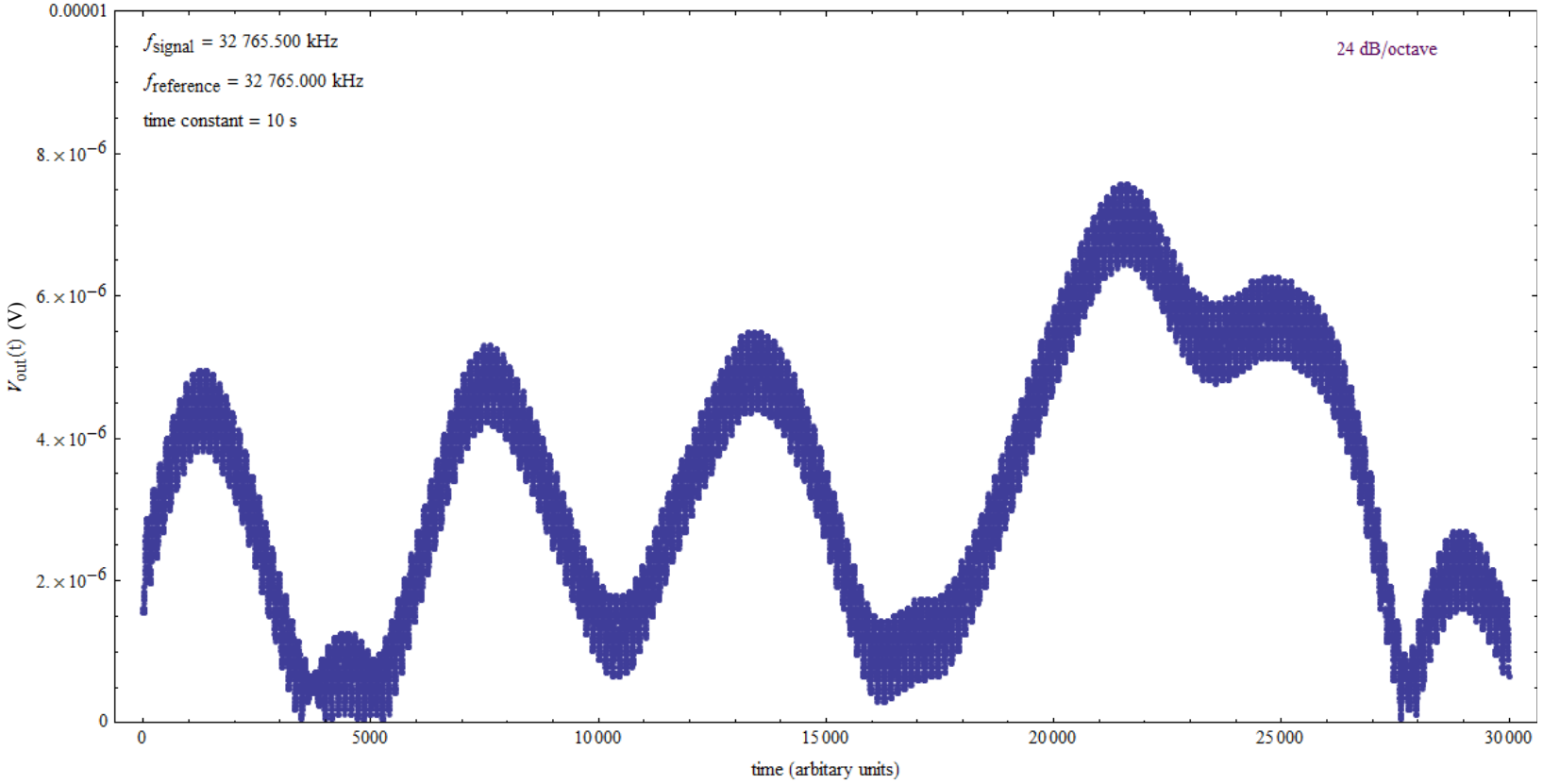


FIG. 3.5. A segment of the SR830 output recorded over four hours at $f_{sig} = 32675.5$ Hz, for 10 s time constant and 24 dB/octave, showing oscillations with larger time periods.

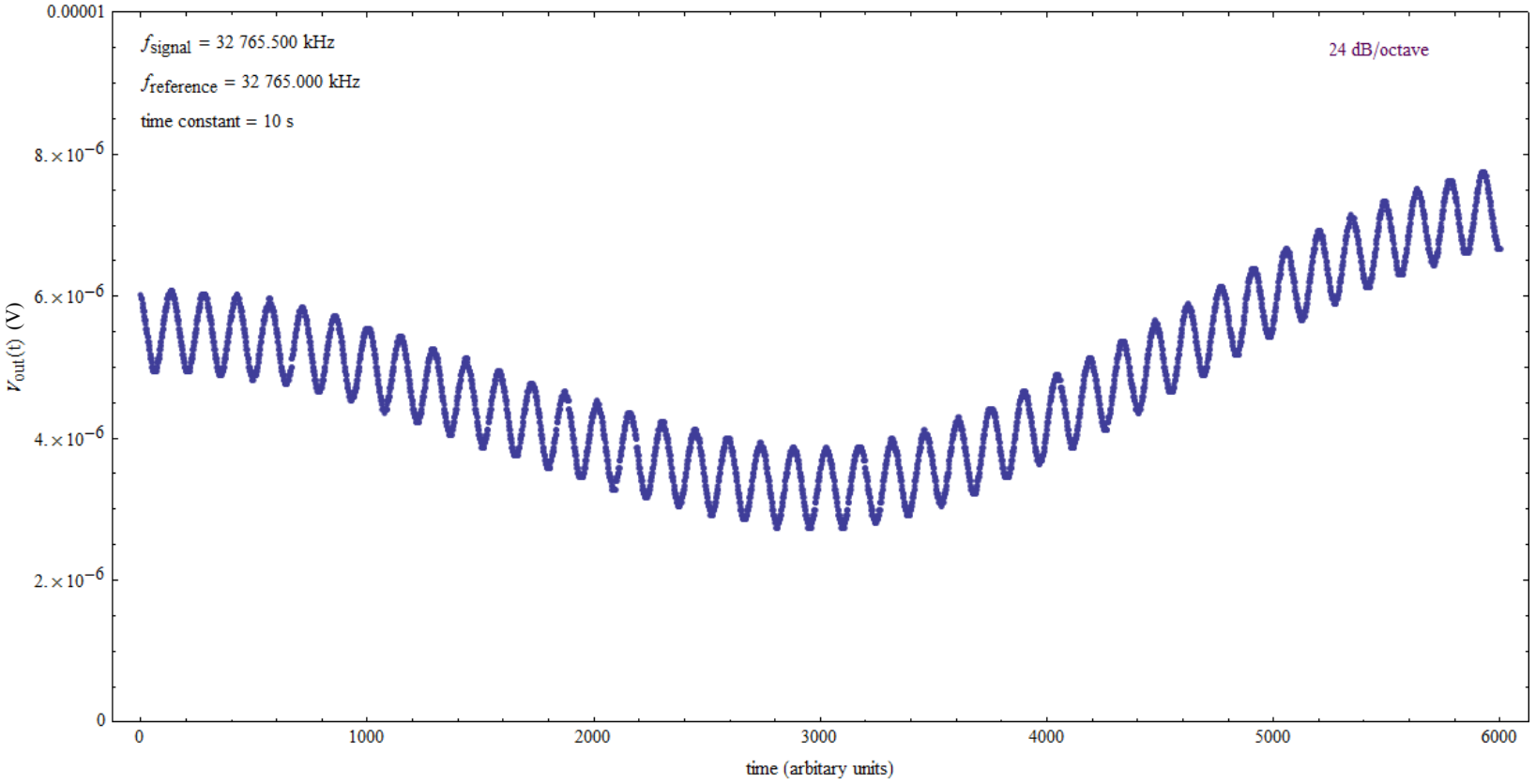


FIG. 3.6. A closer view of SR830 output showed in Fig. 3.5. Oscillations of smaller time period can be seen.

3.3 Fourier transform of the SR830 output

A Fourier transform was carried out on the data from Fig. 3.5. to determine the frequencies which make up the oscillations. As shown in Fig. 3.7, the Fourier transform showed a rather organized structure. The largest frequency peak can be observed near zero, which corresponded to the expected DC output of the lock-in amplitude. However, other peaks at non-zero frequencies can also be observed. This suggested, as expected, that the oscillations were a Fourier superposition of several frequencies, separated by a constant frequency gap –suggestive of a harmonic structure.

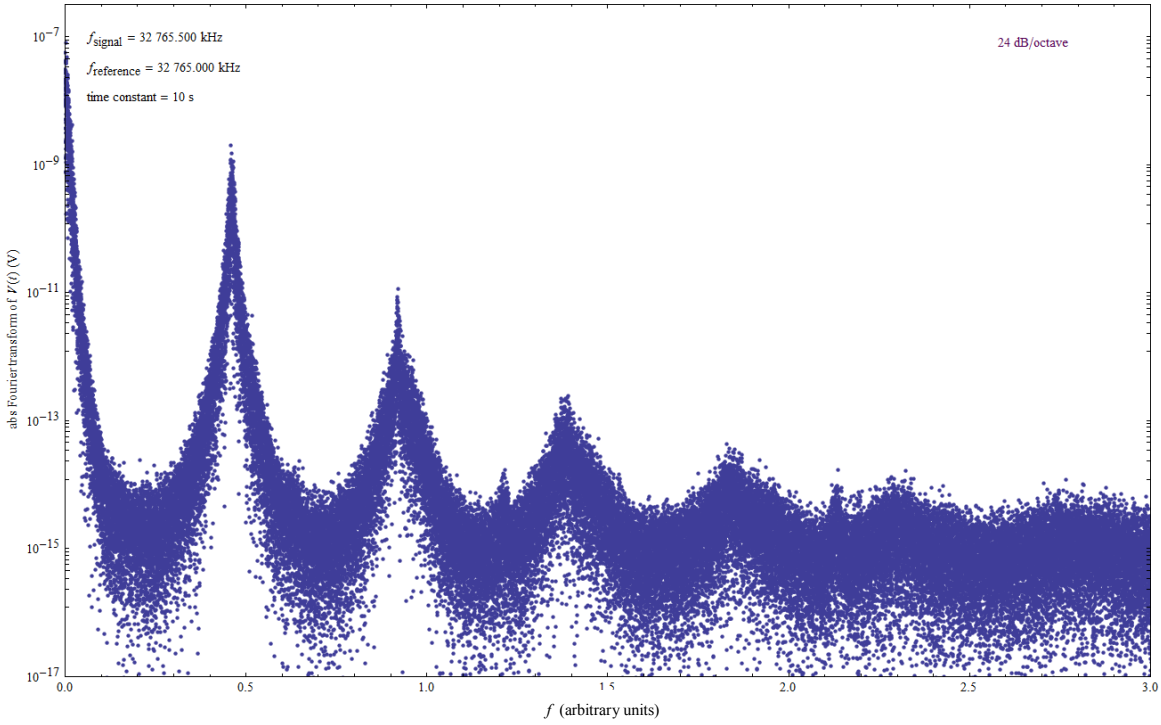


FIG. 3.7. A Fourier transform of the SR830 output data for $f_{sig} = 32675.5$ Hz, for 10 s time constant and 24 dB/octave.

Due to the lack of a proper method to keep track of the time in our recorded data, the frequency values on *x*-axis were not reliable to derive particular frequencies for the peaks. However, some interesting estimates were made. For an n^{th} data point in a real time data, *n* itself was a proxy for time, and was thus used as the arbitrary time unit in our analysis. The average time difference between *n* and *n+1* data point was 0.015625 ms, which for the first three non-zero peaks corresponded to an approximate frequency of 30 kHz, 60 kHz and 90 Hz. Surprisingly, these frequencies were remarkably close to the harmonics of the reference frequency, and the signal frequency. Unfortunately, further analysis of the oscillations could not be carried out due to time constraints.

4. DISCUSSION

4.1. Suggested future work in explaining the oscillations

The exact cause for the oscillations in the SR830 output was not clearly understood. However, several explanations can be put forward for further research. Assuming that the oscillation frequencies are the harmonics of the reference or the signal frequency, it is worth examining that under what mechanism these harmonics translate into oscillations in the SR830 output. Again, due to the lack of reliable time data, we cannot rely on this assumption and should explore other possible explanations as well.

One natural, but highly unlikely, explanation is the induction of an ambient noise through the SR830 front panel input. This could theoretically result in the observed oscillations if the ambient noise has a frequency very close to the reference frequency, and has an amplitude which is oscillating at the observed frequencies. When a 50-Ω terminator was used at the front panel input of the lock-in, the output, interestingly, stabilized to 0 V. However, further experiments could not be carried out to study the response of the output to different front panel conditions.

It will also be of interest to explore the digital workings of the SR830 lock-in amplifier in more detail. Given that the oscillations are most problematic at low R_{rms}, the A/D sampling rate could been relevant to the oscillations. The jumps in the values of the digitally converted V_{in} may introduce their own frequency into the lock-in's operation.

Although it is rather difficult to conceive that why a sampling rate would eventually translate into oscillations in the output, a research into the digital operations of the SR830 can be valuable in explaining the mechanism through which the oscillations become a part of the final output.

Another interesting improvement to the experiment could be the use of a newer function generator model. Agilent Technologies claim 33220A's amplitude accuracy as ± 1 mVpp. Although theoretically an oscillating input amplitude within a ± 1 mVpp range of the selected peak-to-peak can translate into the observed deviations, it will be interesting to see more if newer models of functions generators change the results in any way.

4.2. Conclusion

The widespread use of the SR830 DSP Lock-In Amplifier in the scientific research industry makes it important that we have an accurate understanding of its operations. During our research, we found that at greater time constants, 10 s and 30 s, and at faster filter roll-off settings, 18 dB/octave, and 24 dB/octave, the SR830 output deviates from its theoretical model. These deviations are most likely a result of the non-mitigating oscillations in the lock-in output which can be observed when R_{rms} gets low enough. Fourier analysis of the oscillations suggested that the oscillations were a superposition of more than one frequency, close to harmonics of the reference frequency. Time constraints could not allow us to study the causes of these oscillations further. However, the project builds a strong base for further research into the causes of the mysterious oscillations.

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APPENDIX 1

See attached CD.

APPENDIX 2

For Sample of the *.lvm* data file see next page.

LabVIEW Measurement																		
Writer_Ve	2																	
Reader_Ve	2																	
Separator	Tab																	
Decimal_S	.																	
Multi_Hea	No																	
X_Columns	One																	
Time_Pref	Absolute																	
Operator	tansari																	
Date	4/16/2012																	
Time	10:06.1																	
End_of_Header																		
Channels	16																	
Samples	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1		
Date	4/16/2012	########	########	########	########	########	########	########	########	########	########	########	########	########	########	########		
Time	10:06.1	10:54.2	10:54.2	10:54.9	10:54.9	10:54.9	10:54.4	10:54.9	10:54.9	10:54.9	10:55.0	10:55.0	10:55.0	10:54.0	10:54.2	10:54.4		
X_Dimensi	Time	Time	Time	Time	Time	Time	Time	Time	Time	Time	Time	Time	Time	Time	Time	Time		
X0	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00		
Delta_X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1		
End_of_Header																		
X_Value	Untitled	Untitled 1	Untitled 2	Untitled 3	Untitled 4	Untitled 5	Untitled 6	Untitled 7	Untitled 8	Untitled 9	Untitled 1(	Untitled 1:	Untitled 1:	Untitled 1:	Untitled 1-	Untitled 1!	Comment	
0	32764.5	6.22E-07	94.302	14	3	13	32765	0	0	0	3	0	1	0.7071	32765	101320	Stanford_Research_Systems,SR8	
0	32764.5	6.26E-07	95.496	14	3	13	32765	0	0	0	3	0	1	0.7071	32765	101320	Stanford_Research_Systems,SR8	
0	32764.5	6.33E-07	94.212	14	3	13	32765	0	0	0	3	0	1	0.7071	32765	101320	Stanford_Research_Systems,SR8	
0	32764.5	6.37E-07	95.382	14	3	13	32765	0	0	0	3	0	1	0.7071	32765	101320	Stanford_Research_Systems,SR8	
0	32764.5	6.52E-07	94.398	14	3	13	32765	0	0	0	3	0	1	0.7071	32765	101320	Stanford_Research_Systems,SR8	
0	32764.5	6.48E-07	95.304	14	3	13	32765	0	0	0	3	0	1	0.7071	32765	101320	Stanford_Research_Systems,SR8	
0	32764.5	6.63E-07	94.314	14	3	13	32765	0	0	0	3	0	1	0.7071	32765	101320	Stanford_Research_Systems,SR8	
0	32764.5	6.59E-07	95.196	14	3	13	32765	0	0	0	3	0	1	0.7071	32765	101320	Stanford_Research_Systems,SR8	
0	32764.5	6.78E-07	94.788	14	3	13	32765	0	0	0	3	0	1	0.7071	32765	101320	Stanford_Research_Systems,SR8	
0	32764.5	6.71E-07	95.118	14	3	13	32765	0	0	0	3	0	1	0.7071	32765	101320	Stanford_Research_Systems,SR8	
0	32764.5	6.93E-07	94.968	14	3	13	32765	0	0	0	3	0	1	0.7071	32765	101320	Stanford_Research_Systems,SR8	
0	32764.5	6.85E-07	95.298	14	3	13	32765	0	0	0	3	0	1	0.7071	32765	101320	Stanford_Research_Systems,SR8	
0	32764.5	7.00E-07	95.442	14	3	13	32765	0	0	0	3	0	1	0.7071	32765	101320	Stanford_Research_Systems,SR8	
0	32764.5	6.97E-07	95.466	14	3	13	32765	0	0	0	3	0	1	0.7071	32765	101320	Stanford_Research_Systems,SR8	
0	32764.5	7.15E-07	95.604	14	3	13	32765	0	0	0	3	0	1	0.7071	32765	101320	Stanford_Research_Systems,SR8	
0	32764.5	7.12E-07	95.364	14	3	13	32765	0	0	0	3	0	1	0.7071	32765	101320	Stanford_Research_Systems,SR8	