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FIELD EFFECT TRANSISTOR

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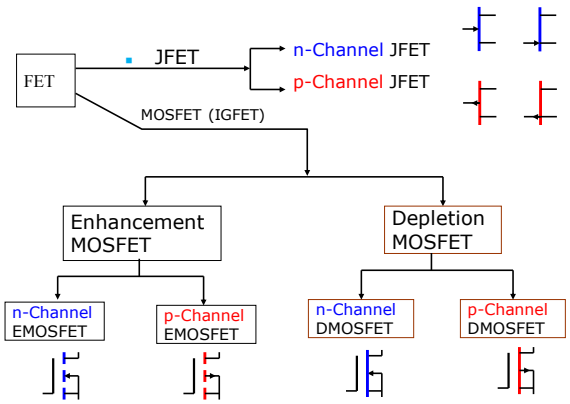
Types of Field Effect Transistors



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Junction FET (JFET)

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Junction Field Effect Transistor (JFET)

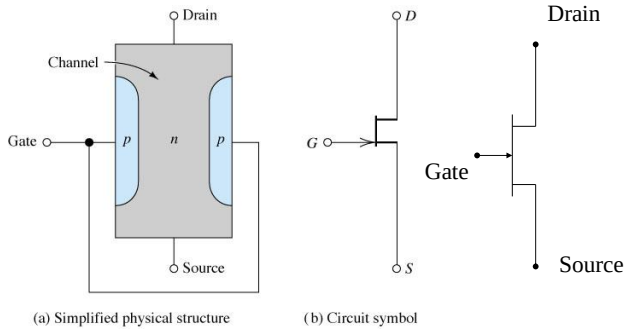

Figure: *n*-Channel JFET.

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FET (Field Effect Transistor)

Few important advantages of FET over conventional Transistors

1. Unipolar device i. e. operation depends on only one type of charge carriers (*h* or *e)*
2. Voltage controlled Device (gate voltage controls drain current)
3. Very high input impedance (≈10^9-10^{12} Ω)
4. Source and drain are interchangeable in most Low-frequency applications
5. Low Voltage Low Current Operation is possible (Low-power consumption)
6. Less Noisy as Compared to BJT
7. No minority carrier storage (Turn off is faster)
8. Self limiting device
9. Very small in size, occupies very small space in ICs

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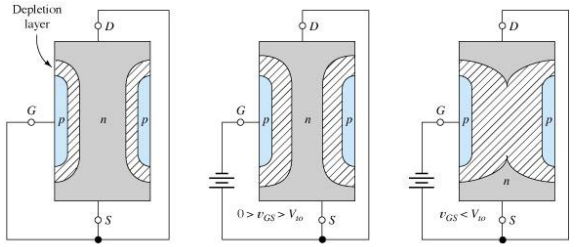
JFET Operation at various VGS



(a) Bias is zero and depletion layer is thin; low-resistance channel exists between the drain and the source

(b) Moderate gate-to-channel reverse bias results in narrower channel

(c) Bias greater than pinch-off voltage; no conductive path from drain to source

Figure: The nonconductive depletion region becomes broader with increased reverse bias. (*Note:* The two gate regions of each FET are connected to each other.)

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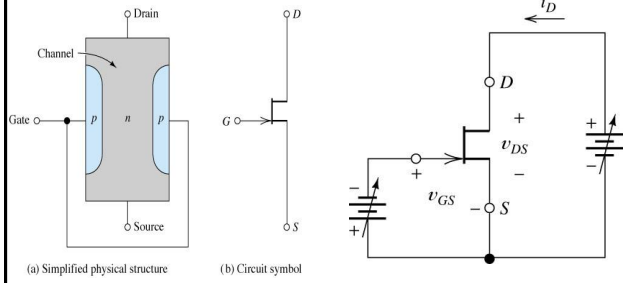
Biasing the JFET



(a) Simplified physical structure

(b) Circuit symbol

Figure: *n*-Channel JFET and Biasing Circuit.

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Transfer Characteristics of n-JFET

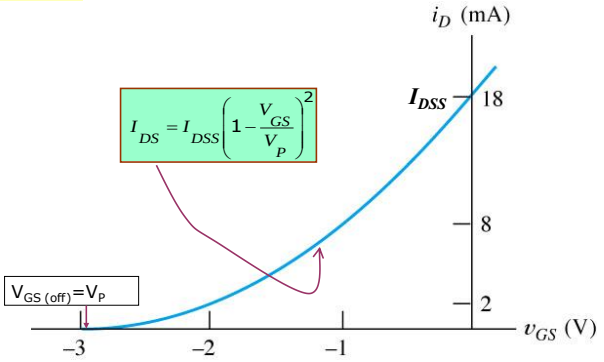


Figure: Transfer (or Mutual) Characteristics of n-Channel JFET

Output or Drain (VD-ID) Characteristics

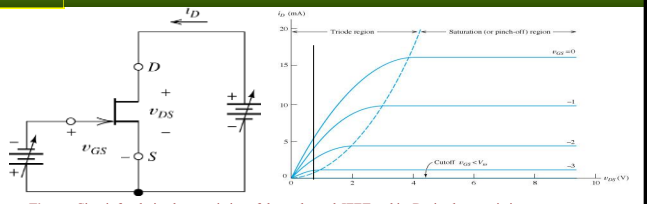


Figure: Circuit for drain characteristics of the *n*-channel JFET and its Drain characteristics.

Non-saturation (Ohmic) Region: $V_{DS} < (V_{GS} - V_P)$

The drain current is given by $I_{DS} = \frac{2I_{DSS}}{V_P^2}\left[(V_{GS} - V_P)V_{DS} - \frac{V_{DS}^2}{2}\right]$

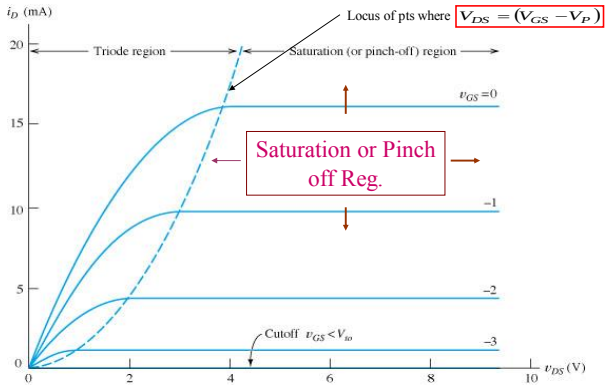
Saturation (or Pinchoff) Region: $V_{DS} \geq (V_{GS} - V_P)$

and $I_{DS} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$

Where, V_P is the pinch off voltage,

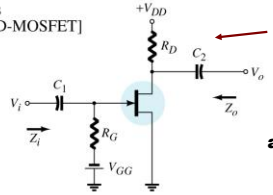
I_{DSS} is the short circuit drain current

V_D-I_D Characteristics of EMOS FET



n-JFET Biasing Circuits

Fixed-bias [JFET or D-MOSFET]



For Fixed Bias Circuit

Applying KVL to gate circuit we get

$V_{GG} = I_G R_G + V_{GS} = V_{GS} = Fixed, \Theta\, I_G = 0$

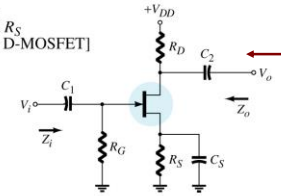
and

$I_{DS} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$

and $V_{DS} = V_{DD} - I_{DS} R_D$

Where, $V_p = V_{GS\text{-}off}$ & I_{DSS} is Short ckt. I_{DS}

Self-bias bypassed R_S [JFET or D-MOSFET]

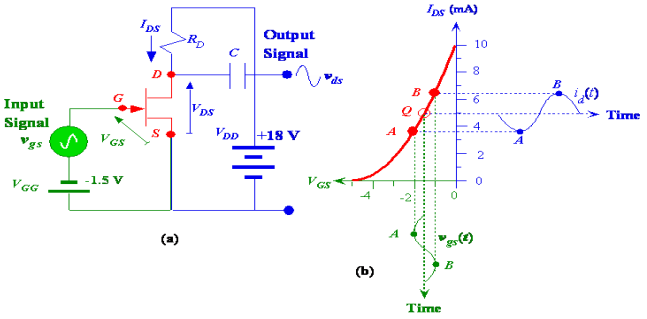


For Self Bias Circuit

$V_{GS} + I_{DS} R_S = 0$

$\therefore I_{DS} = -\frac{V_{GS}}{R_S}$

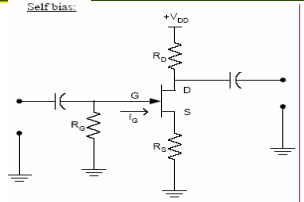
CS Amplifier and Variation in I_D with V_{GS}



(a) Common source (CS) ac amplifier using a JFET.
(b) Explanation of how I_D is modulated by the signal v_{gs} in series with the dc bias voltage V_{GG}.

JFET Self-Bias Amplifier Circuit

Self bias:



Since $I_G = 0$, $V_G = 0$

$V_S = I_D R_S$

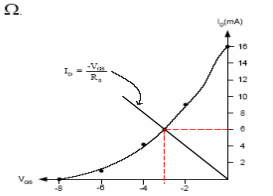
$V_{GS} = -I_D R_S$ $\quad I_D = \frac{-V_{GS}}{R_S}$

$V_{DS} = V_{DD} - I_D(R_D + R_S)$

and $I_{DS} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$

$\therefore I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = -\frac{V_{GS}}{R_S}$

- **Example**: Determine the Q-point values for the self biasing circuit if $V_{GS(off)} = -8$ V, $I_{DSS} = 16$ mA, $V_{DD} = 10$ V, $R_D = 500\ \Omega$, $R_G = 1\ M\Omega$ and $R_S = 500\ \Omega$.



$I_D = 6$ mA

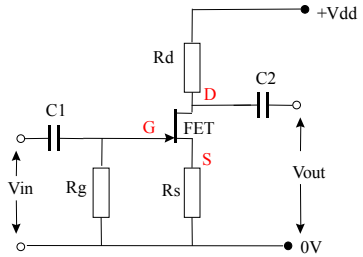
$V_{DS} = 10 - (6\text{mA})(500+500)$

$= 4$ V

$I_{DSS}\left[1 - 2\frac{V_{GS}}{V_P} + \left(\frac{V_{GS}}{V_P}\right)^2\right] + \frac{V_{GS}}{R_S} = 0$

This quadratic equation can be solved for V_{GS} & I_{DS}

Equivalent circuit of CS Amplifier



For drawing an ac equivalent circuit of Amp.

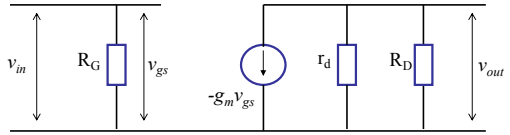
Assume all Capacitors C1, C2 as short circuit elements for ac signal

Short circuit the DC supply

Replace the FET by its small signal model

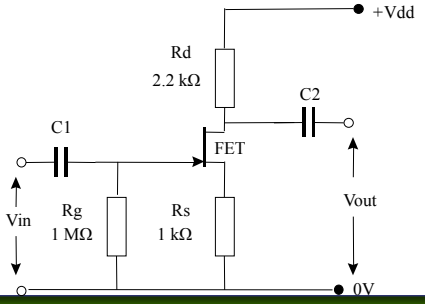
Input imp., $Z_{in} = R_G$

Output imp., $Z_o = r_d \| R_D = \frac{r_d R_D}{r_d + R_D}$



Self–Biased CS FET

- The diagram of common source J-FET amplifier.
- R_D = 2.2 kΩ, R_S = 1 kΩ, Rg = 1 MΩ, V_{DD} = 15 V.
- The parameters of J-FET transistor are:
- V_{GSOFF} = -8 V, I_{DSS} = 5 mA, g_m = 5 mS, r_D = 50 kΩ.



Metal Oxide Semiconductor FET (MOSFET)

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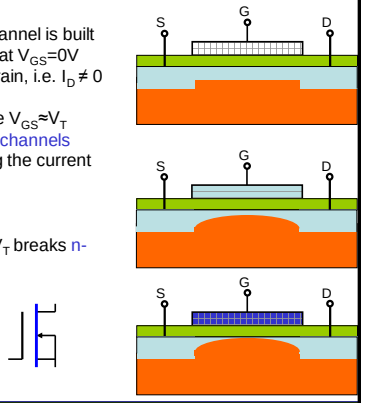
Depletion CMOS

In depletion CMOS transistor the n-channel is built between Source and Drain areas, i.e at V_{GS}=0V the current from Source can flow to Drain, i.e. $I_D \neq 0$

Application of negative voltage to Gate $V_{GS} \approx V_T$ attracts the holes from p-channel to n-channels narrowing a n-channel and decreasing the current I_D .

Further increase of negative to $V_{GS} \approx V_T$ breaks n-channel and cuts the current I_D.



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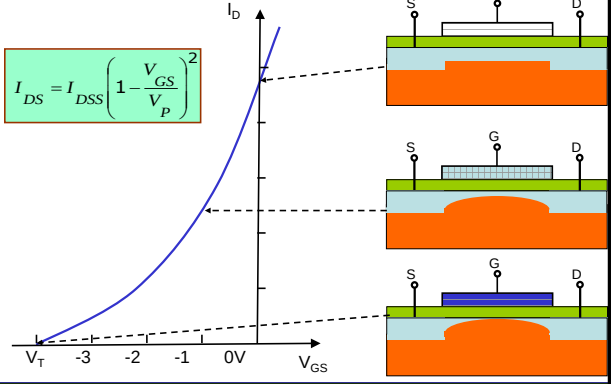
Depletion CMOS

$$I_{DS} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$



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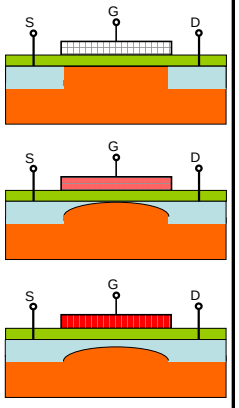
Enhancing CMOS

In enhancing CMOS transistor at V_{GS}=0V the two n-type Source and Drain areas are separated by p-channel – no current from Source to Drain, i.e. I_D=0

Application of positive voltage to Gate $V_{GS} \approx V_T$ attracts the electrons from n-channels to p-channel to build a n-type bridge between S and D, I_D just appears.

Further increase of positive $V_{GS} > V_T$ widens the n-channel and increases the current I_D.



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Enhancing CMOS

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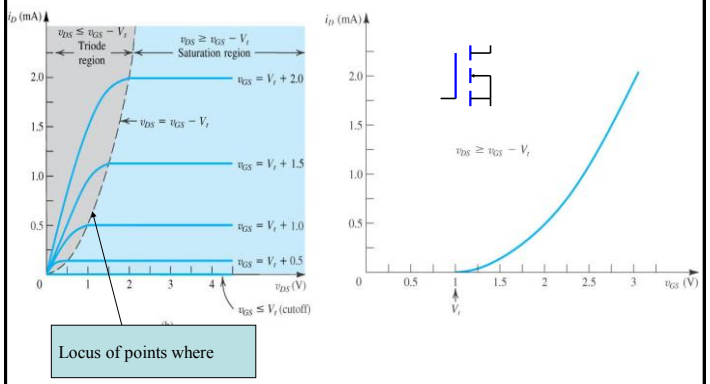
Current-Voltage Relationship of n-EMOSFET



Locus of points where

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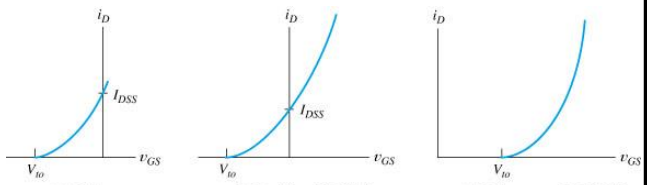
ID vs. VGS for n-channel devices

Drain current versus v_{GS} in the saturation region for *n*-channel devices.



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FET switching Summary

	e-MOSFET	d-MOSFET & FET
n-channel	ON, $V_G > V_T$ OFF, $V_G = 0$	ON, $V_G = 0$ OFF, $V_G < V_T$
p-channel	ON, $V_G < V_T$ OFF, $V_G = 0$	ON, $V_G = 0$ OFF, $V_G > V_T$

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The MOSFET

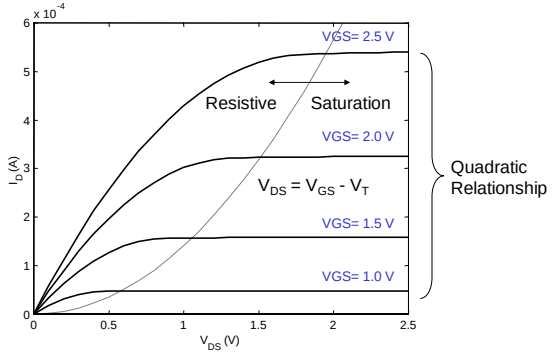
- The major geometrical parameters (dimensions) of importance are the length of the channel (L), the width of the channel (W) and the thickness of the gate oxide t_{ox}.
- In circuit design we can control L and W easily using our layout tools. We can also have some control over t_{ox}, but this is usually fixed by the CMOS process we wish to use (i.e.by the manufacturer or foundry)

Current-Voltage Relations Long-Channel Device

- In the cut-off region the device does not conduct. There is a specific voltage, which depends on the CMOS manufacturing process (Vt), that must be exceeded in order to induce sufficient charge in the channel to allow conduction to take place.
- In the linear region the current varies linearly with Vds for small values of Vds where the quadratic term can be ignored. Thus the device acts a a simple resistor in this region for small Vds.
- When the device is saturated the current becomes independent of Vds and only depends on β and the excess gate voltage above the threshold value. The current scales with the gain factor k_n of the device. This depends on the ratio of the width/length of the conducting channel. For a given length a wider device can conduct more current for a given supplied voltage (has a lower resistance). Note also that for high values of k_n we need t_{ox} to be small. The limiting factor here is that as tox gets smaller the electric field due to the gate voltage gets larger and at some point breaks down the gate oxide and destroys the transistor.

Current-Voltage Relations

If we vary the voltage between the drain and source electrode while keeping the gate electrode at some fixed voltage, we get the current flow shown in this slide



I-V Relations Long-Channel Device

Cut off region

Ids = 0 Vgs <VT

$$I_{DS} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Linear Region: $V_{DS} \leq V_{GS} - V_T$

$$I_D = k'_n \frac{W}{L}\left((V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right)$$

Gain factor kn

kn = kn'W/L

with

$$k'_n = \mu_n C_{ox} = \frac{\mu_n \varepsilon_{ox}}{t_{ox}}$$

Process Transconductance Parameter

V_T: threshold voltage

μ : carrier mobility

Saturation Mode: $V_{DS} \geq V_{GS} - V_T$

Channel Length Modulation

$$I_D = \frac{k'_n}{2}\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

Problems

4. Compare V_{DS} and $V_{GS} - V_T$ — we already know the device is not cutoff since $V_{GS} = 5 > V_T$

$V_{DS} = 2V$ $V_{GS} - V_T = 5 - 1 = 4V$

$V_{DS} < V_{GS} - V_T \Rightarrow$ LINEAR

$I_{DS} = k_n' \frac{W}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right]$ $k_n' = \frac{\varepsilon_{ox}}{t_{ox}}$

$\mu_n = 300 cm^2/Vs$ $t_{ox} = 20nm$ $k_n' = \frac{300 cm^2 Ns \cdot 3.5 \times 10^{-13}}{20 \times 10^{-9} \times 10^{-2}}$

$I_D = 5.25 \times 10^{-5}\left[4 \cdot 2 - \frac{2^2}{2}\right]$

$= 5.25 \times 10^{-5} \cdot 5.6 \approx 1.6 mA$

convert to cm.

$= 5.25 \times 10^{-5}$