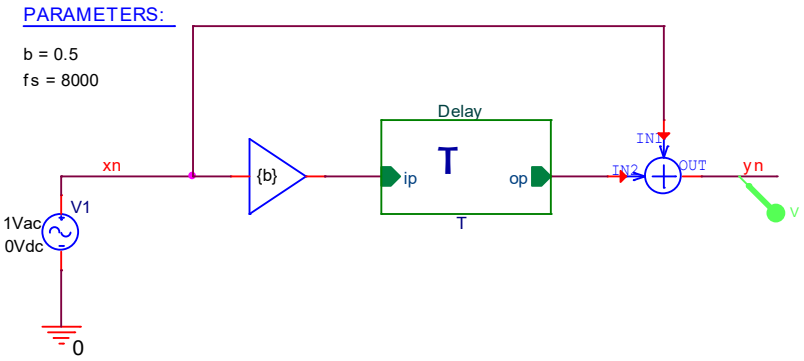
Lab 3: FIR filter frequency response

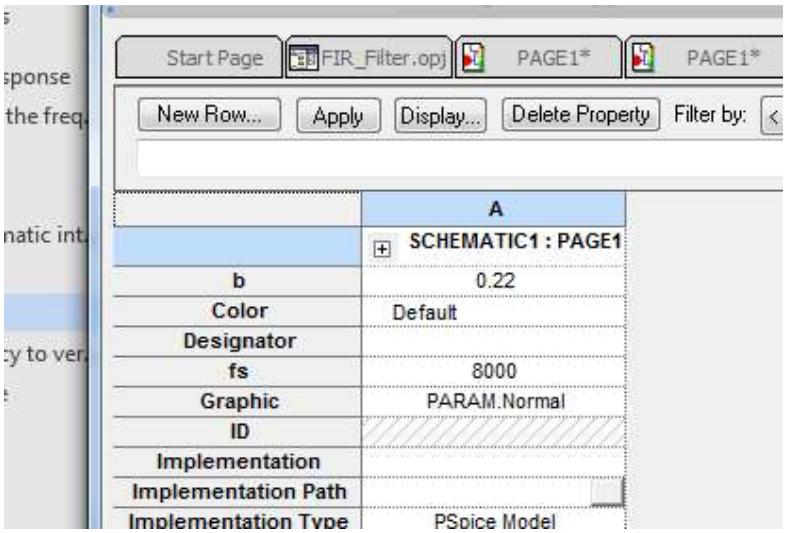
Objective: To investigate the frequency response of an FIR filter

Procedure:

Enter the following schematic into Pspice. When you are setting up the initial project in Pspice you can create it in a directory such as c:\Temp\FIR_filter. It will then be easy to find all of the schematic files and you can back up the entire FIR_filter folder to a USB drive and use for other simulations. The amplifier is called 'GAIN' and the summing element is 'SUM'.

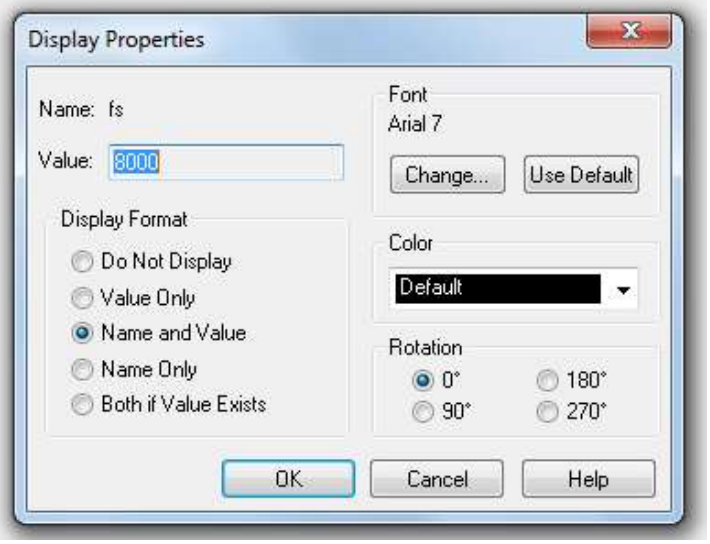


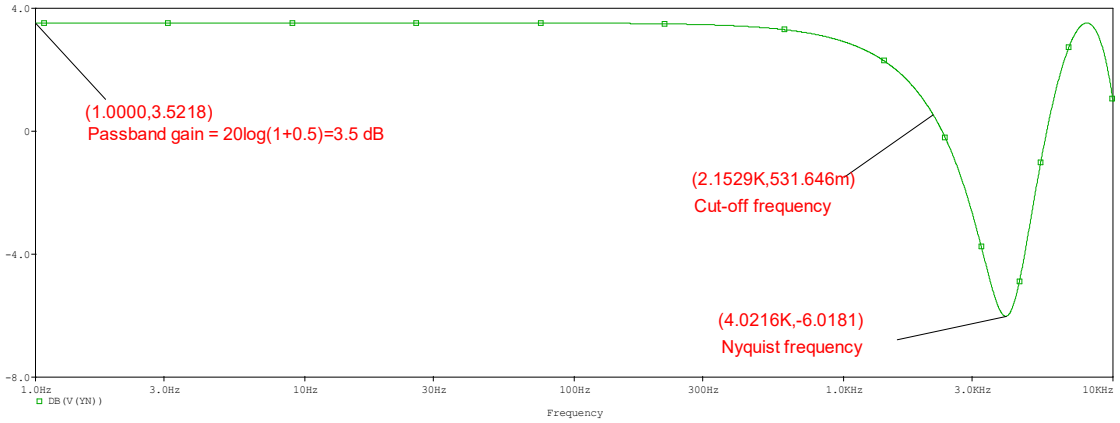
Sweep the input frequency to verify the DC gain and cut-off frequency. See further down for the design of the hierarchical block. Note that the parameters are placed into the ***Param*** part. When you double-click the Param part you can add a new property and its value as follows:



You can then display the parameters by using the display properties as follows:

	A
	SCHEMATIC1 : PAGE1
b	0.22
Color	Default
Designator	
fs	8000
Graphic	PARAM.Normal
ID	
Implementation	
mplementation Path	
nplementation Type	PSpice Model
ocation X-Coordinate	200
ocation Y-Coordinate	160
Name	INS43
Part Reference	1
PCB Footprint	
Power Pins Visible	
Primitive	DEFAULT
PSpiceOnly	TRUE



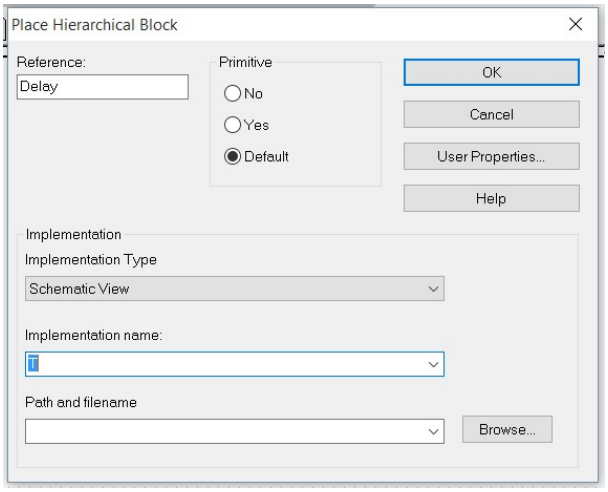


Perform at parametric sweep of the filter coefficient (*b*) from 0.5 to 0.9 in steps of 0.1 and plot the outputs in each case. How does the filter gain and cut-off frequency vary with b? What happens to the frequency response if b=-0.5?

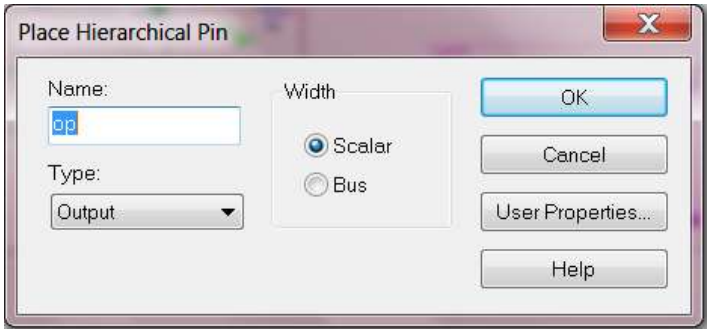
Hierarchical Blocks in Pspice

Procedure:

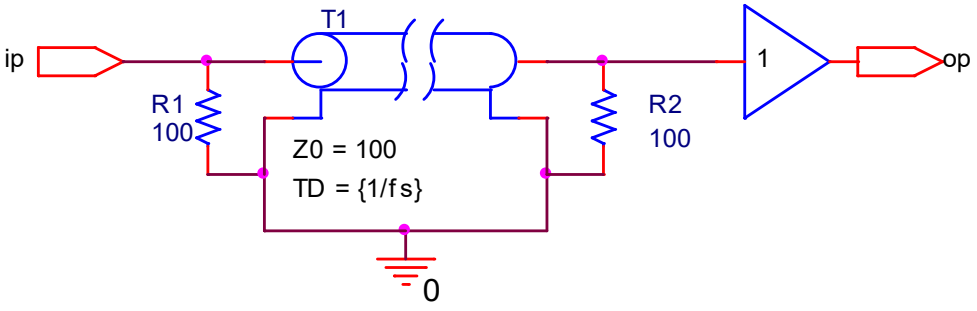
Click on the 'Place Hierarchical Block' on the right-hand side of the screen.  Use the mouse to drag out the shape of the box. Note that the reference in the example below is Delay and the name is T.



Put in the reference name, implementation name and use implementation type as schematic view as shown above. Then click the place pin icon below the hierarchical block icon:



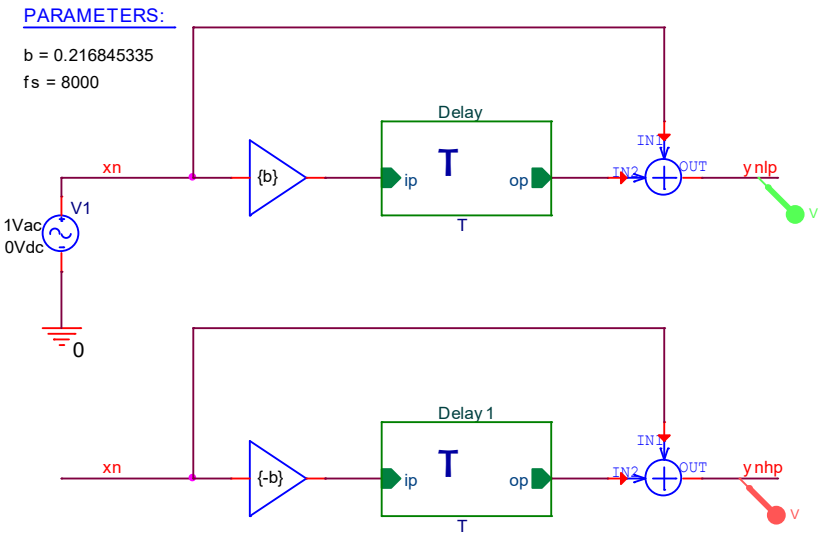
Place the input and output pins. Then right click on the block and descend hierarchy. Connect up as shown below:

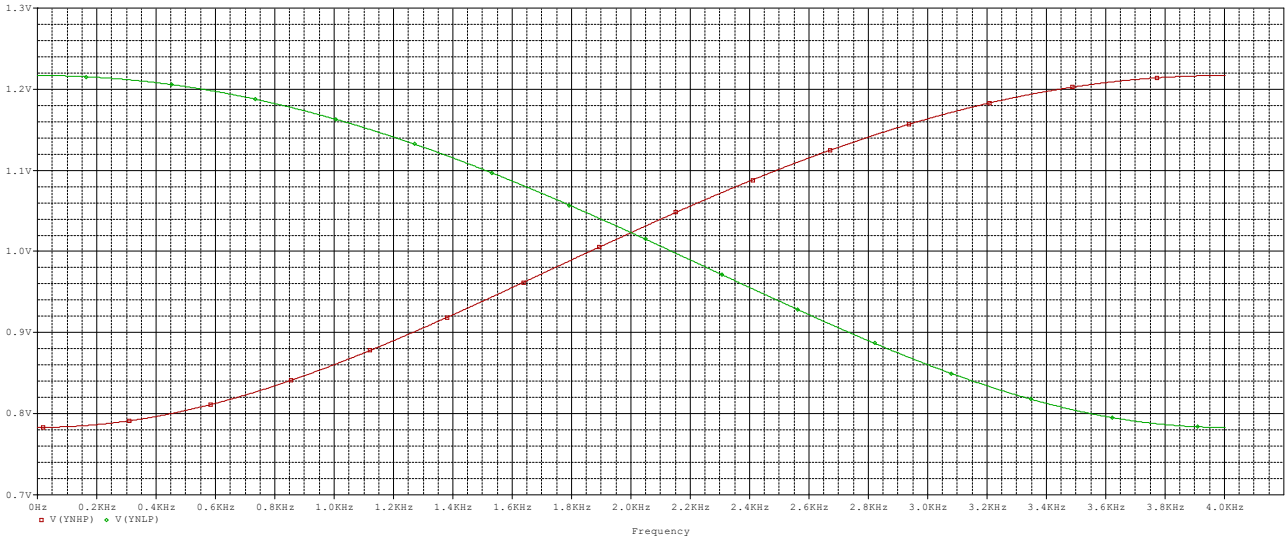


You can now use this schematic as the basis of more complex simulations. You can copy the schematic and edit it appropriately.

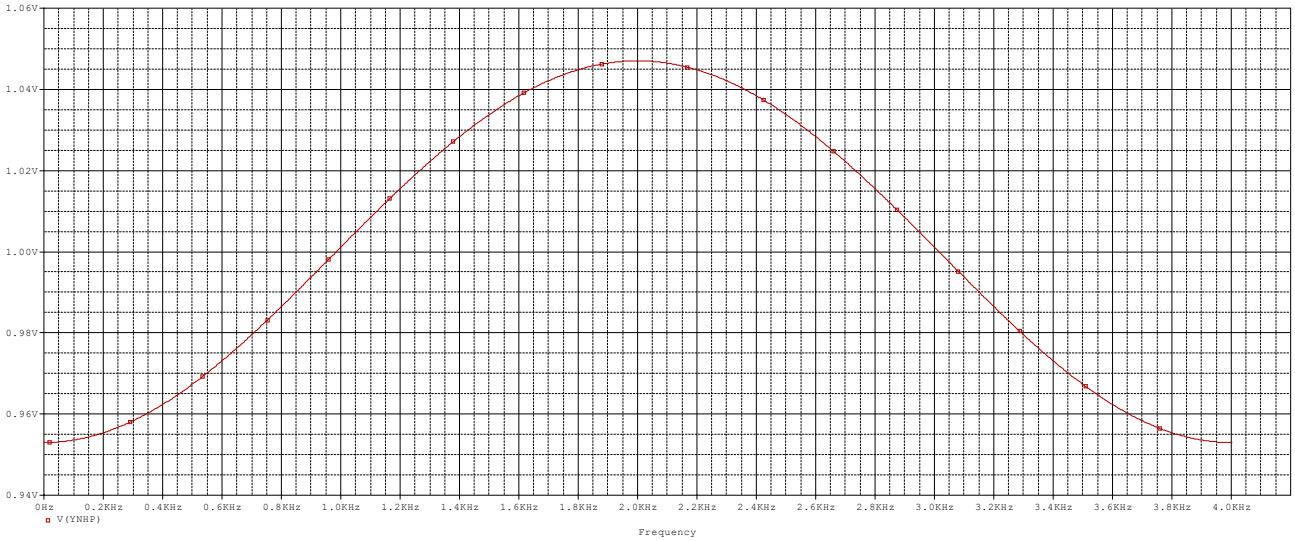
Use an Excel spreadsheet to design a digital low-pass filter with a cut-off frequency of 6000 Hz and a digital high-pass filter with a cut-off frequency of 2000 Hz. Use a sampling frequency of 16000 Hz. Use the equations in the notes provided to design the spreadsheet. The spreadsheet should provide the 'b' coefficient value for each filter.

Connect the LPF to the HPF and plot the combined frequency response. Comment on the result obtained.





To get the combined response you need to connect the LPF output to the HPF input.



Design of an FIR Low Pass 1st Order Digital Filter

fs	fc	Qc	cosQc	1-2cosQc	(2cosQc-1)^2	sqrt((2cosQc-1)^2-1)	b1	b2
16000	6000	2.356194	-0.70711	2.414213562	5.828427125	2.197368227	4.611582	0.216845

Design of an FIR High Pass 1st Order Digital Filter								
fss	fcc	Qcc	cosQc	-(1+2cosQc)'	(2cosQc+1)^2	sqrt((2cosQc+1)^2-1)	b1	b2
16000	2000	0.785398	0.707107	-2.414213562	5.828427125	2.197368227	-0.2168453	-4.61158