

output	[15:0] address
inout	[7:0] data
input	RES
input	DBE L puts deta in Hit
oulpt	RJU
output	ϕ_{i}
oul put	Ø _L
input	clock
input	RDO RAM
input	NMI reg edge Pon
input	NP-CD
	<u>c</u> a



