```vhdl
-----------------------------------------
-- Block code:  testbench_uart_rx_only_top.vhd
-- History:     13.Mar.2018 - 1st version (dqtm)
--                 <date> - <changes>  (<author>)
-- Function: Testbench for uart_rx_only_top in EA999 - Lab2
--
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-- Library & Use Statements
LIBRARY ieee;
use ieee.std_logic_1164.all;

-- Entity Declaration
ENTITY testbench_uart_rx_only_top IS

END testbench_uart_rx_only_top ;


-- Architecture Declaration
ARCHITECTURE struct OF testbench_uart_rx_only_top IS

    -- Components Declaration
COMPONENT uart_rx_only_top
    PORT
    (
        CLOCK_50 :  IN   STD_LOGIC;
        GPIO_1_1 :  IN   STD_LOGIC;
        KEY_N_0 :   IN   STD_LOGIC;
        HEX0_N :    OUT  STD_LOGIC_VECTOR(6 DOWNTO 0);
        HEX1_N :    OUT  STD_LOGIC_VECTOR(6 DOWNTO 0);
        LEDR_0 :    OUT  STD_LOGIC
    );
END COMPONENT;


    -- Signals & Constants Declaration
    -- Inputs
    SIGNAL tb_clock     : std_logic;
    SIGNAL tb_reset_n   : std_logic;
    SIGNAL tb_serdata   : std_logic;
    -- Outputs
    SIGNAL tb_ledr      : std_logic;
    SIGNAL tb_hex_0     : std_logic_vector(6 downto 0);
    SIGNAL tb_hex_1     : std_logic_vector(6 downto 0);

    CONSTANT clk_50M_halfp  : time := 10 ns;        -- Half-Period of Clock 50MHz
    CONSTANT baud_31k250_per : time := 32 us;       -- One-Period of Baud Rate
    31.25KHz

    SIGNAL tb_reg0_hi   : std_logic_vector(3 downto 0); -- to check DUT-internal
    signal
    SIGNAL tb_reg0_lo   : std_logic_vector(3 downto 0);

    SIGNAL tb_test_vector : std_logic_vector(9 downto 0); --
    (stop-bit)+(data-byte)+(start-bit) to shift in serial_in

BEGIN
  -- Instantiations
  DUT: uart_rx_only_top
  PORT MAP (
    CLOCK_50    =>  tb_clock ,
    GPIO_1_1    =>  tb_serdata ,
    KEY_N_0     =>  tb_reset_n ,
    HEX0_N      =>  tb_hex_0 ,
    HEX1_N      =>  tb_hex_1 ,
    LEDR_0      =>  tb_ledr
        );

  -- Clock Generation Process
    generate_clock: PROCESS
    BEGIN
```

```
69          tb_clock <= '1';
70          wait for clk_50M_halfp;
71          tb_clock <= '0';
72          wait for clk_50M_halfp;
73      END PROCESS generate_clock;
74
75
76      -----------------------------------------
77      -- VHDL-2008 Syntax allowing to bind
78      --           internal signals to a debug signal in the testbench
79      -----------------------------------------
80      tb_reg0_hi <= <<signal DUT.hexa_hi : std_logic_vector(3 downto 0) >>;
81      tb_reg0_lo <= <<signal DUT.hexa_lo : std_logic_vector(3 downto 0) >>;
82
83
84    -- Stimuli Process
85      stimuli: PROCESS
86      BEGIN
87          -- STEP 0
88          report "Initialise: define constants and pulse reset on/off";
89          tb_serdata <= '1';
90          tb_test_vector <= B"1_0001_0010_0"; -- (stop-bit)+(data-byte)+(start-bit)
91          ----------------
92          tb_reset_n <= '0';
93          wait for 20 * clk_50M_halfp;
94          tb_reset_n <= '1';
95          wait for 100 us;  -- introduce pause to check HW-bug after reset release
96
97          -- STEP 1
98          report "Send (start-bit)+(data-byte)+(stop-bit) with baud rate 31250 (async
            from clk50M)";
99          wait for 200 * clk_50M_halfp;
100
101         -- shift-direction is LSB first
102         -- START-BIT
103         -- BIT-0 (LSB-first of lower nibbl
104         -- BIT-1
105         -- ...
106         -- BIT-7
107         -- STOP-BIT
108         -- SERDATA BACK TO INACTIVE
109         for I in 0 to 9 loop
110             tb_serdata <= tb_test_vector(I);
111             wait for baud_31k250_per;
112         end loop;
113
114         -- STEP 2
115         report "Wait few clock_50M periods and check parallel output";
116         wait for 20 * clk_50M_halfp;
117         assert (tb_reg0_hi = x"1") report "Reg_0 Lower Nibble Wrong" severity note;
118         assert (tb_reg0_lo = x"2") report "Reg_0 Lower Nibble Wrong" severity note;
119         wait for 20 * clk_50M_halfp;
120
121         -- stop simulation
122         assert false report "All tests passed!" severity failure;
123
124     END PROCESS stimuli;
125
126     -- Comments:
127     -- remember to re-save wave.do after setting radix and time ranges
128     -- use >wave>format>toggle leaf names  to display shorter names
129     -- remark syntax with aux debug signal to track in TB internal DUT signals
130
131 END struct;
132
133
```