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ECE 0257 Midterm Reflection

You should have received an email containing a link to your midterm exam.

Instructions

- Briefly review your exam
- Use SPICE to model and simulate the problem
- Based on the simulation results, re-examine / re-solve the problem and try to identify where you made a mistake, gaps in your knowledge or new insights you gain from simulating the problem
- Fill out the worksheet on the following pages.

Problem #1

Determine R2 such that Vout = 2.4V. Assume that the diodes are all the same semiconductor diode and have a VD = 0.7 Voltage drop at a current of Id = 1 mA and VT = 25 mV

- To simulate this problem, use the Dbreak component from the BREAKOUT library
- We must also change the diode parameters such that it will accurately model the diode
 given in the problem. In order to do this, right click on the diodes, select EDIT PSPICE
 MODEL, and change the model parameters such that it reads similar to the line below:

.model Dbreak D Is=7e-16

 While the simulated result will not match hand calculations exactly, the simulated result should be quite similar to the target value (e.g. Vout = ~2.4V, not 2.1 or 2.2 V)

If you would like to submit a new response to this question, please enter it below. If not, leave the box below blank.

 $R_2 = 140 \text{ ohms}$

If you submitted a new response, you must explain the source of any differences between <u>your</u> original exam response and the correct/simulated results in order to receive credit.

I think that when I first looked at the problem, I thought that V_out was 2.1 V which would be fairly straightforward with the constant voltage-drop model (I think I even drew a 2.1 V voltage source to the side on this problem). I thought that the thermal voltage parameter was added in as extra, unnecessary information. When I went back to the problem to check it, I realized it was 2.4 V and by that time I didn't really have enough time to go through and solve it.

Problem #2 - Part 1

Determine the voltage V_{out} assuming that the diodes are ideal.

- To simulate this problem, use the **Dbreak component** from the **BREAKOUT library** Since SPICE does not model perfect, ideal diodes, the solution that you simulate will

	some differences. However, by observing the currents through the diodes, you lid be able to get an indication of whether or not your original response was correct.
-	ald like to submit a new response to this question, please enter it not, leave the box below blank.
V _{out} =	
Problem #2 Determine the	2 – Part 2 e voltage V_{out} assuming that the diodes follow the constant voltage drop model
The c	constant voltage drop model assumes a 0.7V drop across each conducting diode. current through the simulated diodes might be such that V_D will not be exactly equal 7V, but the simulated result should be quite similar
•	ald like to submit a new response to this question, please enter it not, leave the box below blank.
V _{out} =	
explain the	mitted a new response to either of these questions, you must e source of any differences between <u>your</u> original exam response prect/simulated results in order to receive credit.

Problem #3

Determine the current through diode D9 (i_{D9}), the current through Diode D10 (i_{D10}) and the output voltage (V_{out}). Assume the diodes follow the constant voltage drop model.

- To simulate this problem, use the Dbreak component from the BREAKOUT library
- The constant voltage drop model assumes a 0.7V drop across each conducting diode.
 The current through the simulated diodes might be such that V_D will not be exactly equal to 0.7V, but the simulated result should be quite similar

If you v	vould like to subr	nit a new response	to this question,	please enter it
below.	If not, leave the I	oox below blank.		

i _{D9} = i _{D10} = V _{out} =					
If you submitte differences bet results in orde	ween <u>your</u> ori	ginal exam r	ist explain the esponse and	source of any the correct/simula	ted

Problem #4 - Part 1

Determine V_{out} when $V_{IN} = -1V$

- To simulate this problem, use the **Dbreak component** from the **BREAKOUT library**
- The constant voltage drop model assumes a 0.7V drop across each conducting diode. The current through the simulated diodes might be such that VD will not be exactly equal to 0.7V, but the simulated result should be quite similar

If you would like to submit a new response to this question, please enter it below. If not, leave the box below blank.

V _{out} =	

Problem #4 – Part 2

Sketch the voltage-transfer characteristic (V_{out} vs V_{in}) for an input of -5V $\leq V_{in} \leq +5V$

Modeling this problem requires this problem requires a DC voltage sweep

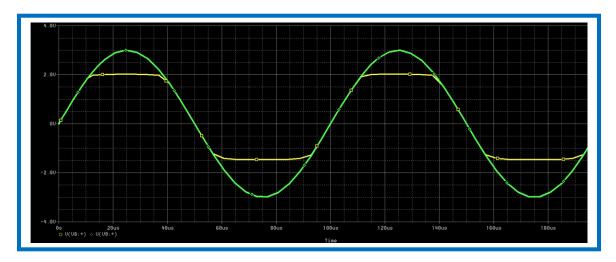
If you would like to submit a new response to this question, please insert an <u>image</u> below. If not, leave the box below blank. This image can be either hand drawn or exported from the simulator.

Problem #4 - Part 3

Sketch the transient output waveform for V_{out} given the following input waveform for V_{in}

- Modeling this problem requires this problem requires a transient simulation.
- The input voltage is a VSIN voltage source with an amplitude of 3V, offset voltage of 0V and a frequency of 1kHz

If you would like to submit a new response to this question, please insert an <u>image</u> below. If not, leave the box below blank. This image can be either hand drawn or exported from the simulator.



If you submitted a new response to part 1, part 2 or part 3, you must explain the source of any differences between <u>your</u> original exam response and the correct/simulated results in order to receive credit.

I think I made a mistake when figuring out how high the output waveform should go when the input waveform is in the positive region. Also, my output waveform should have "hugged" the input waveform more in the regions where V_out = V_in because none of the diodes are conducting. I think I realized this during the test, but when I actually went to draw the plot I was more focused on drawing it at the right points than making the waveforms be equal in those regions.

Determine the output Voltage Vout

- In order to simulate this problem, use the D1N4733 component from the DIODE library
- There are quite a number of additional physics incorporated in to the D1N4733 SPICE model that our calculations do not account for. However, results should be fairly similar

If you would like to submit a new response to this question, please enter it below. If not, leave the box below blank.



Problem #5 – Part 2

Determine the load regulation for this circuit when a 1k ohm load resistance is attached

 In order to model this problem, you will need to compare the change in current through the load after the load is attached

If you would like to submit a new response to this question, please enter it below. If not, leave the box below blank.

Load regulation = -1.74 mV/mA

If you submitted a new response to either of these questions, you must explain the source of any differences between <u>your</u> original exam response and the correct/simulated results in order to receive credit.

For Part 2, I think I just got the formulas for line regulation and load regulation mixed up when I went to look at my notes sheet. I tried to calculate the line regulation, but that was not what the problem asked for.

For the following circuit Vt = 0.5V, k' = 100 uA/V2. If the transistor is fabrication using a L = 90nm integrated circuit process, what should W be set to in order to obtain the following output voltages?

- In order to simulate this problem, use the MBREAKN3 component from the BREAKOUT library
- We must also change the MOSFET parameters such that it will accurately model the
 device given in the problem. In order to do this, right click on the MOSFET, select EDIT
 PSPICE MODEL, and change the model parameters such that it reads similar to the line
 below:

.model Mbreakn NMOS VTO=.5 KP=100u W=YOUR SOLUTION L=90n

 You can start by substituting your original answer for YOUR_SOLUTION and observe to see if the voltages match. The letter n is the suffix for nanometers and u is the suffix for micrometers

If you would like to submit a new response to this question, please enter it below. If not, leave the box below blank.

W =		

If you submitted a new response to either of these questions, you must explain the source of any differences between <u>your</u> original exam response and the correct/simulated results in order to receive credit.

Problem #7 - Part 1

The follow circuit is a digital logic inverter. What region of operation is M7 in (a PMOS transistor) when Vin = Logic Low (0V)?

In order to simulate this problem, use the MBREAKN3 (NMOS) and MBREAKP3 (PMOS) components from the BREAKOUT library

We must also change the MOSFET parameters such that it will accurately model the device given in the problem. In order to do this, right click on the NMOS device, select EDIT PSPICE MODEL, and change the model parameters such that it reads similar to the line below:

.model Mbreakn NMOS VTO=.5 KP=100u W=10u L=1u

• Edit the PMOS device such that it has the following parameters

.model Mbreakp PMOS VTO=.5 KP=50u W=20u L=1u

- You can investigate solutions in a variety of ways.
 - 1) You can set the input voltages to match the conditions described and observe the output voltages.
 - 2) You can disconnect the NMOS/PMOS devices and test them separately. To model the problem, you could fix the drain voltage (Vout) via a DC source to match what the output voltage should be for a given input condition. Then, if you carry out a DC sweep, you can see what regime the device is in at the given Vin.
 - Or 3) observe the current and voltages during a transient simulation and work the equations backwards. Please note, a logic inverter will only have current flow when the input switches, so you would need to use VPULSE in order to verify it

If you would like to submit a new response to this question, please enter it below. If not, leave the box below blank.

Region =	

Problem #7 - Part 2

The follow circuit is a digital logic inverter. What region of operation is M7 in (a PMOS transistor) when Vin = Logic High (5V)?

If you would like to submit a new response to this question, please enter it below. If not, leave the box below blank.

Region = Cutoff

If you submitted a new response to either of these questions, you must
explain the source of any differences between your original exam response
and the correct/simulated results in order to receive credit.

I just made a mistake as to what equation I should use. I should have applied the cutoff equation because that takes precedence over the saturation equations.	

Being able to analyze your quiz and reflect on your thinking process is an essential part of learning.

If you changed any of your results, or gained any new insights about your thinking process / problem solving skills, please summarize below (i.e. How can you use this comparison experience to improve in the future?)

The biggest thing I took from this is that I shouldn't forget to bring my calculator to a midterm that involves a lot of calculations. Even if it didn't affect my actual answers, it definitely threw me off and caused me to feel uncomfortable for most of the test. Beyond that, I just think that I need to think more clearly about my answers and try to reason them out. It's not enough to get an answer that I think could be right – I need to be able to justify how I got there.