Start by renaming registers to physical registers and then draw the timeline. Physical registers are allocated in the order of: p0, p1, p2, p3, p4, …

Cycle	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
lw p0, 8(p10)	EX	MEM	WB																						
addi p1, p0, 20			EX	MEM	WB																				
sw p1, 8(p10)				EX	MEM	WB																			
lw p2, 12(p10)		EX	MEM	WB																					
sw p2, 16(p10)					EX	MEM	WB																		
beq p2, p10, loop			EX	MEM	WB																				
lw p3, 8(p10)			EX	MEM	WB																				

* All instructions have already been dispatched so there will only be EX, MEM, WB stages (no IF or ID).
* When there is a choice, the scheduler always prioritizes older instructions.