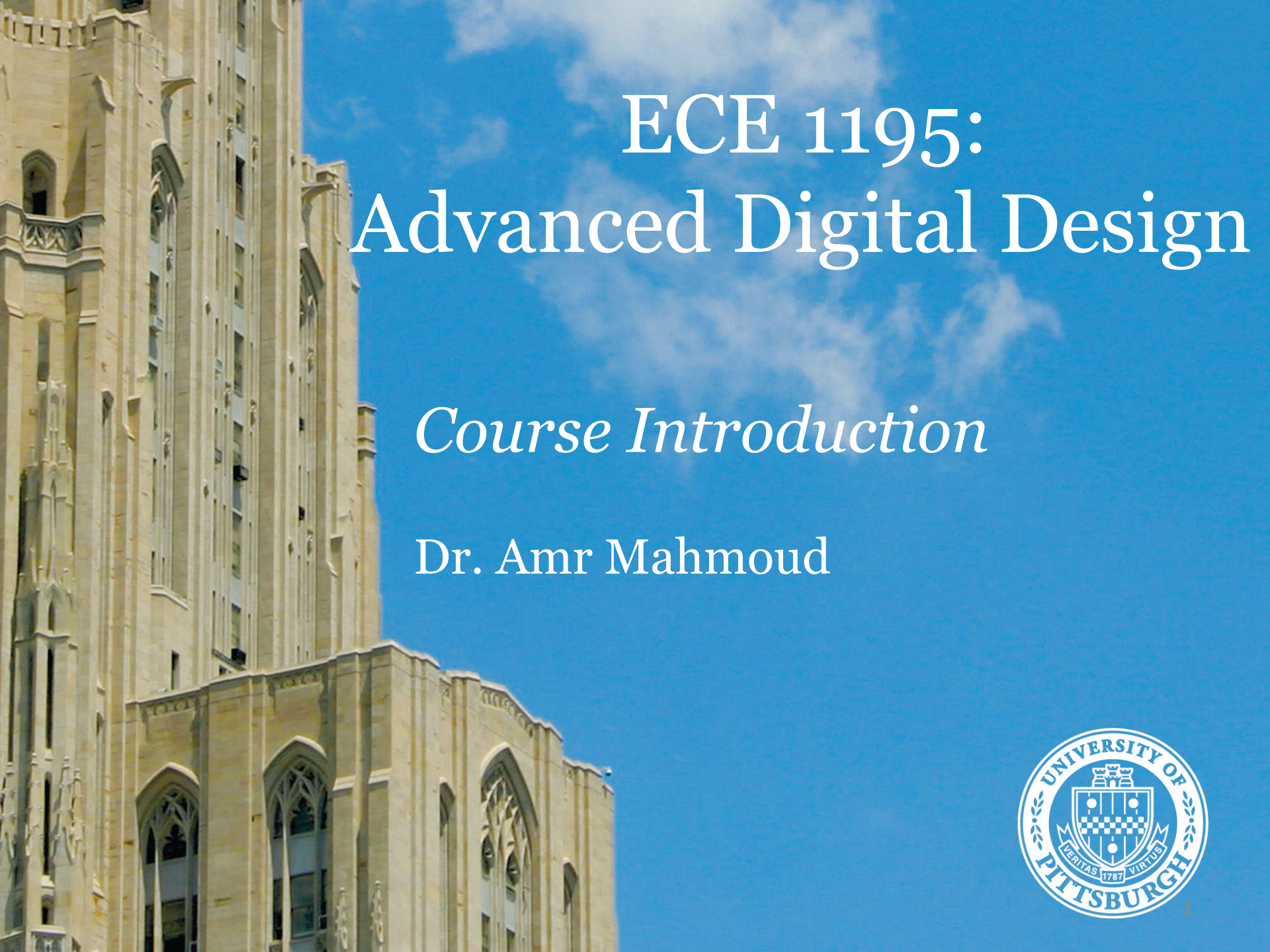

ECE 1195: Advanced Digital Design

Course Introduction

Dr. Amr Mahmoud

Course Description

The objective of this course is to teach the tools and techniques used in the design of large scale digital systems. The course consists of a series of design projects centered on modern microprocessor design. This design experience is intended to teach you both the context and content of the design process. You will learn to use a set of design tools in a modern commercial design flow and about the dynamics of working in a design group. As content, you will explore the design of a modern microprocessor, see the design tradeoffs within its implementation, and learn how to evaluate good (and bad) design

Instructor

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Prerequisites

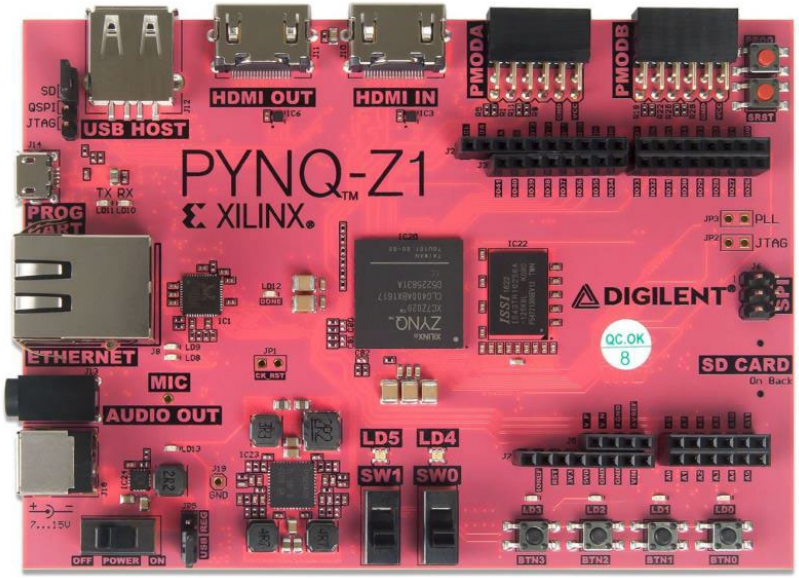
ECE 0201 and ECE 0202

How This Class Will function

- Each Lab will begin with a lecture and will include supplemental lectures during the course of the Lab
- You will spend time **in class** (**and out of class!**) working on your designs
- Submissions will be checked by myself or the TAs – demonstrations are required to receive credit

Tools for this course

- PYNQ-Z1 Kit



Tools for this course

- You will be given the board kit soon.
- Use it for the whole semester.
- Return it back at the end of the semester.

- Failure to return the board may result in a G grade until the board is returned

Tools for this course

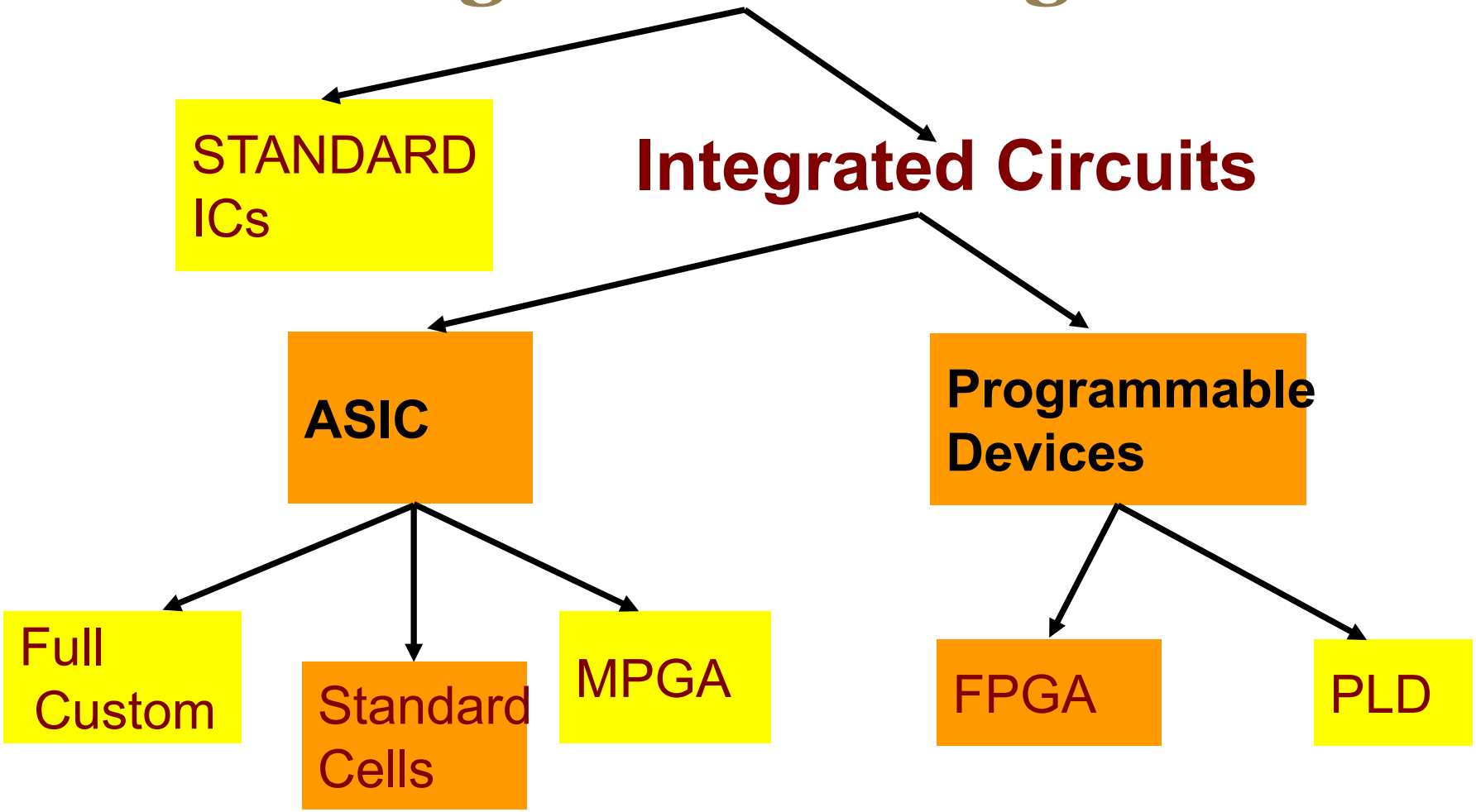
- Vivado HL Design Edition 2018.3

THINGS TO DO TODAY

- Canvas walk-through

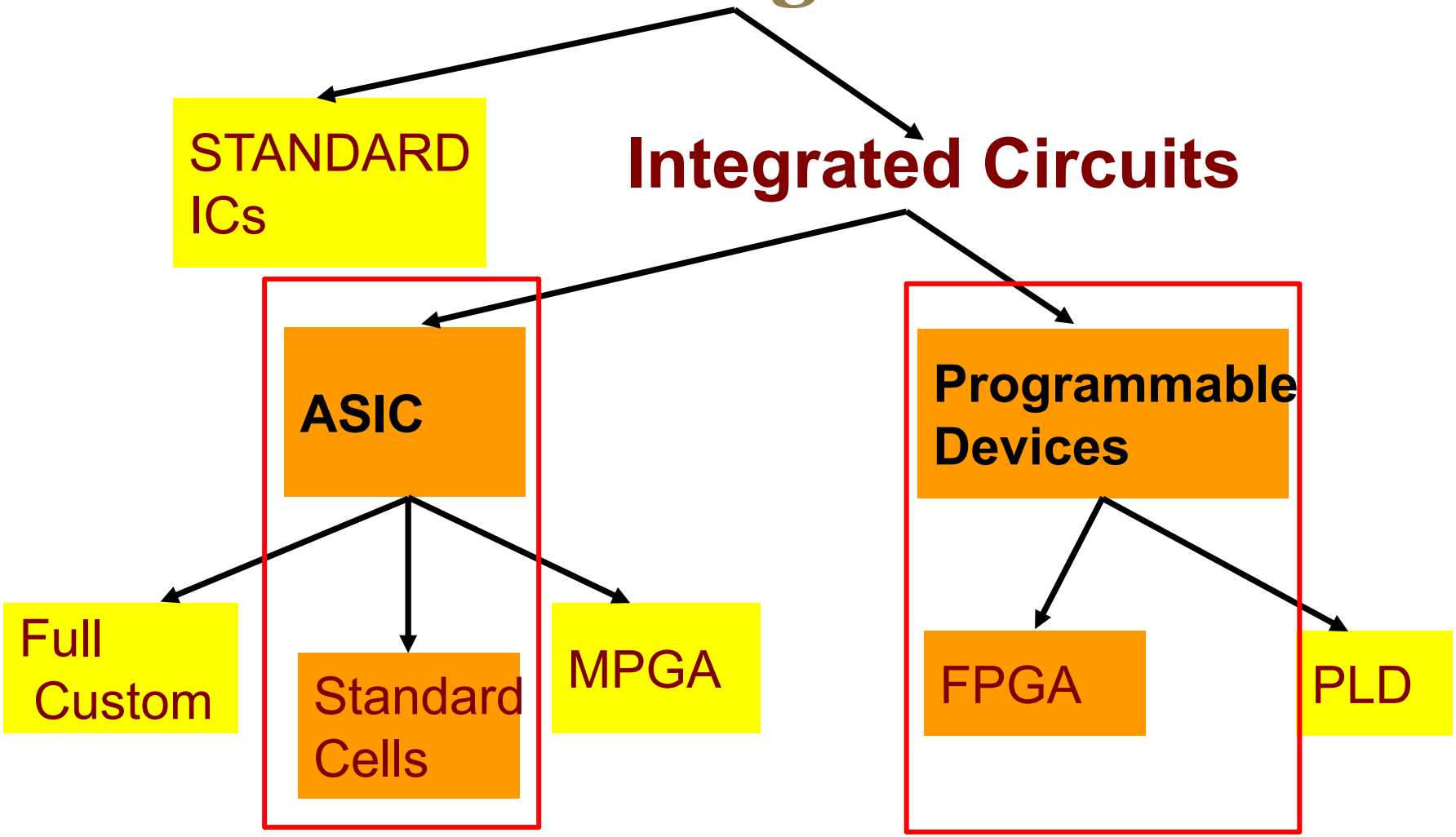
- Complete the following before our next lecture
  - Vivado HLx Design Edition 2018.3
  - Pre-Lab Tutorial

Design Methodologies



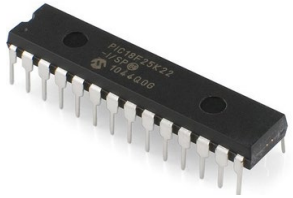
Where do you use the VHDL ???

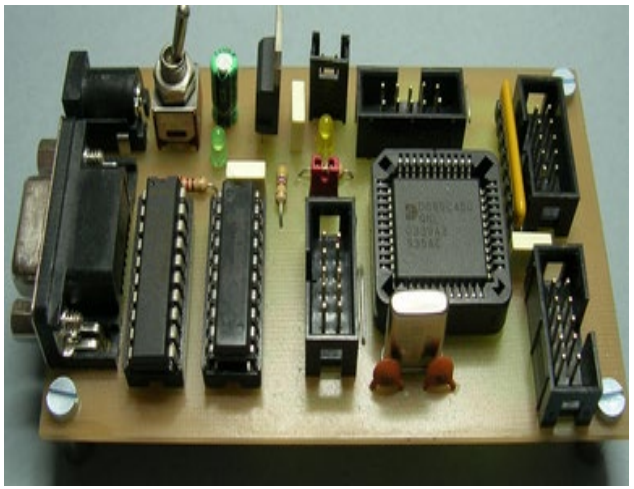
Design



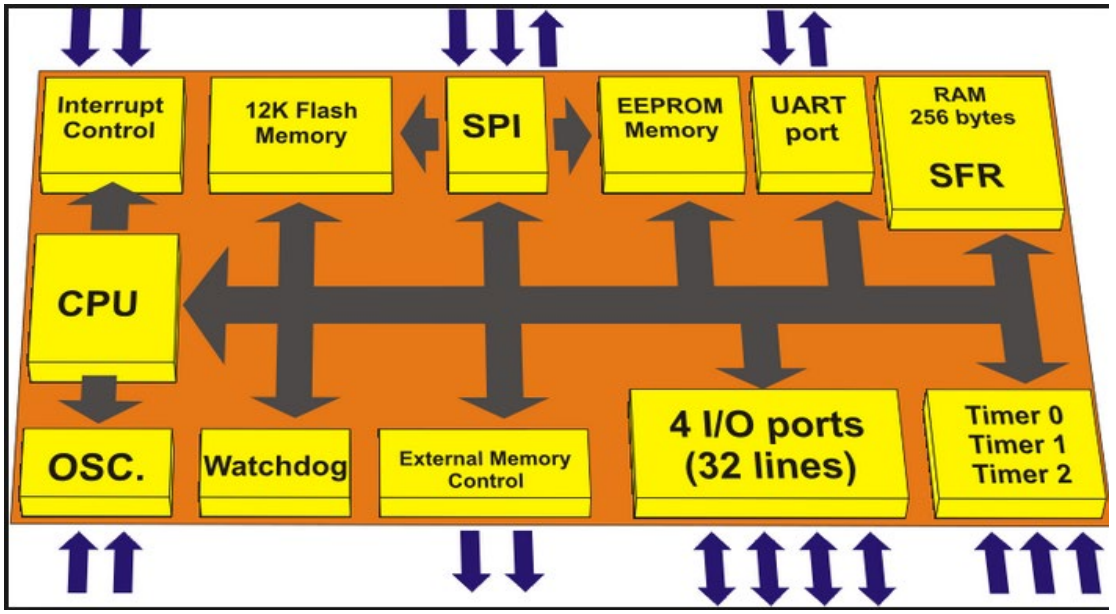
These two approaches are started by VHDL Code

STANDARD ICs

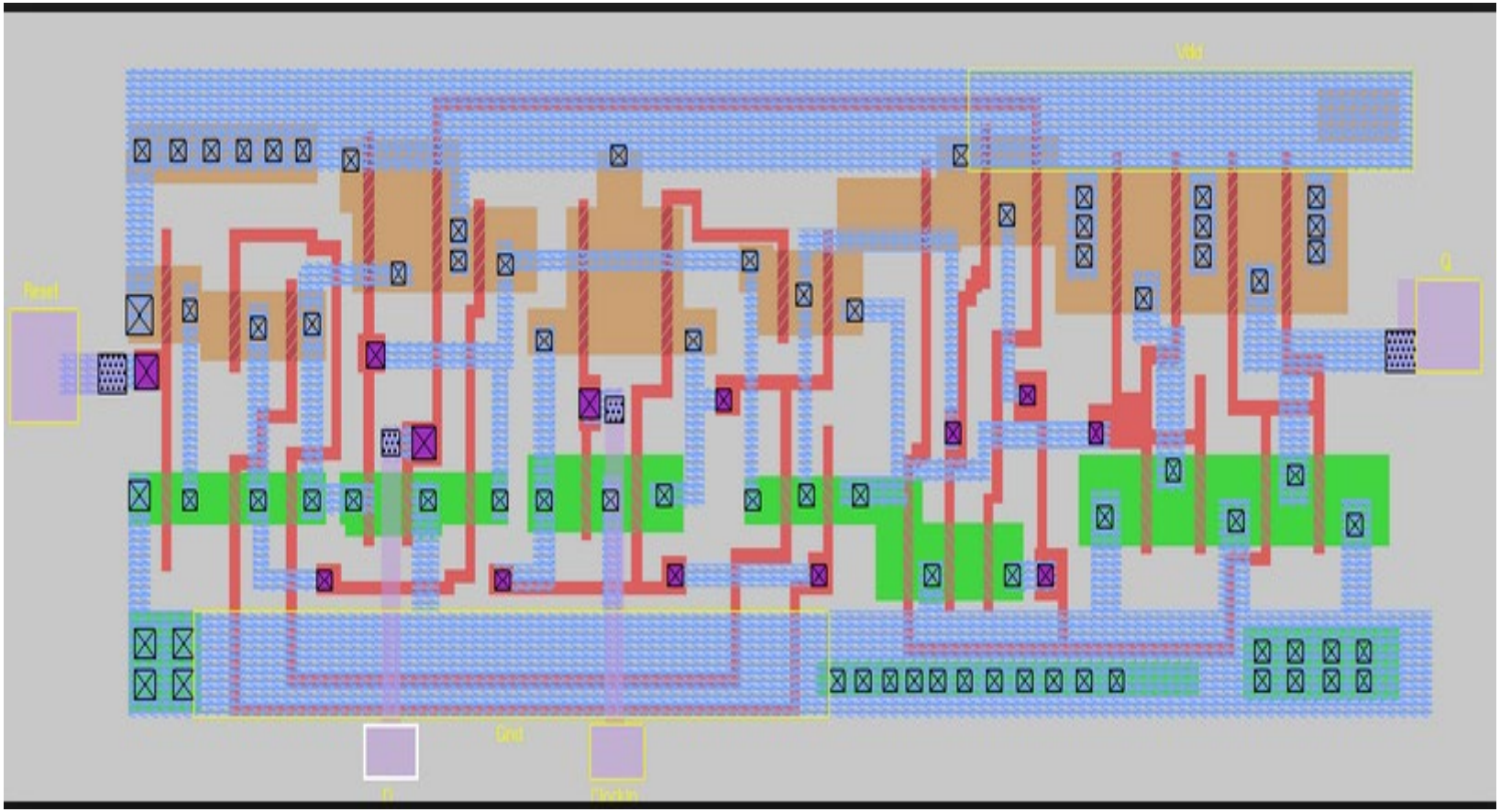




Microcontroller



FULL CUSTOM



ASIC versus FPGA

ASIC
Application **S**pecific
Integrated **C**ircuit

- Designs must be sent for expensive and time consuming fabrication in semiconductor foundry

- Designed all the way from behavioral description to physical layout

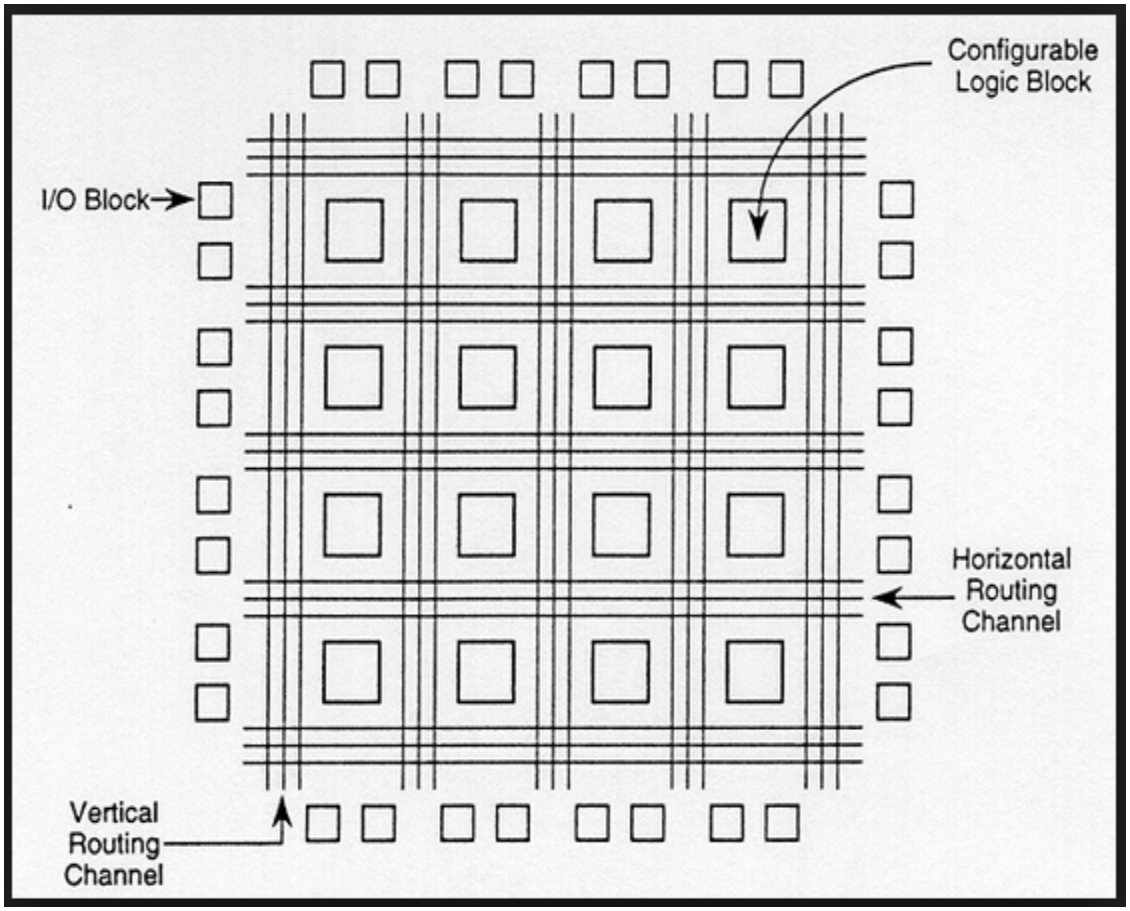
FPGA
Field **P**rogrammable
Gate **A**rray

- Bought off the shelf and reconfigured by designers themselves

- No physical layout design; design ends with a bitstream used to configure a device

What is an FPGA Chip ?

- Field Programmable Gate Array
- A chip that can be configured by user to implement different digital hardware
- Configurable Logic Blocks (CLB) and Programmable Switch Matrices
- Bitstream to configure: function of each block & the interconnection between logic blocks



Source: [Brown99]

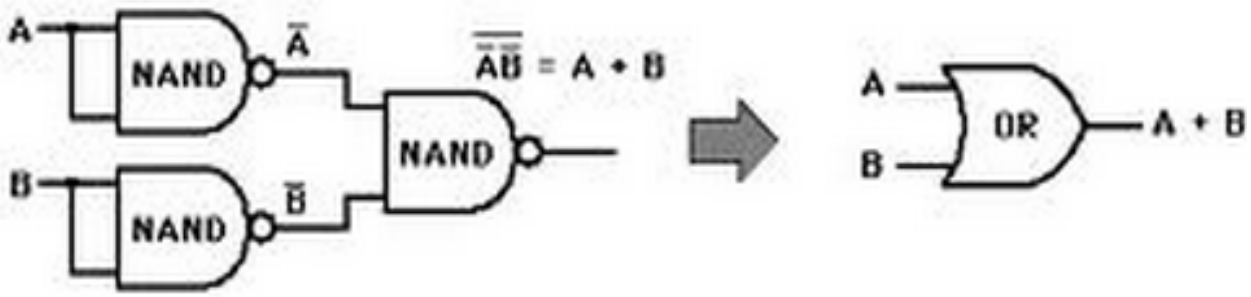
FPGA Example

- Implement F= (A or B) using FPGA if the CLB is an NAND gate.

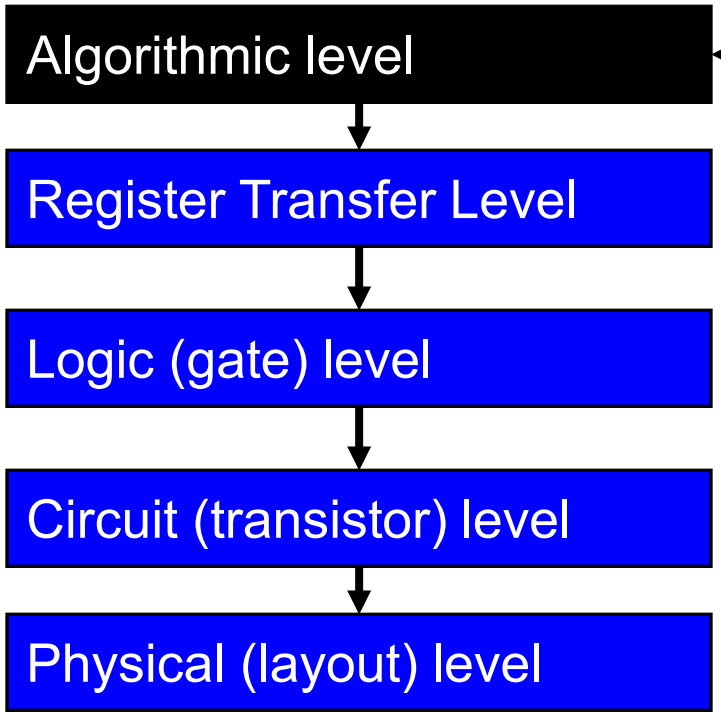
FPGA Example

- Implement F= (A or B) using FPGA if the CLB is an Nand gate.

Solution



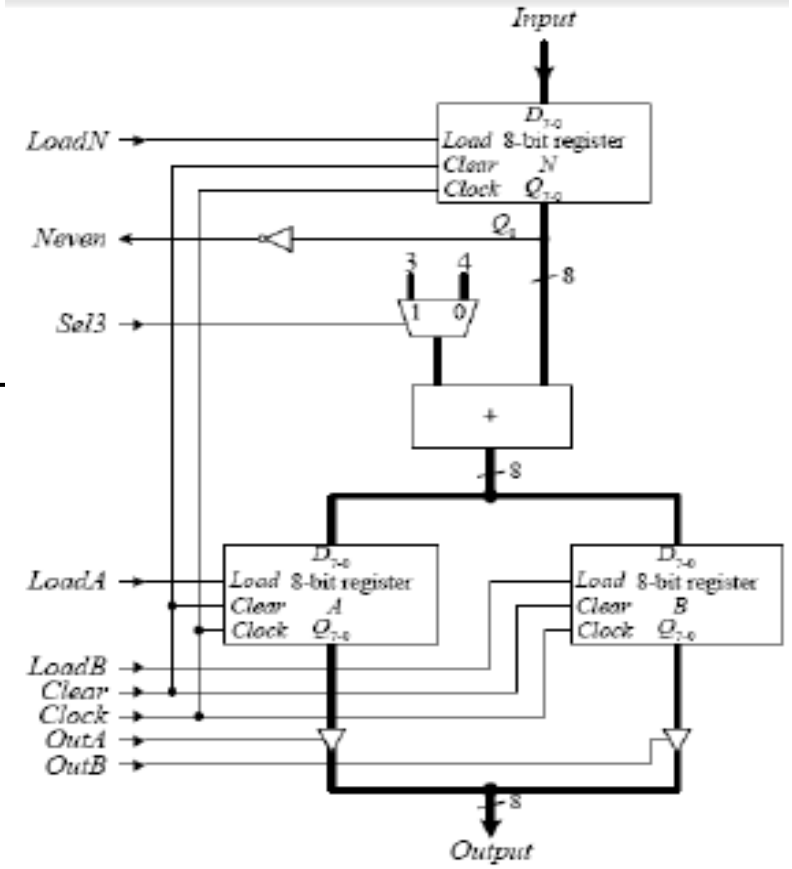
Levels of Design Description




```
input N
if (N is an even number) then
A = 3 + N
else
B = 4 + N
end if
output A
output B
```

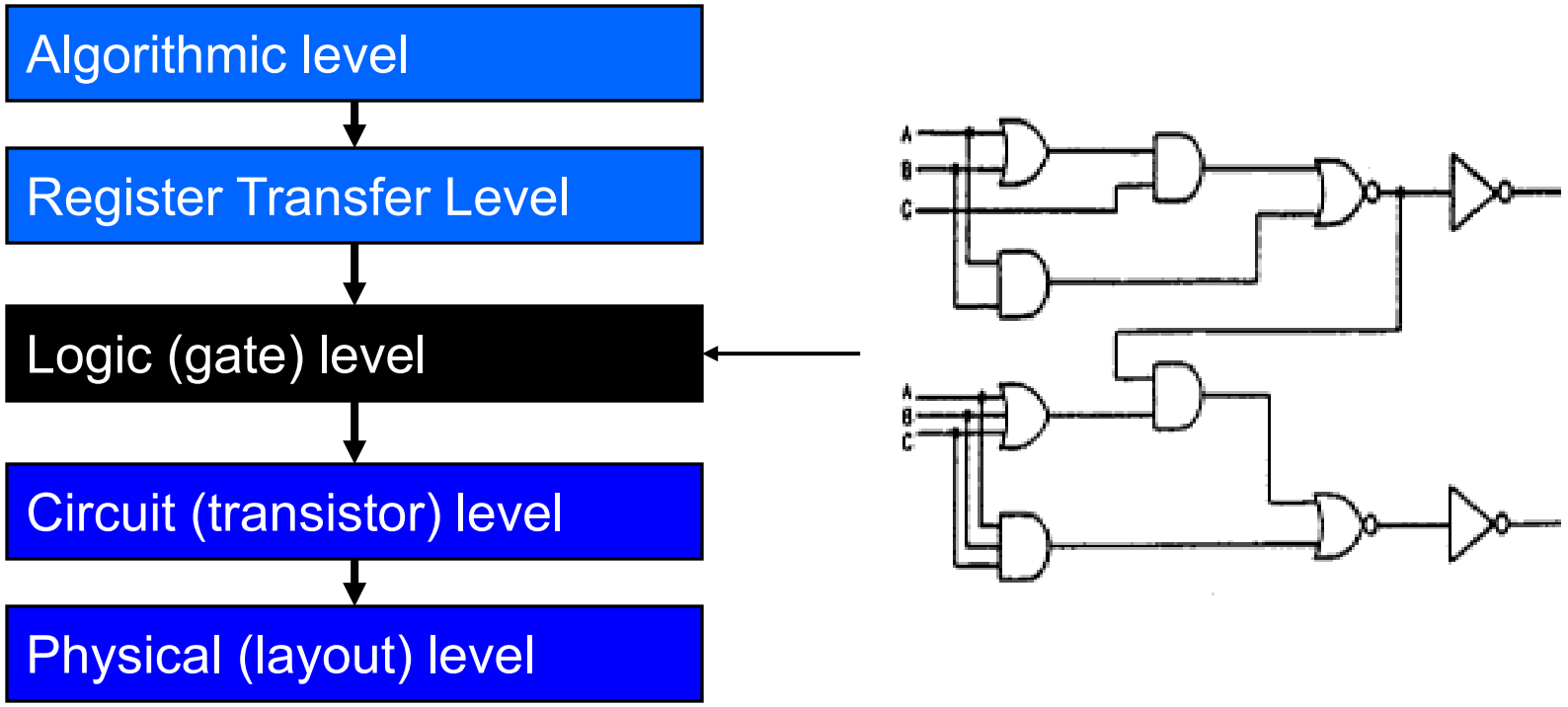
Levels of Design Description

- Algorithmic level
- Register Transfer Level
- Logic (gate) level
- Circuit (transistor) level
- Physical (layout) level



VHDL Description Level

Levels of Design Description



Logic gates also can be described by VHDL

Levels of Design Description

- Algorithmic level
- Register Transfer Level
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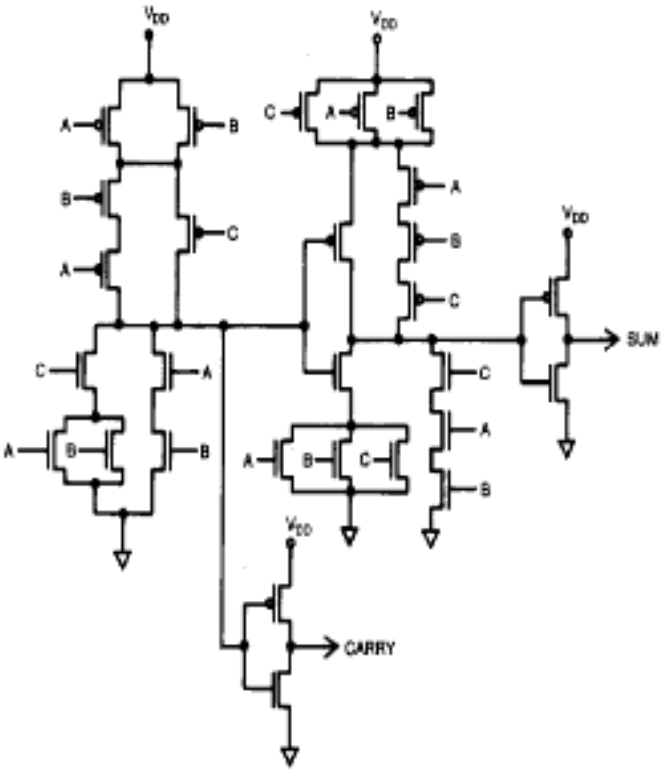
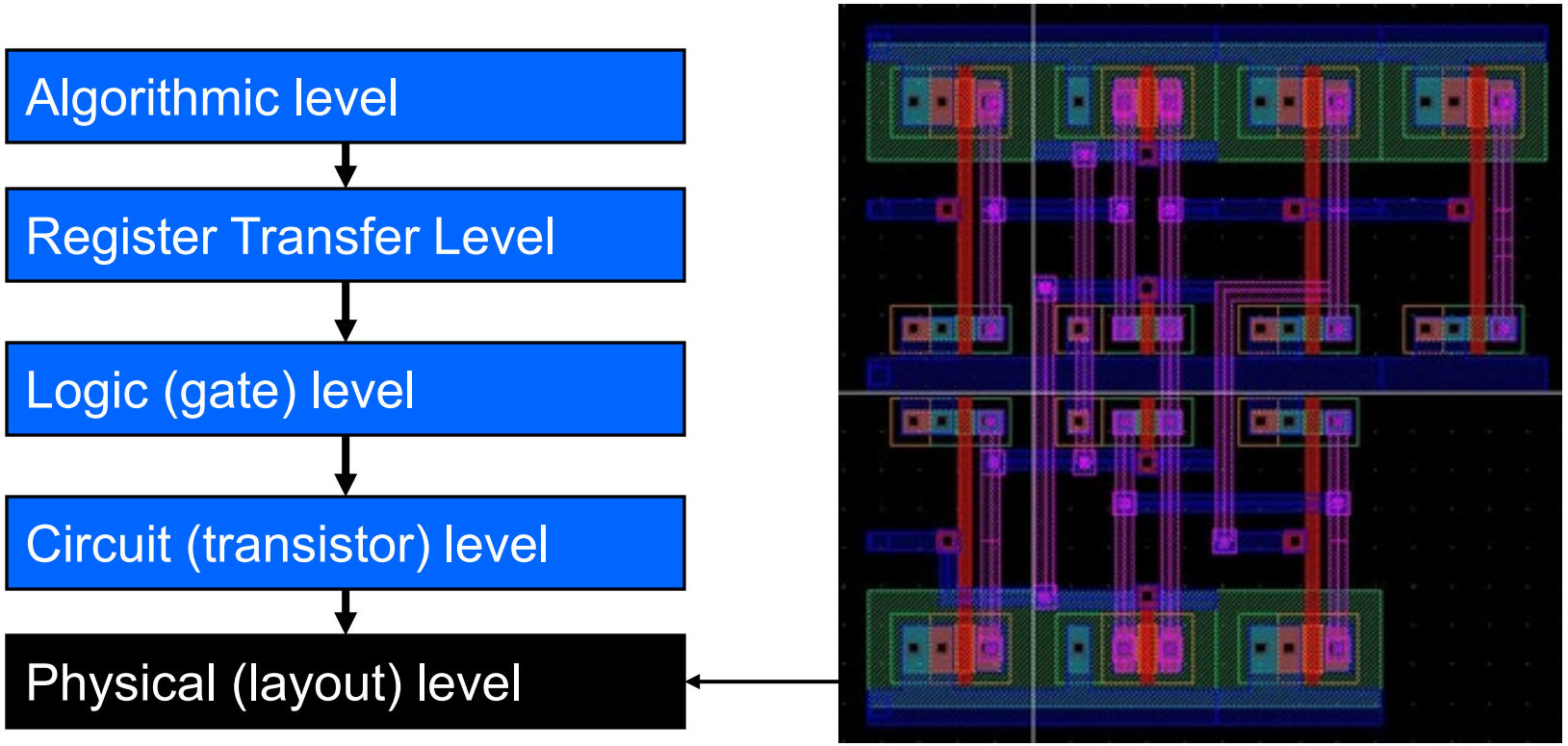
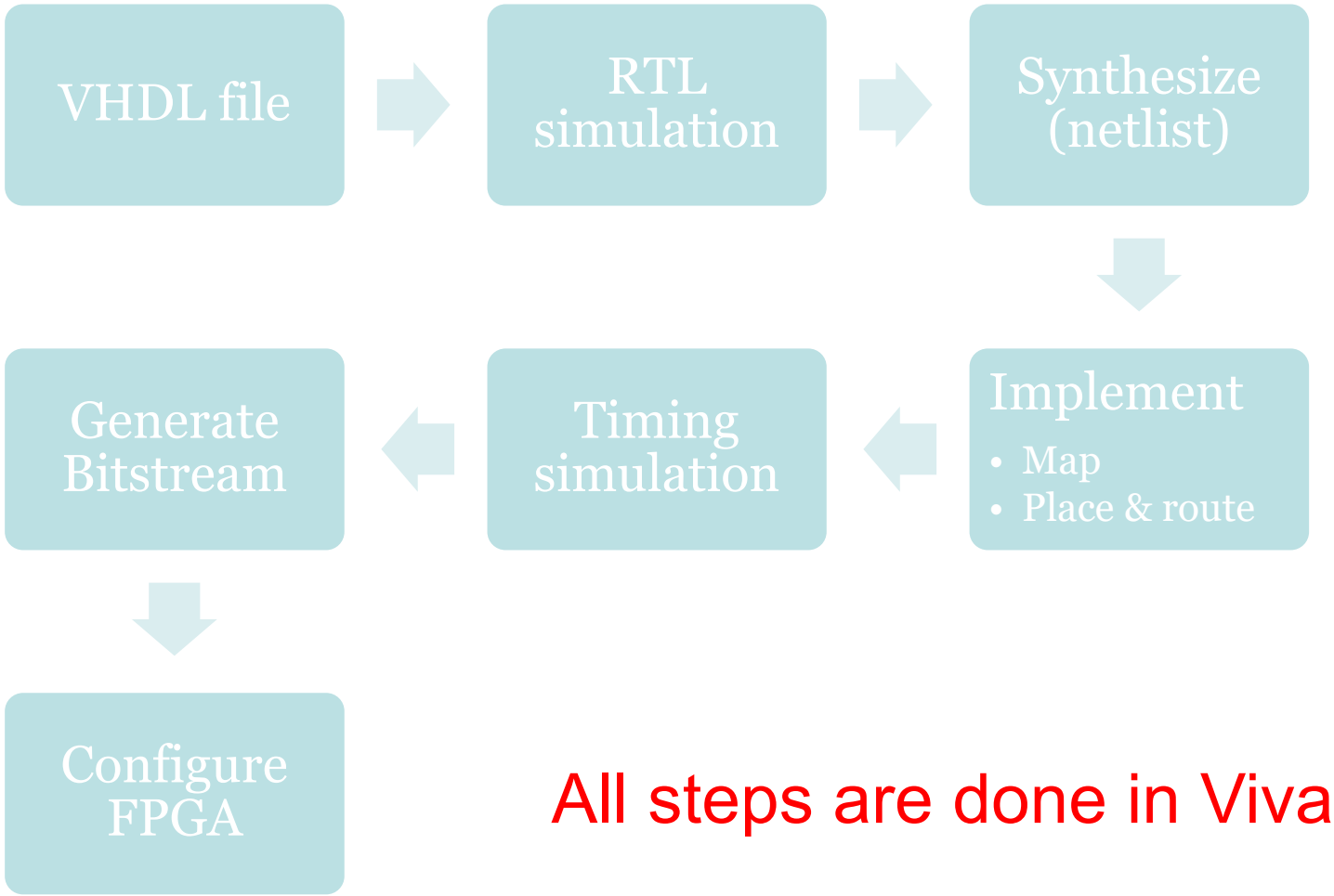
- Physical (layout) level



Levels of Design Description



FPGA Design Flow



All steps are done in Vivavdo