

| Cycle | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 |
|-------------------------|----|----|----|-----|-----|----|----|----|-----|----|----|----|-----|----|----|----|-----|----|----|-----|----|----|----|----|----|
| lw \$t2, 12(\$s0) | IF | ID | EX | MEM | WB | | | | | | | | | | | | | | | | | | | | |
| la \$t0, player_x | | IF | ID | EX | MEM | WB | | | | | | | | | | | | | | | | | | | |
| lw \$t1, 0(\$t0)* | | | IF | - | - | - | ID | EX | MEM | WB | | | | | | | | | | | | | | | |
| addi \$t1, \$t1, 16** | | | | | | | IF | - | - | - | ID | EX | MEM | WB | | | | | | | | | | | |
| blt \$t1, \$t2, loop*** | | | | | | | | | | | IF | - | - | - | ID | EX | MEM | WB | | | | | | | |
| lw \$t2, 12(\$s0)**** | | | | | | | | | | | | | | | - | - | IF | ID | EX | MEM | WB | | | | |

* lw needs to read t0 at ID stage so must wait for WB (writeback) of t0 to complete.

** addi needs to read t1 at ID stage so must wait for WB (writeback) of t1 to complete.

*** blt needs to read t1 at ID stage so must wait for WB (writeback) of t1 to complete.

**** This is the taken branch so when IF is vacated at cycle 15, it will be filled with PC + 4. At cycle 16, branch outcome will be calculated and the PC updated with branch target. Only at cycle 17 can lw be fetched.