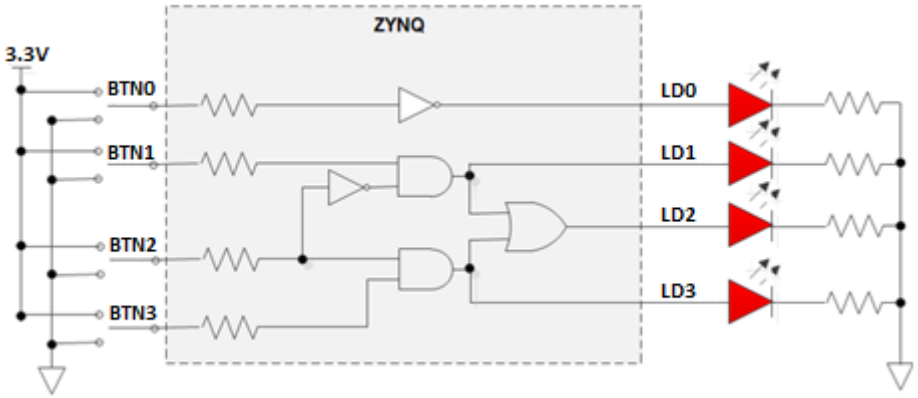
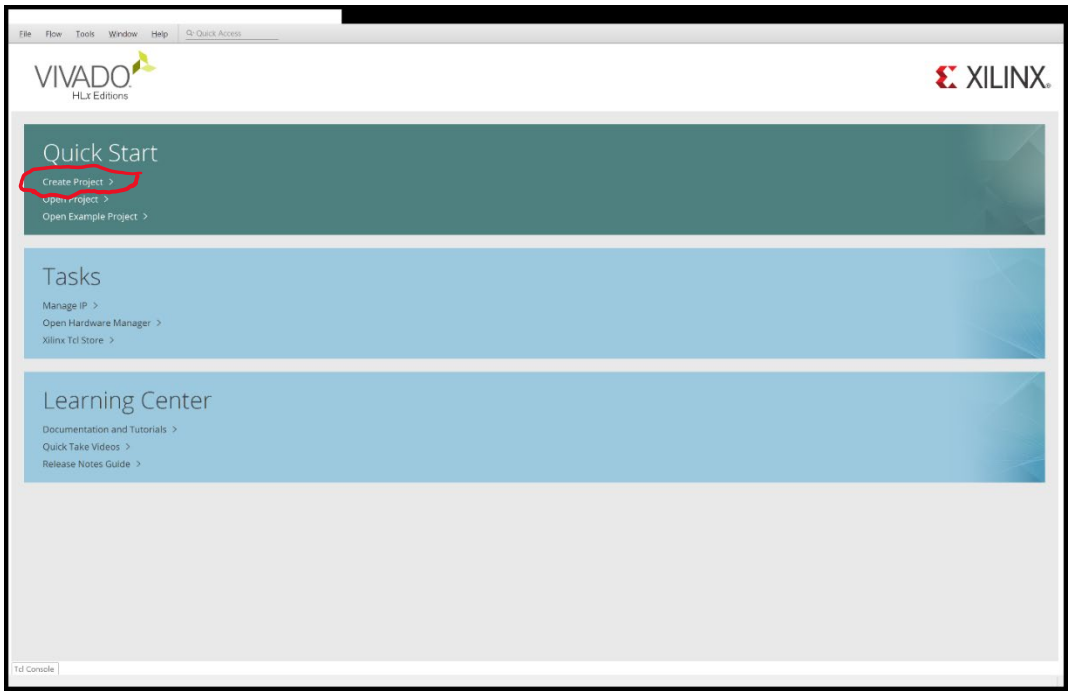
Vivado Design Flow Tutorial

This pre-lab will walk you through the design flow of Vivado, starting by creating a project from scratch, all the way to generating a bit stream and downloading into the PYNQ-Z1 board to test it. You are not required to have any VHDL experience to complete this tutorial, all the VHDL files will be provided to you. Make sure to download the all files associated with this pre-lab. We are going to simulate, synthesize, and implement the following simple logic circuit



1. Creating a new project

Open Vivado 2018.3 (not Vivado HLX 2018.3) and click on create a new project. Click Next



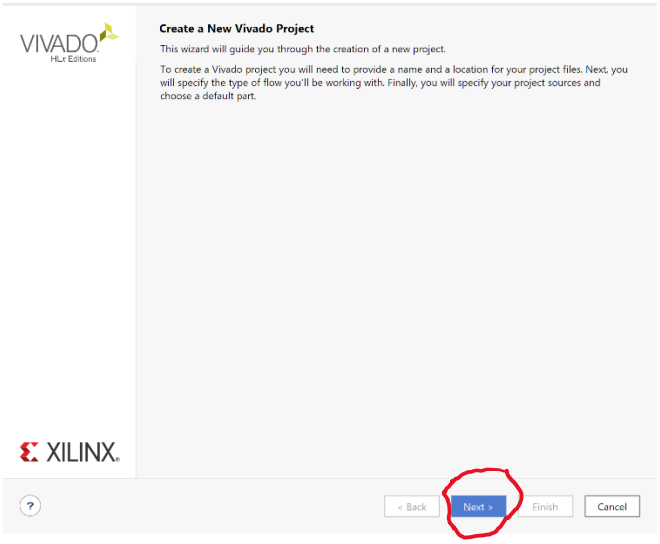


Figure 1 Create a new project

Chose a project name and make sure that the whole path doesn't have any spaces, this is very important. Click Next

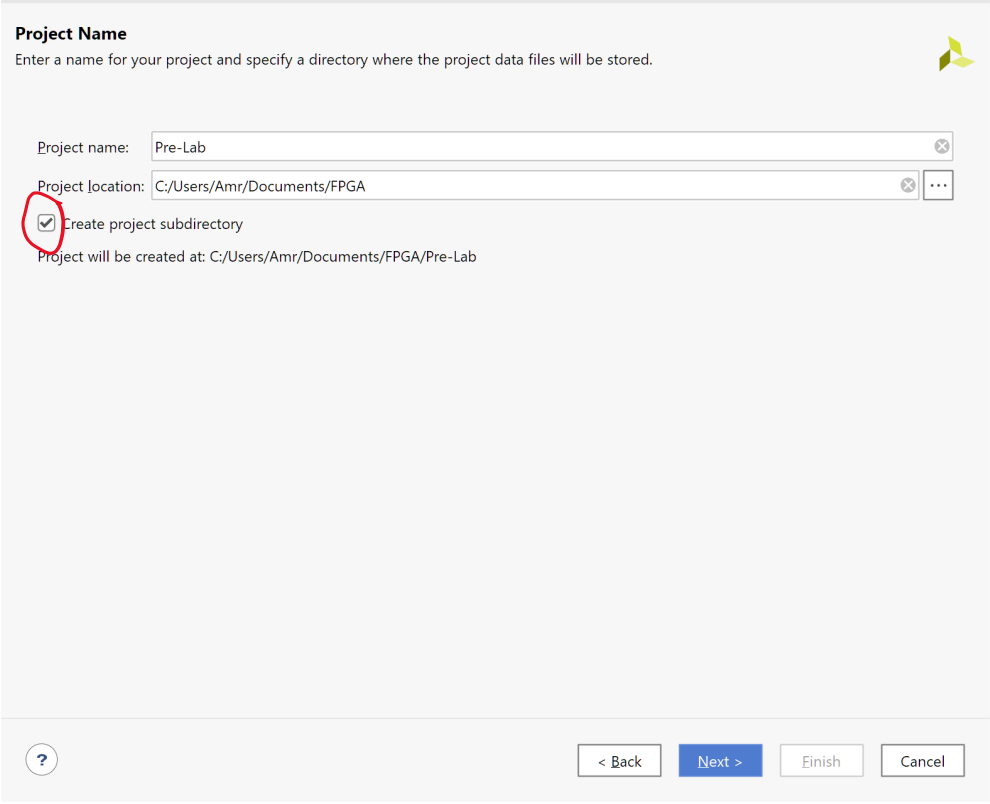


Figure 2 Project name

Choose RTL project. Click Next.

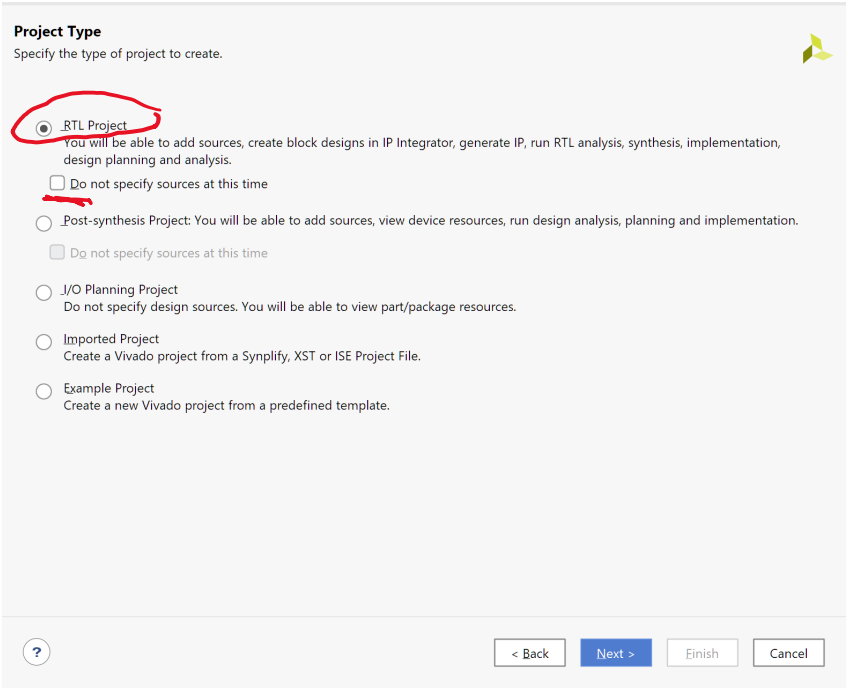


Figure 3 RTL Project

Click "Add Files" then choose "pre_lab.vhd" and "pre_lab_tb.vhd" desing files that came with this tutotial. Make sure to check the Scan and the Copy check boxes. The target language should be VHDL and simulator language should be Mixed. Click Next.

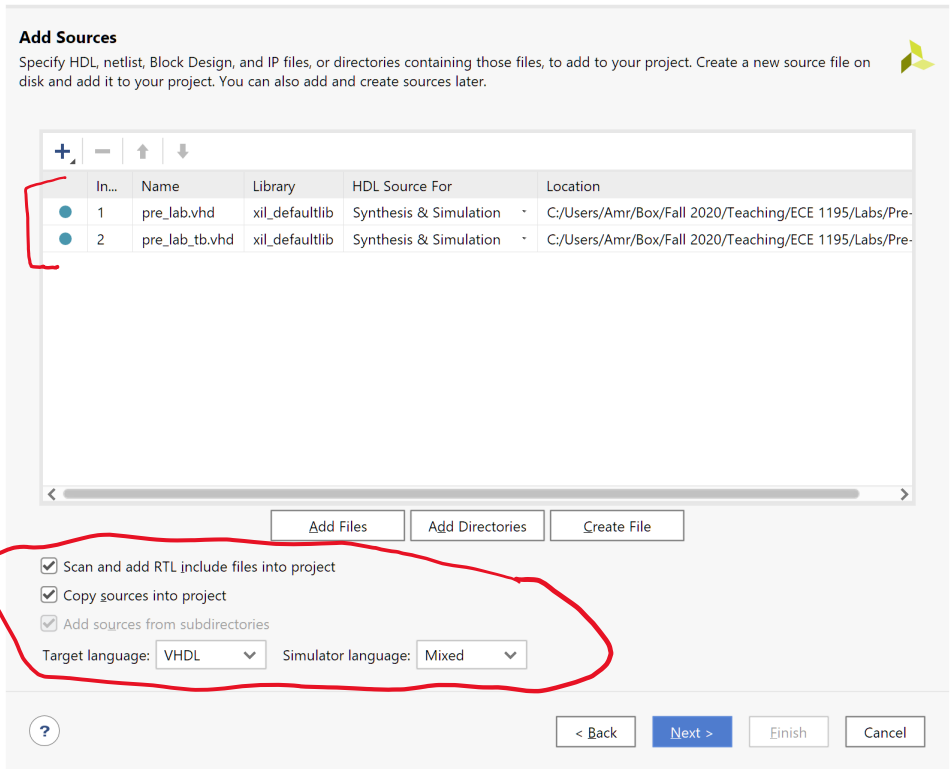


Figure 4 choose the design files

In the Add Constraints window, choose "PYNQ-Z1_C.xdc" constraints file. Make sure to check the Copy check box. Click Next.

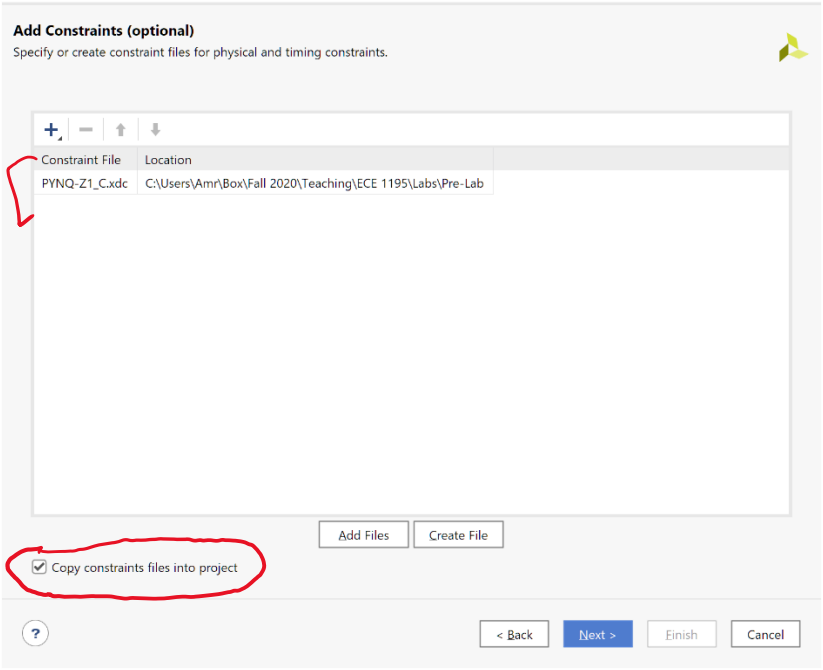


Figure 5 Design Constraint

Note:

This file can be used for your future labs, make sure to save it somewhere handy. This is the file that assigns I/O ports in your designed system to the I/O ports of the board. All the assignable I/O pins are already included and commented out. All you need to do is to uncomment the pin you want to assign and change the name in the "get_ports" function to the pin name of your design. For example, we will be using input buttons of the board and assign them to the input of our design, as can be seen in the picture below.

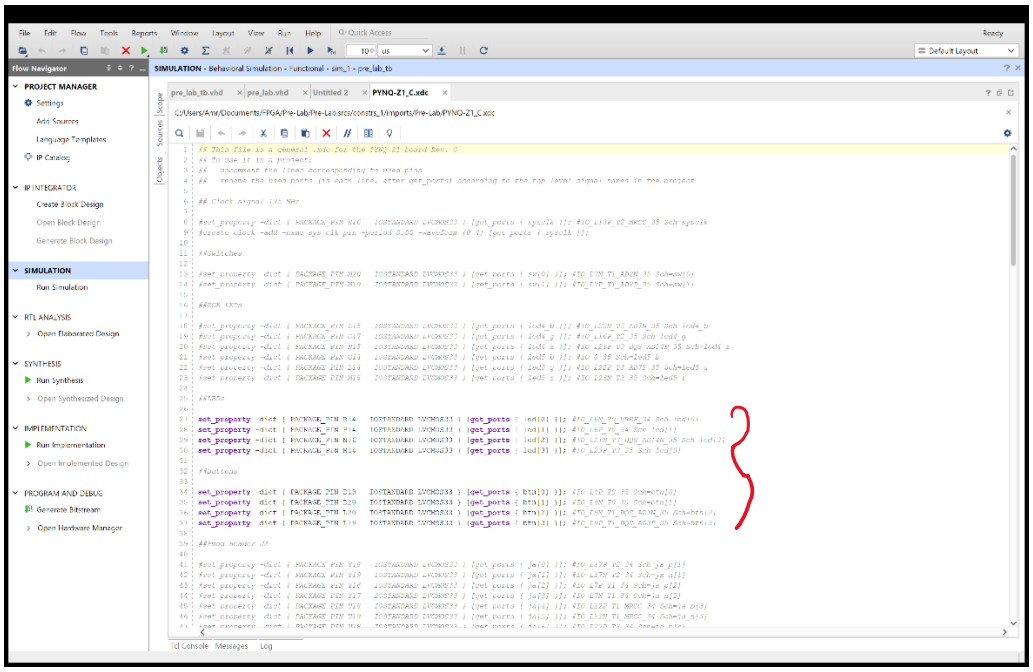
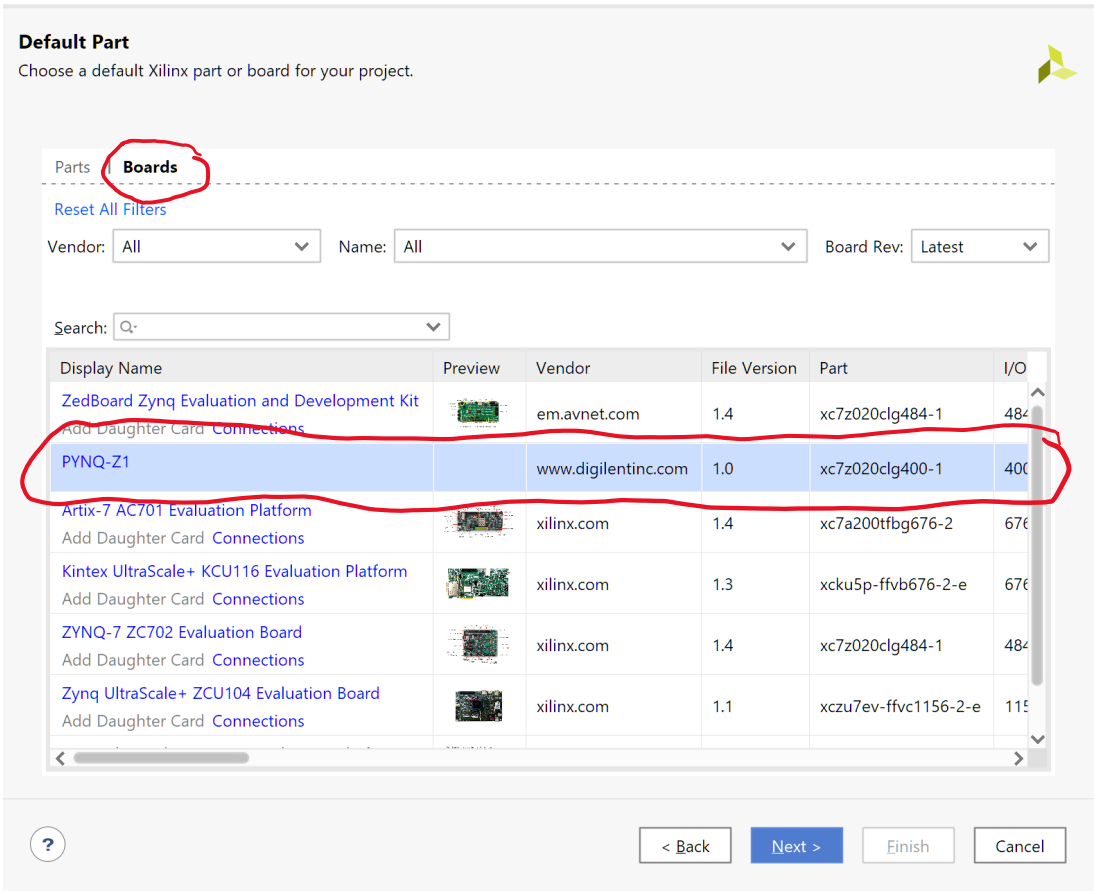


Figure 6 Constraints file

Click on boards then choose the PYNQ-Z1 Board. You would only see this option if you already have completely the Vivado installation tutorial up to the step where you add PYNQ-Z1 board files in the installation directory. Click Next. Click Finish on the final window.



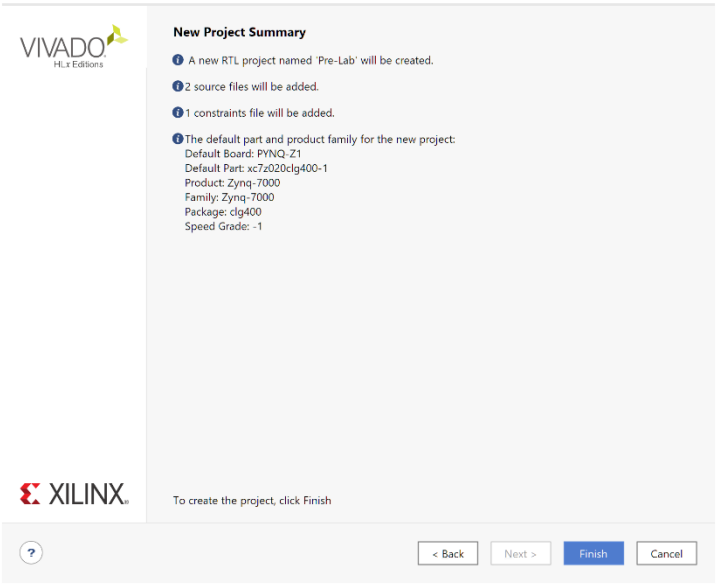


Figure 7 Choosing the board

You should be seeing the following window with the two files imported showing under design sources. Double clicking any of the two files should open them up for editing in the right window. Take sometime and explore the interface around.

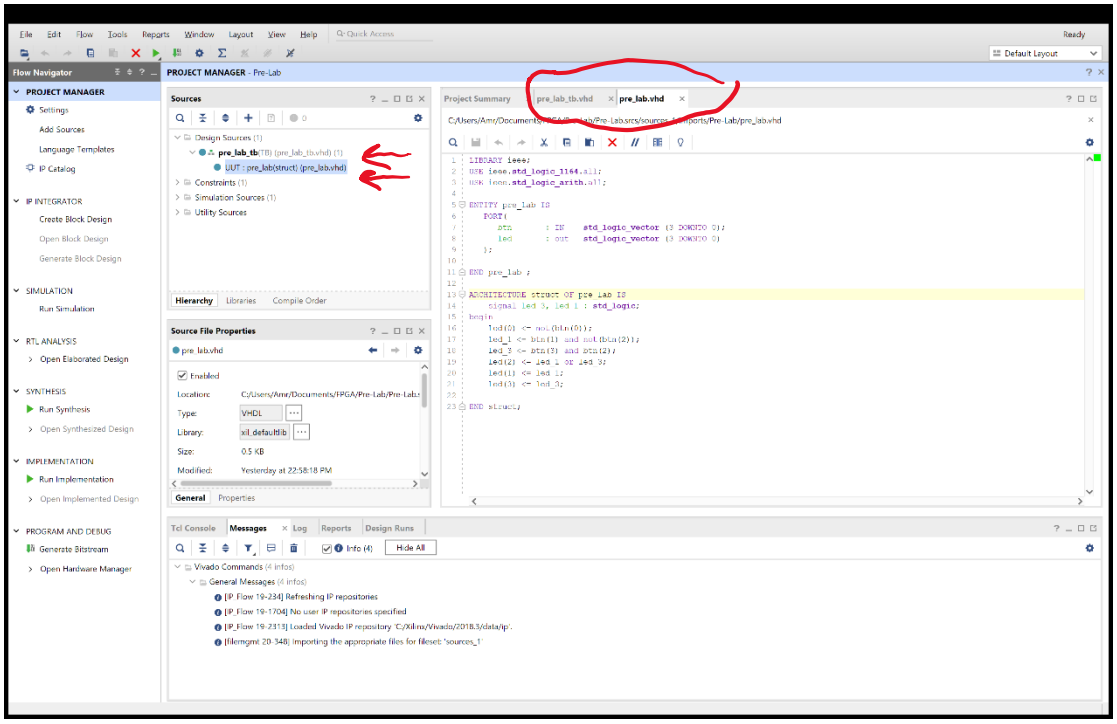


Figure 8 Vivado Interface and Editor

2. Running Simulation, Synthesize, and Generating Bit Stream

From the left menu "Flow Navigator", click on "Run Simulation" then "Run Behavioral Simulation". If any window pops up, click "yes" or "okay". You should be getting the simulation waveform on the right. Play around with it, zoom in and zoom out. Get comfortable with it and verify that the design is working correctly. You can do that by looking at pre_lab_tb.vhd file. From you previous knowledge of VHDL in ECE 0201, you should quickly figure it out. If, for any reason, you don't remember that, make sure that the values of *leds* and *exp_leds* are equal, every time the value of *btns* changes.

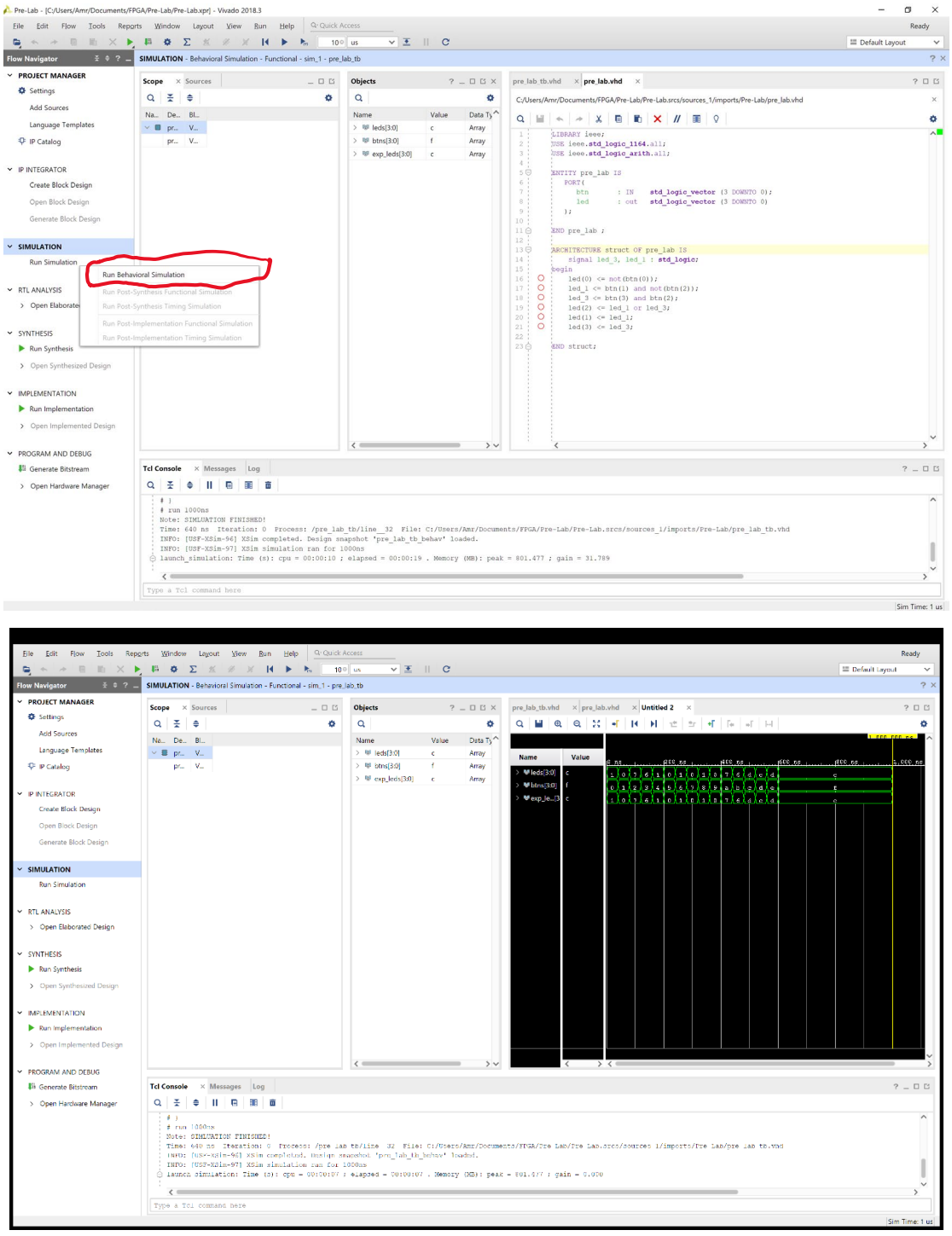


Figure 9 Simulation

Before generating the bitstream, we need to change the Top-Level design to "pre_lab.vhd". Previously, The Top-Level design was the testbench file, "pre_lab_tb.vhd". Viviado automatically detected this as the Top-Level file as it

includes an instantiation of the design component (don't worry it will explained later on). This was okay for the simulation part, as we want to simulate the testbench. But when we generate the bitstream, we need to generate it for the desing that we are going to download on the board, which is "pre_lab.vhd".
Right click on the "pre_lab.vhd" and choose "Set as Top"

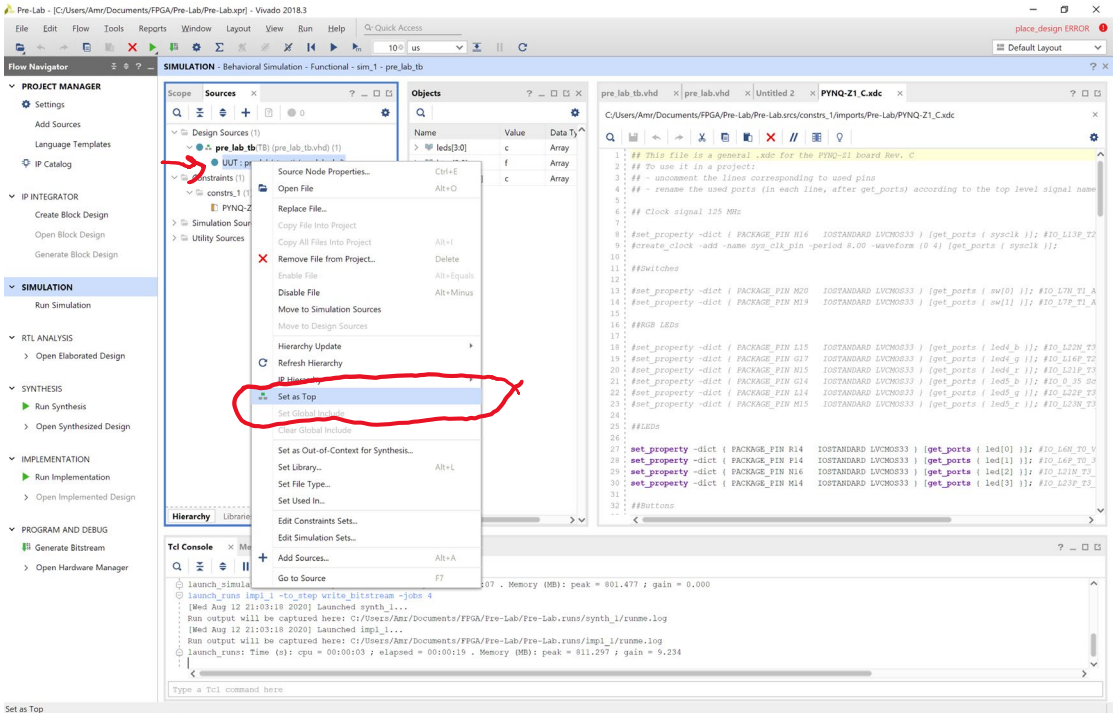


Figure 10 changing the top level

From the left menu “Flow Navigator”, click on “Generate Bitstream” then “yes” on the following window. This will automatically run synthesis and implementation before generating bitstream. If you want to run any of these steps before, just click on the corresponding link in the “Flow Navigator”.

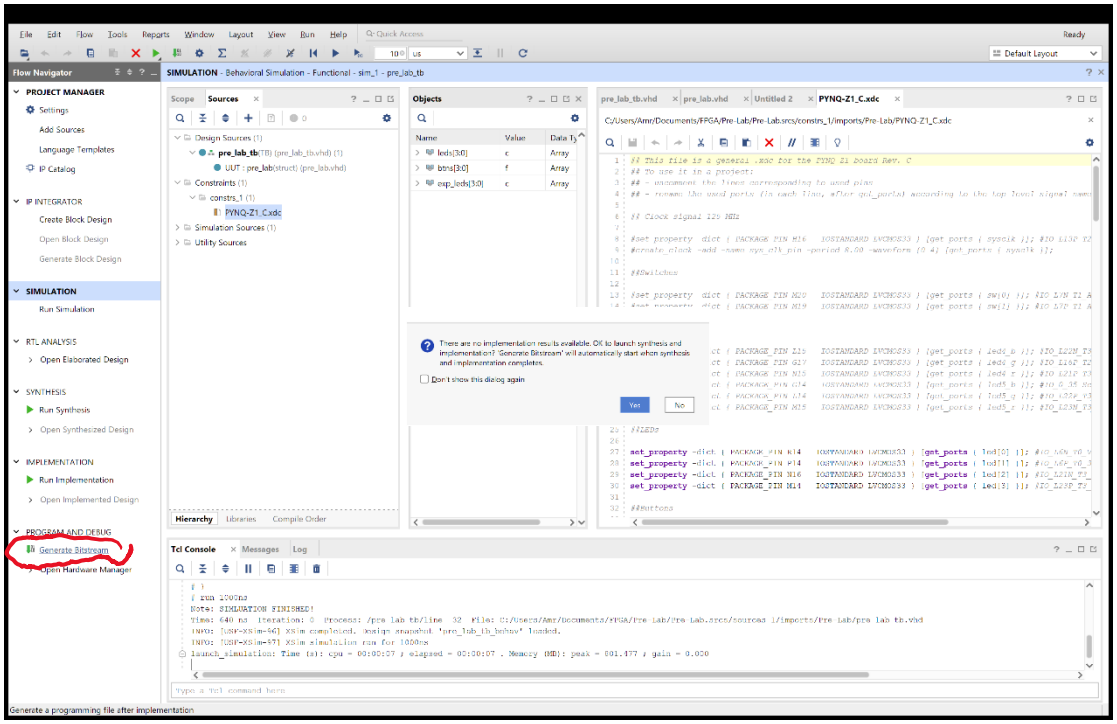


Figure 11 Generating Bitstream

Click Ok.

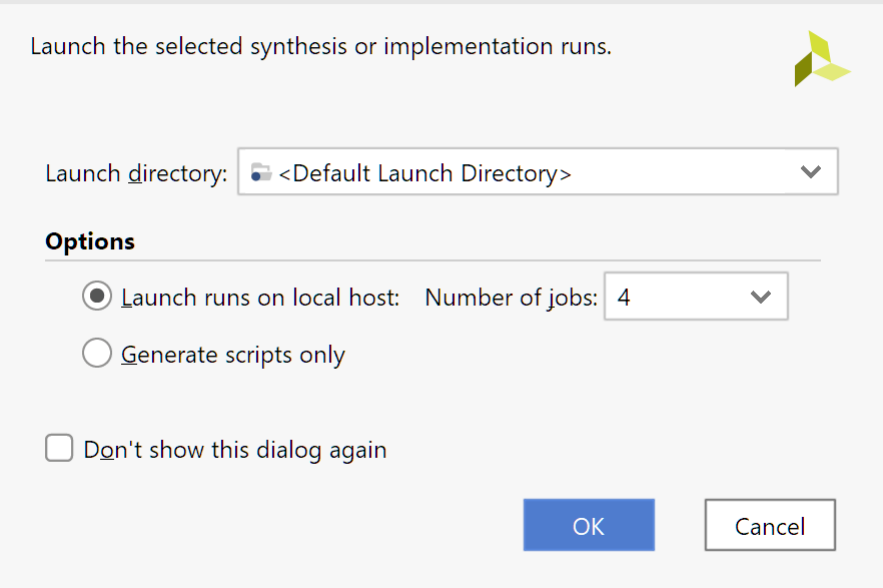


Figure 12 generating Bitstream

You should be seeing this “working sign” on the upper right corner. This is an indication that Vivado is running some background process. In this case, it’s Synthesis. This process might take some time, depending on your laptop speed.

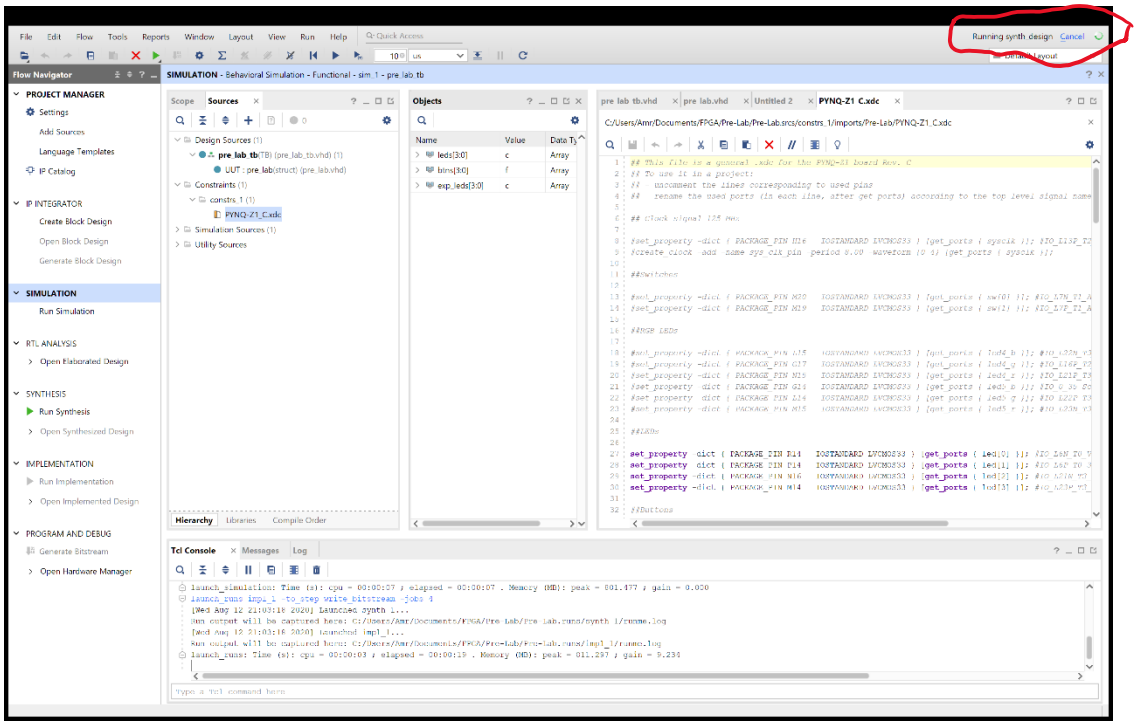


Figure 13 Background Process

When the bitstream generation is successfully generated, the following message will come up. Before clicking okay, we need to connect the PUNQ-Z1 board and get it ready. Connect the board to your computer via the USB Cable and the "**PROG UART**" USB connection on the board. Change **JP5** to "**USB**" and **JP4** to "**JTAG**". Turn the power switch on, you should see **LD13** turning red. Now click okay on the following window.

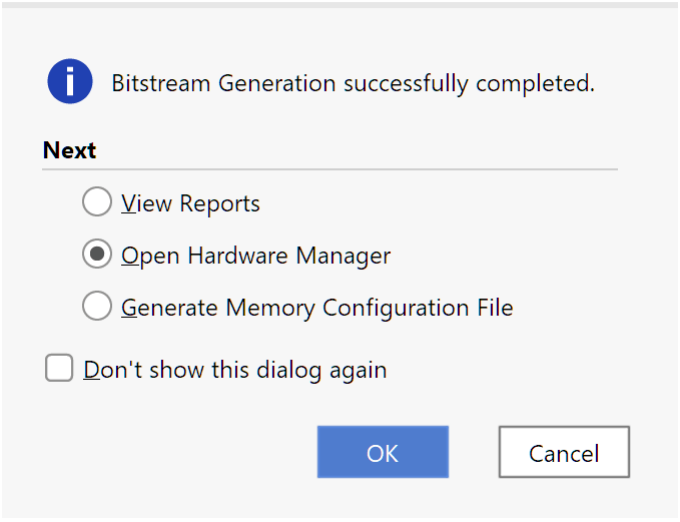


Figure 14 Hardware Manager

If for some reason the hardware was not detected, click on "Open Target" then "Auto Connect". This should successfully connect to the board. Click "Program Device" then "Program" on the following window. This should download the bitstream to the board.

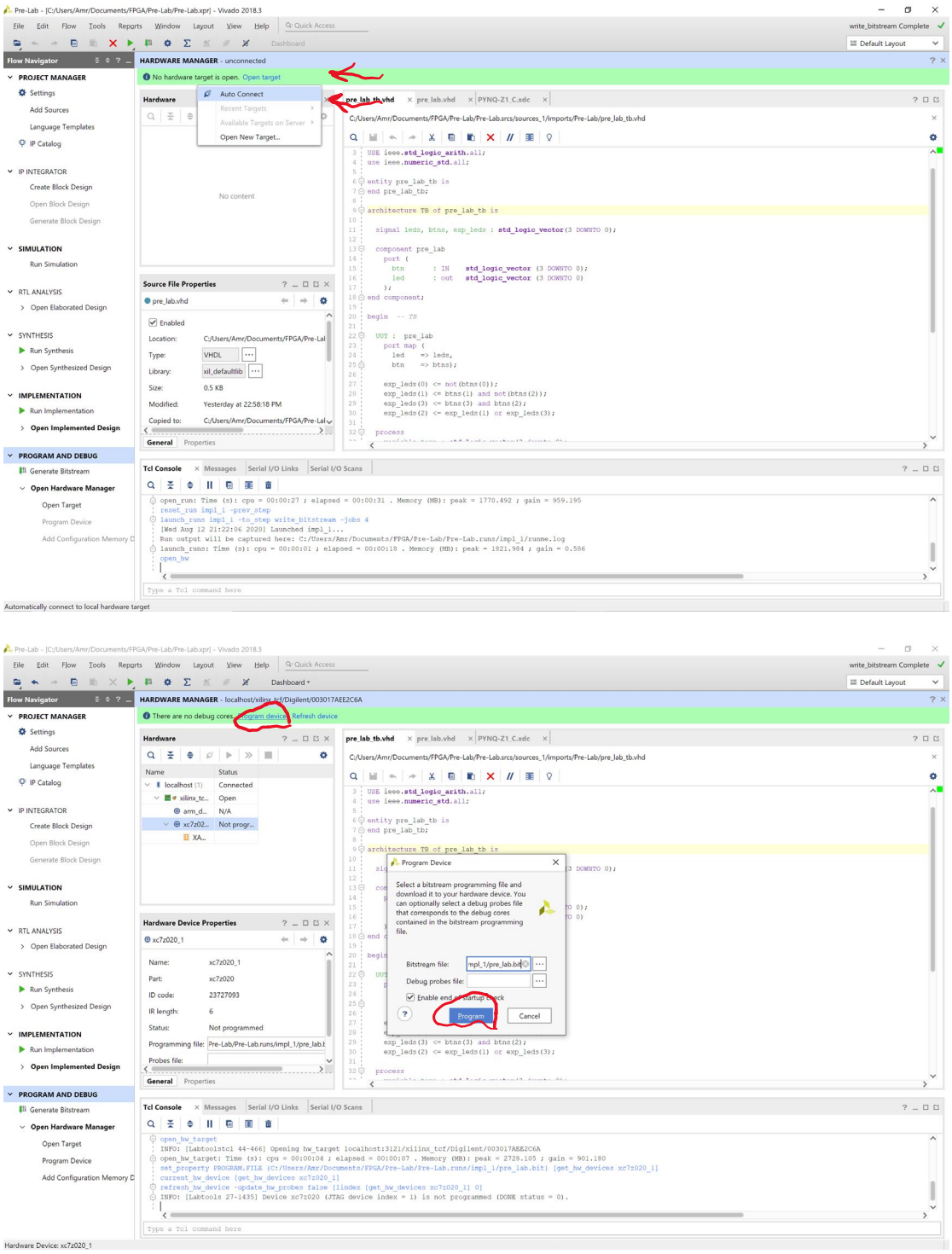


Figure 15 Auto Connect and program

Now the board is programed. **LD12** should turn green. Now play around with the 4 buttons and verify the correct functionality by watching the LEDs.