1. Fill in the state of the cache after fetching instruction for PC 100: STORE (Addr: 39168) [Data L1 Cache] [Instruction L1 Cache] D Rows D Rows Tag Tag Row 0 Row 0 Row 1 Row 1 Row 2 Row 2 Row 3 Row 3 [Unified L2 Cache] **Rows** Tag D Tag D Tag D Tag Row 0 1 1 1224 2. Fill in the state of the cache after fetching instruction for PC 104: STORE (Addr: 39424) [Data L1 Cache] [Instruction L1 Cache] Rows ٧ D D **Rows** Tag Tag Row 0 Row 0 Row 1 Row 1 Row 2 Row 2 Row 3 Row 3 [Unified L2 Cache] **Rows** D Tag D Tag ٧ D Tag ٧ D Tag Row 0 1 1 1224 1 1 2464 3. Fill in the state of the cache after storing data for PC 100: STORE (Addr: 39168) [Data L1 Cache] [Instruction L1 Cache] Rows ٧ D Rows ٧ D Tag Tag Row 0 Row 0 Row 1 Row 1 Row 2 Row 2 Row 3 Row 3 [Unified L2 Cache] **Rows** Tag D Tag D Tag Tag 1 1 1224 2464 Row 0 1 1 4. Fill in the state of the cache after storing data for PC 104: STORE (Addr: 39424) [Data L1 Cache] [Instruction L1 Cache] Rows D D V **Rows** Tag Tag Row 0 Row 0 Row 1 Row 1 Row 2 Row 2 Row 3 Row 3 [Unified L2 Cache] **Rows** D ٧ Tag D Tag D Tag ٧ Tag Row 0 1224 2464 1 1 1 1