

## Homework Assignment #8

ECE 0257 – Spring 2019

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### Collaborators

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### Book Problems

Sedra & Smith 14.2	Sedra & Smith 14.56
Sedra & Smith 14.16	Sedra & Smith 14.57
Sedra & Smith 14.24	Sedra & Smith 14.63
Sedra & Smith 14.31	Sedra & Smith 14.64
Sedra & Smith 14.49	

### Simulation Problems

Resistive Loaded NMOS Inverter (Parts 1 – 5)

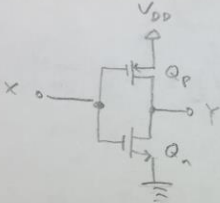
CMOS Inverter (Parts 1 – 6)

### Check-list Before Submission

- ☐ Write within boxes, no boxes are moved
- ☐ Write your full names in designated area
- ☐ Save this file as a PDF before uploading, keep the number of pages (**15**) unchanged
- ☐ Notify “TO BE CONTINUED” accordingly if you used the extra pages (page 12-15)

## Sedra & Smith 14.2

14.2



0.13  $\mu\text{m}$  process  
 $\mu_n C_{ox} = 500 \mu\text{A/V}^2$   
 $\mu_p C_{ox} = 125 \mu\text{A/V}^2$   
 $V_{tn} = -V_{tp} = 0.4 \text{ V}$   
 $V_{DD} = 1.2 \text{ V}$   
 $\left(\frac{W}{L}\right)_n = 1.5$

(a)

$$\frac{1}{k_n' \left(\frac{W}{L}\right)_n (V_{DD} - V_{tn})} = \frac{1}{k_p' \left(\frac{W}{L}\right)_p (V_{DD} - |V_{tp}|)}$$

nmos  $r_{on}$                       pmos  $r_{on}$

$$\frac{1}{(500 \frac{\mu\text{A}}{\text{V}^2})(1.5)(0.8 \text{ V})} = \frac{1}{(125 \frac{\mu\text{A}}{\text{V}^2})\left(\frac{W}{L}\right)_p(0.8 \text{ V})}$$

$$\boxed{\left(\frac{W}{L}\right)_p = 4(1.5) = 6}$$

(b)  $R_{on} = \frac{1}{(500 \frac{\mu\text{A}}{\text{V}^2})(1.5)(0.8 \text{ V})} = \boxed{1.67 \text{ k}\Omega}$

## Sedra & Smith 14.16

$$\text{NMh} = V_{oh} - V_{ih} = 1.8 \text{ V} - 1.2 \text{ V} = \mathbf{0.6 \text{ V}}$$

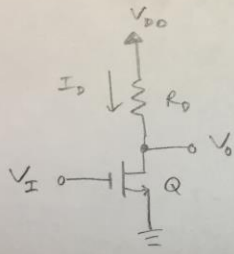
$$\text{NMI} = V_{il} - V_{ol} = 0.9 \text{ V} - 0.2 \text{ V} = \mathbf{0.7 \text{ V}}$$

## Sedra & Smith 12.24

$V_{IH} = 1.2 \text{ V}$   
 $V_{OL} = 0.2 \text{ V}$   
 $V_{OH} = 1.8 \text{ V}$

$NM_H = V_{OH} - V_{IH} = 0.6 \text{ V}$   
 $NM_L = V_{IL} - V_{OL} = 0.7 \text{ V}$

14.24



$V_{OH} = 1.2 \text{ V}$   
 $V_{OL} = 50 \text{ mV}$   
 Current drawn in low output state =  $30 \text{ }\mu\text{A}$   
 $V_t = 0.4 \text{ V}$ ,  $\mu_n C_{ox} = 500 \text{ }\mu\text{A/V}^2$ ,  $\lambda = 0$

$V_{DD}, R_D, \frac{W}{L}$

$50 \text{ mV} = 1.2 \text{ V} \left( \frac{1.67 \text{ k}\Omega}{1.67 \text{ k}\Omega + R_D} \right)$

$.0417 R_D + .06958 = 1.67 \text{ k}\Omega$   
 $R_D = 38.4 \text{ k}\Omega$

$(30 \text{ }\mu\text{A})(38.4 \text{ k}\Omega) + 50 \text{ mV} = V_{DD}$   
 $V_{DD} = 1.202 \text{ V}$

NMOS operates in linear region  
 Output =  $V_{OL} = 50 \text{ mV}$ , Input =  $V_{OH}$

$\frac{V_{OL} - 0}{30 \text{ }\mu\text{A}} = R_{DS} = \frac{50 \text{ mV}}{30 \text{ }\mu\text{A}} = 1.67 \text{ k}\Omega$

14.24 (cont.)

$30 \text{ }\mu\text{A} = \frac{1}{2} \left( 500 \frac{\mu\text{A}}{\text{V}^2} \right) \frac{W}{L} \left( 2(1.202 - 0.4) \cdot 0.05 - 0.05^2 \right)$   
 $\frac{W}{L} = 1.54$

$P_{DC}(\text{High}) = 0 \text{ W}$   
 $P_{DC}(\text{Low}) = (1.202 \text{ V})(30 \text{ }\mu\text{A}) = 3.61 \times 10^{-5} \text{ W}$

Sedra & Smith 14.31

14.31

65-nm process  
 $V_{DD} = 1 \text{ V}$   
 $V_{th} = -V_{thp} = 0.35 \text{ V}$

$\frac{W}{L} = 1.54$

$\mu_n C_{ox} = 2.5 \mu_p C_{ox} = 470 \text{ } \mu\text{A/V}^2$   
 $Q_n \approx Q_p, L = 65 \text{ nm}$   
 $\left(\frac{W}{L}\right)_n = 1.5$

$P_{DC}(\text{High}) = 0.1 \text{ W}$   
 $P_{DC}(\text{Low}) = (1.202 \text{ V})(30 \text{ mA}) = 3.61 \times 10^{-5} \text{ W}$

(a)  $V_m = 0.5 \text{ V}$   
 $\frac{W_p}{W_n} = \frac{\mu_n}{\mu_p} \quad W_p = W_n \frac{\mu_n}{\mu_p} = 97.5 \text{ nm} \left(\frac{2.5}{1}\right)$   
 $W_p = 243.75 \text{ nm}$

$A_{eq} = (65 \text{ nm})(97.5 \text{ nm}) + (65 \text{ nm})(243.75 \text{ nm})$   
 $= 22181.25 \text{ nm}^2$

(b)  $V_{OH} = V_{DD} = 1 \text{ V}$   
 $V_{OL} = 0 \text{ V}$   
 $K_R = \frac{2.5}{1} \cdot \left(\frac{1.5}{3.75}\right) \approx 1$   
 $V_{IH} = \frac{1}{8} (5 V_{DD} - 2 V_t) = \frac{1}{8} (5 - 2(0.35)) = 0.5375 \text{ V}$   
 $V_{IL} = \frac{1}{8} (3 V_{DD} + 2 V_t) = \frac{1}{8} (3 + 2(0.35)) = 0.4625 \text{ V}$   
 $NM_H = NM_L = \frac{1}{8} (3 V_{DD} + 2 V_t) = 0.4625 \text{ V}$

(c)  $R_n = \frac{1}{k'_n \left(\frac{W}{L}\right)_n (V_{DD} - V_{tn})} = \frac{1}{117.5 (1.5) (1.65)} = 872.9 \text{ } \Omega$   
 $R_p = \frac{1}{k'_p \left(\frac{W}{L}\right)_p (V_{DD} - |V_{tp}|)} = \frac{1}{470 (3.75) (1.65)} = 872.9 \text{ } \Omega$

Sedra & Smith 14.49

$\frac{k_p' (W/L)_p (V_{DD} - |V_{tp}|)}{C} = \frac{470(3.75)(.65)}{10} = \boxed{872.9 \text{ } \Omega}$

14.49

0.13  $\mu\text{m}$  technology  
 $C = 10 \text{ fF}$   
 $t_{PHL} = t_{PLH}$   
 $t_p \leq 50 \text{ ps}$   
 $T_p = \frac{t_{PHL} + t_{PLH}}{2}$   
 $t_{PHL} = t_{PLH} \leq 50 \text{ ps}$

$t_{PHL} = 0.69 R_n C$   
 $t_{PLH} = 0.69 R_p C$   
 $L_n = L_p = 0.13 \text{ } \mu\text{m}$   
 $0.69 R_n C = 0.69 R_p C$   
 $R_n = R_p$   
 $\frac{12.5}{W_n} = \frac{30}{W_p}$   
 $\frac{W_p}{W_n} = \frac{30}{12.5} = 2.4$

$R_p = \frac{30}{(W/L)_p} \text{ k}\Omega$

14.49 (cont.)

$50 \text{ ps} = 0.69 \left( \frac{12.5}{W_n} \right) (10 \text{ fF})$   
 $R = 7.25 \text{ k}\Omega$   
 $\frac{30}{(W/L)_p} = 7.25 \rightarrow \left( \frac{W}{L} \right)_p = 4.14$   
 $\frac{12.5}{(W/L)_n} = 7.25 \rightarrow \left( \frac{W}{L} \right)_n = 1.72$

Sedra & Smith 14.56

14.56

$Q_{PA} = P$   
 $Q_{PB} = 2P$   
 $Q_{PC} = 2P$   
 $Q_{PD} = 2P$

$Q_{NA} = 3n$   
 $Q_{NB} = 1.5n$   
 $Q_{NC} = 3n$   
 $Q_{ND} = 3n$

$\frac{30}{(W/L)_p} = 7.25 \rightarrow \left( \frac{W}{L} \right)_p = 4.14$

Sedra & Smith 14.57

$Q_{PA} = 1$        $Q_{NA} = 3n$   
 $Q_{PB} = 2p$        $Q_{NB} = 1.5n$   
 $Q_{PC} = 2p$        $Q_{NC} = 3n$   
 $Q_{PD} = 2p$        $Q_{ND} = 3n$

14.57  
 $(\frac{W}{L})_n = \frac{0.20 \mu m}{0.13 \mu m}$       PUN: Each pMOS =  $2p = \frac{0.80 \mu m}{0.26 \mu m}$   
 $(\frac{W}{L})_p = \frac{0.40 \mu m}{0.13 \mu m}$       PDN: Each nMOS =  $2n = \frac{0.40 \mu m}{0.26 \mu m}$

Two CMOS inverters, each with one n and one p

Total:  $13 (0.40 \times 0.13) + 4 (0.80 \times 0.26) + 2 (0.40 \times 0.13) = 1.248 \mu m^2$

Sedra & Smith 14.63

Two CMOS inverters, each with one n and one p

Total Area =  $1.248 \mu\text{m}^2$

14.63  $L = 0.18 \mu\text{m}$   
 $C_L = 10 \text{ fF}$   
 $V_{DD} = 1.8 \text{ V}$

Energy to charge/discharge load capacitance =

$$E_{DD} = C V_{DD}^2 = (10 \times 10^{-15} \text{ F})(1.8 \text{ V})^2$$

$$= 3.24 \times 10^{-14} \text{ J}$$

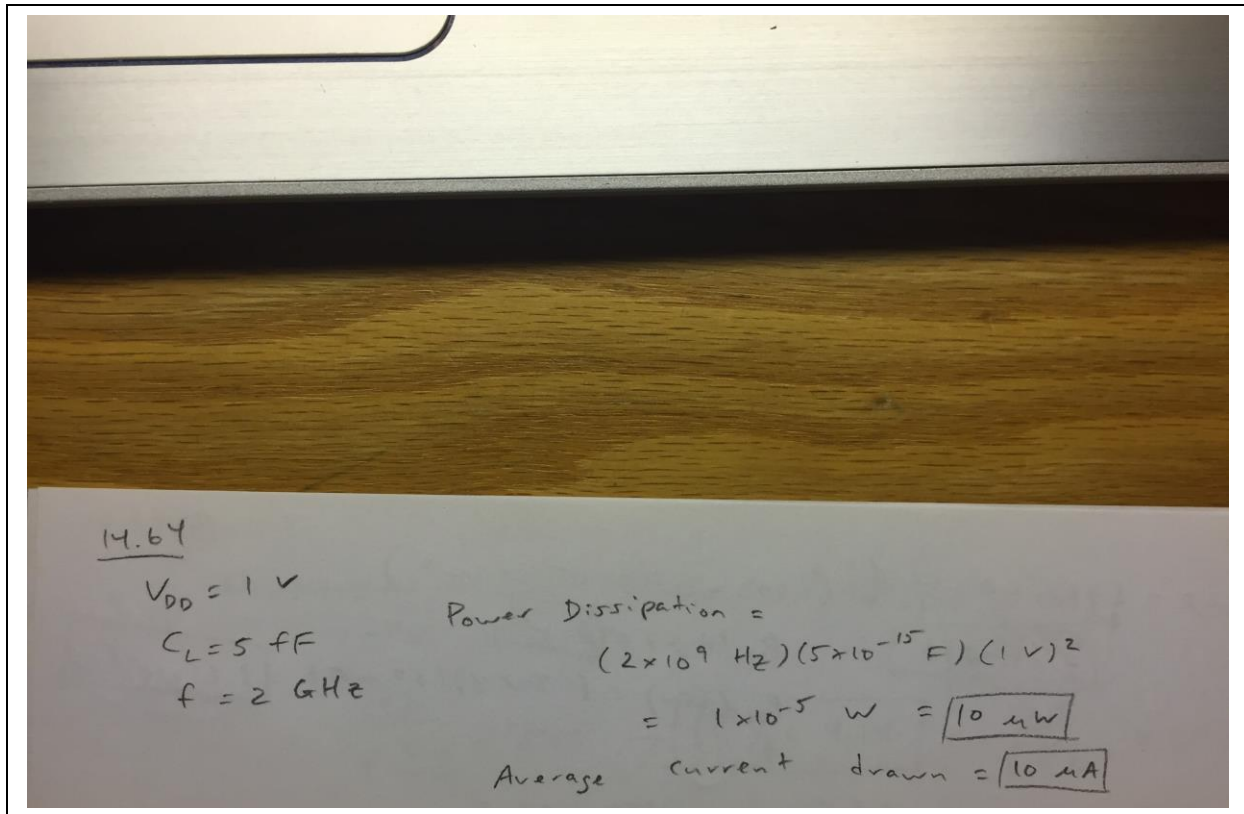
Total Power Dissipated =

$$(2,000,000) \cdot (1,000,000,000 \text{ Hz})(10 \text{ fF})(1.8 \text{ V})^2 = 64.8 \text{ W}$$

Average current drawn =  $36 \text{ A}$

Sedra & Smith 14.64





### Resistive Load NMOS Inverter (1)

$W = 1050 \text{ nm}$ 
 $L = 250 \text{ nm}$ 
 $R = 12.55 \text{ kilo-ohms}$

Part I

$$I_D = \frac{V_{DD} - V_{OL}}{R_L} = \frac{1}{2} k_n' \frac{W}{L} (2(V_{DD} - V_T) V_{OL} - V_{OL}^2)$$

Let  $P = 240 \text{ }\mu\text{W}$ ,  $V_{OL} = 90 \text{ mV}$

$$240 \times 10^{-6} \text{ W} = \frac{2.5}{2} \left( \frac{2.5 - .09}{R_L} \right) \rightarrow \boxed{R_L = 12.55 \text{ k}\Omega}$$

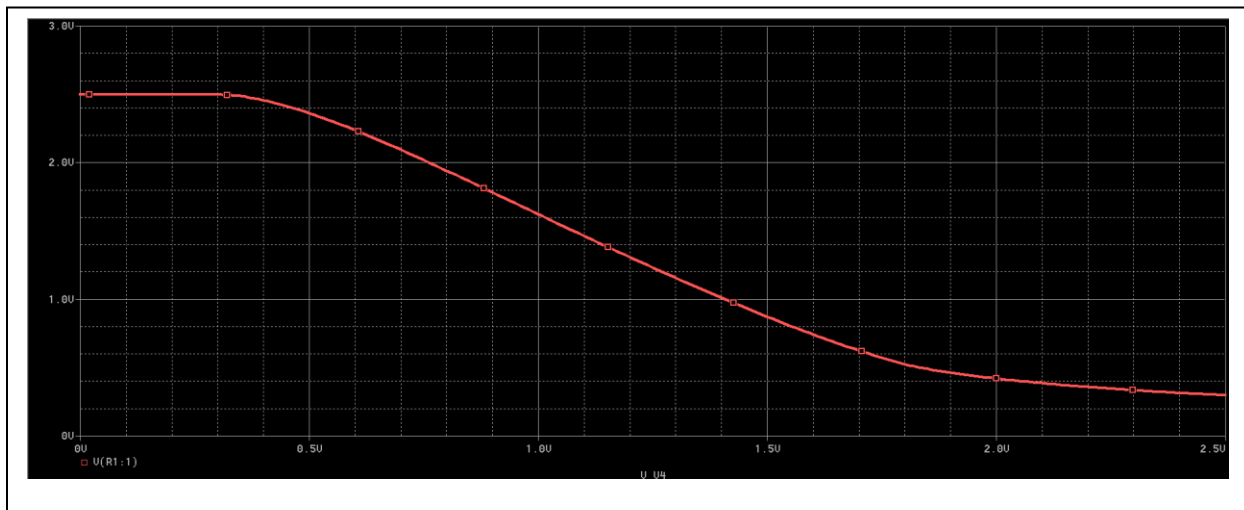
$$\frac{2.5 - .09}{12.55 \text{ k}\Omega} = \frac{1}{2} (2.5 \times 10^{-4}) \left( \frac{W}{L} \right) (2(2.5 - .4238) \cdot 09 - .09^2)$$

$$\frac{W}{L} = 4.2$$

Let  $L = 250 \text{ nm} \rightarrow W = 1050 \text{ nm}$

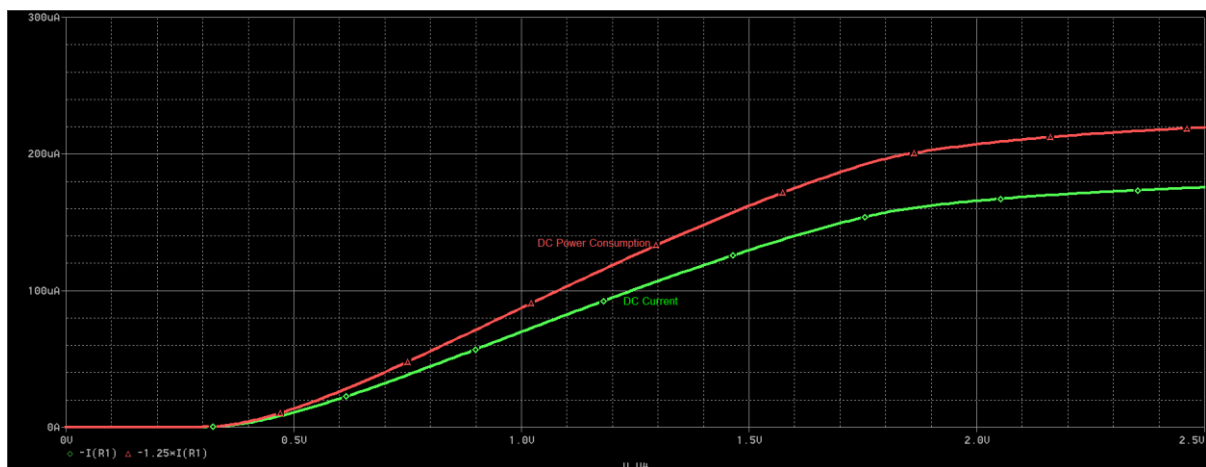


## Resistive Load NMOS Inverter (2)



## Resistive Load NMOS Inverter (3)

*DC Power Consumption = 218.75  $\mu$ W*



#### Resistive Load NMOS Inverter (4)

$$VOL = 300 \text{ mV}$$

$$VIL = 463 \text{ mV}$$

$$VTH = 1.2429 \text{ V}$$

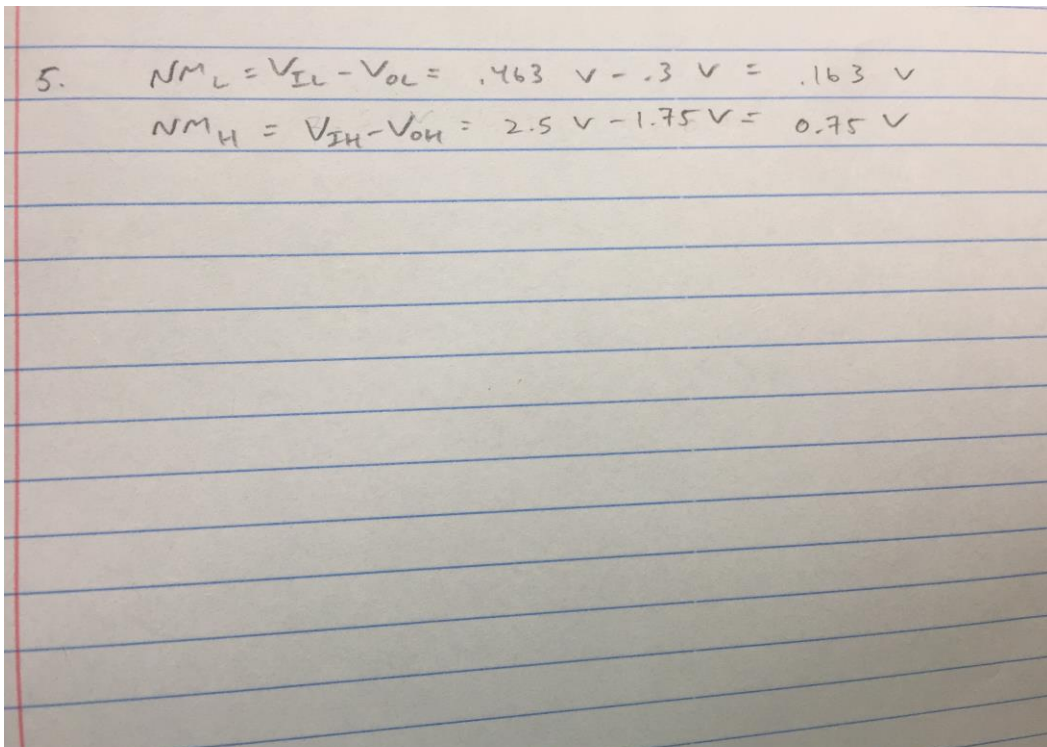
$$VOH = 2.5 \text{ V}$$

$$VIH = 1.75 \text{ V}$$

#### Resistive Load NMOS Inverter (5)

$$NML = .163 \text{ V}$$

$$NMH = .75 \text{ V}$$



5.  $NM_L = V_{IL} - V_{OL} = .463 \text{ V} - .3 \text{ V} = .163 \text{ V}$   
 $NM_H = V_{IH} - V_{OH} = 2.5 \text{ V} - 1.75 \text{ V} = 0.75 \text{ V}$

#### CMOS Inverter (1)

For the NMOS Transistor:

$$W = 360 \text{ nm}$$

$$L = 250 \text{ nm}$$

For the PMOS Transistor:

$$W = 1200 \text{ nm}$$

$$L = 250 \text{ nm}$$

## CMOS Inverter (2 and 3)

$$VOL = 0\text{ V}$$

$$VIL = 1.0579\text{ V}$$

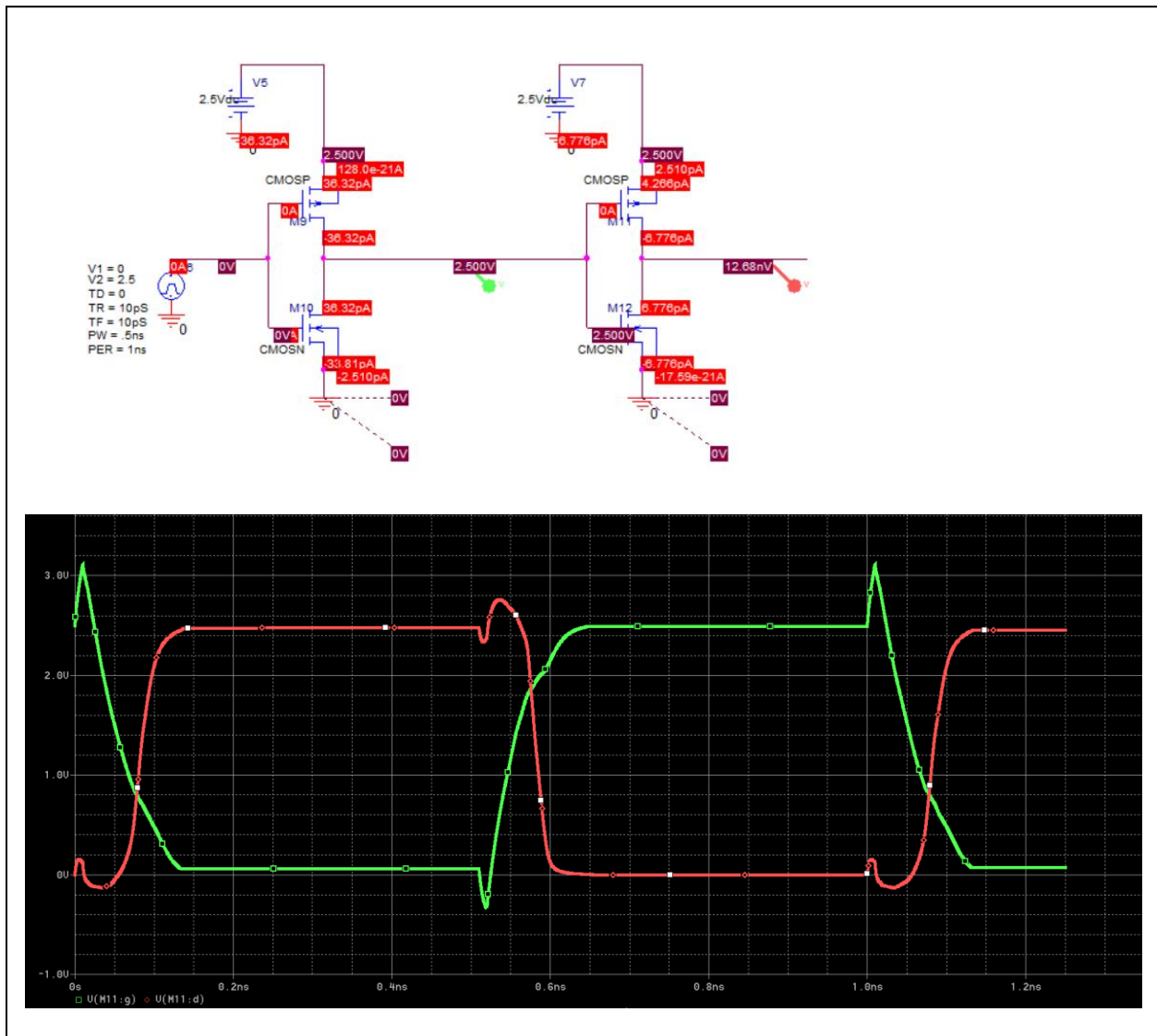
$$VTH = 1.2556\text{ V}$$

$$VOH = 2.5\text{ V}$$

$$VIH = 1.4421\text{ V}$$

$$\text{Average Power Consumption} = 0\text{ W}$$

## CMOS Inverter (4)



### CMOS Inverter (5)

Please enter your re-measured values for:

$$T_R = 126.29 \text{ pS}$$

$$T_{PLH} = 35.3 \text{ pS}$$

$$T_{Pavg} = 33.7 \text{ pS}$$

$$T_F = 153.7 \text{ pS}$$

$$T_{PHL} = 32.1 \text{ pS}$$

The second inverter increased the delay measurements because it effectively increases the capacitance. When the circuit is modeled as an RC-switching circuit, this increase to the capacitance will result in an increase to the RC time constant, meaning that there will be more of a delay for the transistor to reach a certain voltage value.

### CMOS Inverter (6)

*Dynamic Power Consumption* = 186.31  $\mu\text{W}$

I used the equations for  $T_{phl}$  and  $T_{plh}$  to solve for the load capacitance value from the perspective of each propagation delay. I then averaged the two values to get an average load capacitance of  $2.98 \times 10^{-14} \text{ F}$ . I then used this equation to solve for the average dynamic power, the equation for it being  $P = CL * (V_{dd})^2 * f$ .

## EXTRA PAGES

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