1. Fill in the state of the cache after fetching instruction for **PC 100: STORE (Addr: 39168)**

[Data L1 Cache]

Rows	V	D	Tag
Row 0			
Row 1			
Row 2			
Row 3			

[Instruction L1 Cache]

Rows	V	D	Tag
Row 0			
Row 1			
Row 2			
Row 3			

[Unified L2 Cache]

Rows	V	D	Tag	V	D	Tag	V	D	Tag	V	D	Tag
Row 0	1	1	1224									

2. Fill in the state of the cache after fetching instruction for **PC 104: STORE (Addr: 39424)**

[Data L1 Cache]

Rows	V	D	Tag
Row 0			
Row 1			
Row 2			
Row 3			

[Instruction L1 Cache]

Rows	V	D	Tag
Row 0			
Row 1			
Row 2			
Row 3			

[Unified L2 Cache]

Rows	V	D	Tag	V	D	Tag	V	D	Tag	V	D	Tag
Row 0	1	1	1224	1	1	2464						

3. Fill in the state of the cache after storing data for **PC 100: STORE (Addr: 39168)**

[Data L1 Cache]

Rows	V	D	Tag
Row 0			
Row 1			
Row 2			
Row 3			

[Instruction L1 Cache]

Rows	V	D	Tag
Row 0			
Row 1			
Row 2			
Row 3			

[Unified L2 Cache]

Rows	V	D	Tag	V	D	Tag	V	D	Tag	V	D	Tag
Row 0	1	1	1224	1	1	2464						

4. Fill in the state of the cache after storing data for **PC 104: STORE (Addr: 39424)**

[Data L1 Cache]

Rows	V	D	Tag
Row 0			
Row 1			
Row 2			
Row 3			

[Instruction L1 Cache]

Rows	V	D	Tag
Row 0			
Row 1			
Row 2			
Row 3			

[Unified L2 Cache]

Rows	V	D	Tag	V	D	Tag	V	D	Tag	V	D	Tag
Row 0	1	1	1224	1	1	2464						