**PURPOSE**

The purpose of this lab was to design and build a 4-bit ripple counter using 74LS74A flip-flops. The circuit was first created and tested using the Altera Quartus II software. A physical implementation of the circuit was then created using a protoboard and two 74LS74A D flip-flops. The Quartus design and the physical circuit were each tested to verify that the circuit counted from zero to fifteen without interruptions, after which it reset.

For each of these implementations, waveforms of each output bit were generated in conjunction with the input clock signal. As the 4-bit ripple counter is an asynchronous device, there exists a time delay between a change in the input clock signal and any corresponding change in one or more output bits. Such delays were measured and observed, first using the waveform simulator on the Quartus software and then with the oscilloscope for the physical circuit.

**PROCEDURE**

1. Using lecture notes as well as previous knowledge of digital logic, an initial design for a 4-bit counter was sketched out on paper. The design was verified by a teaching assistant.

2. A new project for the design was created in the Altera Quartus II Version 9.1 software, using the MAX+plus II framework. A new schematic file was added to the design.

3. Two 74LS74A flip-flops were added to the design using the part number ‘7474’ in MAX+plus II. Each part contained two flip-flops. The 74LS74A pin configuration is shown below in Figure 1. The logic schematic of a D flip-flop is shown in Figure 2.

4. Since the preset and clear inputs for the 74LS74A are low-true, these inputs were connected to Vcc.

5. The four flip-flops were connected such that the complemented version of the output served as the clock signal for the next flip-flop. This schematic is shown in Figure 3.

6. A file was created in the MAX+plus II Waveform Editor. Using the Node Finder option, the clock and reset inputs were added to the waveform. The four output bits Y0, Y1, Y2, and Y3 were also added to the waveform.

7. The clock input was assigned a value of ‘Clock’ and a period of 50.0 ns. The reset input was assigned a value of logic 1 for the duration of the waveform.

8. The waveform was compiled, simulated, and confirmed to be a correct representation of a 4-bit counter.

9. The time delay was measured between each rising edge of the clock waveform and the point at which all output bits reached the next state. The results were compiled into Table 1. The largest measured delay was 9.25 ns, which was relevant for constructing the physical circuit.

10. The 4-bit counter circuit was implemented on a protoboard using a 555 timer circuit for the clock input. It was necessary to choose the values of two resistors and a capacitor such that the period of the 555 timer was 1000 times greater than the largest measured delay, or 9.25 μs. The calculated resistance values were both 445 Ω, and the calculated capacitance was .01 μF.

Note: After a considerable amount of time was spent with a teaching assistant attempting to debug the 555 timer to no avail, Dr. Jones advised us to instead use the waveform generator to generate the clock signal. The waveform generator was used throughout the rest of the procedure.

11. Channel 1 of the oscilloscope was used to measure the most significant bit output (MSB). The horizontal scale knob was adjusted to show approximately one period of the MSB waveform. The vertical scale knob was used to size the waveform so that the display could accommodate three total waveforms.

12. Channel 1 was connected to Y1 with the display settings determined in Step 11. This waveform was moved to the top of the screen and then saved to the internal memory of the oscilloscope using the REF menu.

13. Y0 was connected to channel 1. The waveform was positioned to be below that of Y1. Likewise, the clock signal was connected to channel 2. This waveform was positioned to be at the bottom of the display.

14. A picture was taken of the display.

15. Y1 was repositioned to be at the bottom of the display. Steps 13 and 14 were repeated with Y2 placed in the middle of the display and Y3 placed at the top.

16. The count sequence of the 4-bit counter was determined to be correct from these two pictures.

17. The clock signal was connected to channel 1 and Y0 was connected to channel 2. Both channels were set to 2 V/div. The time/div was set to 5 μs.

18. The maximum and minimum values of the clock waveform were calculated using the cursors. The average of these two numbers was calculated.

19. The time/div was set to 20.0 ns so that the clock waveform could be seen in detail.

20. The T1 cursor was set to the time when the clock signal crossed the average calculated in Step 18.

21. The time/div was reset to 5 μs and the maximum and minimum values of the Y0 waveform were measured. The average of these two numbers was calculated.

22. The time/div was again set to 20.0 ns so that the Y0 waveform could be seen in detail.

23. The T2 cursor was set to the time when the Y0 waveform crossed the average calculated in Step 21.

24. The resulting Δt value at the bottom of the display was the delay measurement for the Y0 waveform. This value was added to Table 3.

25. Steps 17-24 were repeated with Y1,Y2, and Y3 on channel 2.

26. A picture of the scope display for the delay measurement of Y3 was taken.

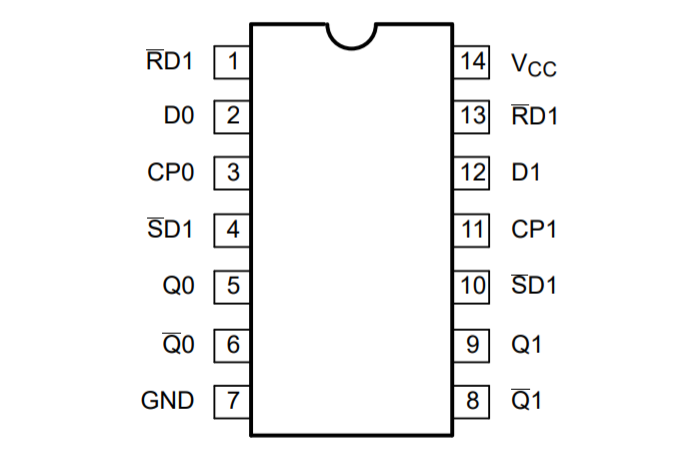
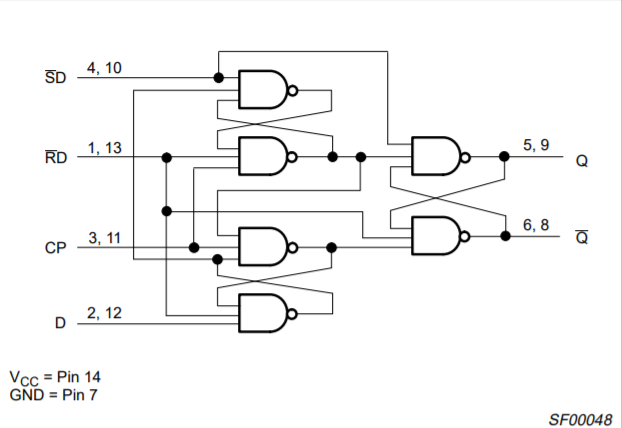
**RESULTS**

Figure 1: The pin configuration of the 74LS74A package.

Figure 2: The logic diagram for a D flip-flop with the pin assignments for the 74LS74A.

Two 74LS74A integrated circuit chips were used in the construction of the 4-bit counter circuit since each chip contains two D flip-flops. Figure 1 above shows the physical layout of the 74LS74A chip, while Figure 2 shows the logic of a D flip-flop, with the actual pin assignments for the 74LS74A labeled.

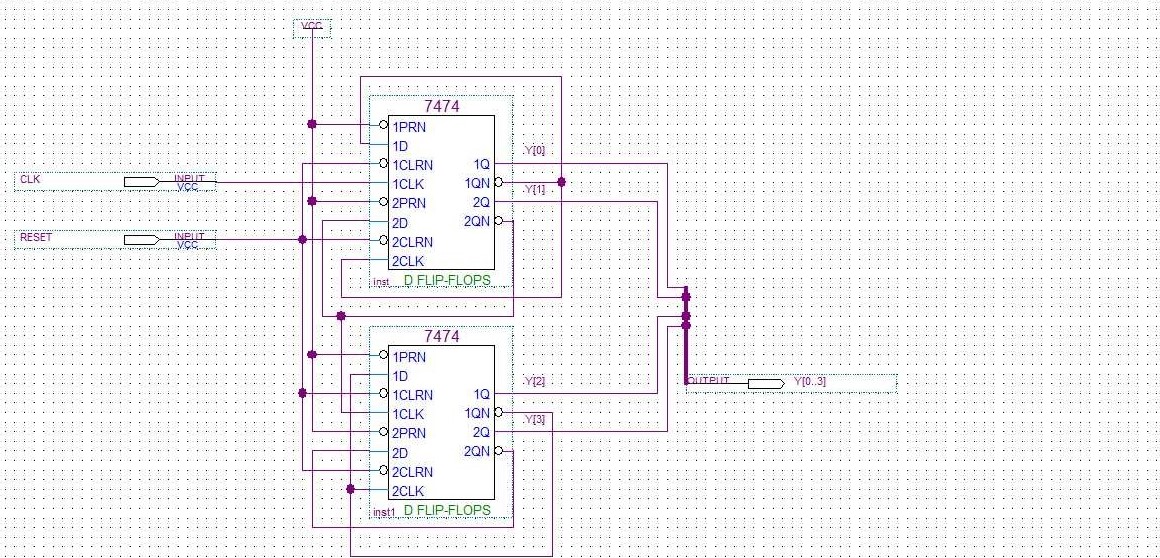
 Figure 3 below shows the schematic designed in the Altera Quartus II software. Starting at the first flip-flop on the top of the figure, the complement of the output Q is tied to the clock signal of the next flip-flop, except for the last output. The time delay for the next flip-flop to change state results in the ripple effect and classifies the counter as asynchronous. The reset (CLRN) and set (PRN) pins on both flip-flops are connected to Vcc.

Figure 3: The 4-bit ripple counter schematic designed on the Altera Quartus software. Y0, the least significant bit, is at the top of the figure.

|  |  |  |
| --- | --- | --- |
| **TRANSITION** | **# OF FLIP-FLOPS CHANGING** | **TIME DELAY (ns)** |
| 0000 → 0001 | 1 | 5.453 |
| 0001 → 0010 | 2 | 7.534 |
| 0010 → 0011 | 1 | 5.597 |
| 0011 → 0100 | 3 | 9.185 |
| 0100 → 0101 | 1 | 5.669 |
| 0101 → 0110 | 2 | 7.606 |
| 0110 → 0111 | 1 | 5.669 |
| 0111 → 1000 | 4 | 9.25 |
| 1000 → 1001 | 1 | 5.59 |
| 1001 → 1010 | 2 | 7.53 |
| 1010 → 1011 | 1 | 5.52 |
| 1011 → 1100 | 3 | 9.25 |
| 1100 → 1101 | 1 | 5.53 |
| 1101 → 1110 | 2 | 7.53 |
| 1110 → 1111 | 1 | 5.60 |
| 1111 → 0000 | 4 | 9.18 |

Table 1: The time delay between the rising edge of the clock signal and the point at which all flip-flops are at the next state.

Table 1 above shows the time delay as the counter increases in value with every clock signal and eventually resets. The average time delay for each number of flip-flops changing is shown below in Table 2. Of note, the average time delay is the same for both three and four flip-flops changing. Indeed, it was observed on the Altera Quartus Waveform Simulator that when the fourth flip-flop changed state, it often did so before the third flip-flop, Figure 4 further below shows this result visually.

|  |  |
| --- | --- |
| **# OF FLIP-FLOPS CHANGING** | **AVERAGE TIME DELAY (ns)** |
| 1 | 5.58 |
| 2 | 7.55 |
| 3 | 9.22 |
| 4 | 9.22 |

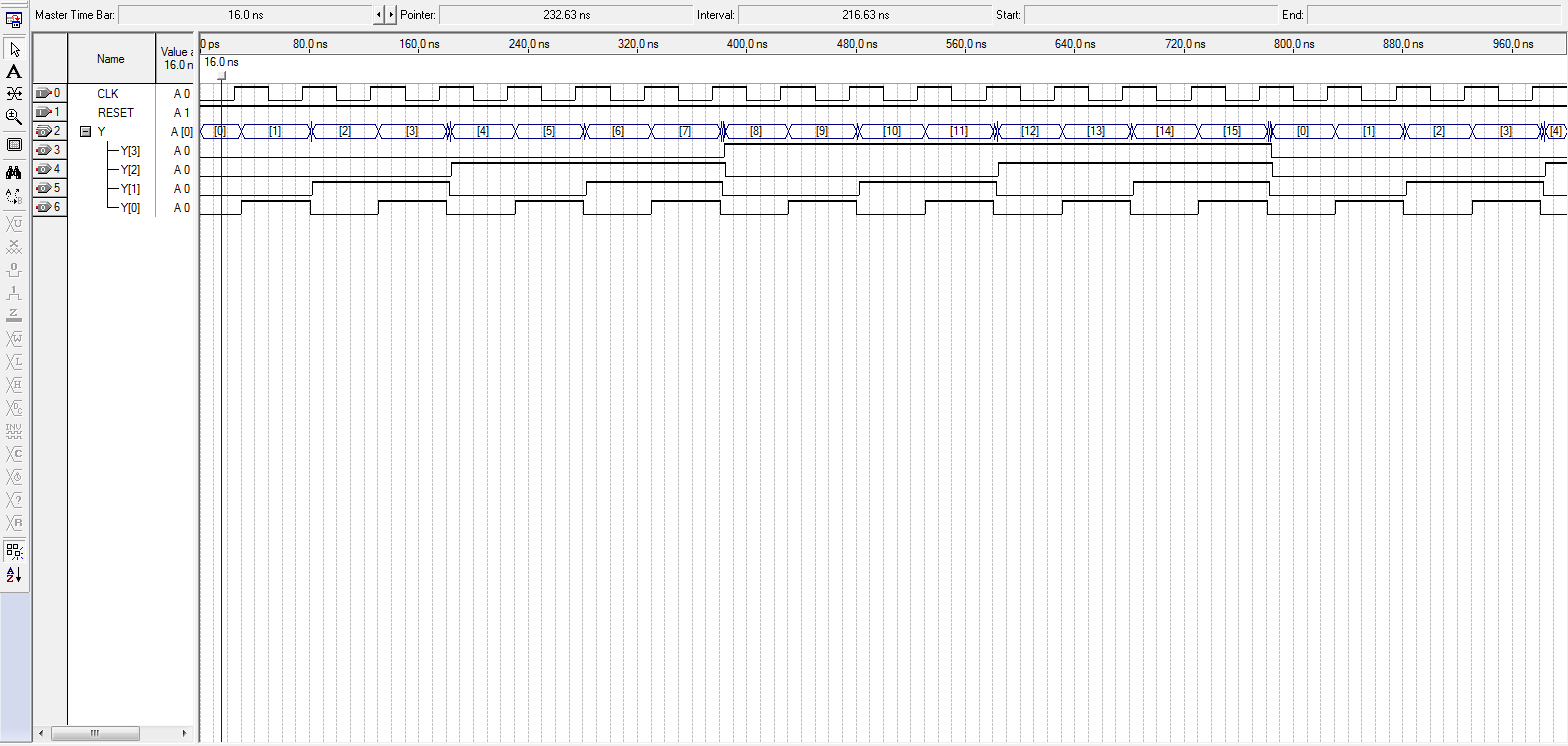
Table 2: The average time delay for each possible number of changing flip-flops.

Figure 4: The waveform representation of the 4-bit counter increasing from 0 to 11. Note that at the transition between 7 and 8, Y[3] changes state before Y[2].

Although Figure 4 is not consistent with the properties of a 4-bit ripple counter, this result can likely be attributed to an issue with the Altera Quartus simulation, as the circuit design was verified by a teaching assistant. It is also possible that either increasing or decreasing the period could eliminate this issue.

As stated above, the waveform generator was used instead of the 555 timer circuit on Dr. Jones’ advice. However, the equations to find the resistances and capacitance for the 555 timer circuit are presented below in Equations 1-3. The capacitance was set at 0.1 μF and the two resistances were to be equal. The time constant of the timer circuit was required to be 9.25 μs, or 1000 times greater than the largest measured time delay. Using this information, the resistance values were calculated to be 445 Ω.

(1)

(2)

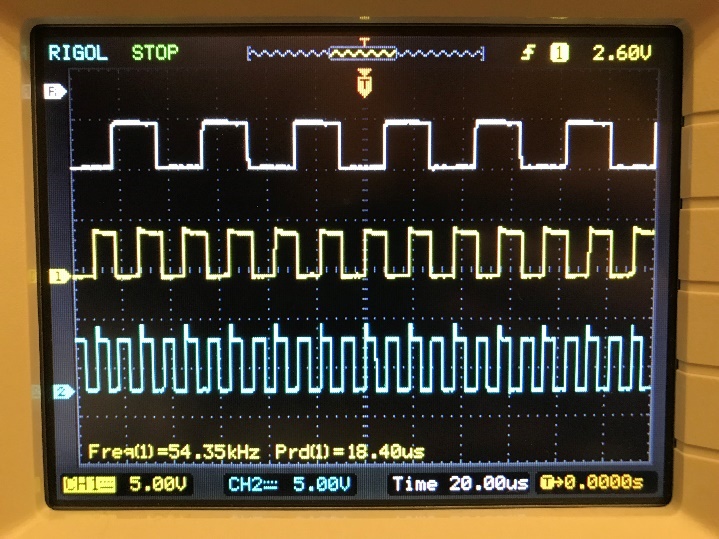
(3)

t1 = 0.693(Ra + Rb)Ct

t2 = 0.693RbCt

T = 0.693(Ra + 2Rb)Ct

Equations 1-3: Equations for calculating the capacitance and resistances of the 555 timer circuit.

 The counter was verified to be functional by creating the two oscilloscope displays shown below in Figures 5 and 6. Y1 was connected to Channel 1 and saved as a reference on the display. Figure 5 shows Y1 at the top of the oscilloscope display with Y0 in the middle and the clock signal on the bottom. The Y0 waveform triggers on the rising edge of the clock signal with a small delay. Similarly, the Y1 waveform triggers on the falling edge of the Y0 waveform. This pattern continues in Figure 6 with the waveforms for Y1, Y2, and Y3, verifying that the counter behaves as expected.

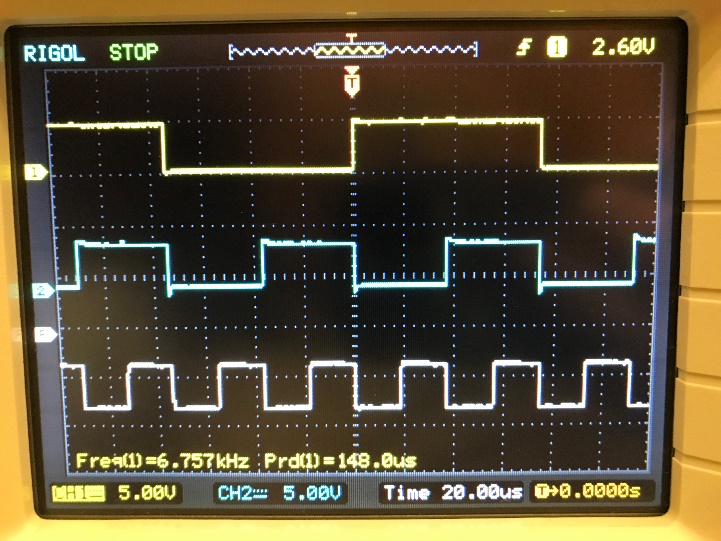


Figure 5: Waveforms from bottom to top - Clock signal, Y0, Y1.

Figure 6: Waveforms from bottom to top – Y1, Y2, Y3.



Figure 7: Oscilloscope display while measuring Y2.

Similar to the measurements recorded for the Altera Quartus simulation in Table 1, the time delays for the physical 4-bit counter circuit were then measured using the cursor tools on the oscilloscope. Figure 7 above shows a picture of the process by which these measurements were taken. Tables 3(a-d) below show the time delay measurement for each output bit.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | Vmax (V) | Vmin (V) | Vavg (V) | T (μs) |
| Clock | 4.96 | 0 | 2.48 | -.06 |
| Y0 | 4.32 | 0 | 2.12 | -.052 |
| Delay | 8 ns | | | |

Table 3a: Time delay measurement for Y0.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | Vmax (V) | Vmin (V) | Vavg (V) | T (μs) |
| Clock | 5.20 | 0 | 2.60 | -27.79 |
| Y1 | 4.24 | 0 | 2.12 | -27.75 |
| Delay | .04 μs | | | |

Table 3b: Time delay measurement for Y1.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | Vmax (V) | Vmin (V) | Vavg (V) | T (μs) |
| Clock | 5.20 | .20 | 2.70 | -24.71 |
| Y2 | 4.80 | -.40 | 2.15 | -24.65 |
| Delay | .06 μs | | | |

Table 3c: Time delay measurement for Y2.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | Vmax (V) | Vmin (V) | Vavg (V) | T (μs) |
| Clock | 5.12 | 0 | 2.52 | -18.39 |
| Y3 | 4.48 | -.08 | 2.28 | -18.34 |
| Delay | .05 μs | | | |

Table 3d: Time delay measurement for Y3.

There was again a bizarre occurrence when measuring the time delay for Y2 and Y3. The delay value for Y3 should be greater than that of Y2, but the data collected does not show this. However, this inconsistency is likely due to the difficulty of measuring values on the oscilloscope. Even when the oscilloscope is paused to result in a still waveform, the values that one measures are not exact. It is entirely possible that, had the cursor or display settings differed slightly, the values measured would agree with the expected behavior of the 4-bit counter circuit.

**CONCLUSIONS**

In this lab, asynchronous counters were examined through the design and creation of a 4-bit ripple counter. The circuit was designed both on the Altera Quartus software and on a protoboard. Waveforms of both circuits were generated and measurements were taken of the time delay between a change in the clock signal and the point at which all outputs changed to the next state. In both cases, it was observed that the waveforms of the third and fourth outputs did not exhibit behavior consistent with that expected of asynchronous counters.

It is possible that we made an error when designing our circuit on the Altera Quartus software, or that our period was not correct for observing the time delay. However, the inconsistencies observed on the oscilloscope for the physical circuit were likely due to the challenges of determining accurate measurements using the cursor tools. We can conclude that, under normal circumstances, it is likely that this delay should increase in an approximately linear fashion as the number of flip-flops changing increases. Moving forward, more attention will be paid to the oscilloscope display settings to confirm that workable data can be collected.

**REFERENCES**

* Dr. Alex Jones’ lecture notes and laboratory manual readings for Lab 9
* Chen Pan (Course Teaching Assistant)
* 74LS74A data sheet
* Daniel Stumpp (Partner)