TB for Venus RISC-V

Chinmay Purandare
Lorenzo Parata
Chongnan Wang
Xiaotian Jiang
Xinxin Qin
Department of Electronics
KTH Royal Institute of Technology
Stockholm, Sweden
Emails: chinmayp@kth.se, parata@ug.kth.se, chongnan@kth.se, xjia@kth.se, xinxinq@kth.se

Abstract

<Contains short summary of the paper>
Main body – Double column format
Text – Font – Times New Rom, 10 pts
Section Headers – Bold Font – Times New Roman, 12 pts
Subsection Headers – Bold font – Times new Roman, 11 pts
Paper length target 4-6 pages.

Keywords

<optional section to help search engines to find the paper>

1. Introduction

<Answers the question: Why do I do this research? The section may also contain which methodology have been used? Any research ethics? Sustainability issues?>

2. Related Work

This section reviews research relevant to developing a testbench for bit-serial RISC-V processors targeting Venus surface applications. We examine RISC-V architectures, high-temperature electronics, FPGA implementation methods, and verification frameworks. These foundations inform the design of a testbench capable of validating processor functionality under extreme environmental constraints.

2.1. RISC-V

Researchers from TU graz developed FazyRV [1], a minimal-area open-source RV32I RISC-V core targeting IoT and low-workload applications, addressing the problem that 32-bit RISC-V processor cores reach a boundary on their minimal size. Their goal was to minimize area demand while fulfilling performance requirements and close the gap between prevalent 32-bit and 1-bit-serial RISC-V cores.

Qian Wei and his colleagues created a comprehensive survey of RISC-V instruction set architecture extensions because while RISC-V is popular for embedded processors [2], there is still a gap between RISC-V's capabilities and the requirements of various emerging computing scenarios like artificial intelligence and cloud computing.
Gautschi et al. conducted a comprehensive comparison of ultra-low-power RISC-V cores for Internet-of-Things applications [3], analyzing the trade-offs between performance and energy efficiency in resource-constrained environments. Their work provides valuable insights into processor design considerations for applications with tight area and power constraints, which directly supports the rationale for bit-serial processor implementations in challenging deployment scenarios such as the 12-pad limitation required for Venus surface operations.

2.2. Processors for Venus

Current research on high-temperature electronics for Venus has shown that SiC ICs can sustain operation for over a year at 500 °C and for months in simulated Venus conditions, supporting sensors and simple microprocessors. This demonstrates the feasibility of long-duration surface missions and motivates concepts like LLISSE targeting low-power seismic monitoring [4].
At the processor level, studies of SiC-based computing infrastructures reveal that current prototypes achieve significantly lower throughput than space-proven silicon systems, yet provide guidelines at the microarchitecture and ISA levels for developing processors able to operate under Venus's extreme environment [5].
Pradhan and colleagues provided a comprehensive review of materials for high-temperature digital electronics [6], highlighting the challenges and solutions for electronic systems operating at temperatures as high as 500°C and beyond. Their work emphasizes the critical importance of developing new material solutions beyond conventional silicon-based devices for applications including space exploration, with specific attention to the extreme conditions encountered in Venus surface missions.

2.3. FPGA

One verification strategy is co-emulation, where the RTL design on the FPGA is run in parallel with a trusted software model, such as the Spike simulator [7], on a host PC. This allows for high-speed verification by comparing the core's architectural state against the simulator in real-time. Furthermore, using FPGAs with RISC-V is advantageous as it allows for optimized hardware, where the FPGA is configured with only the peripherals required for a specific application [8].

2.4. FPGA-Based Verification Frameworks

Kim [9] demonstrated the importance of FPGA-based acceleration for RTL evaluation by introducing automated flows that generate cycle-accurate simulators directly from RTL. This approach reduces the engineering effort compared to earlier manual FPGA frameworks and enables both faster and more reliable pre-silicon verification.

Building on this direction, Qin *et al.* [10] proposed FERIVer, an FPGA-assisted framework for verifying RISC-V processors. Their method exploits the heterogeneous architecture of SoC FPGAs, running an instruction set simulator on the processing system in parallel with the RTL core on the programmable logic. By cross-checking execution states, FERIVer achieves significant speedups over traditional software simulators while maintaining accuracy.

Together, these works highlight how FPGA-based infrastructures provide an effective foundation for validating processor designs before costly SoC fabrication, a goal directly aligned with the testbench methodology developed in this project.

3. Specification

<Outlines the constraints this work has, if any>

4. Architecture

<How do I/we plan to build this gadget given the constraints I have?. This section is sometimes split into subsections like Hardware and Software>

5. Experiments

<What experiments have I done? This is more or less a specification of the experiments.>

6. Results

<What results did I get from the experiments. This section is sometimes merged with the experiments section>

7. Conclusion

<This is a retrospective look at the introduction, and should present answers to the questions asked there and throughout the paper.>

7.1. Future Work

<Optional section that describe possible future work>

References

[1] M. Kissich and M. C. Baunach, "Fazyrv: Closing the gap between 32-bit and bit-serial risc-v cores with a scalable implementation," in *Proc. 21st ACM Int. Conf. on Computing Frontiers (CF '24)*, (Ischia, Italy), pp. 240–248, May 2024.

[2] E. Cui, T. Li, and Q. Wei, "Risc-v instruction set architecture extensions: A survey," *IEEE Access*, vol. 11, pp. 24696–24711, 2023.

[3] M. Gautschi, P. D. Schiavone, A. Traber, F. Zaruba, F. Schuiki, A. Pullini, D. Rossi, E. Flamand, F. K. Gürkaynak, and L. Benini, "Slow and steady wins the race? a comparison of ultra-low-power risc-v cores for internet-of-things applications," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 9, pp. 2387–2397, 2017.

[4] H. Kim, J. Bagherzadeh, and R. G. Dreslinski, "Sic processors for extreme high-temperature venus surface exploration," in *Proc. Design, Automation & Test in Europe Conf. & Exhibition (DATE)*, (Antwerp, Belgium), pp. 406–411, 2022.

[5] T. Kremic, "High temperature electronics for venus surface applications: A summary of recent technical advances," *The Planetary Science Journal*, vol. 2, no. 1, 2021.

[6] D. K. Pradhan, D. C. Moore, A. M. Francis, N. R. Grissom, J. Kupernik, and R. H. Ohme, "Materials for high-temperature digital electronics," *Nature Reviews Materials*, vol. 9, pp. 790–807, 2024.

[7] A. Moreno *et al.*, "An fpga verification, debug and performance platform for risc-v cores," in *Proc. RISC-V Summit Europe*, (Barcelona, Spain), 2023.

[8] Efinix Inc., "Risc-v and fpgas." [Online]. Available: https://www.efinixinc.com/blog/riscv-and-fpgas.html, Jul 2023. [Accessed: Sep. 26, 2025].

[9] D. Kim, *FPGA-Accelerated Evaluation and Verification of RTL Designs*. PhD thesis, Univ. California, Berkeley, Berkeley, CA, USA, May 2019. Tech. Rep. UCB/EECS-2019-57.

[10] K. Qin, X. Guo, M. Schulz, and C. Trinitis, "Feriver: An fpga-assisted emulated framework for rtl verification of risc-v processors," Apr 2025.