

```
1  #include "pwm.h"
2
3  void PWM_Clock(void)
4  {
5      RCC->APB2ENR |= RCC_APB2ENR_TIM1EN | RCC_APB2ENR_TIM15EN | RCC_APB2ENR_IOPAEN | RCC_APB2ENR_IOPBEN |
RCC_APB2ENR_AFIOEN;
6      GPIOA->CRH |= GPIO_CRH_CNF8_1 | GPIO_CRH_MODE8;
7      GPIOA->CRH &= ~GPIO_CRH_CNF8_0 ;
8      GPIOA->CRH |= GPIO_CRH_CNF9_1 | GPIO_CRH_MODE9;
9      GPIOA->CRH &= ~GPIO_CRH_CNF9_0 ;
10 }
11 void PWM_Init(void)
12 {
13     TIM1->CR1 |= TIM_CR1_CEN;
14     TIM1->CR2 |= TIM_CR2_OIS1 | TIM_CR2_OIS2;
15     TIM1->EGR |= TIM_EGR_UG;
16     TIM1->CCMR1 |= TIM_CCMR1_OC1M_2 | TIM_CCMR1_OC1M_1 | TIM_CCMR1_OC1PE | TIM_CCMR1_OC1FE;
17     TIM1->CCMR1 |= TIM_CCMR1_OC2M_2 | TIM_CCMR1_OC2M_1 | TIM_CCMR1_OC2PE | TIM_CCMR1_OC2FE;
18     TIM1->CCER |= TIM_CCER_CC1E | TIM_CCER_CC2E ;
19     TIM1->PSC = 0x450;
20     TIM1->ARR = 0x64;
21     TIM1->CCR1 = 0x0;
22     TIM1->CCR2 = 0x0;
23     TIM1->BDTR |= TIM_BDTR_MOE | TIM_BDTR_OSSI;
24     TIM1->CR1 |= TIM_CR1_ARPE | TIM_CR1_CEN;
25
26
27
28 }
29 void PWM_state0(void)
30 {
31     TIM1->PSC = 0x1000;
32     TIM1->CCR1 = 0x0;
33     TIM1->CCR2 = 0x0;
34     TIM1->EGR = TIM_EGR_UG;
35 }
36 void PWM_state1(void)
37 {
38     TIM1->PSC = 0x190;
39     TIM1->CCR2 = 0x32;
40     TIM1->EGR = TIM_EGR_UG;
41 }
42 void PWM_state2(void)
43 {
44     TIM1->PSC = 0x800;
45     TIM1->CCR1 = 0x32;
46     TIM1->CCR2 = 0x32;
47     TIM1->EGR = TIM_EGR_UG;
48 }
49
```