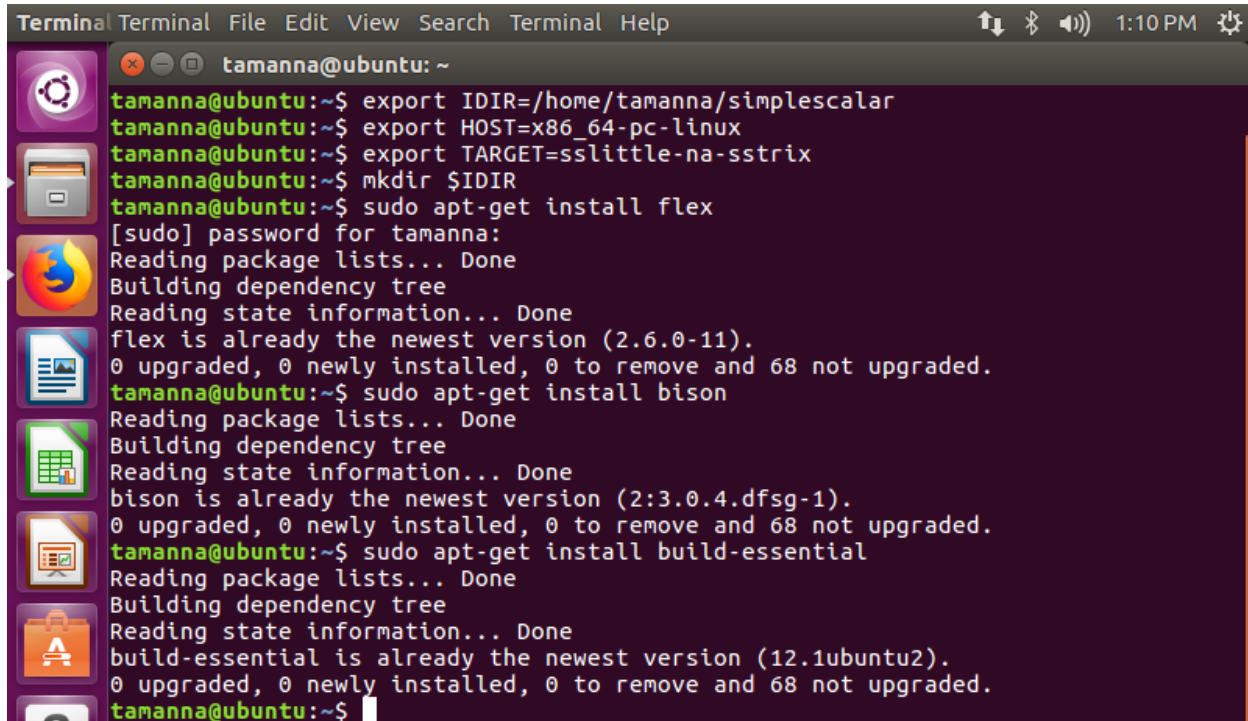


ECE 466 Advanced Computer Architecture
Project 1 Part 1
Tamanna Ravi Rupani
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Setting up the environment to run simulation,



```
Terminal Terminal File Edit View Search Terminal Help 1:10 PM
tamanna@ubuntu: ~
tamanna@ubuntu:~$ export IDIR=/home/tamanna/simplescalar
tamanna@ubuntu:~$ export HOST=x86_64-pc-linux
tamanna@ubuntu:~$ export TARGET=sslittle-na-sstrix
tamanna@ubuntu:~$ mkdir $IDIR
tamanna@ubuntu:~$ sudo apt-get install flex
[sudo] password for tamanna:
Reading package lists... Done
Building dependency tree
Reading state information... Done
flex is already the newest version (2.6.0-11).
0 upgraded, 0 newly installed, 0 to remove and 68 not upgraded.
tamanna@ubuntu:~$ sudo apt-get install bison
Reading package lists... Done
Building dependency tree
Reading state information... Done
bison is already the newest version (2:3.0.4.dfsg-1).
0 upgraded, 0 newly installed, 0 to remove and 68 not upgraded.
tamanna@ubuntu:~$ sudo apt-get install build-essential
Reading package lists... Done
Building dependency tree
Reading state information... Done
build-essential is already the newest version (12.1ubuntu2).
0 upgraded, 0 newly installed, 0 to remove and 68 not upgraded.
tamanna@ubuntu:~$
```

1. What is the performance of running the program, equake, under the default system setup (without changing any simulation parameters) using command:./sim-outorder -fastfwd 500000000 -max:inst 200000000 equake.ss < equake.in ?

Solution: Here, we will be performing the simulation for 200 Million instructions after fast forwarding the first 500 Million instructions, in an out-order fashion.

Output Parameters: -

Total no of instructions committed = 2000000000

Total no of loads committed = 45202627

Total no of stores committed = 19506919

Total simulation time in seconds (sim_elapsed_time) = 96

Performance Parameters: -

sim_IPC = 1.6905 (instructions per cycle)

sim_CPI = 0.5916 (Cycles per instruction)

sim_cycle = 118311204 (Total simulation time in cycles)

Note: Refer APPENDIX I for screenshots of the simulation.

2. How much is the performance loss if the processor uses in-order execution instead of the default out-of-order execution to run the program?

Solution:

Output Parameters: -

Total no of instructions committed = 2000000000

Total no of loads committed = 45202627

Total no of stores committed = 19506919.0000

Total simulation time in seconds (sim_elapsed_time) = 89

Performance Parameters: -

sim_IPC = 0.7790 (instructions per cycle)

sim_CPI = 1.2837 (Cycles per instruction)

sim_cycle = 256746884 (Total simulation time in cycles)

Analysis made from the above data

Order	IPC value	CPI value
Out-Order Execution	1.6905	0.5916
In-order Execution	0.7790	1.2837

What we observe is, when we run the program (out-order execution), CPI value is less as compared to the CPI value of in-order execution. So, if we compare the performance of both the executions, there is some performance loss in latter execution method.

On the other hand, more the IPC, better the performance.

IPC_{out} indicates for out-order execution

IPC_{in} indicates for in-order execution

$$\begin{aligned}
 & (\text{IPC}_{\text{out}} - \text{IPC}_{\text{in}}) / \text{IPC}_{\text{out}} * 100 \\
 &= (1.6905 - 0.7790) / 1.6905 * 100 \\
 &= 53.9189\%
 \end{aligned}$$

We can conclude that there is a performance loss in in-order execution by a percentage of **53.69189%** based on IPC values. So, it is preferable to use out-order execution for the better performance.

Note: Refer APPENDIX II for screenshots of the simulation.

3. The above experiments only perform detailed simulation on 200 million instructions. Based on the simulator running time in Question 1, estimate how long it would take to simulate the program's execution in detail from beginning to end using the default configuration. Note: Do not actually run the detailed simulation from beginning to end. It may take hours or even days to finish depending on the speed of your computer.

Solution: Time taken to simulate the program's execution from the beginning till the end is 4381s or 1hr 13mins.

Total no. of instructions in the "equake.ss" program is 165643487723.

Note: Refer APPENDIX III for screenshots of the simulation.

4. An advantage of using simulator is that you can vary the processor parameters to see their performance impact and find the optimal configuration. The default configuration has a 16KB instruction cache and a 16KB data cache. Use simulation to find the optimal instruction and data cache size for the equake. Assume the block size and associativity are the same as the default configuration. Show the changes of cache miss rates and overall performance to support your claim.

Solution:

The default cache size is said to be 16 KB for both instruction cache and data cache.

Here we will change the level 1 instruction cache and level 1 data cache in a range of 1 KB to 128 KB.

We will also compare the loss in the performance of the machine with respect to the default 16KB cache size and its simulation statistics.

Instruction input for 1 KB cache

```
./sim-outorder -cache:dl1 dl1:8:32:4:1 -cache:il1 il1:32:32:1:1 -fastfwd 500000000 -max:inst 200000000 equake.ss < equake.in
```

Performance statistics

sim_IPC 0.5773
sim_CPI 1.7323

Performance loss in comparison to 16KB cache

$$\begin{aligned} & [[\text{sim_IPC (16 KB)} - \text{sim_IPC (1 KB)}] / \text{sim_IPC (16 KB)}] * 100 \\ & = [(1.6905 - 0.5773) / 1.6905] * 100 \\ & = 65.85\% \end{aligned}$$

Note: Refer APPENDIX IV for screenshots of the simulation.

Instruction input for 4 KB cache

```
./sim-outorder -cache:dl1 dl1:32:32:4:l -cache:il1 il1:128:32:1:l -fastfwd 5000000000 -max:inst  
2000000000 quake.ss < quake.in
```

Performance statistics

sim_IPC 0.7359
sim_CPI 1.3588

Performance loss in comparison to 16KB cache

$$\begin{aligned} & [[\text{sim_IPC (16 KB)} - \text{sim_IPC (4 KB)}] / \text{sim_IPC (16 KB)}] * 100 \\ & = [(1.6905 - 0.7359) / 1.6905] * 100 \\ & = 56.46\% \end{aligned}$$

Note: Refer APPENDIX IV for screenshots of the simulation.

Instruction input for 8 KB cache

```
./sim-outorder -cache:dl1 dl1:64:32:4:l -cache:il1 il1:256:32:1:l -fastfwd 5000000000 -max:inst  
2000000000 quake.ss < quake.in
```

Performance statistics

sim_IPC 1.1022
sim_CPI 0.9073

Performance loss in comparison to 16KB cache

$$\begin{aligned} & [[\text{sim_IPC (16 KB)} - \text{sim_IPC (8 KB)}] / \text{sim_IPC (16 KB)}] * 100 \\ & = [(1.6905 - 1.1022) / 1.6905] * 100 \\ & = 34.8\% \end{aligned}$$

Note: Refer APPENDIX IV for screenshots of the simulation.

Instruction input for 32 KB cache

```
./sim-outorder -cache:dl1 dl1:256:32:4:l -cache:il1 il1:1024:32:1:l -fastfwd 500000000 -max:inst  
2000000000 equake.ss < equake.in
```

Performance statistics

```
sim_IPC 1.6909  
sim_CPI 0.5914
```

Performance loss in comparison to 16KB cache

$$\begin{aligned} & [[\text{sim_IPC (16 KB)} - \text{sim_IPC (32 KB)}] / \text{sim_IPC (16 KB)}] * 100 \\ & = [(1.6905 - 1.6909) / 1.6905] * 100 \\ & = 0.023\% \end{aligned}$$

Note: Refer APPENDIX IV for screenshots of the simulation.

Instruction input for 64 KB cache

```
./sim-outorder -cache:dl1 dl1:512:32:4:l -cache:il1 il1:2048:32:1:l -fastfwd 500000000 -max:inst  
2000000000 equake.ss < equake.in
```

Performance statistics

```
sim_IPC 2.0144  
sim_CPI 0.4964
```

Performance loss in comparison to 16KB cache

$$\begin{aligned} & [[\text{sim_IPC (16 KB)} - \text{sim_IPC (64 KB)}] / \text{sim_IPC (16 KB)}] * 100 \\ & = [(1.6905 - 2.0144) / 1.6905] * 100 \\ & = 19.16\% \end{aligned}$$

Note: Refer APPENDIX IV for screenshots of the simulation.

Instruction input for 128 KB cache

```
./sim-outorder -cache:dl1 dl1:1024:32:4:l -cache:il1 il1:4096:32:1:l -fastfwd 500000000 -max:inst  
2000000000 equake.ss < equake.in
```

Performance statistics

```
sim_IPC 2.0692  
sim_CPI 0.4833
```

Performance loss in comparison to 16KB cache

$$\begin{aligned} & [[\text{sim_IPC (16 KB)} - \text{sim_IPC (128 KB)}] / \text{sim_IPC (16 KB)}] * 100 \\ & = [(1.6905 - 2.0692) / 1.6905] * 100 \\ & = 22.40\% \end{aligned}$$

Note: Refer APPENDIX IV for screenshots of the simulation.

Instruction and data cache size	sim_IPC	sim_CPI	il1.miss_rate	dl1.miss_rate	Performance loss compared to default configuration (16 KB IPC)
1 KB	0.5773	1.7323	0.1749	0.0181	65.85%
4 KB	0.7359	1.3588	0.1319	0.0016	56.46%
8 KB	1.1022	0.9073	0.0723	0.0009	34.8%
16 KB (default)	1.6905	0.5916	0.0223	0.0007	Default. Thus 0%
32 KB	1.6909	0.5914	0.0223	0.0007	0.023%
64 KB	2.0144	0.4964	0.0027	0.0007	19.16%
128 KB	2.0692	0.4833	0.0000	0.0007	22.40%

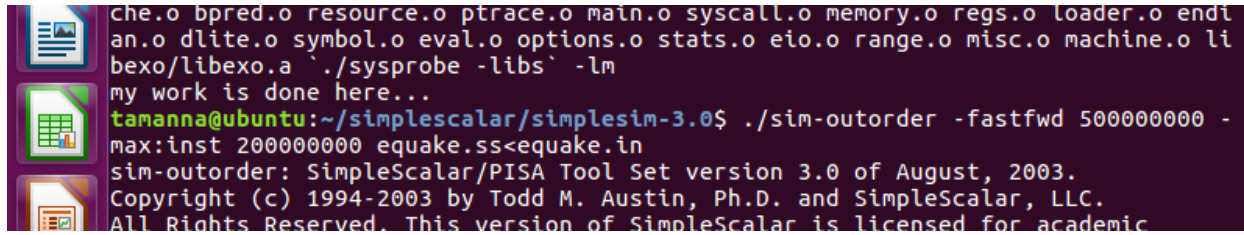
From the above table we can observe two things and conclude the following,

If we consider the performance loss between the two machines with different cache sizes, 32 KB instruction and data cache machine has a 0.023% performance loss in comparison to the default 16KB cache machine. We can also observe that 16 KB cache and 32 KB cache machine has a very minute difference in its IPC and miss rates. Hence in this term, 32 KB instruction and data cache would be an optimal option.

But if we consider the instruction cache miss rate and data cache miss rate, 128KB cache has 0 instruction cache miss rate in comparison to 16 KB instruction cache and a 0.0007 data cache miss rate in comparison to 16 KB data cache miss rate. In this manner, 128 KB would be an optimal option of cache size.

APPENDIX I

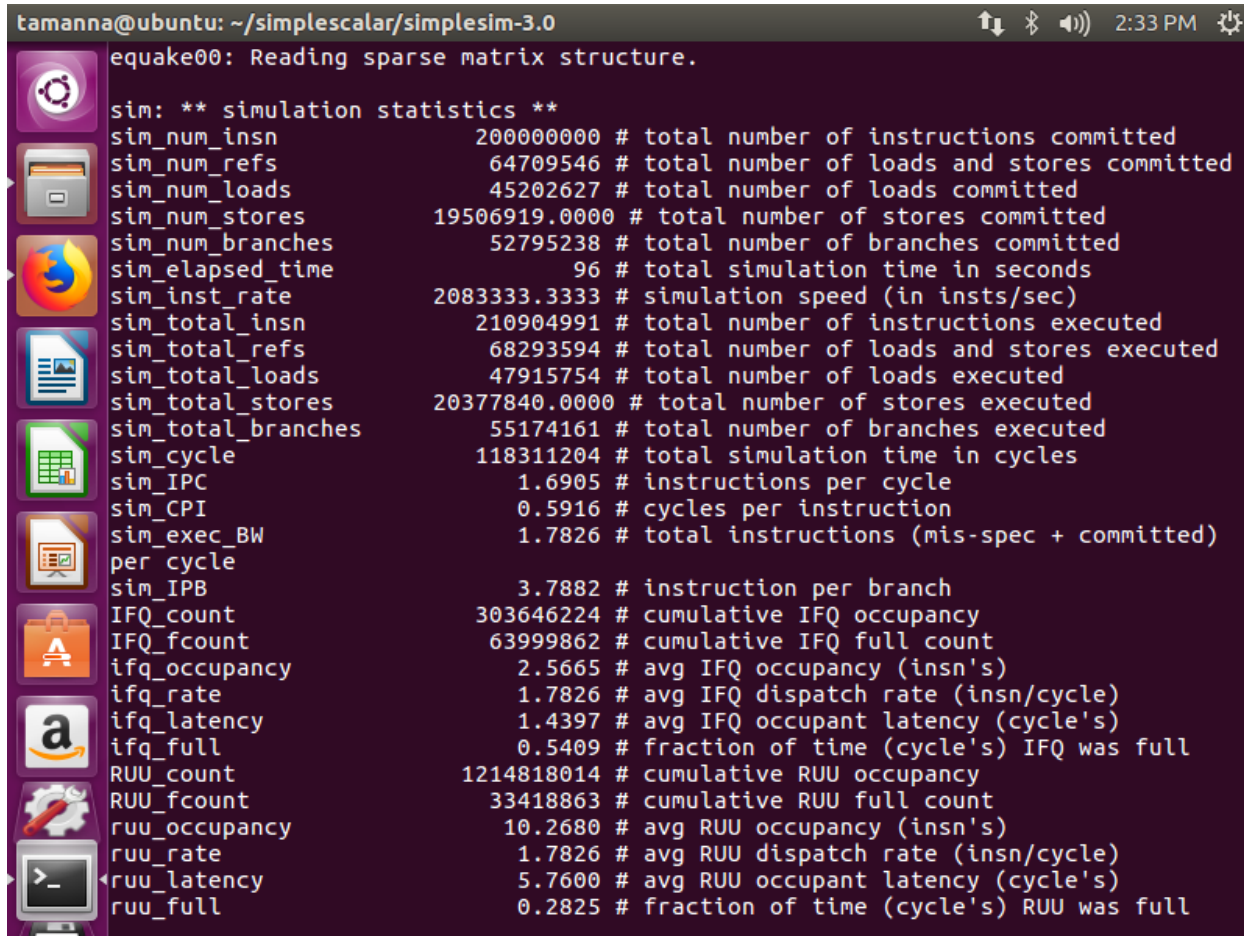
Command



A terminal window with a dark background and light-colored text. The prompt is 'tamanna@ubuntu:~/simplescalar/simplesim-3.0\$'. The command being executed is './sim-outorder -fastfwd 500000000 -max:inst 2000000000 quake.ss<quake.in'. The output shows the SimpleScalar/PISA Tool Set version 3.0 of August, 2003, and copyright information.

```
che.o bpred.o resource.o ptrace.o main.o syscall.o memory.o regs.o loader.o endt
an.o dlite.o symbol.o eval.o options.o stats.o eio.o range.o misc.o machine.o li
bexo/libexo.a `./sysprobe -libs` -lm
my work is done here...
tamanna@ubuntu:~/simplescalar/simplesim-3.0$ ./sim-outorder -fastfwd 500000000 -
max:inst 2000000000 quake.ss<quake.in
sim-outorder: SimpleScalar/PISA Tool Set version 3.0 of August, 2003.
Copyright (c) 1994-2003 by Todd M. Austin, Ph.D. and SimpleScalar, LLC.
All Rights Reserved. This version of SimpleScalar is licensed for academic
```

Simulation statistics



A terminal window showing the output of the 'sim' command. The prompt is 'tamanna@ubuntu:~/simplescalar/simplesim-3.0'. The output displays various simulation statistics for the 'quake00' simulation.

```
tamanna@ubuntu:~/simplescalar/simplesim-3.0
quake00: Reading sparse matrix structure.

sim: ** simulation statistics **
sim_num_insn      200000000 # total number of instructions committed
sim_num_refs      64709546 # total number of loads and stores committed
sim_num_loads     45202627 # total number of loads committed
sim_num_stores    19506919.0000 # total number of stores committed
sim_num_branches  52795238 # total number of branches committed
sim_elapsed_time   96 # total simulation time in seconds
sim_inst_rate     2083333.3333 # simulation speed (in insts/sec)
sim_total_insn    210904991 # total number of instructions executed
sim_total_refs    68293594 # total number of loads and stores executed
sim_total_loads   47915754 # total number of loads executed
sim_total_stores  20377840.0000 # total number of stores executed
sim_total_branches 55174161 # total number of branches executed
sim_cycle         118311204 # total simulation time in cycles
sim_IPC           1.6905 # instructions per cycle
sim_CPI           0.5916 # cycles per instruction
sim_exec_BW       1.7826 # total instructions (mis-spec + committed)
per cycle
sim_IPB           3.7882 # instruction per branch
IFQ_count         303646224 # cumulative IFQ occupancy
IFQ_fcount        63999862 # cumulative IFQ full count
ifq_occupancy     2.5665 # avg IFQ occupancy (insn's)
ifq_rate          1.7826 # avg IFQ dispatch rate (insn/cycle)
ifq_latency       1.4397 # avg IFQ occupant latency (cycle's)
ifq_full          0.5409 # fraction of time (cycle's) IFQ was full
RUU_count         1214818014 # cumulative RUU occupancy
RUU_fcount        33418863 # cumulative RUU full count
ruu_occupancy     10.2680 # avg RUU occupancy (insn's)
ruu_rate          1.7826 # avg RUU dispatch rate (insn/cycle)
ruu_latency       5.7600 # avg RUU occupant latency (cycle's)
ruu_full          0.2825 # fraction of time (cycle's) RUU was full
```

APPENDIX II

Command

```
mem.plab_miss_rate 0.0000 # First level page table miss rate  
tamanna@ubuntu:~/simplescalar/simplesim-3.0$ ./sim-outorder -issue:inorder -fast  
fwd 500000000 -max:inst 200000000 equake.ss<equake.in  
sim-outorder: SimpleScalar/PISA Tool Set version 3.0 of August, 2003.  
Copyright (c) 1994-2003 by Todd M. Austin, Ph.D. and SimpleScalar, LLC.  
All Rights Reserved. This version of SimpleScalar is licensed for academic  
non-commercial use. No portion of this work may be used by any commercial  
entity or for any commercial purpose without the prior written permission
```

Observations Made after the Simulation is done

```
tamanna@ubuntu: ~/simplescalar/simplesim-3.0 2:35 PM  
equake00: Reading sparse matrix structure.  
sim: ** simulation statistics **  
sim_num_insn 200000000 # total number of instructions committed  
sim_num_refs 64709546 # total number of loads and stores committed  
sim_num_loads 45202627 # total number of loads committed  
sim_num_stores 19506919.0000 # total number of stores committed  
sim_num_branches 52795238 # total number of branches committed  
sim_elapsed_time 89 # total simulation time in seconds  
sim_inst_rate 2247191.0112 # simulation speed (in insts/sec)  
sim_total_insn 201508858 # total number of instructions executed  
sim_total_refs 65055754 # total number of loads and stores executed  
sim_total_loads 45548293 # total number of loads executed  
sim_total_stores 19507461.0000 # total number of stores executed  
sim_total_branches 52795439 # total number of branches executed  
sim_cycle 256746884 # total simulation time in cycles  
sim_IPC 0.7790 # instructions per cycle  
sim_CPI 1.2837 # cycles per instruction  
sim_exec_BW 0.7849 # total instructions (mis-spec + committed)  
per cycle  
sim_IPB 3.7882 # instruction per branch  
IFQ_count 894249767 # cumulative IFQ occupancy  
IFQ_fcount 211392506 # cumulative IFQ full count  
ifq_occupancy 3.4830 # avg IFQ occupancy (insn's)  
ifq_rate 0.7849 # avg IFQ dispatch rate (insn/cycle)  
ifq_latency 4.4378 # avg IFQ occupant latency (cycle's)  
ifq_full 0.8233 # fraction of time (cycle's) IFQ was full  
RUU_count 696464385 # cumulative RUU occupancy  
RUU_fcount 0 # cumulative RUU full count  
ruu_occupancy 2.7126 # avg RUU occupancy (insn's)  
ruu_rate 0.7849 # avg RUU dispatch rate (insn/cycle)  
ruu_latency 3.4562 # avg RUU occupant latency (cycle's)  
ruu_full 0.0000 # fraction of time (cycle's) RUU was full
```


APPENDIX III

Command

```
tamanna@ubuntu:~/simplescalar/simplesim-3.0$ ./sim-safe equake.ss<equake.in
sim-safe: SimpleScalar/PISA Tool Set version 3.0 of August, 2003.
Copyright (c) 1994-2003 by Todd M. Austin, Ph.D. and SimpleScalar, LLC.
All Rights Reserved. This version of SimpleScalar is licensed for academic
```

Observations Made after the Simulation is done

```
tamanna@ubuntu: ~/simplescalar/simplesim-3.0 4:05 PM
5903: -3.98e+00 -4.62e+00 -6.76e+00
16745: 6.61e-03 2.52e-02 -1.00e-01
Time step 3840
5903: -3.98e+00 -4.62e+00 -6.76e+00
16745: 2.45e-03 2.66e-02 -1.01e-01
equake00: 30169 nodes 151173 elems 3855 timesteps
equake00: Done. Terminating the simulation.

sim: ** simulation statistics **
sim_num_insn      165643487723 # total number of instructions executed
sim_num_refs      78603143990 # total number of loads and stores executed
sim_elapsed_time   4381 # total simulation time in seconds
sim_inst_rate     37809515.5725 # simulation speed (in insts/sec)
ld_text_base      0x00400000 # program text (code) segment base
ld_text_size      132784 # program text (code) size in bytes
ld_data_base      0x10000000 # program initialized data segment base
ld_data_size      16384 # program init'ed '.data' and uninit'ed '.bs
s' size in bytes
ld_stack_base     0x7ffffc000 # program stack segment base (highest addres
s in stack)
ld_stack_size     16384 # program initial stack size
ld_prog_entry     0x00400140 # program entry point (initial PC)
ld_environ_base   0x7fff8000 # program environment base address
ld_target_big_endian 0 # target executable endian-ness, non-zero if
big endian
mem.page_count    10394 # total number of pages allocated
mem.page_mem      41576k # total size of memory pages allocated
mem.ptab_misses   3253141 # total first level page table misses
mem.ptab_accesses 906494437826 # total page table accesses
mem.ptab_miss_rate 0.0000 # first level page table miss rate

tamanna@ubuntu:~/simplescalar/simplesim-3.0$
```

APPENDIX IV

Command for 1 KB cache

```
tamanna@ubuntu:~/simplescalar/simplesim-3.0$ ./sim-outorder -cache:dl1 dl1:8:32:4:l -cache:il1 il1:32:32:1:l -fastfwd 500000000 -max:inst 200000000 equake.ss < equake.in
sim-outorder: SimpleScalar/PISA Tool Set version 3.0 of August, 2003.
Copyright (c) 1994-2003 by Todd M. Austin, Ph.D. and SimpleScalar, LLC.
```

Cache value for 1 KB cache

```
-lsq:size 8 # load/store queue (LSQ) size
-cache:dl1 dl1:8:32:4:l # l1 data cache config, i.e., {<config>|none}
-cache:dl1lat 1 # l1 data cache hit latency (in cycles)
-cache:dl2 ul2:1024:64:4:l # l2 data cache config, i.e., {<config>|none}
-cache:dl2lat 6 # l2 data cache hit latency (in cycles)
-cache:il1 il1:32:32:1:l # l1 inst cache config, i.e., {<config>|dl1|dl2|none}
-cache:il1lat 1 # l1 instruction cache hit latency (in cycles)
-cache:il2 dl2 # l2 instruction cache config, i.e., {<config>|dl2|none}
-cache:il2lat 6 # l2 instruction cache hit latency (in cycles)
```

Simulation statistics for 1 KB cache

```
tamanna@ubuntu: ~/simplescalar/simplesim-3.0 8:42 AM
sim: ** fast forwarding 500000000 insts **
equake00: Reading nodes.
equake00: Reading elements.
sim: ** starting performance simulation **
equake00: Reading sparse matrix structure.

sim: ** simulation statistics **
sim_num_insn 200000000 # total number of instructions committed
sim_num_refs 64709546 # total number of loads and stores committed
sim_num_loads 45202627 # total number of loads committed
sim_num_stores 19506919.0000 # total number of stores committed
sim_num_branches 52795238 # total number of branches committed
sim_elapsed_time 270 # total simulation time in seconds
sim_inst_rate 740740.7407 # simulation speed (in insts/sec)
sim_total_insn 210368917 # total number of instructions executed
sim_total_refs 68165502 # total number of loads and stores executed
sim_total_loads 47794382 # total number of loads executed
sim_total_stores 20371120.0000 # total number of stores executed
sim_total_branches 55099079 # total number of branches executed
sim_cycle 346463401 # total simulation time in cycles
sim_IPC 0.5773 # instructions per cycle
sim_CPI 1.7323 # cycles per instruction
sim_exec_BW 0.6072 # total instructions (mis-spec + committed) per cycle
sim_IPB 3.7882 # instruction per branch
IFQ_count 260492461 # cumulative IFQ occupancy
IFQ_fcount 48254812 # cumulative IFQ full count
ifq_occupancy 0.7519 # avg IFQ occupancy (insn's)
ifq_rate 0.6072 # avg IFQ dispatch rate (insn/cycle)
ifq_latency 1.2383 # avg IFQ occupant latency (cycle's)
ifq_full 0.1393 # fraction of time (cycle's) IFQ was full
RUU_count 1043156569 # cumulative RUU occupancy
RUU_fcount 19282309 # cumulative RUU full count
```

Cache misses for 1 KB cache

```
tamanna@ubuntu: ~/simplescalar/simplesim-3.0
bpred_bimod.ras_rate.PP      1.0000 # RAS prediction rate (i.e., RAS hits/used RAS)
il1.accesses                  259159792 # total number of accesses
il1.hits                      213823722 # total number of hits
il1.misses                    45336070 # total number of misses
il1.replacements              45336038 # total number of replacements
il1.writebacks                0 # total number of writebacks
il1.invalidations             0 # total number of invalidations
il1.miss_rate                 0.1749 # miss rate (i.e., misses/ref)
il1.repl_rate                 0.1749 # replacement rate (i.e., repls/ref)
il1.wb_rate                   0.0000 # writeback rate (i.e., wrbks/ref)
il1.inv_rate                  0.0000 # invalidation rate (i.e., invs/ref)
dl1.accesses                  65731636 # total number of accesses
dl1.hits                      64540109 # total number of hits
dl1.misses                    1191527 # total number of misses
dl1.replacements              1191495 # total number of replacements
dl1.writebacks                310688 # total number of writebacks
dl1.invalidations             0 # total number of invalidations
dl1.miss_rate                 0.0181 # miss rate (i.e., misses/ref)
dl1.repl_rate                 0.0181 # replacement rate (i.e., repls/ref)
dl1.wb_rate                   0.0047 # writeback rate (i.e., wrbks/ref)
dl1.inv_rate                  0.0000 # invalidation rate (i.e., invs/ref)
ul2.accesses                  46838285 # total number of accesses
ul2.hits                      46816485 # total number of hits
ul2.misses                    21800 # total number of misses
ul2.replacements              17704 # total number of replacements
ul2.writebacks                14732 # total number of writebacks
ul2.invalidations             0 # total number of invalidations
ul2.miss_rate                 0.0005 # miss rate (i.e., misses/ref)
ul2.repl_rate                 0.0004 # replacement rate (i.e., repls/ref)
ul2.wb_rate                   0.0003 # writeback rate (i.e., wrbks/ref)
ul2.inv_rate                  0.0000 # invalidation rate (i.e., invs/ref)
itlb.accesses                 259159792 # total number of accesses
```





















Command for 4 KB cache

```
tamanna@ubuntu:~/simplescalar/simplesim-3.0$ ./sim-outorder -cache:dl1 dl1:32:32
:4:l -cache:il1 il1:128:32:1:l -fastfwd 500000000 -max:inst 2000000000 quake.ss
< quake.in
sim-outorder: SimpleScalar/PISA Tool Set version 3.0 of August, 2003.
Copyright (c) 1994-2003 by Todd M. Austin, Ph.D. and SimpleScalar, LLC.
All Rights Reserved. This version of SimpleScalar is licensed for academic
```





















Cache value for 4 KB cache

```
l1sq.size                     8 # l1 store queue (LSQ) size
-cache:dl1                    dl1:32:32:4:l # l1 data cache config, i.e., {<config>|none}
-cache:dl1lat                  1 # l1 data cache hit latency (in cycles)
-cache:dl2                     ul2:1024:64:4:l # l2 data cache config, i.e., {<config>|none}
-cache:dl2lat                  6 # l2 data cache hit latency (in cycles)
-cache:il1                     il1:128:32:1:l # l1 inst cache config, i.e., {<config>|dl1|dl2|
none}
-cache:il1lat                  1 # l1 instruction cache hit latency (in cycles)
-cache:il2                     dl2 # l2 instruction cache config, i.e., {<config>|dl2
|none}
-cache:il2lat                  6 # l2 instruction cache hit latency (in cycles)
```



Simulation statistics for 4 KB cache

	sim: ** simulation statistics **
	sim_num_insn 200000000 # total number of instructions committed
	sim_num_refs 64709546 # total number of loads and stores committed
	sim_num_loads 45202627 # total number of loads committed
	sim_num_stores 19506919.0000 # total number of stores committed
	sim_num_branches 52795238 # total number of branches committed
	sim_elapsed_time 267 # total simulation time in seconds
	sim_inst_rate 749063.6704 # simulation speed (in insts/sec)
	sim_total_insn 210860377 # total number of instructions executed
	sim_total_refs 68280628 # total number of loads and stores executed
	sim_total_loads 47908591 # total number of loads executed
	sim_total_stores 20372037.0000 # total number of stores executed
	sim_total_branches 55161501 # total number of branches executed
	sim_cycle 271764251 # total simulation time in cycles
	sim_IPC 0.7359 # instructions per cycle
	sim_CPI 1.3588 # cycles per instruction
	sim_exec_BW 0.7759 # total instructions (mis-spec + committed)
	per cycle
	sim_IPB 3.7882 # instruction per branch
	IFQ_count 263417618 # cumulative IFQ occupancy

Cache misses for 4 KB cache

)
	il1.accesses 246905880 # total number of accesses
	il1.hits 214332196 # total number of hits
	il1.misses 32573684 # total number of misses
	il1.replacements 32573556 # total number of replacements
	il1.writebacks 0 # total number of writebacks
	il1.invalidations 0 # total number of invalidations
	il1.miss_rate 0.1319 # miss rate (i.e., misses/ref)
	il1.repl_rate 0.1319 # replacement rate (i.e., repls/ref)
	il1.wb_rate 0.0000 # writeback rate (i.e., wrbks/ref)
	il1.inv_rate 0.0000 # invalidation rate (i.e., invs/ref)
	dl1.accesses 65458295 # total number of accesses
	dl1.hits 65352399 # total number of hits
	dl1.misses 105896 # total number of misses
	dl1.replacements 105768 # total number of replacements
	dl1.writebacks 38925 # total number of writebacks
	dl1.invalidations 0 # total number of invalidations
	dl1.miss_rate 0.0016 # miss rate (i.e., misses/ref)
	dl1.repl_rate 0.0016 # replacement rate (i.e., repls/ref)
	dl1.wb_rate 0.0006 # writeback rate (i.e., wrbks/ref)
	dl1.inv_rate 0.0000 # invalidation rate (i.e., invs/ref)
	ul2.accesses 32718505 # total number of accesses
	ul2.hits 32696685 # total number of hits
	ul2.misses 21820 # total number of misses
	ul2.replacements 17724 # total number of replacements
	ul2.writebacks 14716 # total number of writebacks
	ul2.invalidations 0 # total number of invalidations

Command for 8 KB cache

```
 tamanna@ubuntu:~/simplescalar/simplesim-3.0$ ./sim-outorder -cache:dl1 dl1:64:32  
:4:l -cache:il1 il1:256:32:1:l -fastfwd 500000000 -max:inst 2000000000 quake.ss  
< quake.in  
 sim-outorder: SimpleScalar/PISA Tool Set version 3.0 of August, 2003.
```


Cache value for 8 KB cache

```

-cache:dl1      dl1:64:32:4:l # l1 data cache config, i.e., {<config>|none}
-cache:dl1lat   1 # l1 data cache hit latency (in cycles)
-cache:dl2      ul2:1024:64:4:l # l2 data cache config, i.e., {<config>|none}
-cache:dl2lat   6 # l2 data cache hit latency (in cycles)
-cache:il1      il1:256:32:1:l # l1 inst cache config, i.e., {<config>|dl1|dl2|
none}
-cache:il1lat   1 # l1 instruction cache hit latency (in cycles)
-cache:il2      dl2 # l2 instruction cache config, i.e., {<config>|dl2
|none}
-cache:il2lat   6 # l2 instruction cache hit latency (in cycles)

```

Simulation statistics for 8 KB cache

```

sim: ** simulation statistics **
sim_num_insn      200000000 # total number of instructions committed
sim_num_refs      64709546 # total number of loads and stores committed
sim_num_loads     45202627 # total number of loads committed
sim_num_stores    19506919.0000 # total number of stores committed
sim_num_branches  52795238 # total number of branches committed
sim_elapsed_time  257 # total simulation time in seconds
sim_inst_rate     778210.1167 # simulation speed (in insts/sec)
sim_total_insn    210900769 # total number of instructions executed
sim_total_refs    68292434 # total number of loads and stores executed
sim_total_loads   47914737 # total number of loads executed
sim_total_stores  20377697.0000 # total number of stores executed
sim_total_branches 55173587 # total number of branches executed
sim_cycle         181457255 # total simulation time in cycles
sim_IPC           1.1022 # instructions per cycle
sim_CPI           0.9073 # cycles per instruction
sim_exec_BW       1.1623 # total instructions (mis-spec + committed)
per cycle
sim_IPB           3.7882 # instruction per branch
IFQ_count         278694851 # cumulative IFQ occupancy

```

Cache misses for 8 KB cache

```

il1.accesses      231094211 # total number of accesses
il1.hits          214378296 # total number of hits
il1.misses        16715915 # total number of misses
il1.replacements  16715672 # total number of replacements
il1.writebacks    0 # total number of writebacks
il1.invalidations 0 # total number of invalidations
il1.miss_rate     0.0723 # miss rate (i.e., misses/ref)
il1.repl_rate     0.0723 # replacement rate (i.e., repls/ref)
il1.wb_rate       0.0000 # writeback rate (i.e., wrbks/ref)
il1.inv_rate      0.0000 # invalidation rate (i.e., invs/ref)
dl1.accesses      65344843 # total number of accesses
dl1.hits          65283964 # total number of hits
dl1.misses        60879 # total number of misses
dl1.replacements  60623 # total number of replacements
dl1.writebacks    36645 # total number of writebacks
dl1.invalidations 0 # total number of invalidations
dl1.miss_rate     0.0009 # miss rate (i.e., misses/ref)
dl1.repl_rate     0.0009 # replacement rate (i.e., repls/ref)
dl1.wb_rate       0.0006 # writeback rate (i.e., wrbks/ref)
dl1.inv_rate      0.0000 # invalidation rate (i.e., invs/ref)
ul2.accesses      16813439 # total number of accesses
ul2.hits          16791591 # total number of hits
ul2.misses        21848 # total number of misses
ul2.replacements  17752 # total number of replacements
ul2.writebacks    14705 # total number of writebacks

```

Command for 32 KB cache

```

tamanna@ubuntu:~/simplescalar/simplesim-3.0$ ./sim-outorder -cache:dl1 dl1:256:32:4:l -cache:il1 il1:1024:32:1:l -fastfwd 500000000 -max:inst 2000000000 quake.s
s < quake.in
sim-outorder: SimpleScalar/PISA Tool Set version 3.0 of August, 2003.
Copyright (c) 1994-2003 by Todd M. Austin, Ph.D. and SimpleScalar LLC

```

Cache value for 32 KB cache

```

-cache:dl1          dl1:256:32:4:l # l1 data cache config, i.e., {<config>|none}
-cache:dl1lat       1 # l1 data cache hit latency (in cycles)
-cache:dl2          ul2:1024:64:4:l # l2 data cache config, i.e., {<config>|none}
-cache:dl2lat       6 # l2 data cache hit latency (in cycles)
-cache:il1          il1:1024:32:1:l # l1 inst cache config, i.e., {<config>|dl1|dl2
|none}
-cache:il1lat       1 # l1 instruction cache hit latency (in cycles)
-cache:il2          dl2 # l2 instruction cache config, i.e., {<config>|dl2
|none}

```

Simulation statistics for 32 KB cache

```

sim: ** simulation statistics **
sim_num_insn          200000000 # total number of instructions committed
sim_num_refs          64709546 # total number of loads and stores committed
sim_num_loads          45202627 # total number of loads committed
sim_num_stores        19506919.0000 # total number of stores committed
sim_num_branches       52795238 # total number of branches committed
sim_elapsed_time       159 # total simulation time in seconds
sim_inst_rate         1257861.6352 # simulation speed (in insts/sec)
sim_total_insn        210905111 # total number of instructions executed
sim_total_refs        68293602 # total number of loads and stores executed
sim_total_loads        47915754 # total number of loads executed
sim_total_stores       20377848.0000 # total number of stores executed
sim_total_branches     55174166 # total number of branches executed
sim_cycle             118280546 # total simulation time in cycles
sim_IPC                1.6909 # instructions per cycle
sim_CPI                0.5914 # cycles per instruction
sim_exec_BW            1.7831 # total instructions (mis-spec + committed)

```

Cache misses for 32 KB cache

```

il1.accesses          214384565 # total number of accesses
il1.hits              214384565 # total number of hits
il1.misses            4893715 # total number of misses
il1.replacements      4893243 # total number of replacements
il1.writebacks        0 # total number of writebacks
il1.invalidations     0 # total number of invalidations
il1.miss_rate         0.0223 # miss rate (i.e., misses/ref)
il1.repl_rate         0.0223 # replacement rate (i.e., repls/ref)
il1.wb_rate           0.0000 # writeback rate (i.e., wrbks/ref)
il1.inv_rate          0.0000 # invalidation rate (i.e., invs/ref)
dl1.accesses          65343077 # total number of accesses
dl1.hits              65299941 # total number of hits
dl1.misses            43136 # total number of misses
dl1.replacements      42112 # total number of replacements
dl1.writebacks        34993 # total number of writebacks
dl1.invalidations     0 # total number of invalidations
dl1.miss_rate         0.0007 # miss rate (i.e., misses/ref)
dl1.repl_rate         0.0006 # replacement rate (i.e., repls/ref)
dl1.wb_rate           0.0005 # writeback rate (i.e., wrbks/ref)
dl1.inv_rate          0.0000 # invalidation rate (i.e., invs/ref)
ul2.accesses          4971844 # total number of accesses
ul2.hits              4950019 # total number of hits
ul2.misses            21825 # total number of misses

```

Command for 64 KB cache

```
tamanna@ubuntu:~/simplescalar/simplesim-3.0$ ./sim-outorder -cache:dl1 dl1:512:32:4:l -cache:il1 il1:2048:32:1:l -fastfwd 500000000 -max:inst 2000000000 quake.s  
s < quake.in  
sim-outorder: SimpleScalar/PISA Tool Set version 3.0 of August, 2003.
```

Cache value for 64 KB cache

```
-cache:dl1      dl1:512:32:4:l # l1 data cache config, i.e., {<config>|none}  
-cache:dl1lat   1 # l1 data cache hit latency (in cycles)  
-cache:dl2      ul2:1024:64:4:l # l2 data cache config, i.e., {<config>|none}  
-cache:dl2lat   6 # l2 data cache hit latency (in cycles)  
-cache:il1      il1:2048:32:1:l # l1 inst cache config, i.e., {<config>|dl1|dl2  
|none}  
-cache:il1lat   1 # l1 instruction cache hit latency (in cycles)  
-cache:il2      dl2 # l2 instruction cache config, i.e., {<config>|dl2  
|none}
```

Simulation statistics for 64 KB cache

```
sim: ** simulation statistics **  
sim_num_insn      200000000 # total number of instructions committed  
sim_num_refs      64709546 # total number of loads and stores committed  
sim_num_loads      45202627 # total number of loads committed  
sim_num_stores     19506919.0000 # total number of stores committed  
sim_num_branches   52795238 # total number of branches committed  
sim_elapsed_time   198 # total simulation time in seconds  
sim_inst_rate      1010101.0101 # simulation speed (in insts/sec)  
sim_total_insn     210905148 # total number of instructions executed  
sim_total_refs     68293602 # total number of loads and stores executed  
sim_total_loads     47915755 # total number of loads executed  
sim_total_stores    20377847.0000 # total number of stores executed  
sim_total_branches 55174169 # total number of branches executed  
sim_cycle          99283172 # total simulation time in cycles  
sim_IPC            2.0144 # instructions per cycle  
sim_CPI            0.4964 # cycles per instruction  
sim_exec_BW        2.1243 # total instructions (mis-spec + committed)
```

Cache misses for 64 KB cache

```
il1.accesses      214384907 # total number of accesses  
il1.hits          214384907 # total number of hits  
il1.misses        576201 # total number of misses  
il1.replacements  575679 # total number of replacements  
il1.writebacks    0 # total number of writebacks  
il1.invalidations 0 # total number of invalidations  
il1.miss_rate      0.0027 # miss rate (i.e., misses/ref)  
il1.repl_rate      0.0027 # replacement rate (i.e., repls/ref)  
il1.wb_rate        0.0000 # writeback rate (i.e., wrbks/ref)  
il1.inv_rate       0.0000 # invalidation rate (i.e., invs/ref)  
dl1.accesses      65343073 # total number of accesses  
dl1.hits          65300134 # total number of hits  
dl1.misses        42939 # total number of misses  
dl1.replacements  40891 # total number of replacements  
dl1.writebacks    34194 # total number of writebacks  
dl1.invalidations 0 # total number of invalidations  
dl1.miss_rate      0.0007 # miss rate (i.e., misses/ref)  
dl1.repl_rate      0.0006 # replacement rate (i.e., repls/ref)  
dl1.wb_rate        0.0005 # writeback rate (i.e., wrbks/ref)  
dl1.inv_rate       0.0000 # invalidation rate (i.e., invs/ref)  
ul2.accesses      653334 # total number of accesses
```


Command for 128 KB cache

```
tamanna@ubuntu:~/simplescalar/simplesim-3.0$ ./sim-outorder -cache:dl1 dl1:1024:32:4:l -cache:il1 il1:4096:32:1:l -fastfwd 500000000 -max:inst 200000000 equake.ss < equake.in
sim-outorder: SimpleScalar/PISA Tool Set version 3.0 of August, 2003.
Copyright (c) 1994-2003 by Todd M. Austin, Ph.D. and SimpleScalar, LLC
```

Cache for 128 KB cache value

```
-lsq:size                8 # load/store queue (LSQ) size
-cache:dl1              dl1:1024:32:4:l # l1 data cache config, i.e., {<config>|none}
-cache:dl1lat           1 # l1 data cache hit latency (in cycles)
-cache:dl2              ul2:1024:64:4:l # l2 data cache config, i.e., {<config>|none}
-cache:dl2lat           6 # l2 data cache hit latency (in cycles)
-cache:il1              il1:4096:32:1:l # l1 inst cache config, i.e., {<config>|dl1|dl2|none}
-cache:il1lat           1 # l1 instruction cache hit latency (in cycles)
-cache:il2              dl2 # l2 instruction cache config, i.e., {<config>|dl2|none}
-cache:il2lat           6 # l2 instruction cache hit latency (in cycles)
```

Simulation statistics for 128 KB cache

```
sim: ** simulation statistics **
sim_num_insn            200000000 # total number of instructions committed
sim_num_refs            64709546 # total number of loads and stores committed
sim_num_loads           45202627 # total number of loads committed
sim_num_stores          19506919.0000 # total number of stores committed
sim_num_branches        52795238 # total number of branches committed
sim_elapsed_time        186 # total simulation time in seconds
sim_inst_rate           1075268.8172 # simulation speed (in insts/sec)
sim_total_insn          211245818 # total number of instructions executed
sim_total_refs          68520718 # total number of loads and stores executed
sim_total_loads         47915755 # total number of loads executed
sim_total_stores        20604963.0000 # total number of stores executed
sim_total_branches      55174166 # total number of branches executed
sim_cycle               96657289 # total simulation time in cycles
sim_IPC                 2.0692 # instructions per cycle
sim_CPI                 0.4833 # cycles per instruction
sim_exec_BW             2.1855 # total instructions (mis-spec + committed)
```

Cache misses for 128 KB cache

```
il1.accesses            214953224 # total number of accesses
il1.hits                214952693 # total number of hits
il1.misses               531 # total number of misses
il1.replacements        0 # total number of replacements
il1.writebacks          0 # total number of writebacks
il1.invalidations       0 # total number of invalidations
il1.miss_rate           0.0000 # miss rate (i.e., misses/ref)
il1.repl_rate           0.0000 # replacement rate (i.e., repls/ref)
il1.wb_rate             0.0000 # writeback rate (i.e., wrbks/ref)
il1.inv_rate            0.0000 # invalidation rate (i.e., invs/ref)
dl1.accesses            65343073 # total number of accesses
dl1.hits                65300142 # total number of hits
dl1.misses              42931 # total number of misses
dl1.replacements        38835 # total number of replacements
dl1.writebacks          32284 # total number of writebacks
dl1.invalidations       0 # total number of invalidations
dl1.miss_rate           0.0007 # miss rate (i.e., misses/ref)
dl1.repl_rate           0.0006 # replacement rate (i.e., repls/ref)
dl1.wb_rate             0.0005 # writeback rate (i.e., wrbks/ref)
dl1.inv_rate            0.0000 # invalidation rate (i.e., invs/ref)
```