

ECE 469
Project 3 Part A
Tamanna Ravi Rupani
665679988
Niranjani Venkatesan
675456032

Workload report: How many hours have you spent on this part? Which activity takes the most significant amount of time? This will not affect your grade (unless omitted).

Topic	No of hours
Understanding and studying the FSM and Control Word	1.5
Understanding Multi-Cycle MIPS	2
Execution of Controller in SystemVerilog and debugging errors	2
Execution of Datapath in SystemVerilog and debugging errors	2
Quartus Part	0.5
Report Writing	1.5
Total	9.5

Understanding the Multicycle MIPS, writing the code accordingly took longer time

A completed Main Decoder output table (Table 4).

State (Name)	PC Write	Mem Write	IR Write	Reg Write	ALU SrcA	Branch	Interrupt	MemtoReg	RegDst	ALUSrcB[1:0]	PCSrc[1:0]	ALUOp[1:0]	FSM Control Word
0 (Fetch)	1	0	1	0	0	0	0	0	0	01	00	00	0x5010
1 (Decode)	0	0	0	0	0	0	0	0	0	11	00	00	0x0030
2 (MemAdr)	0	0	0	0	1	0	0	0	0	10	00	00	0x0420
3 (MemRd)	0	0	0	0	0	0	1	0	0	00	00	00	0x0100
4 (MemWB)	0	0	0	1	0	0	0	1	0	00	00	00	0x0880
5 (MemWr)	0	1	0	0	0	0	1	0	0	00	00	00	0x2100
6 (RtypeEx)	0	0	0	0	1	0	0	0	0	00	00	10	0x0402
7 (RtypeWB)	0	0	0	1	0	0	0	0	1	00	00	00	0x0840
8 (BeqEx)	0	0	0	0	1	1	0	0	0	00	01	01	0x0605
9 (AddiEx)	0	0	0	0	1	0	0	0	0	10	00	00	0x0420
10 (AddiWB)	0	0	0	1	0	0	0	0	0	00	00	00	0x0800
11 (JEx)	1	0	0	0	0	0	0	0	0	00	10	00	0x4008

The SystemVerilog for your controller, maindec, and aludec modules

Controller:

```
C:\intelFPGA_lite\17.1\modelsim_ase\win32a64em\YDL\controller.sv - Default
Ln#
1 module controller(input logic clk, reset,
2   input logic [5:0] op, funct,
3   input logic zero,
4   output logic poen, memwrite, irwrite, regwrite,
5   output logic alusrcra, lord, memtoreg, regdst,
6   output logic [1:0] alusrcb, psrcr,
7   output logic [2:0] alucontrol);
8
9   logic [1:0] aluop;
10  logic branch, powrite;
11  logic skip;
12  logic [3:0] state;
13  logic [14:0] controls;
14
15  //Main Decoder and ALU Decoder subunits.
16  maindec md(clk, reset, op, powrite, memwrite, irwrite, regwrite, alusrcra, branch, lord, memtoreg, regdst, alusrcb, psrcr, aluop, state, controls);
17
18  aludec ad(funct, aluop, alucontrol);
19
20  assign skip = branch & zero;
21
22  assign poen = powrite ? powrite : skip;
23
24 endmodule
25
26 module maindec(input logic clk, reset,
27   input logic [5:0] op,
28   output logic powrite, memwrite, irwrite, regwrite,
29   output logic alusrcra, branch, lord, memtoreg, regdst,
30   output logic [1:0] alusrcb, psrcr,
31   output logic [1:0] aluop, output logic [3:0] state, output logic [14:0] controls);
32
33
34
35
36
37
38
39
40
41
42
43
44
45
46
47
48
49
50
51
52
53
54
55
56
57
58
59
60
61
62
63
64
65
66
67
68
69
70
71
72
73
74
75
76
77
78
79
80
81
82
83
84
85
86
87
88
89
90
91
92
93
94
95
96
97
98
99
100
101
102
103
104
105
106
107
108
109
110
111
112
113
114
115
116
117
118
119
120
121
122
123
124
125
126
127
128
129
130
131
132
133
134
135
136
137
138
139
140
141
142
143
144
145
146
147
148
149
150
151
152
153
154
155
156
157
158
159
160
161
162
163
164
165
166
167
168
169
170
171
172
173
174
175
176
177
178
179
180
181
182
183
184
185
186
187
188
189
190
191
192
193
194
195
196
197
198
199
200
201
202
203
204
205
206
207
208
209
210
211
212
213
214
215
216
217
218
219
220
221
222
223
224
225
226
227
228
229
230
231
232
233
234
235
236
237
238
239
240
241
242
243
244
245
246
247
248
249
250
251
252
253
254
255
256
257
258
259
260
261
262
263
264
265
266
267
268
269
270
271
272
273
274
275
276
277
278
279
280
281
282
283
284
285
286
287
288
289
290
291
292
293
294
295
296
297
298
299
300
301
302
303
304
305
306
307
308
309
310
311
312
313
314
315
316
317
318
319
320
321
322
323
324
325
326
327
328
329
330
331
332
333
334
335
336
337
338
339
340
341
342
343
344
345
346
347
348
349
350
351
352
353
354
355
356
357
358
359
360
361
362
363
364
365
366
367
368
369
370
371
372
373
374
375
376
377
378
379
380
381
382
383
384
385
386
387
388
389
390
391
392
393
394
395
396
397
398
399
400
401
402
403
404
405
406
407
408
409
410
411
412
413
414
415
416
417
418
419
420
421
422
423
424
425
426
427
428
429
430
431
432
433
434
435
436
437
438
439
440
441
442
443
444
445
446
447
448
449
450
451
452
453
454
455
456
457
458
459
460
461
462
463
464
465
466
467
468
469
470
471
472
473
474
475
476
477
478
479
480
481
482
483
484
485
486
487
488
489
490
491
492
493
494
495
496
497
498
499
500
501
502
503
504
505
506
507
508
509
510
511
512
513
514
515
516
517
518
519
520
521
522
523
524
525
526
527
528
529
530
531
532
533
534
535
536
537
538
539
540
541
542
543
544
545
546
547
548
549
550
551
552
553
554
555
556
557
558
559
560
561
562
563
564
565
566
567
568
569
570
571
572
573
574
575
576
577
578
579
580
581
582
583
584
585
586
587
588
589
590
591
592
593
594
595
596
597
598
599
600
601
602
603
604
605
606
607
608
609
610
611
612
613
614
615
616
617
618
619
620
621
622
623
624
625
626
627
628
629
630
631
632
633
634
635
636
637
638
639
640
641
642
643
644
645
646
647
648
649
650
651
652
653
654
655
656
657
658
659
660
661
662
663
664
665
666
667
668
669
670
671
672
673
674
675
676
677
678
679
680
681
682
683
684
685
686
687
688
689
690
691
692
693
694
695
696
697
698
699
700
701
702
703
704
705
706
707
708
709
710
711
712
713
714
715
716
717
718
719
720
721
722
723
724
725
726
727
728
729
730
731
732
733
734
735
736
737
738
739
740
741
742
743
744
745
746
747
748
749
750
751
752
753
754
755
756
757
758
759
760
761
762
763
764
765
766
767
768
769
770
771
772
773
774
775
776
777
778
779
780
781
782
783
784
785
786
787
788
789
790
791
792
793
794
795
796
797
798
799
800
801
802
803
804
805
806
807
808
809
810
811
812
813
814
815
816
817
818
819
820
821
822
823
824
825
826
827
828
829
830
831
832
833
834
835
836
837
838
839
840
841
842
843
844
845
846
847
848
849
850
851
852
853
854
855
856
857
858
859
860
861
862
863
864
865
866
867
868
869
870
871
872
873
874
875
876
877
878
879
880
881
882
883
884
885
886
887
888
889
890
891
892
893
894
895
896
897
898
899
900
901
902
903
904
905
906
907
908
909
910
911
912
913
914
915
916
917
918
919
920
921
922
923
924
925
926
927
928
929
930
931
932
933
934
935
936
937
938
939
940
941
942
943
944
945
946
947
948
949
950
951
952
953
954
955
956
957
958
959
960
961
962
963
964
965
966
967
968
969
970
971
972
973
974
975
976
977
978
979
980
981
982
983
984
985
986
987
988
989
990
991
992
993
994
995
996
997
998
999
1000
1001
1002
1003
1004
1005
1006
1007
1008
1009
1010
1011
1012
1013
1014
1015
1016
1017
1018
1019
1020
1021
1022
1023
1024
1025
1026
1027
1028
1029
1030
1031
1032
1033
1034
1035
1036
1037
1038
1039
1040
1041
1042
1043
1044
1045
1046
1047
1048
1049
1050
1051
1052
1053
1054
1055
1056
1057
1058
1059
1060
1061
1062
1063
1064
1065
1066
1067
1068
1069
1070
1071
1072
1073
1074
1075
1076
1077
1078
1079
1080
1081
1082
1083
1084
1085
1086
1087
1088
1089
1090
1091
1092
1093
1094
1095
1096
1097
1098
1099
1100
1101
1102
1103
1104
1105
1106
1107
1108
1109
1110
1111
1112
1113
1114
1115
1116
1117
1118
1119
1120
1121
1122
1123
1124
1125
1126
1127
1128
1129
1130
1131
1132
1133
1134
1135
1136
1137
1138
1139
1140
1141
1142
1143
1144
1145
1146
1147
1148
1149
1150
1151
1152
1153
1154
1155
1156
1157
1158
1159
1160
1161
1162
1163
1164
1165
1166
1167
1168
1169
1170
1171
1172
1173
1174
1175
1176
1177
1178
1179
1180
1181
1182
1183
1184
1185
1186
1187
1188
1189
1190
1191
1192
1193
1194
1195
1196
1197
1198
1199
1200
1201
1202
1203
1204
1205
1206
1207
1208
1209
1210
1211
1212
1213
1214
1215
1216
1217
1218
1219
1220
1221
1222
1223
1224
1225
1226
1227
1228
1229
1230
1231
1232
1233
1234
1235
1236
1237
1238
1239
1240
1241
1242
1243
1244
1245
1246
1247
1248
1249
1250
1251
1252
1253
1254
1255
1256
1257
1258
1259
1260
1261
1262
1263
1264
1265
1266
1267
1268
1269
1270
1271
1272
1273
1274
1275
1276
1277
1278
1279
1280
1281
1282
1283
1284
1285
1286
1287
1288
1289
1290
1291
1292
1293
1294
1295
1296
1297
1298
1299
1300
1301
1302
1303
1304
1305
1306
1307
1308
1309
1310
1311
1312
1313
1314
1315
1316
1317
1318
1319
1320
1321
1322
1323
1324
1325
1326
1327
1328
1329
1330
1331
1332
1333
1334
1335
1336
1337
1338
1339
1340
1341
1342
1343
1344
1345
1346
1347
1348
1349
1350
1351
1352
1353
1354
1355
1356
1357
1358
1359
1360
1361
1362
1363
1364
1365
1366
1367
1368
1369
1370
1371
1372
1373
1374
1375
1376
1377
1378
1379
1380
1381
1382
1383
1384
1385
1386
1387
1388
1389
1390
1391
1392
1393
1394
1395
1396
1397
1398
1399
1400
1401
1402
1403
1404
1405
1406
1407
1408
1409
1410
1411
1412
1413
1414
1415
1416
1417
1418
1419
1420
1421
1422
1423
1424
1425
1426
1427
1428
1429
1430
1431
1432
1433
1434
1435
1436
1437
1438
1439
1440
1441
1442
1443
1444
1445
1446
1447
1448
1449
1450
1451
1452
1453
1454
1455
1456
1457
1458
1459
1460
1461
1462
1463
1464
1465
1466
1467
1468
1469
1470
1471
1472
1473
1474
1475
1476
1477
1478
1479
1480
1481
1482
1483
1484
1485
1486
1487
1488
1489
1490
1491
1492
1493
1494
1495
1496
1497
1498
1499
1500
1501
1502
1503
1504
1505
1506
1507
1508
1509
1510
1511
1512
1513
1514
1515
1516
1517
1518
1519
1520
1521
1522
1523
1524
1525
1526
1527
1528
1529
1530
1531
1532
1533
1534
1535
1536
1537
1538
1539
1540
1541
1542
1543
1544
1545
1546
1547
1548
1549
1550
1551
1552
1553
1554
1555
1556
1557
1558
1559
1560
1561
1562
1563
1564
1565
1566
1567
1568
1569
1570
1571
1572
1573
1574
1575
1576
1577
1578
1579
1580
1581
1582
1583
1584
1585
1586
1587
1588
1589
1590
1591
1592
1593
1594
1595
1596
1597
1598
1599
1600
1601
1602
1603
1604
1605
1606
1607
1608
1609
1610
1611
1612
1613
1614
1615
1616
1617
1618
1619
1620
1621
1622
1623
1624
1625
1626
1627
1628
1629
1630
1631
1632
1633
1634
1635
1636
1637
1638
1639
1640
1641
1642
1643
1644
1645
1646
1647
1648
1649
1650
1651
1652
1653
1654
1655
1656
1657
1658
1659
1660
1661
1662
1663
1664
1665
1666
1667
1668
1669
1670
1671
1672
1673
1674
1675
1676
1677
1678
1679
1680
1681
1682
1683
1684
1685
1686
1687
1688
1689
1690
1691
1692
1693
1694
1695
1696
1697
1698
1699
1700
1701
1702
1703
1704
1705
1706
1707
1708
1709
1710
1711
1712
1713
1714
1715
1716
1717
1718
1719
1720
1721
1722
1723
1724
1725
1726
1727
1728
1729
1730
1731
1732
1733
1734
1735
1736
1737
1738
1739
1740
1741
1742
1743
1744
1745
1746
1747
1748
1749
1750
1751
1752
1753
1754
1755
1756
1757
1758
1759
1760
1761
1762
1763
1764
1765
1766
1767
1768
1769
1770
1771
1772
1773
1774
1775
1776
1777
1778
1779
1780
1781
1782
1783
1784
1785
1786
1787
1788
1789
1790
1791
1792
1793
1794
1795
1796
1797
1798
1799
1800
1801
1802
1803
1804
1805
1806
1807
1808
1809
1810
1811
1812
1813
1814
1815
1816
1817
1818
1819
1820
1821
1822
1823
1824
1825
1826
1827
1828
1829
1830
1831
1832
1833
1834
1835
1836
1837
1838
1839
1840
1841
1842
1843
1844
1845
1846
1847
1848
1849
1850
1851
1852
1853
1854
1855
1856
1857
1858
1859
1860
1861
1862
1863
1864
1865
1866
1867
1868
1869
1870
1871
1872
1873
1874
1875
1876
1877
1878
1879
1880
1881
1882
1883
1884
1885
1886
1887
1888
1889
1890
1891
1892
1893
1894
1895
1896
1897
1898
1899
1900
1901
1902
1903
1904
1905
1906
1907
1908
1909
1910
1911
1912
1913
1914
1915
1916
1917
1918
1919
1920
1921
1922
1923
1924
1925
1926
1927
1928
1929
1930
1931
1932
1933
1934
1935
1936
1937
1938
1939
1940
1941
1942
1943
1944
1945
1946
1947
1948
1949
1950
1951
1952
1953
1954
1955
1956
1957
1958
1959
1960
1961
1962
1963
1964
1965
1966
1967
1968
1969
1970
1971
1972
1973
1974
1975
1976
1977
1978
1979
1980
1981
1982
1983
1984
1985
1986
1987
1988
1989
1990
1991
1992
1993
1994
1995
1996
1997
1998
1999
2000
2001
2002
2003
2004
2005
2006
2007
2008
2009
2010
2011
2012
2013
2014
2015
2016
2017
2018
2019
2020
2021
2022
2023
2024
2025
2026
2027
2028
2029
2030
2031
2032
2033
2034
2035
2036
2037
2038
2039
2040
2041
2042
2043
2044
2045
2046
2047
2048
2049
2050
2051
2052
2053
2054
2055
2056
2057
2058
2059
2060
2061
2062
2063
2064
2065
2066
2067
2068
2069
2070
2071
2072
2073
2074
2075
2076
2077
2078
2079
2080
2081
2082
2083
2084
2085
2086
2087
2088
2089
2090
2091
2092
2093
2094
2095
2096
2097
2098
2099
2100
2101
2102
2103
2104
2105
2106
2107
2108
2109
2110
2111
2112
2113
2114
2115
2116
2117
2118
2119
2120
2121
2122
2123
2124
2125
2126
2127
2128
2129
2130
2131
2132
2133
2134
2135
2136
2137
2138
2139
2140
2141
2142
2143
2144
2145
2146
2147
2148
2149
2150
2151
2152
2153
2154
2155
2156
2157
2158
2159
2160
2161
2162
2163
2164
2165
2166
2167
2168
2169
2170
2171
2172
2173
2174
2175
2176
2177
2178
2179
2180
2181
2182
2183
2184
2185
2186
2187
2188
2189
2190
2191
2192
2193
2194
2195
2196
2197
2198
2199
2200
2201
2202
2203
2204
2205
2206
2207
2208
2209
2210
2211
2212
2213
2214
2215
2216
2217
2218
2219
2220
2221
2222
2223
2224
2225
2226
2227
2228
2229
2230
2231
2232
2233
2234
2235
2236
2237
2238
2239
2240
2241
2242
2243
2244
2245
2246
2247
2248
2249
2250
2251
2252
2253
2254
2255
2256
2257
2258
2259
2260
2261
2262
2263
2264
2265
2266
2267
2268
2269
2270
2271
2272
2273
2274
2275
2276
2277
2278
2279
2280
2281
2282
2283
2284
2285
2286
2287
2288
2289
2290
2291
2292
2293
2294
2295
2296
2297
2298
2299
2300
2301
2302
2303
2304
2305
2306
2307
2308
2309
2310
2311
2312
2313
2314
2315
2316
2317
2318
2319
2320
2321
2322
2323
2324
2325
2326
2327
2328
2329
2330
2331
2332
2333
2334
2335
2336
2337
2338
2339
2340
2341
2342
2343
2344
2345
2346
2347
2348
2349
2350
2351
2352
2353
2354
2355
2356
2357
2358
2359
2360
2361
2362
2363
2364
2365
2366
2367
2368
2369
2370
2371
2372
2373
2374
2375
2376
2377
2378
2379
2380
2381
2382
2383
2384
2385
2386
2387
2388
2389
2390
2391
2392
2393
2394
2395
2396
2397
2398
2399
2400
2401
2402
2403
2404
2405
2406
2407
2408
2409
2410
2411
2412
2413
2414
2415
2416
2417
2418
2419
2420
2421
2422
2423
2424
2425
2426
2427
2428
2429
2430
2431
2432
2433
2434
2435
2436
2437
2438
2439
2440
2441
2442
2443
2444
2445
2446
2447
2448
2449
2450
2451
2452
2453
2454
2455
2456
2457
2458
2459
2460
2461
2462
2463
2464
2465
2466
2467
2468
2469
2470
2471
2472
2473
2474
2475
2476
2477
2478
2479
2480
2481
2482
2483
2484
2485
2486
2487
2488
2489
2490
2491
2492
2493
2494
2495
2496
2497
2498
2499
2500
2501
2502
2503
2504
2505
2506
2507
2508
2509
2510
2511
2512
2513
2514
2515
2516
2517
2518
2519
2520
2521
2522
2523
2524
2525
2526
2527
2528
2529
2530
2531
2532
2533
2534
2535
2536
2537
2538
2539
2540
2541
2542
2543
2544
2545
2546
2547
2548
2549
2550
2551
2552
2553
2554
2555
2556
2557
2558
2559
2560
2561
2562
2563
2564
2565
2566
2567
2568
2569
2570
2571
2572
2573
2574
2575
2576
2577
2578
2579
2580
2581
2582
2583
2584
2585
2586
2587
2588
2589
2590
2591
2592
2593
2594
2595
2596
2597
2598
2599

```

```
C:\intelFPGA_lite\17.1\modelsim_ase\win32aocem\ydl\controller.sv - Default
Ln#
77      default: nextstate = 4'hx; // should never happen
78    endcase
79    MEMRD: nextstate = MEMWB;
80    MEMWB: nextstate = FETCH;
81    MEMWR: nextstate = FETCH;
82    RIYPEEX: nextstate = RIYPEWB;
83    RIYPEWB: nextstate = FETCH;
84    BEQEX: nextstate = FETCH;
85    ADDIEX: nextstate = ADDIWB;
86    ADDIWB: nextstate = FETCH;
87    JEX: nextstate = FETCH;
88    default: nextstate = 4'hx; // should never happen
89  endcase
90
91  //output logic
92  assign {pwrite, memwrite, irwrite, regwrite, alusrc, branch, lord, memstore, regdst, alusrcb, pcsrc, aluop} = controls;
93
94  always_comb
95  case (state)
96    FETCH: controls = 15'h5010;
97    DECODE: controls = 15'h0030;
98    MEMADDR: controls = 15'h0420;
99    MEMRD: controls = 15'h0100;
100   MEMWB: controls = 15'h0880;
101   MEMWR: controls = 15'h2100;
102   RIYPEEX: controls = 15'h0402;
103   RIYPEWB: controls = 15'h0840;
104   BEQEX: controls = 15'h0605;
105   ADDIEX: controls = 15'h0420;
106   ADDIWB: controls = 15'h0800;
107   JEX: controls = 15'h4008;
108   default: controls = 15'hxxxx; // should never happen
  endcase
List  multi_testbench.sv  controller.sv  multi_mips.sv
```

AluDec:

```
C:\intelFPGA_lite\17.1\modelsim_ase\win32aocem\ydl\controller.sv - Default
Ln#
113  module aludec(input logic [5:0] funct,
114               input logic [1:0] aluop,
115               output logic [2:0] alucontrol);
116
117    always_comb
118    case (aluop)
119      2'b00: alucontrol <= 3'b010; // add (for lw/sw/addi)
120      2'b01: alucontrol <= 3'b110; // sub (for beq)
121      default: case (funct) // R-type instructions
122        6'b100000: alucontrol <= 3'b010; // add
123        6'b100010: alucontrol <= 3'b110; // sub
124        6'b100100: alucontrol <= 3'b000; // and
125        6'b100101: alucontrol <= 3'b001; // or
126        6'b101010: alucontrol <= 3'b111; // slt
127        default: alucontrol <= 3'bxxx; // should never happen
128      endcase
129    endcase
130
131  endmodule
132
133
```

Your controllertest testbench.

```
133 module controller_testbench();
134   logic clk;
135   logic reset;
136   logic [5:0] op, funct;
137   logic zero;
138   logic pccn, memwrite, irwrite, regwrite;
139   logic alusrcb, ldrd, memtoreg, regdst;
140   logic [1:0] alusrcb, pccr;
141   logic [2:0] alucontrol;
142   controller dut (clk, reset, op, funct, zero, pccn, memwrite, irwrite, regwrite, alusrcb, ldrd, memtoreg, regdst, alusrcb, pccr, alucontrol);
143   initial
144   begin
145     reset <= 1; # 5; reset <= 0;
146   end
147   always
148   begin
149     clk <= 1; # 5; clk <= 0; # 5;
150   end
151   initial
152   begin
153     op = 6'b000000; funct = 6'b100000; zero = 0; #40;
154     op = 6'b000000; funct = 6'b100010; zero = 0; #40;
155     op = 6'b000000; funct = 6'b100100; zero = 0; #40;
156     op = 6'b000000; funct = 6'b100101; zero = 0; #40;
157     op = 6'b000000; funct = 6'b101010; zero = 0; #40;
158     op = 6'b100011; funct = 6'b000000; zero = 0; #50;
159     op = 6'b101011; funct = 6'b000000; zero = 0; #40;
160     op = 6'b000100; funct = 6'b000000; zero = 0; #30;
161     op = 6'b000100; funct = 6'b000000; zero = 1; #30;
162     op = 6'b001000; funct = 6'b000000; zero = 0; #40;
163     op = 6'b000010; funct = 6'b000000; zero = 0;
164   end
165 endmodule
```

Yes, it matches to our expectations and we have received expected outputs.

A completed copy of Table 5 indicating the expected outcome of running the test program.

Cycle	Reset	PC	Instr	(FSM) State	SrcA	Src B	AluResult	Zero	FSM Control Word
1	1	00	0	0	0	04	04	0	5010
2	0	04	addi 20020005	1	04	x	x	0	0030
3	0	04	addi 20020005	9	00	05	05	0	0420
4	0	04	addi 20020005	10	x	x	x	0	0800
5	0	04	addi 20020005	0	04	04	08	0	5010
6	0	08	addi 2003000c	1	08	x	x	0	0030
7	0	08	addi 2003000c	9	00	0C	0C	0	0420
8	0	08	addi 2003000c	10	x	x	x	0	0800
9	0	08	addi 2003000c	0	08	04	0C	0	5010
10	0	0C	addi 2067fff7	1	0C	x	x	0	0030
11	0	0C	addi 2067fff7	9	0C	fff7	03	0	0420
12	0	0C	addi 2067fff7	10	x	x	x	0	0800
13	0	0C	addi 2067fff7	0	0C	04	10	0	5010
14	0	10	or 00e22025	1	10	x	x	0	0030
15	0	10	or 00e22025	6	03	05	07	0	0402
16	0	10	or 00e22025	7	x	x	x	0	0840
17	0	10	or 00e22025	0	10	04	14	0	5010
18	0	14	and 00642824	1	14	x	x	0	0030
19	0	14	and 00642824	6	0C	07	04	0	0402
20	0	14	and 00642824	7	x	x	x	0	0840
21	0	14	and 00642824	0	14	04	18	0	5010
22	0	18	add 00a42820	1	18	x	x	0	0030
23	0	18	add 00a42820	6	04	07	0B	0	0402
24	0	18	add 00a42820	7	x	x	x	0	0840
25	0	18	add 00a42820	0	18	04	1C	0	5010
26	0	1C	beq 10a7000a	1	1C	x	x	0	0030
27	0	1C	beq 10a7000a	8	0B	03	08	0	0605
28	0	1C	beq 10a7000a	0	1C	04	20	0	5010
29	0	20	slt 0064202a	1	20	x	x	0	0030
30	0	20	slt 0064202a	6	1C	07	0	1	0402
31	0	20	slt 0064202a	7	x	x	x	0	0840
32	0	20	slt 0064202a	0	20	04	24	0	5010
33	0	24	beq 10800001	1	24	x	x	0	0030
34	0	24	beq 10800001	8	00	00	00	1	0605
35	0	24	beq 10800001	0	24	08	2C	0	5010
36	0	2C	slt 00e2202a	1	2C	x	x	0	0030
37	0	2C	slt 00e2202a	6	03	05	01	0	0402
38	0	2C	slt 00e2202a	7	x	x	x	0	0840

39	0	2C	slt 00e2202a	0	28	04	30	0	5010
40	0	30	add 00853820	1	30	x	x	0	0030
41	0	30	add 00853820	6	01	0B	0C	0	0402
42	0	30	add 00853820	7	x	x	x	0	0840
43	0	30	add 00853820	0	30	04	34	0	5010
44	0	34	sub 00e23822	1	34	x	x	0	0030
45	0	34	sub 00e23823	6	0C	05	07	0	0402
46	0	34	sub 00e23824	7	x	x	x	0	0840
47	0	34	sub 00e23825	0	34	04	38	0	5010
48	0	38	sw ac670044	1	38	x	x	0	0030
49	0	38	sw ac670044	2	0C	44	50	0	0420
50	0	38	sw ac670044	5	x	x	x	0	2100
51	0	38	sw ac670044	0	38	04	3C	0	5010
52	0	3C	lw 8c020050	1	3C	x	x	x	0030
53	0	3C	lw 8c020050	2	00	50	50	0	0420
54	0	3C	lw 8c020050	3	x	x	x	0	0100
55	0	3C	lw 8c020050	4	x	x	x	0	0880
56	0	3C	lw 8c020050	0	3C	04	40	0	5010
57	0	40	j 08000011	1	40	x	x	x	0030
58	0	40	j 08000011	11	40	x	x	x	4008
59	0	40	j 08000011	0	44	04	48	0	5010
60	0	48	sw ac020054	1	48	x	x	x	0030
61	0	48	sw ac020054	2	00	54	54	0	0420
62	0	48	sw ac020054	5	x	x	x	0	2100

SystemVerilog code of the datapath

```
module datapath(input logic clk, reset,
input logic pcen, irwrite, regwrite,
input logic alusrca, iord, memtoreg, regdst,
input logic [1:0] alusrcb, pcsrc,
input logic [2:0] alucontrol,
output logic [5:0] op, funct,
output logic zero,
output logic [31:0] adr, writedata,
input logic [31:0] readdata);

//Internal signals of the datapath module.

logic [4:0] writereg;
logic [31:0] pcnext, pc;
logic [31:0] instr, data, srca, srcb;
logic [31:0] a;
logic [31:0] aluresult, aluout;
logic [31:0] signimm; // the sign-extended immediate
logic [31:0] signimmsh; // the sign-extended immediate shifted left by 2
logic [31:0] wd3, rd1, rd2;
logic [31:0] jsignimm;

//op and funct fields to controller
assign op = instr[31:26];
assign funct = instr[5:0];

flopr #(32) pcreg(clk, reset,pcen, pcnext, pc);

mux2 #(32) adrchoose(pc, aluout, iord, adr);
```

```
flop1 #(32) instrchoose(clk, reset, irwrite, readdata, instr);
```

```
flop #(32) datachoose(clk, reset, readdata, data);
```

```
mux2 #(5) wrmux(instr[20:16], instr[15:11], regdst, writereg);
```

```
mux2 #(32) resmux(aluout, data, memtoreg, wd3);
```

```
regfile rf(clk, regwrite, instr[25:21], instr[20:16], writereg, wd3, rd1, rd2);
```

```
flop2 #(32) srcreg(clk, reset, rd1, rd2, a, writedata);
```

```
mux2 #(32) srcchoice(pc, a, alusrca, srca);
```

```
signext se(instr[15:0], signimm);
```

```
sl2 immsh(signimm, signimmsh);
```

```
mux4 #(32) srcbchoice (writedata, 32'b100, signimm, signimmsh, alusrcb, srcb);
```

```
aluproj alu(srca, srcb, alucontrol, aluresult, zero);
```

```
flop #(32) aluchoose(clk, reset, aluresult, aluout);
```

```
jsignim jsi(instr, jsignimm);
```

```
mux3 aluchoice(aluresult, aluout, jsignimm, pcsrc, pcnext);
```

```
endmodule
```

```
//-----Register File-----
```

```
module regfile(input logic clk,  
input logic we3,  
input logic [4:0] ra1, ra2, wa3,  
input logic [31:0] wd3,  
output logic [31:0] rd1, rd2);
```

```
logic [31:0] rf[31:0];
```

```
always_ff @(posedge clk)  
if (we3  
rf[wa3] <= wd3;
```

```
assign rd1=(ra1 !=0) ? rf[ra1] : 0;  
assign rd2=(ra2 !=0) ? rf[ra2] : 0;
```

```
endmodule
```

```
//-----
```

```
//-----Alu-----
```

```
module aluproj(input logic [31:0] a, b,  
input logic [2:0] F,  
output logic [31:0] Y,  
output logic zero);  
logic [31:0] S , B;
```

```
assign B = F[2]? ~b:b;
```

```
assign S = a + B + F[2];
```

```

always_comb
case(F[1:0])
2'b00 : Y = a & B;
2'b01 : Y = a | B;
2'b10 : Y = S;
2'b11 : Y = {31'b0,S[31]};
endcase

```

```

always_comb
if ( Y === 32'b0)
zero = 1;
else zero =0;

```

```

endmodule

//-----
//-----To store values into register-----
module flop #(parameter WIDTH=8) (input logic clk, reset,
input logic [WIDTH-1:0] d,
output logic [WIDTH-1:0] q);

always_ff @(posedge clk, posedge reset)
if (reset) q <= 0;
else q <= d;

endmodule

//-----
//-----Register to save A and B values-----
module flop2 #(parameter WIDTH=8) (input logic clk, reset,
input logic [WIDTH-1:0] d1, d2,

```

```
output logic [WIDTH-1:0] q1,q2);
```

```
always_ff @(posedge clk, posedge reset)
```

```
if (reset)
```

```
begin
```

```
q1 <= 0;
```

```
q2 <= 0;
```

```
end
```

```
else
```

```
begin
```

```
q1 <= d1;
```

```
q2 <= d2;
```

```
end
```

```
endmodule
```

```
//-----
```

```
//----- To store pc value only when en is 1-----
```

```
module flopr #(parameter WIDTH=8) (input logic clk, reset, pcen,
```

```
input logic [WIDTH-1:0] d,
```

```
output logic [WIDTH-1:0] q);
```

```
always_ff @(posedge clk, posedge reset)
```

```
if (reset) q <= 0;
```

```
else if (pcen) q <= d;
```

```
endmodule
```

```
//-----
```

```
//-----Sign extend for immediate values-----
```

```
module signext(input logic [15:0] a,
```

```
output logic [31:0] y);
```

```
assign y={{16{a[15]}}, a};
```

```
endmodule
```

```
//-----
```

```
//-----Left shift for beq instruction-----
```

```
module sl2(input logic [31:0] a,
```

```
output logic [31:0] y);
```

```
assign y={a[29:0], 2'b00};
```

```
endmodule
```

```
//-----
```

```
//-----Left shift for Jump instruction-----
```

```
module jsignim(input logic [31:0] a,
```

```
output logic [31:0] y);
```

```
assign y={a[31:28], {a[25:0], 2'b00}};
```

```
endmodule
```

```
//-----
```

```
//-----MUX for 2 choices-----
```

```
module mux2 #(parameter WIDTH=8) (input logic [WIDTH-1:0] d0, d1,
```

```
input logic s,
```

```
output logic [WIDTH-1:0] y);
```

```
assign y=s ? d1 : d0;
```

```
endmodule
```

```
//-----
```

```
//-----MUX for 3 choices-----
```

```
module mux3 #(parameter WIDTH = 8) (input logic [WIDTH-1:0] d0, d1, d2,  
input logic [1:0] s,  
output logic [WIDTH-1:0] y);
```

```
assign #1 y = s[1] ? d2 : (s[0] ? d1 : d0);
```

```
endmodule
```

```
//-----
```

```
//-----Mux for 4 choices-----
```

```
module mux4 #(parameter WIDTH = 8) (input logic [WIDTH-1:0] d0, d1, d2, d3,  
input logic [1:0] s,  
output logic [WIDTH-1:0] y);
```

```
always_comb
```

```
case(s)
```

```
2'b00: y = d0;
```

```
2'b01: y = d1;
```

```
2'b10: y = d2;
```

```
2'b11: y = d3;
```

```
endcase
```

```
endmodule
```

```
//-----
```

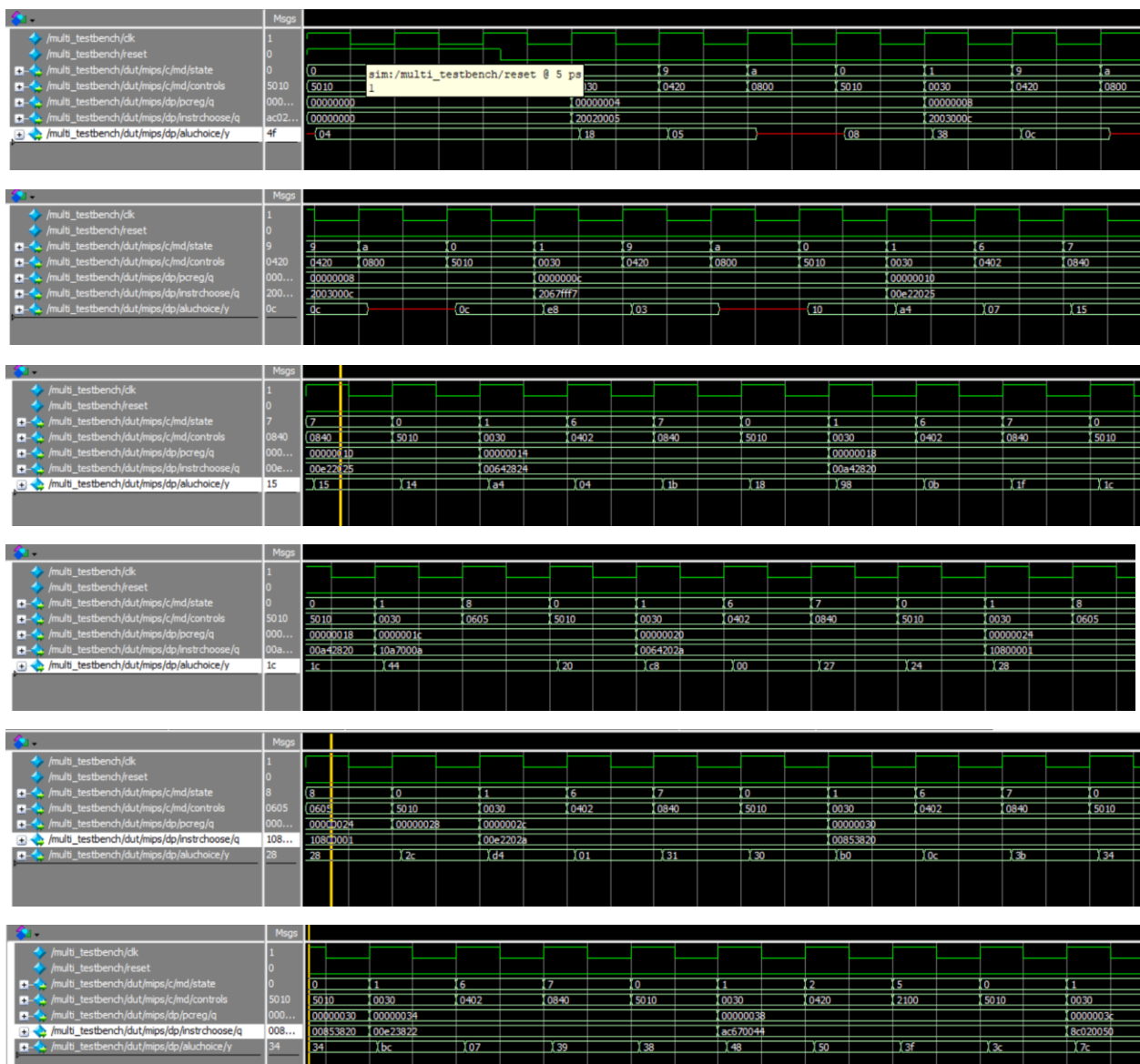
Simulation waveforms of the processor showing *CLK*, *Reset*, *state*, *PC*, *instr*, and *ALUResult* in this order while running the test program. As always, output the values in hex (or decimal if that is more readable) and make sure they are readable. Do the results match your expectations? Does the program indicate Simulation Succeeded?

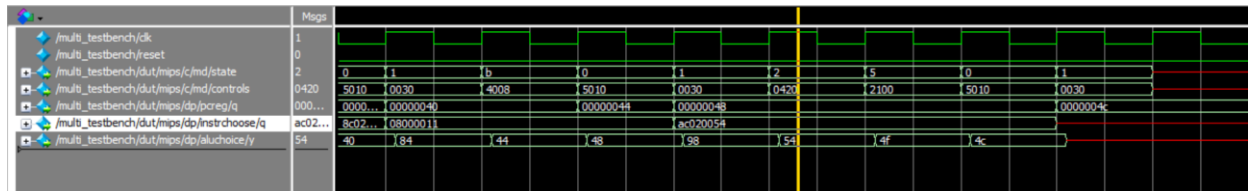
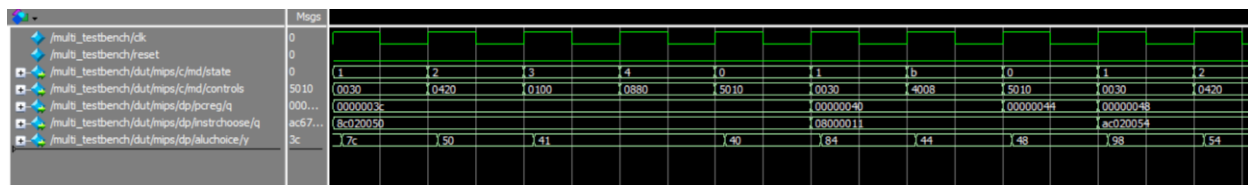
Note: pcreg/q = PC

Instrchoose/q = instruction

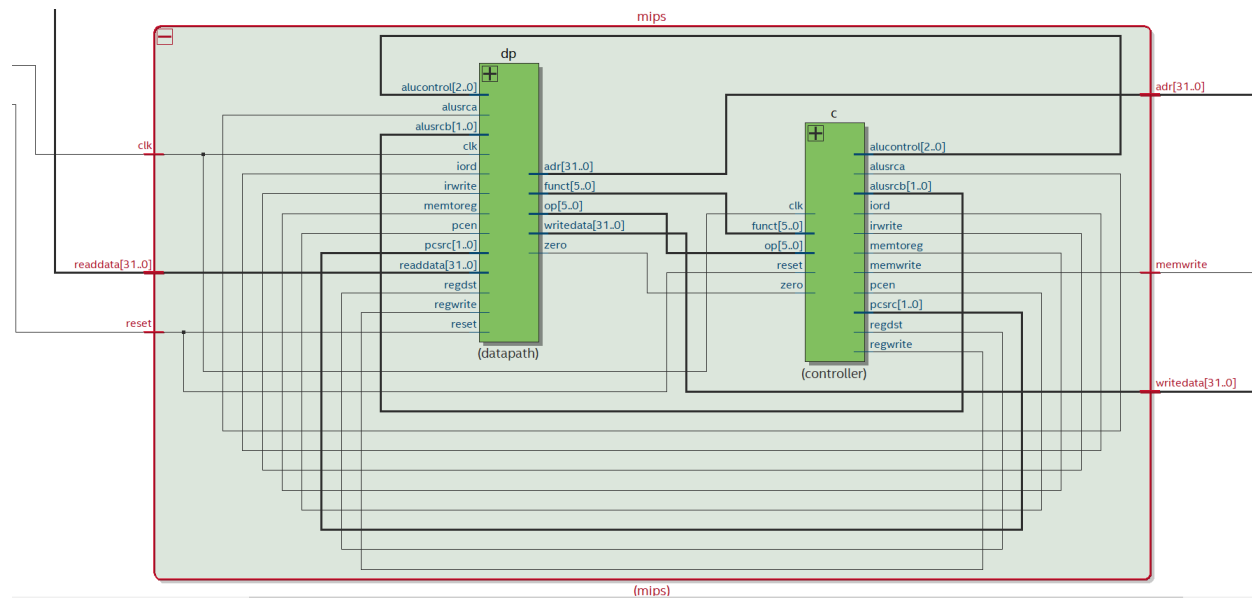
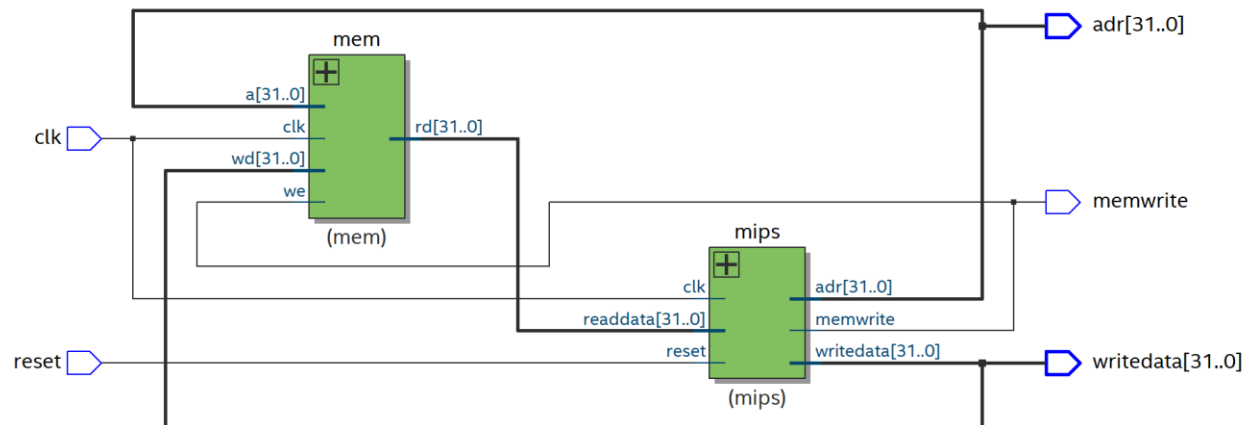
Aluchoice/y = aluout

Yes, it matches to our expectations and we have received expected outputs in the waveform as expected from the table 5.





RTL view from Quartus' compilation result of your MIPS processor.



Aludec



The screenshot shows a C# code editor with a light blue background. A line of code is highlighted in yellow: `int[] micosres(2,0);`. A red cursor is positioned at the end of this line. A red rectangular box is drawn around the code, and a red line extends from the box to the right, ending at the edge of the editor window.