



RK3588

Hardware

Design Guide

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Preface

Overview

This document mainly introduces the key points and precautions of RK3588 processor hardware design, aiming to help RK customers shorten the product design cycle, improve product design stability and reduce failure rate. Please refer to the requirements of this guide for hardware design and try to use the relevant core templates released by RK. If changes are required for special reasons, please strictly follow the high-speed digital circuit design requirements and RK product PCB design requirements.

conduct.

Chip model

The chip model corresponding to this document is: RK3588

Applicable Targets

This document is primarily intended for the following engineers:

ÿ Hardware development engineer

ÿ Layout Engineer ÿ

Technical Support Engineer

ÿ Test Engineer

Change Log

The revision history accumulates the descriptions of each document update. The latest version of the document contains the updated contents of all previous document versions.

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1 System Overview

1.1 Overview

RK3588 is a high-performance, low-power application processor chip, which consists of 4 Cortex-A76 and 4 Cortex-A55 and independent NEON coprocessor integration for ARM PCs, edge computing, personal mobile internet devices, and other multimedia products.

The RK3588 has built-in multiple powerful embedded hardware engines, providing excellent performance for high-end applications. It supports H.265 and VP9 decoders at 8K@60fps, H.264 decoders at 8k@30fps, and AV1 decoders at 4K@60fps. It also supports H.264 and H.265 encoders at 8K@30fps, high-quality JPEG encoders/decoders, and specialized image pre-processors and post-processors.

Built-in 3D GPU, fully compatible with OpenGL ES1.1/2.0/3.2, OpenCL 2.2 and Vulkan 1.2. Special 2D with MMU
The hardware engine will maximize display performance and provide a smooth operating experience.

Introduced a new generation of fully hardware-based 48M pixel ISP (Image Signal Processor), which implements many algorithm accelerators, such as HDR, 3A, LSC, 3DNR, 2DNR, sharpening, dehazing, fisheye correction, gamma correction, etc.

The built-in NPU supports INT4/INT8/INT16/FP16 mixed operations, with a computing power of up to 6TOP. In addition, with its strong compatibility, it can easily convert network models based on a series of frameworks such as TensorFlow/MXNet/PyTorch/Caffe.

RK3588 has a high-performance 4-channel external memory interface (LPDDR4/LPDDR4X/LPDDR5) that can support demanding storage
It also provides a complete set of peripheral interfaces to flexibly support various applications.

1.2 Chip Block Diagram

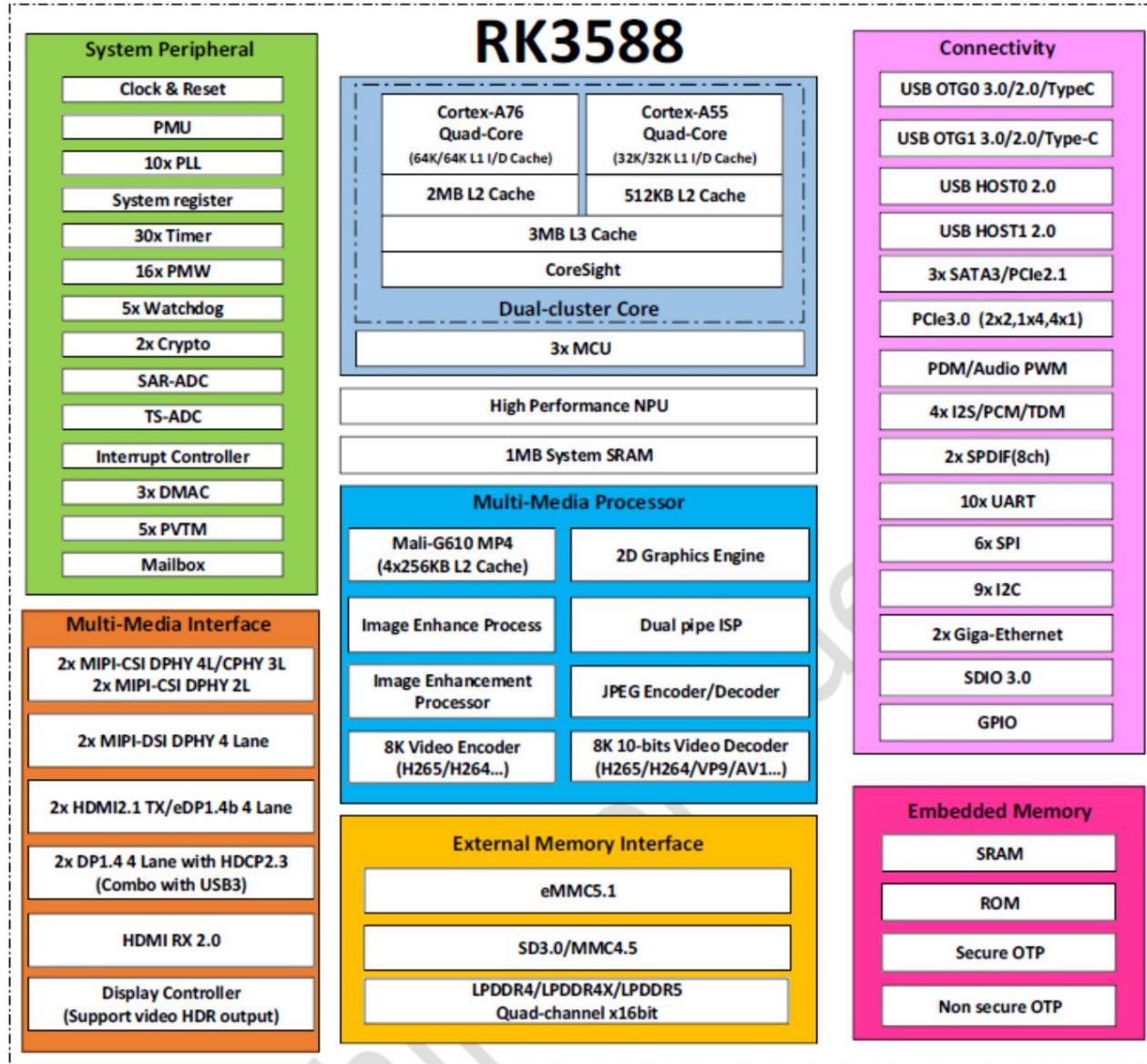


Figure 1-1 RK3588 block diagram

1.3 Application Block Diagram

1.3.1 RK3588 EVB Application Block Diagram

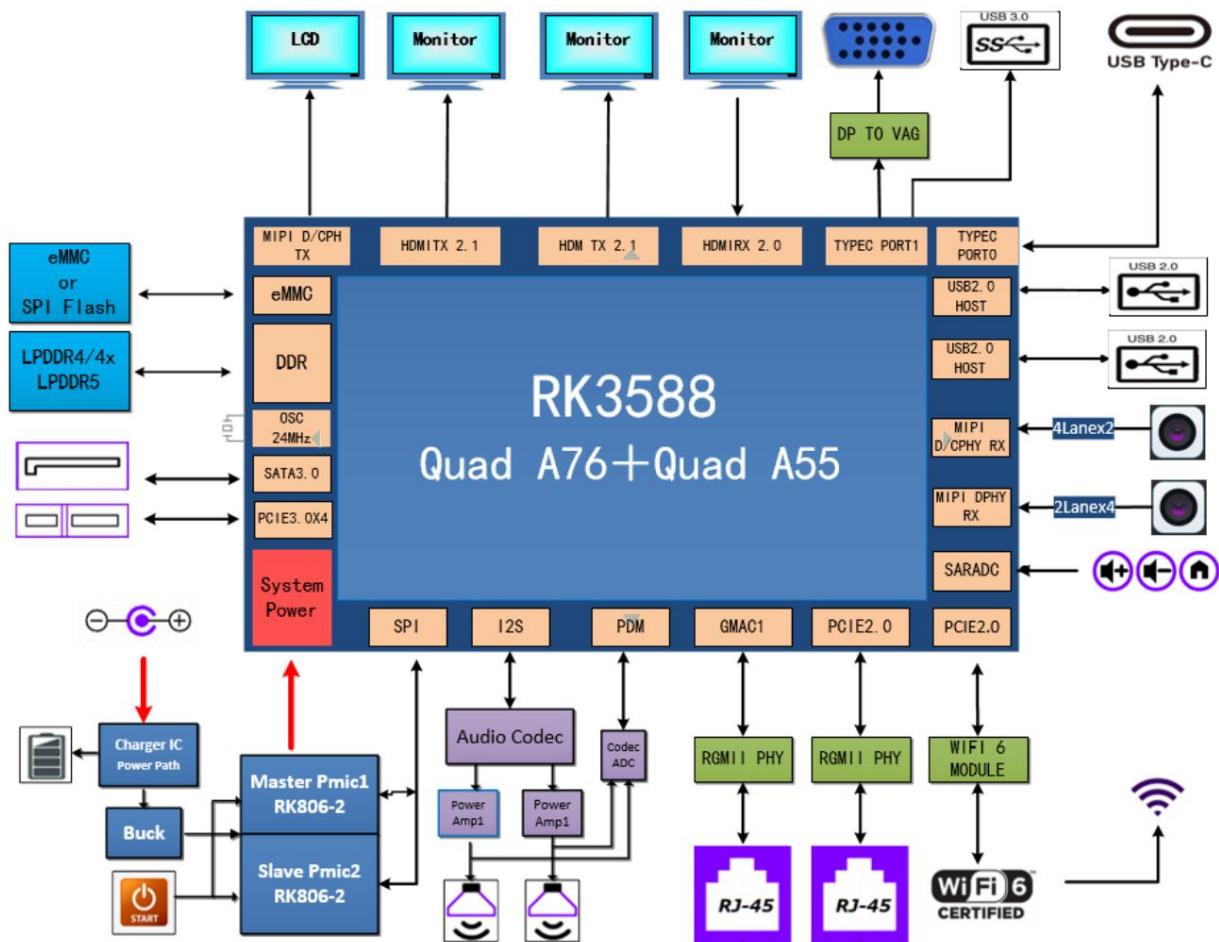


Figure 1-2 RK3588 EVB application block diagram

1.3.2 RK3588 Smart NVR Application Block Diagram

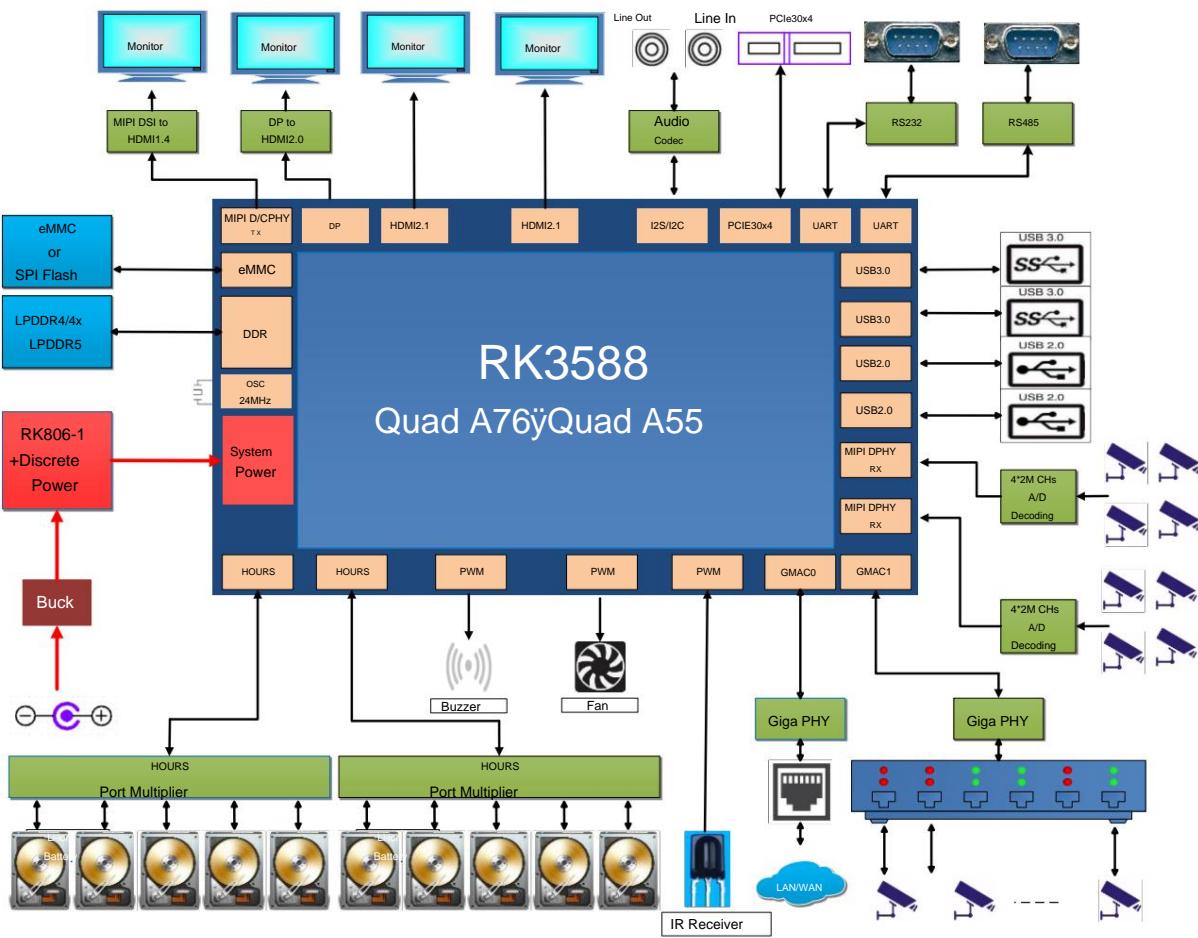


Figure 1-3 RK3588 Smart NVR Application Diagram

The above is an example application block diagram of the RK3588 chip solution. For more details, please refer to the reference design schematic diagram released by our company.

2 Schematic Design Suggestions

2.1 Minimum System Design

2.1.1 Clock Circuit

The oscillator circuit inside the RK3588 chip and the external 24MHz crystal together form the system clock, as shown in Figure 2-1.

The network must be connected in series with a 22ohm resistor to limit current and prevent overdrive. The 510Kohm resistor between the XOUT24M and XIN24M networks cannot be

Feel free to modify.

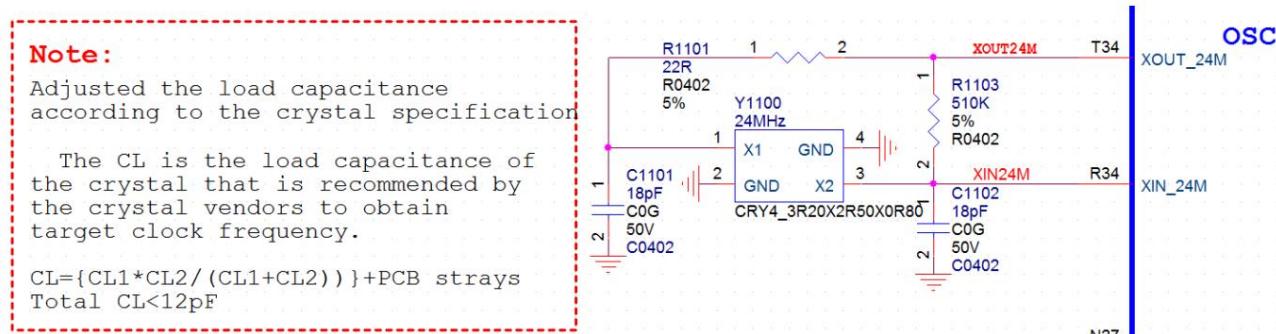


Figure 2-1 RK3588 crystal connection method and device parameters



Notice

Note1 \diamond Crystal selection CL Value not exceeding $12pF$

Note2 \diamond Crystal load capacitance should be based on the actual crystal used CL Capacitor value selection and control the frequency tolerance at room temperature $20ppm$ Within;

$18pF$ The capacitance value corresponding to the crystal selected by our company is not a universal value. The load capacitor material is recommended to be *COG* or *NPO*

It is recommended to use patch 4Pin crystals, of which 2 individual GND Pins and PCB The ground of the board is fully connected to enhance the clock resistance ESD Interference capability.

The system clock can also be directly generated by an external active crystal circuit with a clock amplitude of 1.0V.

XIN24M pin is input, XOUT24M pin is floating, and the clock parameters are shown in Table 2-1 below:

Table 2-1 RK3588 24MHz clock requirements

parameter	Maximum			describe
	Minimum	specification	unit	
frequency	24.000000		MHz	
Frequency deviation	+/-20		ppm	
Clock amplitude	1		In	Peak-to-peak value
Operating temperature	-20	80	°C	
ESR	/	40	Ohm	

When the RK3588 chip is in standby mode, it can choose to switch the working clock source to the clock provided by the PMU_PVTM module or the external input clock.

32.768KHz clock, turn off the OSC oscillation circuit, can get better chip standby power consumption, at this time only supports PMUIO1 and PMUIO2 circuit

For IO interrupt wakeup in the source domain, if the required wakeup source is related to the 24MHz clock, the 24MHz clock cannot be turned off.

The clock oscillator ring integrated in the PVTM (Process-Voltage-Temperature Monitor) module can generate a clock whose frequency is determined by the clock

The delay unit of the oscillation ring circuit determines the clock generated by the chip and can be used as the clock source for the chip to standby. When using the external input 32.768KHz clock

When the RK3588 chip is in sleep mode, the optimal chip standby power consumption can be achieved, and the PVTM module can also be turned off at this time.

The external input 32.768KHz clock can be obtained from the external RTC clock source. The RK3588 32.768KHz clock input pin is shown in the figure below:

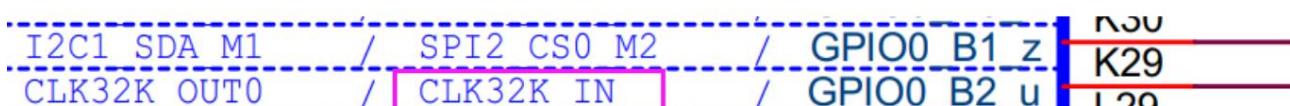


Figure 2-2 RK3588 32.768KHz standby clock input pin

The external 32.768kHz RTC clock parameters are shown in Table 2-2:

Table 2-2 RK3588 32.768KHz clock requirements

parameter	specification			describe
	Minimum	maximum	unit	
frequency	32.768000		kHz	
Frequency deviation	+/-30		ppm	
Clock amplitude	0.65*VDD	VDD+0.3V	In	VDD: PMUIO1 supply voltage
Operating temperature	-20	80	°C	
Duty cycle	45	55	%	



Notice

When using this function, this pin **IOMUX** Must be set to **CLK32K_IN** function, the input amplitude must meet **PMUIO1 Domian** Power supply requirements.

RK3588 can provide working clock to peripherals:

ÿ REFCLK_OUT: Reserved clock output pin, selected according to actual needs;

ÿ CLK32K_OUT0: 32.768KHz clock output, which can be provided to WIFI, BT, PCIe and other devices as sleep or working clock;

ÿ CLK32K_OUT1: 32.768KHz clock output, which can be provided to WIFI, BT, PCIe and other devices as sleep or working clock;

ETH0_REFCLKO_25M: 25MHz clock output, which can be provided to Ethernet PHY and other devices as the working clock;

ETH1_REFCLKO_25M: 25MHz clock output, which can be provided to Ethernet PHY and other devices as the working clock;

ÿ GMAC0_CLKINOUT: 50MHz, 125MHz clock input or output, can be provided to Ethernet PHY as RMII data

Data transmission and data reception reference clock

ÿ GMAC1_CLKINOUT: 50MHz, 125MHz clock input or output, can be provided to Ethernet PHY as RMII data

Data transmission and data reception reference clock

ÿ MIPI_CAMERA0_CLK----MIPI_CAMERA4_CLK: Default 24MHz clock output, can be provided to Camera, etc.

The device can be used as a working clock; other frequencies can also be obtained through PLL frequency division, and each clock channel supports outputting different frequencies.

ÿ PCIE20_REF_CLKP/N: Input or output 100M clock, the default clock frequency is 100M, for PCIE2.0 devices.

PCIE30_REF_CLKP/N: Input 100M clock. The external clock generator inputs 100M clock for the PCIE3.0 controller.



Notice

The above clock I/O Domain With peripherals/IT

The voltage levels must match. If they do not match, a level conversion circuit must be added. Please evaluate whether the requirements can be met based on the clock requirements of the peripheral devices.

2.1.2 Reset/Watchdog/TSADC Circuit

The hardware reset of RK3588 chip is input through Pin M31 (NPOR_u), which must be controlled externally and is valid at low level.

The shortest reset time required for the chip to be stable and work normally is 100 24MHz main clock cycles, which is at least 4us.

Pin M31 (NPOR_u) needs to add a 100nF capacitor to eliminate jitter on the reset signal, enhance anti-interference ability, and prevent false

Triggering a system abnormal reset.

The pull-up power supply of the RESET_L network must be consistent with the IO power domain (PMUIO1_1V8) where the NPOR pin is located.

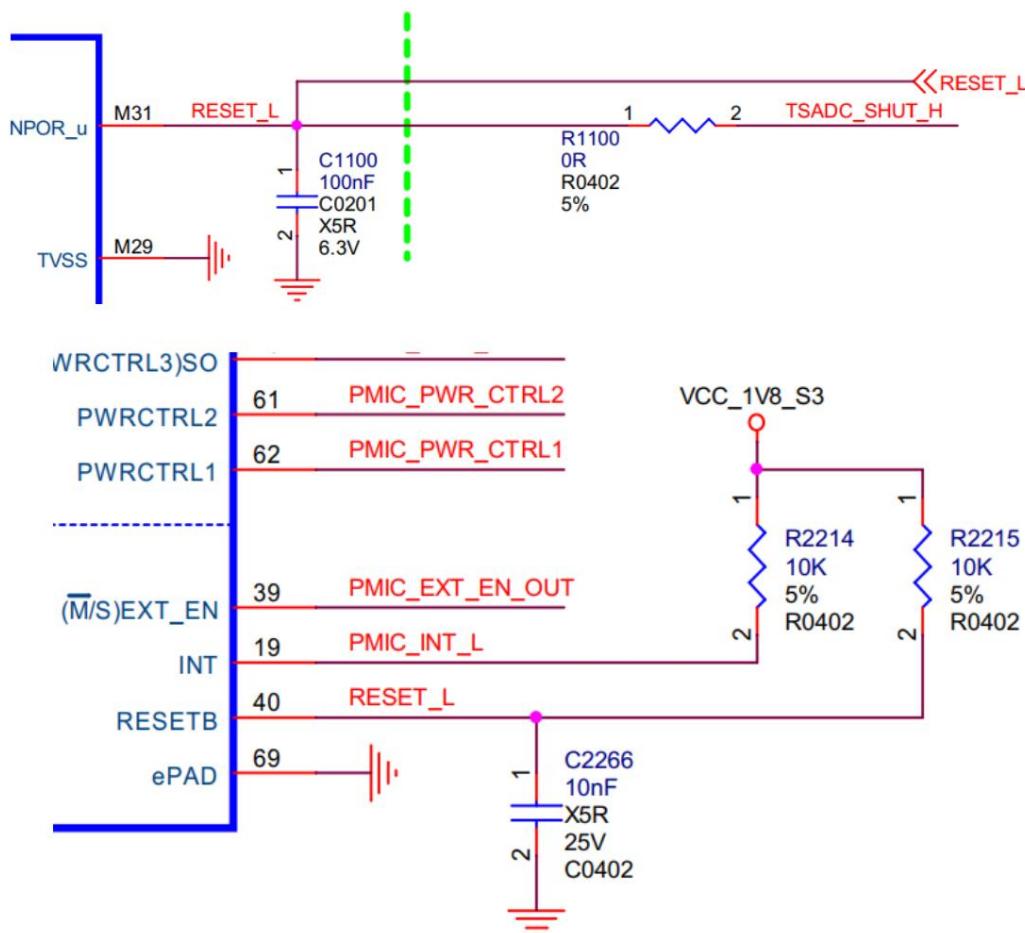


Figure 2-3 RK3588 reset input (RK806-1/2 solution)

The RK3588 chip integrates a Watchdog Timer. When a reset signal is generated, the TSADC_SHUT pin can output a low level to perform hardware reset on RK3588.

The RK3588 chip integrates seven TSADC (Temperature-Sensor ADC) modules. When the internal temperature of the chip exceeds the threshold, it can

The RK3588 chip can be reset by sending the internal TSHUT signal to the CRU module, or by outputting a low level through the TSADC_SHUT pin.

Perform hardware reset on RK3588. As shown in Figure 2-3 above, the TSADC_SHUT network is connected to the RESETn network.

The RK3588 reset signal path diagram is as follows:

ÿ Dual PMIC solution:

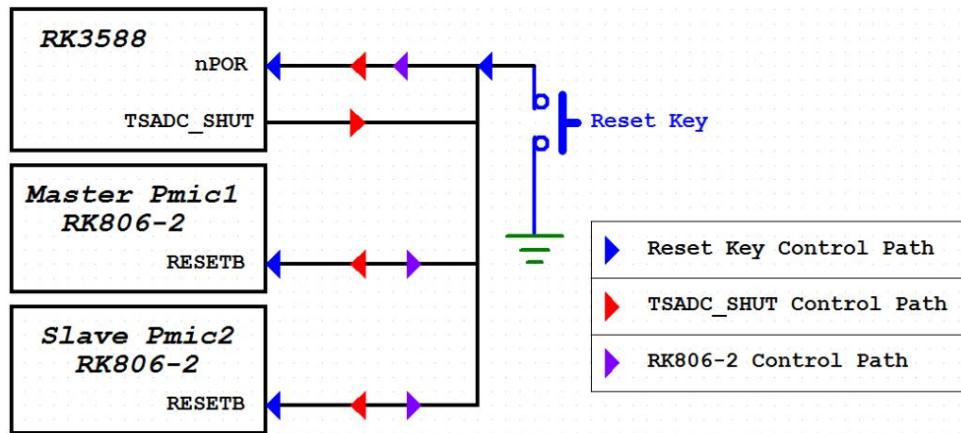


Figure 2-4 RK3588 reset signal path diagram - dual PMIC solution

ÿ Single PMIC solution

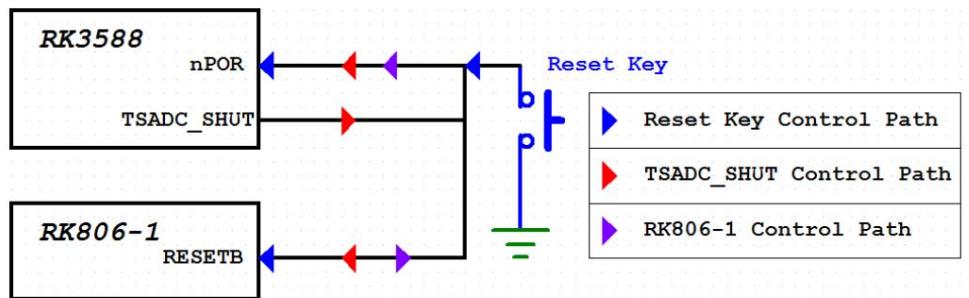


Figure 2-5 RK3588 reset signal path diagram - single PMIC solution

When the RESETB pin of RK806-1/2 is powered on for the first time, after all power supplies are powered on, RESETB will delay the setting time.

After a certain time, the low level jumps to a high level (open drain output), completing the power-on reset process; when RK806-1/2 is in working or sleep mode, if the RESETB pin is pulled low, then RK806-1/2 will also restart, and the restart power-on sequence is the same as the first power-on.

2.1.3 PMU Unit Circuit

To meet the low power consumption requirement, RK3588 is designed with a power management unit (PMU) to control the internal power supply of the chip. This module can support the IO control of the chip internal registers or PMUIO power domain to control the peripheral power circuit and realize power supply for other functional modules. and power off, and can also support IO interrupt wake-up, thereby realizing the standby and wake-up functions of the chip.

2.1.4 System boot sequence

The RK3588 chip supports multiple boot modes. After the chip is reset, the boot code integrated in the chip can be used in the following interfaces: The device boots, and the specific boot order can be selected according to actual application requirements (see the description of "Boot Order Selection" below)

- ÿ Serial Flash(FSPI)
- ÿ eMMC
- ÿ SDMMC Card

If there is no boot code in the above device, you can use the USB2.0 OTG0 interface TYPEC0_USB20_OTG_DP/

The TYPEC0_USB20_OTG_DM signal downloads the system code to these devices.

Boot order selection:

The boot sequence of RK3588 can be set through SARADC_IN0_BOOT Pin (PIN AM16), from the corresponding

Peripheral startup, as shown in the table below, the hardware is configured with different pull-up and pull-down resistor values to design the peripheral boot sequence for seven modes: LEVEL1-LEVEL7.

The corresponding configuration can be made according to actual application requirements.

BOOT MODE CONFIG

TABLE 1

Item	Rup	Rdown	ADC	VOL	BOOT MODE
LEVEL1	DNP	100K	0	0V	USB (Maskrom mode)
LEVEL2	100K	20K	682	0.3V	SD Card-USB
LEVEL3	100K	51K	1365	0.6V	EMMC-USB
LEVEL4	100K	100K	2047	0.9V	FSPI M0-USB
LEVEL5	100K	200K	2730	1.2V	FSPI M1-USB
LEVEL6	100K	500K	3412	1.5V	FSPI M2-USB
LEVEL7	100K	DNP	4095	1.8V	FSPI_M2-FSPI_M1-FSPI_M0-EMMC-SD Card-USB



Figure 2-6 RK3588 boot order selection

According to the above LEVEL1 setting, SARADC_IN0_BOOT is short-circuited to ground, which can make the device enter the Maskrom state without going through Short circuit EMMC_CLK/DATA to enter Maskrom; SARADC_IN1 is used to short circuit to ground to enter Recovery state; other SARADC

The port can be configured according to application requirements.



Notice

Note1 SARADC_IN0_BOOT for BOOT Configuration dedicated pins, cannot be used for other functions

Note2 RK3588 Not supported from PCIe BOOT , if there is PCIe Interface SSD The hard disk boot requirement needs to be FSPI Interface SPI FLASH

At startup, pass SPI FLASH The code first boots PCIe Driver, then load SSD The system inside, thus completing the startup

2.1.5 System initialization configuration signal

There is an important signal in RK3588 that affects the system startup configuration. It needs to be configured and kept stable before powering on:

SDMMC_DET pin (Pin P31): determines whether the VCCIO2 power domain IO is SDMMC or JTAG function

After the system reset is completed, the chip will configure the default power-on function of the corresponding module according to the input level of this pin.

The ARM JTAG function of RK3588 is multiplexed with the SDMMC function, and the IOMUX is switched through the SDMMC_DET pin.

function, so this pin also needs to be configured before power on, otherwise the ARM JTAG function will have no output and will affect the debugging during the boot phase.

SDMMC no output will affect the SDMMC boot function.

U1000D

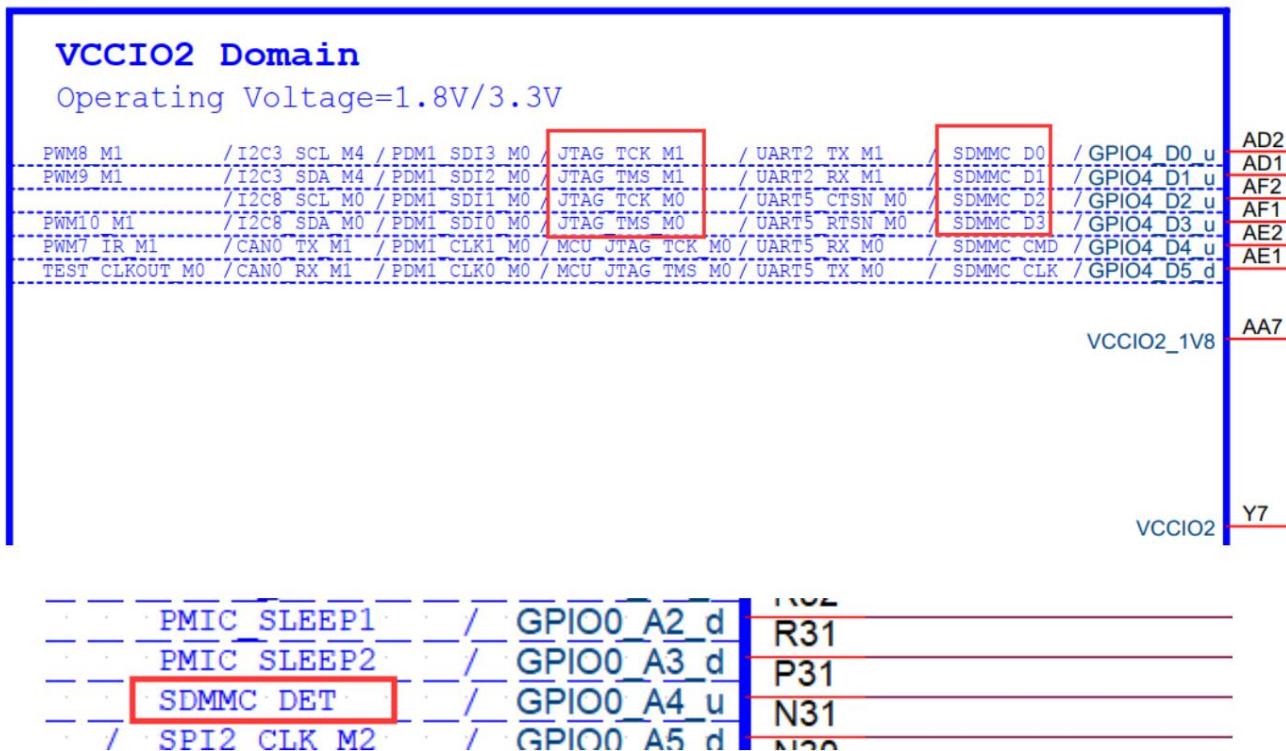


Figure 2-7 RK3588 SDMMC/ARM JTAG multiplexing pins and SDMMC DET pins

- ÿ If the pin is detected as high level, the corresponding IO switches to ARM JTAG function;
- ÿ When it is detected as low level (most SD cards will pull down this pin if inserted, if no special processing is required), the corresponding IO switches to SDMMC functionality;
- ÿ After the system is up, the IOMUX can be controlled by the register, and the pin can be released;
- ÿ For easy query, the configuration status and function of this pin correspond to the following table:

Table 2-3 RK3588 system initialization configuration signal description

Signal Name	Internal pull-up and pull-down	describe
SDMMC_DET	Pull-up	SDMMC/ARM JTAG pin multiplexing selection control signal: 0: Identify as SD card insertion, SDMMC/ARM JTAG pin multiplexed as SDMMC function; 1: Not recognized as SD card insertion, SDMMC/ARM JTAG pin multiplexing is ARM JTAG function (Default)

2.1.6 JTAG and UART Debug Circuits

The ARM JTAG interface of the RK3588 chip complies with the IEEE1149.1 standard, and the PC can be connected via SWD mode (two-wire mode).

DSTREAM emulator, debugs the ARM Core inside the chip.

When connecting to the emulator during the boot phase, you need to ensure that the SDMMC_DET pin is at a high level, otherwise you will not be able to enter the JTAG debugger.

Test mode, the configuration of this management is described in the previous section.

After the system starts up, it will switch to register-controlled IOMUX. The ARM JTAG interface description is shown in the following table:

Table 2-4 RK3588 JTAG Debug Interface Signals

Signal Name	describe
JTAG_TCK_M0/M1	SWD mode clock input
JTAG_TMS_M0/M1	SWD mode data input and output

The JTAG connection method and standard connector pin definition are shown in the figure below:

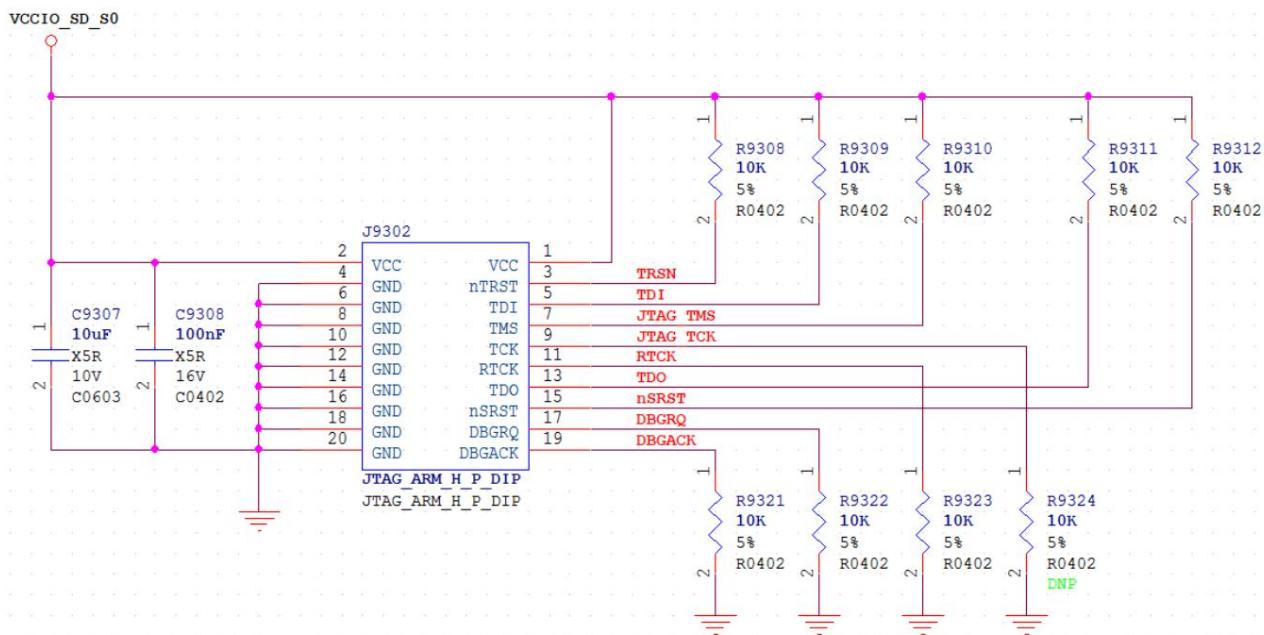
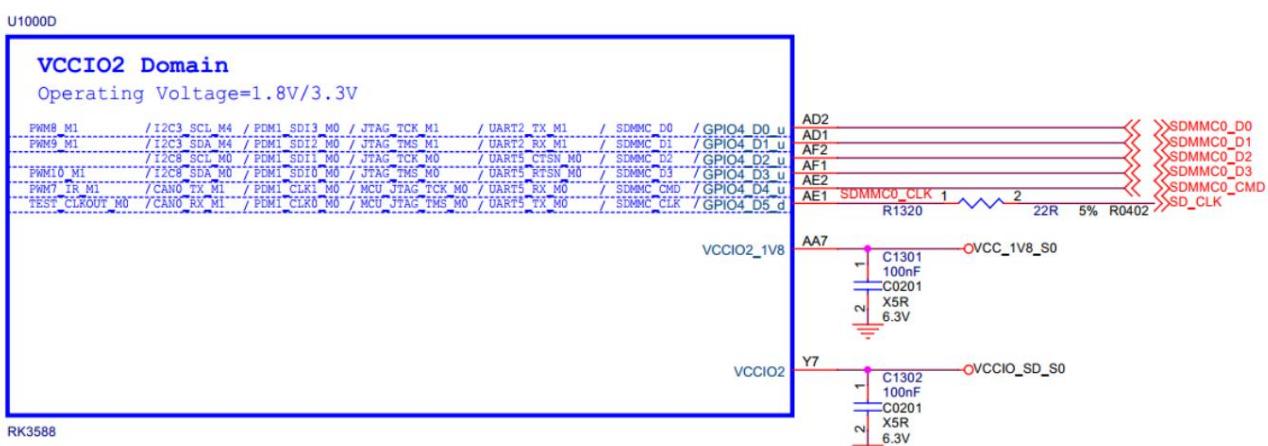


Figure 2-8 RK3588 JTAG connection diagram

If there is no SD Card function, it is recommended to reserve the ARM JTAG function for debugging convenience. The reserved circuit is as shown below:

ÿ Note that VCCIO2_1V8 (PIN AA7) must be powered and the power supply voltage must be VCC_1V8_S0 (1.8V);

ÿ VCCIO2 (PIN Y7) must be powered. The power supply voltage can be VCCIO_SD_S0 (3.3V).



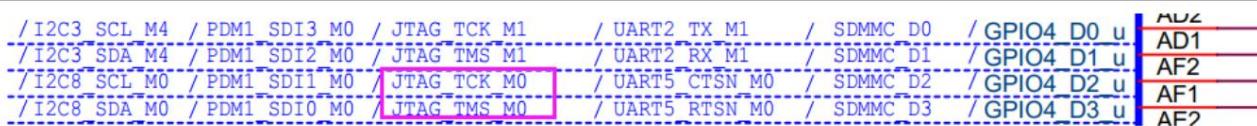


Figure 2-9 RK3588 ARM JTAG pins

The MCU_JTAG module of RK3588 is not open to the public yet and does not require any special processing.

RK3588 UART Debug selects UART2_RX_M0/UART2_TX_M0 by default, and the default baud rate is 1500000Bd.

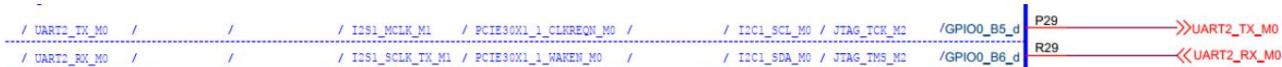


Figure 2-10 RK3588 UART2 M0 pin

The 100 ohm resistor connected in series with UART2_RX_M0/UART2_TX_M0 must not be removed, and a TVS tube should be added to enhance the anti-static surge capability and prevent damage to the chip pins during the development process. It is recommended to reserve 2.54 pins as much as possible. If conditions are unavailable, it is recommended to use test points larger than 0.7mm to facilitate soldering.

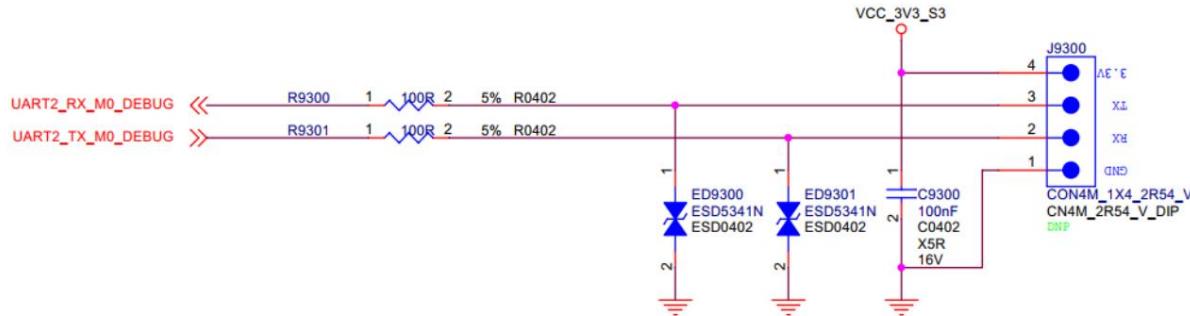


Figure 2-11 RK3588 Debug UART2 connection diagram

2.1.7 DDR Circuit

2.1.7.1 DDR Controller Introduction

The RK3588 DDR controller interface supports the JEDEC SDRAM standard interface. The controller has the following features:

Compatible with LPDDR4/LPDDR4X/LPDDR5 standards; Supports 64-bit

data bus width, consisting of 4 16-bit DDR channels, with a maximum addressable address of 8GB per channel; 4

The channel capacity can support a total capacity of up to 32GB;

Two 16-bit channels form a 32-bit channel. Two 32-bit channels (i.e., CH0 and CH1 in the diagram) cannot use particles with different capacities, such as 4GB+2GB.

Supports Power Down, Self Refresh and other modes; Programmable

output with dynamic PVT compensation and ODT impedance adjustment.

2.1.7.2 Circuit Design Recommendations

The schematics of the RK3588 DDR PHY and each DRAM chip must be consistent with the reference design, including the power decoupling capacitors.

RK3588 can support LPDDR4/LPDDR4X and LPDDR5. These DRAMs have different I/O signals.

Select the corresponding signal, the RK3588 DDR PHY I/O Map table is as follows:

Table 2-5 RK3588 DDR PHY I/O Map

DDR signal	LPDDR4/4x	LPDDR5
DDR_CH0_DQ0_A	DDR_CH0_DQ0_A	DDR_CH0_DQ0_A
DDR_CH0_DQ1_A	DDR_CH0_DQ1_A	DDR_CH0_DQ1_A
DDR_CH0_DQ2_A	DDR_CH0_DQ2_A	DDR_CH0_DQ2_A
DDR_CH0_DQ3_A	DDR_CH0_DQ3_A	DDR_CH0_DQ3_A
DDR_CH0_DQ4_A	DDR_CH0_DQ4_A	DDR_CH0_DQ4_A
DDR_CH0_DQ5_A	DDR_CH0_DQ5_A	DDR_CH0_DQ5_A
DDR_CH0_DQ6_A	DDR_CH0_DQ6_A	DDR_CH0_DQ6_A
DDR_CH0_DQ7_A	DDR_CH0_DQ7_A	DDR_CH0_DQ7_A
DDR_CH0_DQ8_A	DDR_CH0_DQ8_A	DDR_CH0_DQ8_A
DDR_CH0_DQ9_A	DDR_CH0_DQ9_A	DDR_CH0_DQ9_A
DDR_CH0_DQ10_A	DDR_CH0_DQ10_A	DDR_CH0_DQ10_A
DDR_CH0_DQ11_A	DDR_CH0_DQ11_A	DDR_CH0_DQ11_A
DDR_CH0_DQ12_A	DDR_CH0_DQ12_A	DDR_CH0_DQ12_A
DDR_CH0_DQ13_A	DDR_CH0_DQ13_A	DDR_CH0_DQ13_A
DDR_CH0_DQ14_A	DDR_CH0_DQ14_A	DDR_CH0_DQ14_A
DDR_CH0_DQ15_A	DDR_CH0_DQ15_A	DDR_CH0_DQ15_A
DDR_CH0_WCK0P_A	/	DDR_CH0_WCK0P_A
DDR_CH0_WCK0N_A	/	DDR_CH0_WCK0N_A
DDR_CH0_WCK1P_A	/	DDR_CH0_WCK1P_A
DDR_CH0_WCK1N_A	/	DDR_CH0_WCK1N_A
DDR_CH0_DQS0P_A	DDR_CH0_DQS0P_A	DDR_CH0_DQS0P_A
DDR_CH0_DQS0N_A	DDR_CH0_DQS0N_A	DDR_CH0_DQS0N_A
DDR_CH0_DQS1P_A	DDR_CH0_DQS1P_A	DDR_CH0_DQS1P_A
DDR_CH0_DQS1N_A	DDR_CH0_DQS1N_A	DDR_CH0_DQS1N_A
DDR_CH0_DM0_A	DDR_CH0_DM0_A	DDR_CH0_DM0_A
DDR_CH0_DM1_A	DDR_CH0_DM1_A	DDR_CH0_DM1_A
DDR_CH0_A0_A	DDR_CH0_A0_A	DDR_CH0_A0_A
DDR_CH0_A1_A	DDR_CH0_A1_A	DDR_CH0_A1_A
DDR_CH0_A2_A	DDR_CH0_A2_A	DDR_CH0_A2_A
DDR_CH0_A3_A	DDR_CH0_A3_A	DDR_CH0_A3_A
DDR_CH0_A4_A	DDR_CH0_A4_A	DDR_CH0_A4_A
DDR_CH0_A5_A	DDR_CH0_A5_A	DDR_CH0_A5_A

DDR signal	LPDDR4/4x	LPDDR5
DDR_CH0_A6_A	DDR_CH0_A6_A	DDR_CH0_A6_A
DDR_CH0_CK_A	DDR_CH0_CK_A	DDR_CH0_CK_A
DDR_CH0_CKB_A	DDR_CH0_CKB_A	DDR_CH0_CKB_A
DDR_CH0_LP4/4X_CS0_A	DDR_CH0_LP4/4X_CS0_A	/
DDR_CH0_LP4/4X_CS1_A	DDR_CH0_LP4/4X_CS1_A	/
DDR_CH0_LP4/4X_CKE0/LP5_CS0_A	DDR_CH0_LP4/4X_CKE0_A	DDR_CH0_LP5_CS0_A
DDR_CH0_LP4/4X_CKE1/LP5_CS1_A	DDR_CH0_LP4/4X_CKE1_A	DDR_CH0_LP5_CS1_A
DDR_CH0_ZQ_A	DDR_CH0_ZQ_A	DDR_CH0_ZQ_A
DDR_CH0_RESET_A	DDR_CH0_RESET_A	DDR_CH0_RESET_A
DDR_CH0_DQ0_B	DDR_CH0_DQ0_B	DDR_CH0_DQ0_B
DDR_CH0_DQ1_B	DDR_CH0_DQ1_B	DDR_CH0_DQ1_B
DDR_CH0_DQ2_B	DDR_CH0_DQ2_B	DDR_CH0_DQ2_B
DDR_CH0_DQ3_B	DDR_CH0_DQ3_B	DDR_CH0_DQ3_B
DDR_CH0_DQ4_B	DDR_CH0_DQ4_B	DDR_CH0_DQ4_B
DDR_CH0_DQ5_B	DDR_CH0_DQ5_B	DDR_CH0_DQ5_B
DDR_CH0_DQ6_B	DDR_CH0_DQ6_B	DDR_CH0_DQ6_B
DDR_CH0_DQ7_B	DDR_CH0_DQ7_B	DDR_CH0_DQ7_B
DDR_CH0_DQ8_B	DDR_CH0_DQ8_B	DDR_CH0_DQ8_B
DDR_CH0_DQ9_B	DDR_CH0_DQ9_B	DDR_CH0_DQ9_B
DDR_CH0_DQ10_B	DDR_CH0_DQ10_B	DDR_CH0_DQ10_B
DDR_CH0_DQ11_B	DDR_CH0_DQ11_B	DDR_CH0_DQ11_B
DDR_CH0_DQ12_B	DDR_CH0_DQ12_B	DDR_CH0_DQ12_B
DDR_CH0_DQ13_B	DDR_CH0_DQ13_B	DDR_CH0_DQ13_B
DDR_CH0_DQ14_B	DDR_CH0_DQ14_B	DDR_CH0_DQ14_B
DDR_CH0_DQ15_B	DDR_CH0_DQ15_B	DDR_CH0_DQ15_B
DDR_CH0_WCK0P_B	/	DDR_CH0_WCK0P_B
DDR_CH0_WCK0N_B	/	DDR_CH0_WCK0N_B
DDR_CH0_WCK1P_B	/	DDR_CH0_WCK1P_B
DDR_CH0_WCK1N_B	/	DDR_CH0_WCK1N_B
DDR_CH0_DQS0P_B	DDR_CH0_DQS0P_B	DDR_CH0_DQS0P_B
DDR_CH0_DQS0N_B	DDR_CH0_DQS0N_B	DDR_CH0_DQS0N_B
DDR_CH0_DQS1P_B	DDR_CH0_DQS1P_B	DDR_CH0_DQS1P_B
DDR_CH0_DQS1N_B	DDR_CH0_DQS1N_B	DDR_CH0_DQS1N_B
DDR_CH0_DM0_B	DDR_CH0_DM0_B	DDR_CH0_DM0_B
DDR_CH0_DM1_B	DDR_CH0_DM1_B	DDR_CH0_DM1_B
DDR_CH0_A0_B	DDR_CH0_A0_B	DDR_CH0_A0_B
DDR_CH0_A1_B	DDR_CH0_A1_B	DDR_CH0_A1_B
DDR_CH0_A2_B	DDR_CH0_A2_B	DDR_CH0_A2_B

DDR signal	LPDDR4/4x	LPDDR5
DDR_CH0_A3_B	DDR_CH0_A3_B	DDR_CH0_A3_B
DDR_CH0_A4_B	DDR_CH0_A4_B	DDR_CH0_A4_B
DDR_CH0_A5_B	DDR_CH0_A5_B	DDR_CH0_A5_B
DDR_CH0_A6_B	DDR_CH0_A6_B	DDR_CH0_A6_B
DDR_CH0_CK_B	DDR_CH0_CK_B	DDR_CH0_CK_B
DDR_CH0_CKB_B	DDR_CH0_CKB_B	DDR_CH0_CKB_B
DDR_CH0_LP4/4X_CS0_B	DDR_CH0_LP4/4X_CS0_B	/
DDR_CH0_LP4/4X_CS1_B	DDR_CH0_LP4/4X_CS1_B	/
DDR_CH0_LP4/4X_CKE0/LP5_CS0_B	DDR_CH0_LP4/4X_CKE0_B	DDR_CH0_LP5_CS0_B
DDR_CH0_LP4/4X_CKE1/LP5_CS1_B	DDR_CH0_LP4/4X_CKE1_B	DDR_CH0_LP5_CS1_B
DDR_CH0_ZQ_B	DDR_CH0_ZQ_B	DDR_CH0_ZQ_B
DDR_CH0_RESET_B	DDR_CH0_RESET_B	DDR_CH0_RESET_B
DDR_CH1_DQ0_C	DDR_CH1_DQ0_C	DDR_CH1_DQ0_C
DDR_CH1_DQ1_C	DDR_CH1_DQ1_C	DDR_CH1_DQ1_C
DDR_CH1_DQ2_C	DDR_CH1_DQ2_C	DDR_CH1_DQ2_C
DDR_CH1_DQ3_C	DDR_CH1_DQ3_C	DDR_CH1_DQ3_C
DDR_CH1_DQ4_C	DDR_CH1_DQ4_C	DDR_CH1_DQ4_C
DDR_CH1_DQ5_C	DDR_CH1_DQ5_C	DDR_CH1_DQ5_C
DDR_CH1_DQ6_C	DDR_CH1_DQ6_C	DDR_CH1_DQ6_C
DDR_CH1_DQ7_C	DDR_CH1_DQ7_C	DDR_CH1_DQ7_C
DDR_CH1_DQ8_C	DDR_CH1_DQ8_C	DDR_CH1_DQ8_C
DDR_CH1_DQ9_C	DDR_CH1_DQ9_C	DDR_CH1_DQ9_C
DDR_CH1_DQ10_C	DDR_CH1_DQ10_C	DDR_CH1_DQ10_C
DDR_CH1_DQ11_C	DDR_CH1_DQ11_C	DDR_CH1_DQ11_C
DDR_CH1_DQ12_C	DDR_CH1_DQ12_C	DDR_CH1_DQ12_C
DDR_CH1_DQ13_C	DDR_CH1_DQ13_C	DDR_CH1_DQ13_C
DDR_CH1_DQ14_C	DDR_CH1_DQ14_C	DDR_CH1_DQ14_C
DDR_CH1_DQ15_C	DDR_CH1_DQ15_C	DDR_CH1_DQ15_C
DDR_CH1_WCK0P_C	/	DDR_CH1_WCK0P_C
DDR_CH1_WCK0N_C	/	DDR_CH1_WCK0N_C
DDR_CH1_WCK1P_C	/	DDR_CH1_WCK1P_C
DDR_CH1_WCK1N_C	/	DDR_CH1_WCK1N_C
DDR_CH1_DQS0P_C	DDR_CH1_DQS0P_C	DDR_CH1_DQS0P_C
DDR_CH1_DQS0N_C	DDR_CH1_DQS0N_C	DDR_CH1_DQS0N_C
DDR_CH1_DQS1P_C	DDR_CH1_DQS1P_C	DDR_CH1_DQS1P_C
DDR_CH1_DQS1N_C	DDR_CH1_DQS1N_C	DDR_CH1_DQS1N_C
DDR_CH1_DM0_C	DDR_CH1_DM0_C	DDR_CH1_DM0_C
DDR_CH1_DM1_C	DDR_CH1_DM1_C	DDR_CH1_DM1_C

DDR signal	LPDDR4/4x	LPDDR5
DDR_CH1_A0_C	DDR_CH1_A0_C	DDR_CH1_A0_C
DDR_CH1_A1_C	DDR_CH1_A1_C	DDR_CH1_A1_C
DDR_CH1_A2_C	DDR_CH1_A2_C	DDR_CH1_A2_C
DDR_CH1_A3_C	DDR_CH1_A3_C	DDR_CH1_A3_C
DDR_CH1_A4_C	DDR_CH1_A4_C	DDR_CH1_A4_C
DDR_CH1_A5_C	DDR_CH1_A5_C	DDR_CH1_A5_C
DDR_CH1_A6_C	DDR_CH1_A6_C	DDR_CH1_A6_C
DDR_CH1_CK_C	DDR_CH1_CK_C	DDR_CH1_CK_C
DDR_CH1_CKB_C	DDR_CH1_CKB_C	DDR_CH1_CKB_C
DDR_CH1_LP4/4X_CS0_C	DDR_CH1_LP4/4X_CS0_C	/
DDR_CH1_LP4/4X_CS1_C	DDR_CH1_LP4/4X_CS1_C	/
DDR_CH1_LP4/4X_CKE0/LP5_CS0_C	DDR_CH1_LP4/4X_CKE0_C	DDR_CH1_LP5_CS0_C
DDR_CH1_LP4/4X_CKE1/LP5_CS1_C	DDR_CH1_LP4/4X_CKE1_C	DDR_CH1_LP5_CS1_C
DDR_CH1_ZQ_C	DDR_CH1_ZQ_C	DDR_CH1_ZQ_C
DDR_CH1_RESET_C	DDR_CH1_RESET_C	DDR_CH1_RESET_C
DDR_CH1_DQ0_D	DDR_CH1_DQ0_D	DDR_CH1_DQ0_D
DDR_CH1_DQ1_D	DDR_CH1_DQ1_D	DDR_CH1_DQ1_D
DDR_CH1_DQ2_D	DDR_CH1_DQ2_D	DDR_CH1_DQ2_D
DDR_CH1_DQ3_D	DDR_CH1_DQ3_D	DDR_CH1_DQ3_D
DDR_CH1_DQ4_D	DDR_CH1_DQ4_D	DDR_CH1_DQ4_D
DDR_CH1_DQ5_D	DDR_CH1_DQ5_D	DDR_CH1_DQ5_D
DDR_CH1_DQ6_D	DDR_CH1_DQ6_D	DDR_CH1_DQ6_D
DDR_CH1_DQ7_D	DDR_CH1_DQ7_D	DDR_CH1_DQ7_D
DDR_CH1_DQ8_D	DDR_CH1_DQ8_D	DDR_CH1_DQ8_D
DDR_CH1_DQ9_D	DDR_CH1_DQ9_D	DDR_CH1_DQ9_D
DDR_CH1_DQ10_D	DDR_CH1_DQ10_D	DDR_CH1_DQ10_D
DDR_CH1_DQ11_D	DDR_CH1_DQ11_D	DDR_CH1_DQ11_D
DDR_CH1_DQ12_D	DDR_CH1_DQ12_D	DDR_CH1_DQ12_D
DDR_CH1_DQ13_D	DDR_CH1_DQ13_D	DDR_CH1_DQ13_D
DDR_CH1_DQ14_D	DDR_CH1_DQ14_D	DDR_CH1_DQ14_D
DDR_CH1_DQ15_D	DDR_CH1_DQ15_D	DDR_CH1_DQ15_D
DDR_CH1_WCK0P_D	/	DDR_CH1_WCK0P_D
DDR_CH1_WCK0N_D	/	DDR_CH1_WCK0N_D
DDR_CH1_WCK1P_D	/	DDR_CH1_WCK1P_D
DDR_CH1_WCK1N_D	/	DDR_CH1_WCK1N_D
DDR_CH1_DQS0P_D	DDR_CH1_DQS0P_D	DDR_CH1_DQS0P_D
DDR_CH1_DQS0N_D	DDR_CH1_DQS0N_D	DDR_CH1_DQS0N_D
DDR_CH1_DQS1P_D	DDR_CH1_DQS1P_D	DDR_CH1_DQS1P_D

DDR signal	LPDDR4/4x	LPDDR5
DDR_CH1_DQS1N_D	DDR_CH1_DQS1N_D	DDR_CH1_DQS1N_D
DDR_CH1_DM0_D	DDR_CH1_DM0_D	DDR_CH1_DM0_D
DDR_CH1_DM1_D	DDR_CH1_DM1_D	DDR_CH1_DM1_D
DDR_CH1_A0_D	DDR_CH1_A0_D	DDR_CH1_A0_D
DDR_CH1_A1_D	DDR_CH1_A1_D	DDR_CH1_A1_D
DDR_CH1_A2_D	DDR_CH1_A2_D	DDR_CH1_A2_D
DDR_CH1_A3_D	DDR_CH1_A3_D	DDR_CH1_A3_D
DDR_CH1_A4_D	DDR_CH1_A4_D	DDR_CH1_A4_D
DDR_CH1_A5_D	DDR_CH1_A5_D	DDR_CH1_A5_D
DDR_CH1_A6_D	DDR_CH1_A6_D	DDR_CH1_A6_D
DDR_CH1_CK_D	DDR_CH1_CK_D	DDR_CH1_CK_D
DDR_CH1_CKB_D	DDR_CH1_CKB_D	DDR_CH1_CKB_D
DDR_CH1_LP4/4X_CS0_D	DDR_CH1_LP4/4X_CS0_D	/
DDR_CH1_LP4/4X_CS1_D	DDR_CH1_LP4/4X_CS1_D	/
DDR_CH1_LP4/4X_CKE0/LP5_CS0_D	DDR_CH1_LP4/4X_CKE0_D	DDR_CH1_LP5_CS0_D
DDR_CH1_LP4/4X_CKE1/LP5_CS1_D	DDR_CH1_LP4/4X_CKE1_D	DDR_CH1_LP5_CS1_D
DDR_CH1_ZQ_D	DDR_CH1_ZQ_D	DDR_CH1_ZQ_D
DDR_CH1_RESET_D	DDR_CH1_RESET_D	DDR_CH1_RESET_D

For LPDDR4/LPDDR4x/LPDDR5:

þ The order of DQ and CA cannot be swapped and must be assigned according to the reference diagram.

DDR PHY ZQ must be connected to the VDDQ_DDR_S0 power supply with a 240ohm 1% resistor.

With built-in Retention function, during the DDR self-refresh period, the power pin of DDR_CH_VDDQ_CKE on the DDR controller side needs to be kept

The VDDQ power supply of the DDR particle can also be turned off after tCKELOCK is turned off for 5ns, while other power supplies cannot be turned off.

close.

LPDDR5 introduces the WCK clock; LPDDR5 has two working clocks, CK_t and CK_c, which are used to control commands and addresses.

One is WCK_t and WCK_c, WCK can be 2 times or 4 times the CK frequency; when Write, WCK is

The clock is also the Write data strobe; when Read, WCK is the clock of DQ and RDQS, and RDQS is the Read data strobe signal.

RK3588 supports DVFS Mode (when running LPDDR5). DVFS mode supports both VDD2L (0.9V) and VDD2H (1.05V).

The MCU switches between two voltages, namely, it uses VDD2H voltage when running at high frequency and VDD2L voltage when running at low frequency.

2.1.7.3 DDR Particle Peripheral Circuit Design

The ZQ terminal of LPDDR4/4x/LPDDR5 must be connected to the VDDQ_DDR_S0 power supply with a 240-ohm 1% resistor.

þ The ODT_CA of LPDDR4/4x must be connected to the VDD2_DDR_S3 power supply with a 10Kohm 5% resistor;

2.1.7.4 DDR Topology and Matching Design

When LPDDR4/4x 2 32-bit, DQ and CA adopt point-to-point topology

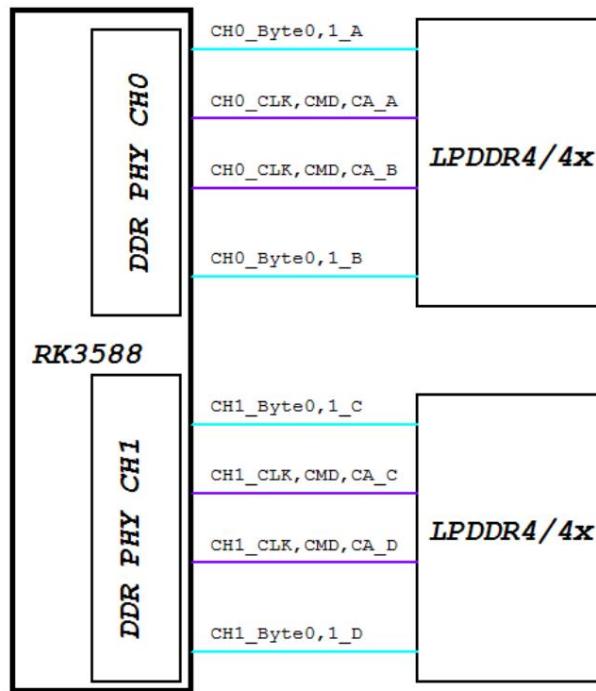


Figure 2-12 LPDDR4 point-to-point topology

Matching method: LPDDR4 particle DQ, CLK, CMD, and CA all support ODT, and all can be connected point-to-point.

When using 2 32-bit LPDDR5 chips, DQ and CA adopt a point-to-point topology

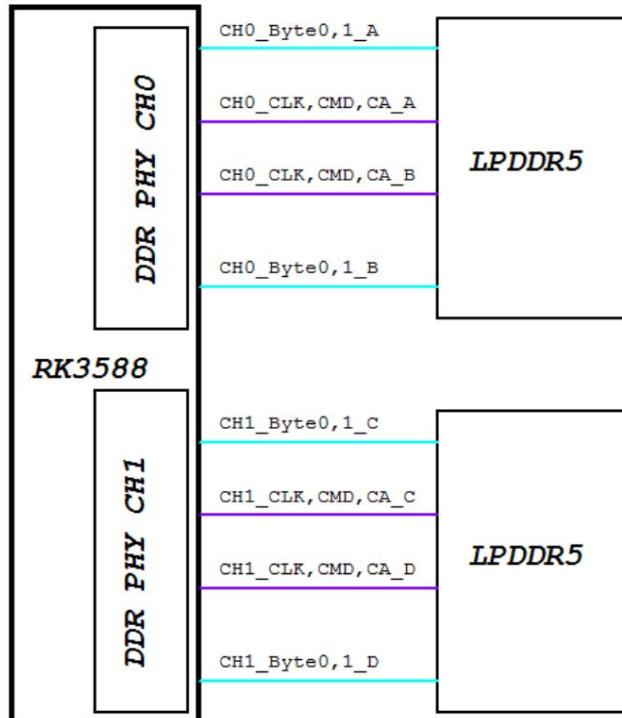


Figure 2-13 LPDDR5 point-to-point topology

Matching method: LPDDR5 particle DQ, CLK, CMD, and CA all support ODT, and all can be connected point-to-point.

2.1.7.5 DDR Power Supply Design and Power-On Sequence Requirements

The RK3588 DDR PHY power supply is summarized as follows:

DDR PHY Power		LPDDR4/4x	LPDDR5
DDR PLL Power	DDR_CH0/1_PLL_DVDD	0.75v-0.85v	0.75v-0.85v
	DDR_CH0/1_PLL_AVDD1V8	1.8v	1.8v
MEMORY INTERFACE POWER		0.75v-0.85v	0.75v-0.85v
DIGITAL CORE POWER		0.75v-0.85v	0.75v-0.85v
DDR IO POWER		0.6v	0.5v
CK Power		0.6v	0.5v
LP4/4X_CKE&LP5_CS & Reset Power		1.1v	1.05v

Note: The voltage values in the above table are all Typ values

The power supply for LPDDR4/4x/LPDDR5 chips is summarized as follows:

DDR particle power		LPDDR4	LPDDR4x	LPDDR5
Core Power1	VDD1	1.8v	1.8v	1.8v
Core Power2&CA Power	VDD2/VDD2H	VDD2=1.1v	VDD2=1.1v	VDD2H=1.05v
	VDD2L	/	/	0.9v
I/O Buffer Power	VDDQ	1.1v	0.6v	0.5v

Note: The voltage values in the above table are all Typ values

When using a dual PMIC power supply solution, pay attention to the power supply circuit:

þ The PMIC model is RK806-2. Please note that according to the actual DRAM particles used, modify the PMIC2 RK806-2 FB9 synchronously.

The voltage divider resistor value of (pin66) makes the VDDQ_DDR_S0 output voltage match the chip.

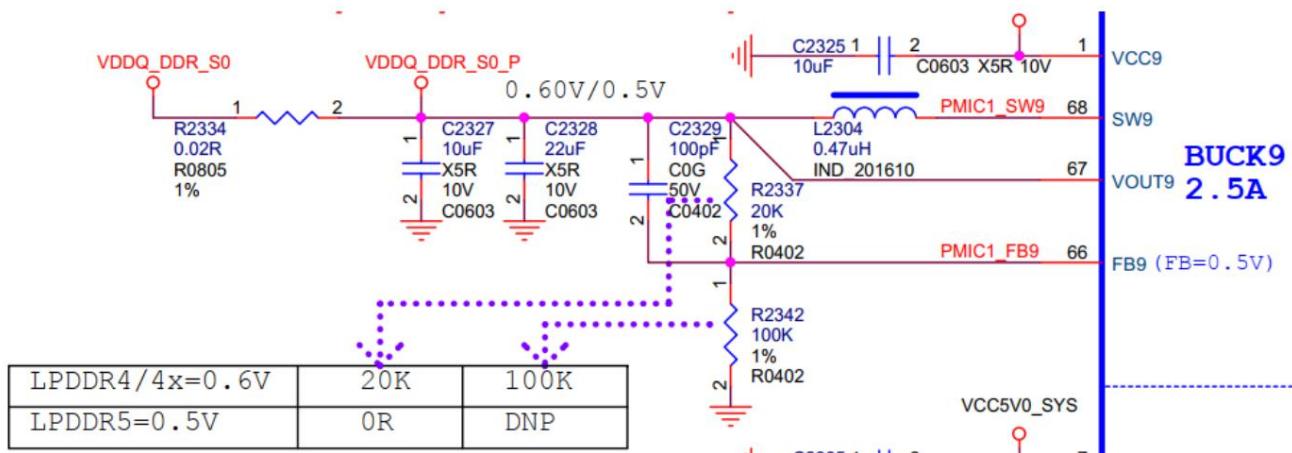


Figure 2-14 RK806-2 BUCK9 FB parameter adjustment

ŷ The PMIC model is RK806-2. Please note that according to the actual DRAM particles used, modify PMIC1 RK806-2 FB9 simultaneously.

The resistance of the voltage divider resistor (pin66) makes the VDD2_DDR_S3 output voltage match the chip.

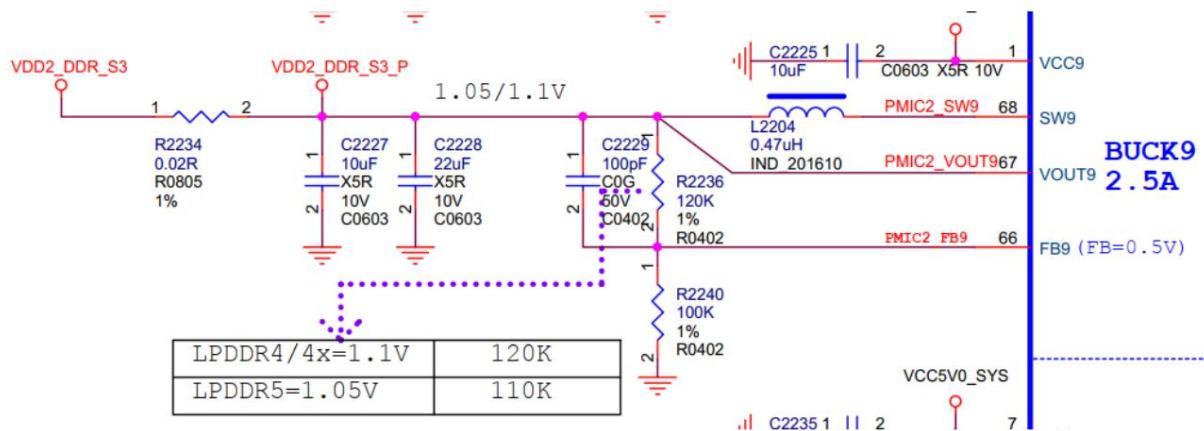


Figure 2-15 RK806-2 BUCK9 FB parameter adjustment

When using a single PMIC power supply solution, the power supply circuit should

pay attention to the following points: ŷ The PMIC model is RK806-1. Please note that according to the actual DRAM particles used, the PMIC RK806-1 FB9 (pin66) should be modified synchronously.

The voltage divider resistor value is set to match the VDDQ_DDR_S0 output voltage with the chip.

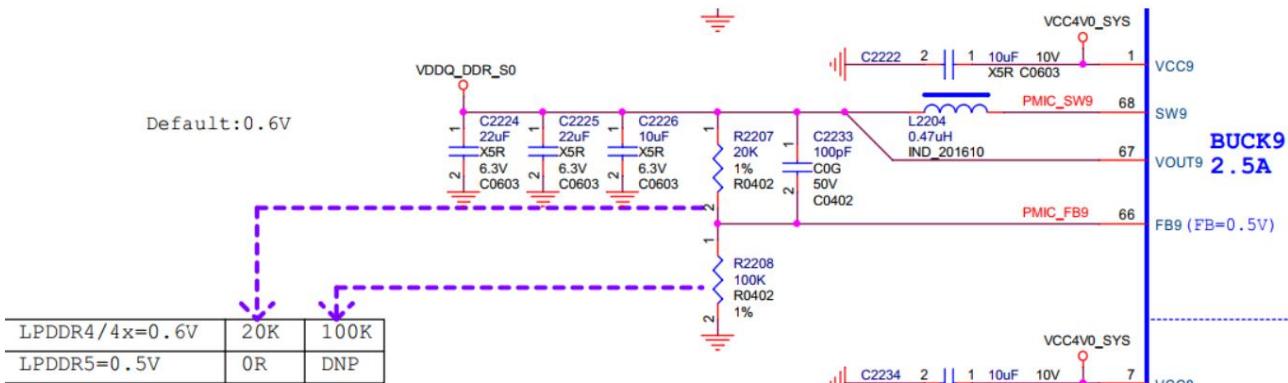


Figure 2-16 RK806-1 BUCK9 FB parameter adjustment

ŷ If the PMIC model is RK806-1, please note that according to the actual DRAM chip used, the voltage divider resistor value of PMIC RK806-1 FB6 (pin31) should be modified synchronously to make

the VDD2_DDR_S3 output voltage match the chip.

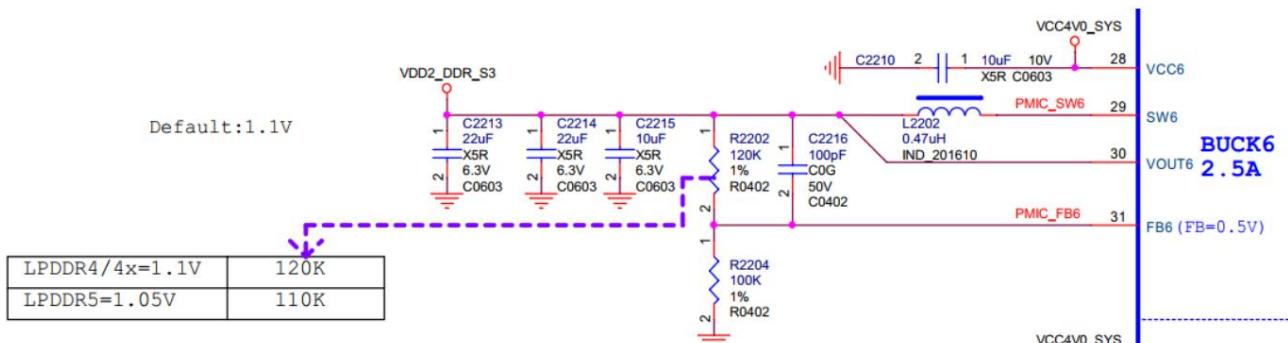


Figure 2-17 RK806-1 BUCK6 FB parameter adjustment

The RK3588 reference template provides LPDDR4 and LPDDR4x compatible designs.

LP4XD200P232SD10H1_4266MHz", it should be noted that the corresponding circuit must be selected according to the actual material.

When attaching LPDDR4 chips, only the R3811 resistor shown in the figure below needs to be attached. The R3808 resistor does not need to be attached.

When mounting LPDDR4x chips, only resistor R3808 as shown in the figure below is required. R3811 is not required.

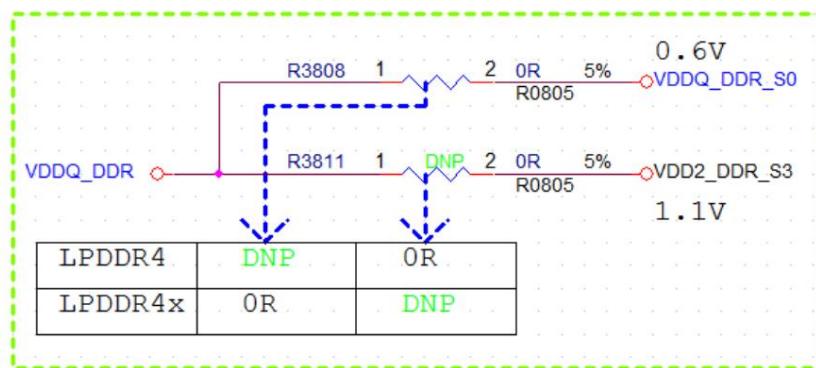


Figure 2-18 Power supply selection for LPDDR4/LPDDR4x compatible designs

For the power-on timing requirements of various DRAM types, please refer to the JEDEC standards.

The power-on sequence of LPDDR4/4x SDRAM is shown in the figure below:

1. While applying power (after Ta), RESET_n is recommended to be LOW ($\leq 0.2 \times V_{DD2}$) and all other inputs must be between VILmin and VIHmax. The device outputs remain at High-Z while RESET_n is held LOW. Power supply voltage ramp requirements are provided in Table 5. V_{DD1} must ramp at the same time or earlier than V_{DD2} . V_{DD2} must ramp at the same time or earlier than V_{DDQ} .

Table 5 — Voltage Ramp Conditions

After	Applicable Conditions
Ta is reached	V_{DD1} must be greater than V_{DD2}
	V_{DD2} must be greater than $V_{DDQ} - 200$ mV

NOTE 1 Ta is the point when any power supply first reaches 300 mV.

NOTE 2 Voltage ramp conditions in Table 5 apply between Ta and power-off (controlled or uncontrolled).

NOTE 3 Tb is the point at which all supply and reference voltages are within their defined ranges.

NOTE 4 Power ramp duration tINIT0 (Tb-Ta) must not exceed 20ms.

NOTE 5 The voltage difference between any of V_{SS} and V_{SSQ} pins must not exceed 100 mV.

Figure 2-19 LPDDR4/4x SDRAM power-on sequence

The power-on sequence of LPDDR5 SDRAM is shown in the figure below:

- 1) While applying power (after Ta), RESET_n is recommended to be LOW ($\leq 0.2 \times V_{DD2H}$) and all other inputs shall be between VILmin and VIHmax. The SDRAM outputs remain at High-Z while RESET_n is held LOW. Power supply voltage ramp requirements are provided in Table 17. V_{DD1} must ramp at the same time or earlier than V_{DD2H} . V_{DD2H} must ramp at the same time or earlier than V_{DD2L} . V_{DD2L} must ramp at the same time or earlier than V_{DDQ} .

Table 17 — Voltage Ramp Conditions

After	Applicable Conditions
Ta is reached	V_{DD1} must be greater than V_{DD2H}
	V_{DD2H} must be equal to or greater than V_{DD2L}
	V_{DD2L} must be greater than $V_{DDQ}-200mV$

NOTE 1 Ta is the point when any power supply first reaches 300mV.

NOTE 2 Voltage ramp conditions in Table 17 apply between Ta and power-off (controlled or uncontrolled).

NOTE 3 Tb is the point at which all supply voltages are within their defined ranges.

NOTE 4 Power ramp duration tINIT0 (Tb-Ta) must not exceed 20ms.

Figure 2-20 LPDDR5 SDRAM power-on sequence

2.1.7.6 DDR Supported Models

For the RK3588 DDR particle support list, please refer to Rockchip Microelectronics' "Rockchip_Support_List_DDR" document, which can be found at Rockchip.

Download the Redmine platform for microelectronics:

The document is not yet completed, and the address will be attached after it is released.

2.1.8 eMMC Circuit

2.1.8.1 eMMC Controller Introduction

The RK3588 eMMC controller has the following features:

- ÿ Compatible with 5.1, 5.0, 4.51, and 4.41 specifications; ÿ Supports three data bus widths: 1 bit, 4 bit, and 8 bit; ÿ Supports HS400 mode, and is backward compatible with HS200, DDR50 and other modes; ÿ Supports CMD Queue.

2.1.8.2 eMMC Circuit Design Recommendations

RK3588 eMMC interface and FSPI Flash (a multiplexed port FSPI_M0) interface are multiplexed. When designing the eMMC interface, eMMC

Please refer to the reference schematic for signal connection, including decoupling capacitors for each power supply.

When using eMMC, the boot code is placed in the eMMC.

2.1.8.3 eMMC Topology and Matching Design

eMMC connection diagram:

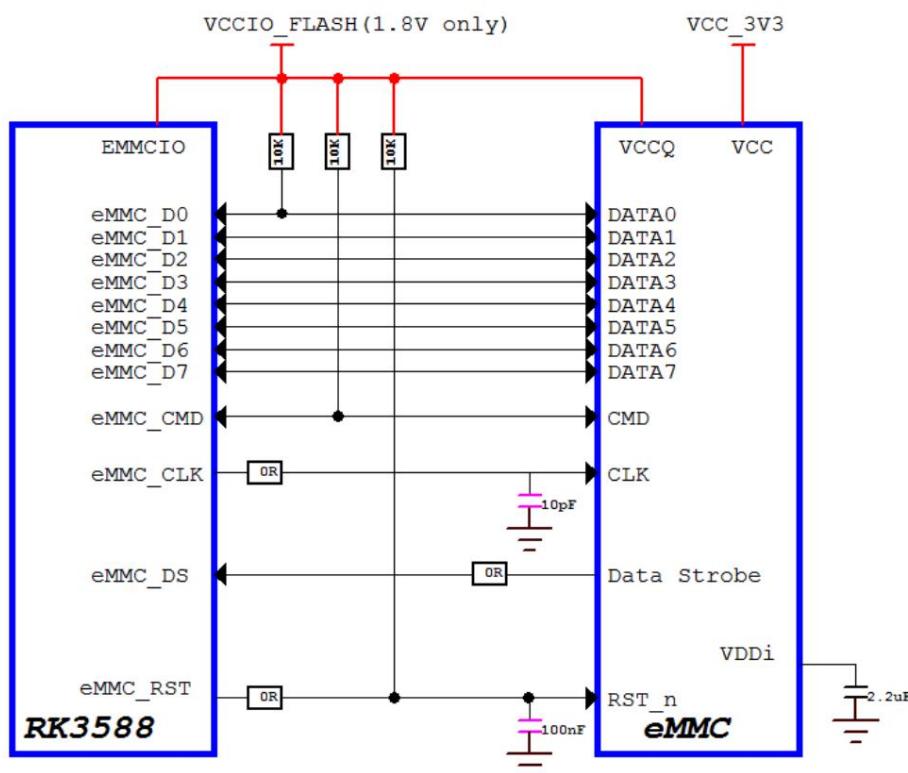


Figure 2-21 eMMC connection diagram

Table 2-6 shows the recommended pull-up and pull-down and matching design for the eMMC interface.

Table 2-6 RK3588 eMMC interface design

Signal	Pull up and down inside the chip	Connection method	Description (chip side)
eMMC_D[7:0] pull-up		Direct connection, D0 needs to be connected to a pull-up resistor. The recommended value is 10K ohm, other Data Pull-up resistor inside the RK3588 chip	eMMC data sending/receiving
eMMC_CLK	drop down	Connect a 0ohm resistor in series with the RK3588 terminal	eMMC clock transmission
eMMC_CMD	Pull-up	Direct connection, external pull-up resistor is required, resistance value is recommended Recommended 10K ohm	eMMC command send/receive
eMMC_DATA_ Strobe	drop down	Connect a 0ohm resistor in series with the eMMC terminal and Reserve 47K ohm pull-down resistor	eMMC data and command reception reference Strobe

2.1.8.4 eMMC Power-On Sequence Requirements

The eMMC interface of the RK3588 chip belongs to the EMMCIO power domain, has only one set of power supplies, and has no timing requirements.

eMMC chips have two power supplies. Please refer to the JEDEC standard for the power-on sequence:

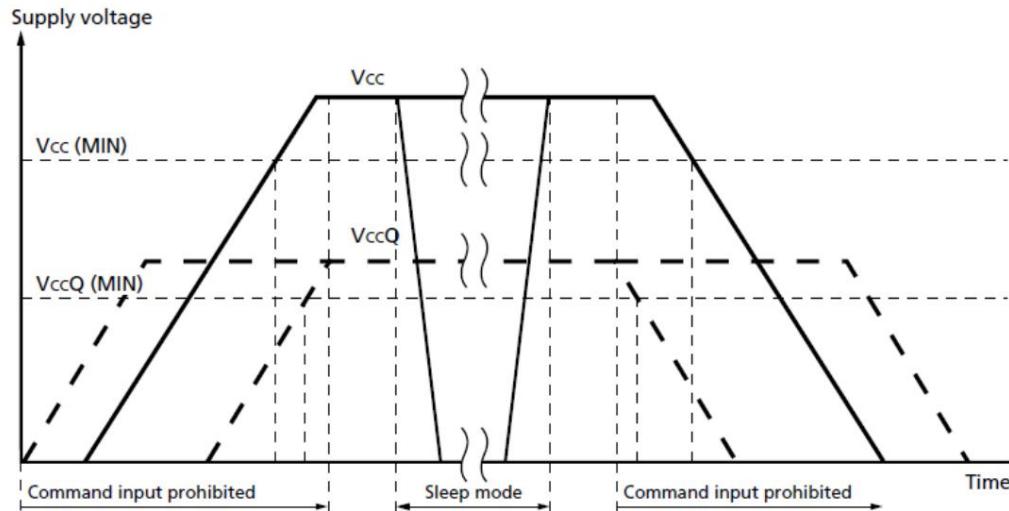


Figure 2-22 eMMC chip power-on and power-off timing

2.1.8.5 List of eMMC-supported models

For the list of RK3588 eMMC particles supported, please refer to Rockchip Electronics' RKeMMCSupportList document.

Download from the Redmine platform:

The document is not yet completed, and the address will be attached after it is released.

2.1.9 FSPI Flash Circuit

2.1.9.1 Introduction to the FSPI Flash (Boot Support) Interface

FSPI is a flexible serial interface controller. There is one FSPI controller in the RK3588 chip, which can be used to connect FSPI devices.

The RK3588 FSPI controller has the following features:

- ÿ Support serial NOR Flash and serial Nand Flash;
- ÿ Support SDR mode;
- ÿ Supports 1-wire, 2-wire and 4-wire modes.



Notice:

RK3588 FSPI Interface for connecting **Boot** of **SPI Flash** It is not recommended to use it for other functions. **SPI FLASH**

2.1.9.2 FSPI Flash Circuit Design Recommendations

The RK3588 FSPI Flash interface has three multiplexed interfaces (suffix _M0, suffix _M1, suffix _M2, only one can be used at the same time).

The three multiplexed interfaces are distributed in three power domains, namely EMMCIO (supports only 1.8V), VCCIO3 (supports only 1.8V), VCCIO5 (Support 1.8V/3.3V) in three power domains.

When designing the FSPI Flash interface, please follow the reference schematic for FSPI Flash signal connections, including the power decoupling capacitors for each channel.

When using FSPI Flash, the boot code is placed in FSPI Flash. Be sure to pay attention to the IO drive voltage mode of the corresponding power domain of RK3588.

Check whether the mode configuration and the actual supply voltage match.

2.1.9.3 FSPI Flash Topology and Matching Design

FSPI Flash connection diagram:

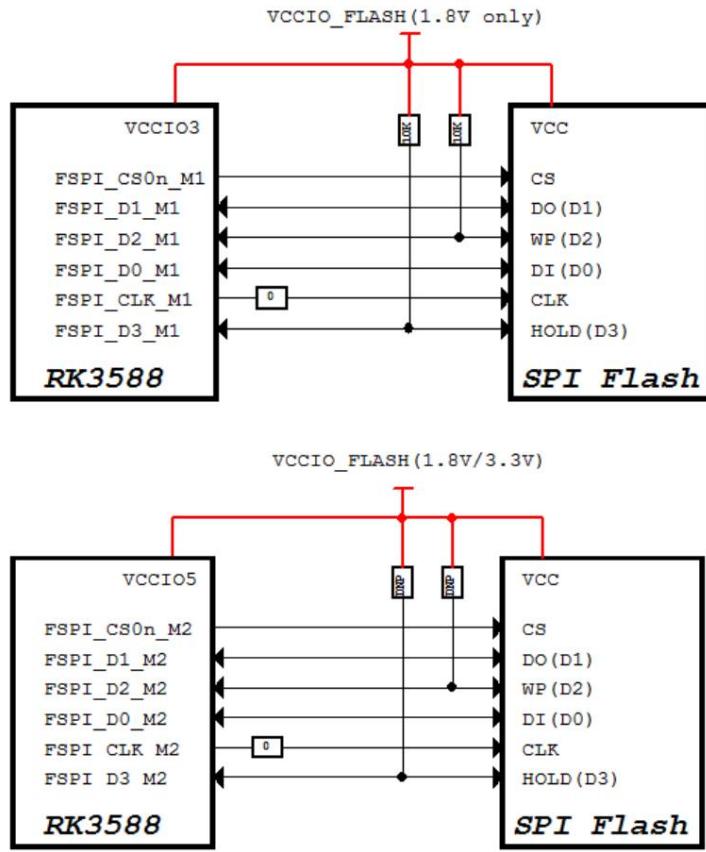


Figure 2-23 FSPI Flash connection diagram

The pull-up and matching design recommendations for the FSPI interface are shown in the following table:

Table 2-7 RK3588 FSPI interface design

Signal	Pull up and down inside the chip	Connection method	Description (chip side)
FSPI_D[3:y0]	D2 Pull-Down D0/D1/D3 pull-up	Direct connection; D2, D3 need to reserve pull-up resistors externally. The recommended reserved resistance value is 10K ohm	FSPI data transmission/reception
FSPI0_CLK	drop down	Connect a 0ohm resistor in series with the RK3588 terminal	FSPI clock transmission
FSPI0_CS0n	Pull-up	Direct connection	FSPI chip select signal

2.1.9.4 FSPI power-on timing requirements

The RK3588 chip FSPI Flash interface has only one power supply and no timing requirements.

SPI Flash has only one power supply, which must be the same as the power domain power supply corresponding to the selected FSPI interface.

2.1.9.5 SPI Flash Supported Models

For the RK3588 SPI Flash particle support list, please refer to Rockchip Electronics' "RK_SpiNor_and_SLC_Nand_SupportList" document.

This document can be downloaded from Rockchip's redmine platform:

The document is not yet completed, and the address will be attached after it is released.

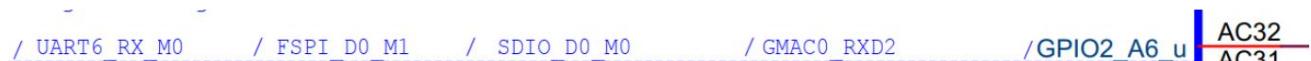
2.1.10 GPIO Circuit

In RK3588, there are two types of GPIO: one that supports only 1.8V, and the other that supports 1.8V/3.3V.

2.1.10.1 GPIO Pin Name Description

For example, the following functions GMAC0_RXD2, SDIO_D0_M0, FSPI_D0_M1 and UART6_RX_M0 are multiplexed on GPIO2_A6

Above, only one of the functions can be selected for use during allocation.



Except for the boot-related GPIO, the rest of the IO reset defaults to input;

GPIOx_xx_u, where _u means that the IO reset default state is internal pull-up; GPIOx_xx_d,

where _d means that the IO reset default state is internal pull-down; GPIOx_xx_z, where

_z means that the IO reset default state is high impedance; The suffix _M0 or M1 or

_M2 of each function name means that the same function is multiplexed to different IOs, and only one of them can be selected at the same time.

For example, when selecting the UART2 function, you must select the combination of UART2_TX_M0 and UART2_RX_M0. It does not support

The combination of UART2_TX_M0 and UART2_RX_M1 has the same constraints for all functions with different IOMUX.

2.1.10.2 GPIO drive capability

In RK3588, GPIO provides multiple levels of drive strength adjustment, most of which are Level 0-5 and some GPIOs are Level 0-3.

For details, please refer to the RK3588_PinOut document. In addition, the initial default drive strength varies depending on the GPIO type. Please refer to the chip TRM for configuration modification. You can also refer to the "SupportDriveStrength" and "DefaultIO DriveStrength" columns in Table 5 of the RK3588_PinOut document.

2.1.10.3 GPIO Power Supply

The power pins of the GPIO power domain are described as follows:

Table 2-8 RK3588 GPIO power pin description

Power domain	IO type	Pin Name	describe
PMUIO1	1.8V	PMUIO1	1.8V Only IO supply for this GPIO domain (group).
PMUIO2	1.8V/3.3V	PMUIO2	1.8V or 3.3V IO supply for this GPIO domain (group).
EMMCIO 1.8V		EMMCIO	1.8V Only IO supply for this GPIO domain (group).
VCCIO1	1.8V	VCCIO1	1.8V Only IO supply for this GPIO domain (group).
VCCIO2	1.8V/3.3V	VCCIO2	1.8V or 3.3V IO supply for this GPIO domain (group).
VCCIO3	1.8V	VCCIO3	1.8V Only IO supply for this GPIO domain (group).
VCCIO4	1.8V/3.3V	VCCIO4	1.8V or 3.3V IO supply for this GPIO domain (group).
VCCIO5	1.8V/3.3V	VCCIO5	1.8V or 3.3V IO supply for this GPIO domain (group).
VCCIO6	1.8V/3.3V	VCCIO6	1.8V or 3.3V IO supply for this GPIO domain (group).

PMUIO1, EMMCIO, VCCIO1, and VCCIO3 are fixed-level power domains and cannot be configured.

PMUIO2, VCCIO2, VCCIO[4:6] power domain **RK3588** chip can automatically identify the voltage of the hardware configuration, without the need for software

Configure according to the hardware supply voltage.

Reference Documents:

1) DTS configuration documentation: None

2) Checklist: None

ÿ In addition, please note that the IO level of the power domain must be consistent with the IO level of the connected peripheral chip/device;

ÿ Each power domain power supply pin must be placed near at least one 100nF decoupling capacitor. For detailed design, see the reference schematic diagram. Do not delete it at will.

remove;

ÿ If all IOs in a power domain are not used, the power supply of this power domain can be unpowered and the pin can be left floating.

(TYPEC0 excluded)

2.2 Power Supply Design

2.2.1 Introduction to RK3588 Power Supply

2.2.1.1 RK3588 chip power requirements

Table 2-9 RK3588 chip power requirements

Module	Power pin	describe
PLL	PLL_DVDD0V75\PLL_AVDD1V8	System PLL power supply
DDR PLL	DDR_CH0_PLL_DVDD\DDR_CH0_PLL_AVDD1V8 DDR_CH1_PLL_DVDD\DDR_CH1_PLL_AVDD1V8	DDR PLL power supply
DDR_MIF	DDR_CH0_VDD\DDR_CH1_VDD_MIF	DDR memory controller power supply
DDR_VDD	DDR_CH0_VDD\DDR_CH1_VDD	DDR digital core power supply
DDR_VDDQ_CK	DDR_CH0_VDDQ_CK\DDR_CH1_VDDQ_CK	CK voltage of LPDDR4/4X and LPDDR5 <small>source</small>
DDR_VDDQ_CKE	DDR_CH0_VDDQ_CKE\DDR_CH1_VDDQ_CKE	LPDDR4/4X_CKE \ LPDDR5_CS &RESET power supply
DDR_VDDQ	DDR_CH0_VDDQ\DDR_CH1_VDDQ	DDR IO power supply (except ck\cke\reset Power supply)
CPU_BIG0	VDD_CPU_BIG0	A76_0, A76_1 power supply
CPU_BIG0_MEM	VDD_CPU_BIG0_MEM	CPU_BIG0 Memory related power
CPU_BIG1	VDD_CPU_BIG1	A76_2, A76_3 power supply
CPU_BIG1_MEM	VDD_CPU_BIG1_MEM	CPU_BIG1 memory-related power
DSU\LT_CPU	VDD_CPU_LIT	DSU unit, CPU_LIT(A55), L3 cache power supply
CPU_LIT_MEM	VDD_CPU_LIT_MEM	DSU unit, CPU_LIT(A55), L3 Memory-related power supply of cache
GPU	VDD_GPU	GPU power supply
CPU_GPU_MEM	VDD_GPU_MEM	VDD_GPU memory related power supply
NPU	VDD_NPU	NPU power supply
CPU_NPU_MEM	VDD_NPU_MEM	VDD_NPU memory related power supply
LOGIC	VDD_LOG	Logic power supply
VDENC	VDD_VDENC	DECODE/ENCODE power supply
VDENC_MEM	VDD_VDENC_MEM	DECODE/ENCODE Memory <small>source</small>
PMU_0V75	PMU_0V75	PMU logic power supply
OSC	OSC_1V8	Crystal oscillator circuit power supply
IT	PMUIO1_1V8\PMUIO2_1V8\PMUIO2\EMMCIO_1V8\ VCCIO2_1V8\VCCIO2\VCCIO1_1V8\VCCIO3_1V8\ VCCIO4_1V8\VCCIO4\VCCIO5_1V8\VCCIO5\	Power supply for each GPIO

Module	Power pin	describe
	VCCIO6_1V8\VCCIO6	
SARADC	SARADC_AVDD_1V8	Power supply for SAR ADC and TSADC
OTP	OTP_VDDOTP_0V75	OTP Power Supply
USB2.0 PHY	USB20_DVDD_0V75\USB20_AVDD_1V8 USB20_AVDD_3V3	USB2.0 HOST and OTG2.0 PHY <small>source</small>
USB3.0 PHY	TYPEC0_DP0_VDD_0V85\TYPEC0_DP0_VDDA_0V85 TYPEC0_DP0_VDDH_1V8 TYPEC1_DP1_VDD_0V85\TYPEC1_DP1_VDDA_0V85 TYPEC1_DP1_VDDH_1V8	USB 3.0 OTG power supply
PCIe3.0 PHY	PCIE30_PORT0_AVDD0V75, PCIE30_PORT0_AVDD1V8\PCIE30_PORT1_AVDD0V75 PCIE30_PORT1_AVDD1V8	PCIe 3.0 PHY power supply
PCIe2.0 PHY	PCIE20_SATA30_0_AVDD_0V85 PCIE20_SATA30_0_AVDD_1V8 PCIE20_SATA30_1_AVDD_0V85 PCIE20_SATA30_1_AVDD_1V8 PCIE20_SATA30_USB30_2_AVDD_0V85 PCIE20_SATA30_USB30_2_AVDD_1V8	PCIE20/SATA30/USB30 COMBO PHY-related power supplies
MIPI D/C Combo PHY	MIPI_D/C_PHY0_VDD MIPI_D/C_PHY0_VDD_1V2 MIPI_D/C_PHY0_VDD_1V8 MIPI_D/C_PHY1_VDD MIPI_D/C_PHY1_VDD_1V2 MIPI_D/C_PHY1_VDD_1V8	MIPI D/C Combo PHY related power supply
MIPI CSI PHY	MIPI_CSI0_AVDD0V75 MIPI_CSI0_AVCC1V8, MIPI_CSI1_AVDD0V75 MIPI_CSI1_AVCC1V8	MIPI DPHY CSI Power
HDMI/eDP TX PHY	HDMI/EDP_TX0_VDD_0V75\HDMI/EDP_TX0_AVDD_0V75 HDMI/EDP_TX0_VDD_IO_1V8 HDMI/EDP_TX0_VDD_CMN_1V8 HDMI/EDP_TX1_VDD_0V75HDMI/EDP_TX1_AVDD_0V75 HDMI/EDP_TX1_VDD_IO_1V8 HDMI/EDP_TX1_VDD_CMN_1V8	HDMI2.1/eDP1.3 Combo phy power supply
HDMI RX PHY	HDMI_RX_AVDD0V75 HDMI_RX_VPH3V3 HDMI_RX_DVDD3V3	HDMI 2.0 RX PHY power supply

2.2.1.2 RK3588 chip power-on timing requirements

In theory, the low voltage of the same module should be applied first, followed by the high voltage; the same modules with the same voltage should be powered on together. There is no timing requirement between different modules. After the last voltage is powered on and stabilized, RESETn must be released for at least 1ms (if RESETn also resets other peripherals, the requirements of the peripherals must also be met. Generally, it is released within 5ms-200ms).

The typical power-on sequence recommended by the reference diagram is as follows:

Digital power supply:

```

PMU_0V75/PLL_DVDD_0V75 ý VDD_LOGIC ý
VDD_BIG0/1/VDD_GPU/VDD_NPU/VDD_VDENC ý
VDD_BIG0/1_MEM/VDD_GPU_MEM/VDD_NPU_MEM/VDD_VDENC_MEM
ý SARADC:
    VDD_LOGIC ý SARADC_AVDD_1V8
    ý OTP ý
    VDD_LOGIC ý OTP_VDDOTP_0V75
    ý USB PHY ý
    USB20_DVDD_0V75 ý USB20_AVDD_1V8 ý USB20_AVDD_3V3
    TYPEC_DP_VDD_0V85 /TYPEC_DP_VDDA_0V85 ý TYPEC_DP_VDDH_1V8
    ý MIPI D/C_PHY ý
    MIPI_D/C_PHY_VDD ý MIPI_D/C_PHY_VDD_1V8 ý MIPI_D/C_PHY_VDD_1V2
    ý MIPI CSI PHY ý
    MIPI_CSI_AVDD0V75 ý MIPI_CSI_AVCC1V8
    ý HDMI RX PHY ý
    HDMI_RX_AVDD0V75 ý HDMI_RX_VPH3V3 / HDMI_RX_DVDD3V3
    ý HDMI/eDP TX Combo PHY ý
    HDMI/EDP_TX_VDD_0V75 / HDMI/EDP_TX_AVDD_0V75 ý HDMI/EDP_TX_VDD_IO_1V8 /
    HDMI/EDP_TX_VDD_CMN_1V8
    ý PCIE20/SATA30 Combo PHY ý
    PCIE20_SATA30_AVDD_0V85 ý PCIE20_SATA30_AVDD_1V8
    PCIE20/SATA30/USB30 Combo PHY
    PCIE20_SATA30_USB30_AVDD_0V85 ý PCIE20_SATA30_USB30_AVDD_1V8
    ý DDR PHY ý
    DDR_CH_VDD / DDR_VDD_MIF ý DDR_CH_VDDQ_CKE ý DDR_VDDQ

```

According to the power network names assigned in the reference schematic, the overall recommended power-on sequence is as follows:

```

VDD_0V75_S3 ý AVDD_0V75_S0 ý VDD_0V75_PLL_S0 ý VDD_0V75_HDMI_EDP_S0 ý VDD_0V85_S0 ý
AVDD_V085_S0 ý VDD_DDR_S0 ý VDD_DDR_PLL_S0 ý VDD_LOGIC ý VCC_1V8_S0 ý AVDD_1V8_S0 ý
VCC_1V8_S3 ý VDD1_1V8_DDR_S3 ý VDD_1V8_PLL_S0 ý AVDD1V8_DDR_PLL_S0 ý VDD2_DDR_S3 ý
AVDD_1V2_S0 ý VDD2L_0V9_DDR_S3 ý VCC_3V3_S0 ý VCC_3V3_S3 ý VDDQ_DDR_S0 ý VCCIO_SD_S0 ý
VCC_3V3_SD_S0 ý VDD_CPU_LIT_S0 ý VDD_CPU_LITMEM ý VDD_CPU_BIG0_S0 ý
VDD_CPU_BIG0_MEM_S0 ý VDD_CPU_BIG1_S0 ý VDD_CPU_BIG1_MEM_S0 ý RESETn

```

2.2.1.3 RK3588 chip power-off timing requirements

During the power-off process, RESETn must be pulled low first, and then all power supplies are powered off.

2.2.2 Power Supply Design Recommendations

2.2.2.1 Power-on and standby circuit solutions

The power supply status of each module when RK3588 is powered on for the first time is as follows:

Table 2-10 Power supply requirements for each module when RK3588 is powered on for the first time

Module	Power pin	Power supply requirements for the first time
DDR PLL	DDR_CH0/1_PLL_DVDD _y	Power supply required
	DDR_CH0/1_PLL_AVDD1V8	
SYSPLL	PLL_DVDD0V75 _y PLL_AVDD1V8	Power supply required
CPU	VDD_CPU_BIG0 _y VDD_CPU_BIG1 _y	Power supply required
	VDD_CPU_BIG0_MEM _y	
	VDD_CPU_BIG1_MEM _y	
GPU	VDD_GPU _y VDD_GPU_MEM	Power supply required
NPU	VDD_NPU _y VDD_NPU_MEM	Power supply required
VDENC	VDD_VDENC,VDD_VDENC_MEM	Power supply required
LIT	VDD_CPU_LIT _y VDD_CPU_LIT_MEM	Power supply required
Logic	VDD_LOGIC	Power supply required
PMU Logic	PMU_0V75	Power supply required
DDR	DDR_CH0/1_VDD _y DDR_CH0/1_VDD_MIF _y	Power supply required
	DDR_CH0/1_VDDDQ _y DDR_CH0/1_VDDDQ_CK _y	
	DDR_CH0/1_VDDDQ_CKE	
GPIO	PMUIO1 _y PMUIO2	Power supply required
GPIO	EMMCIO_1V8	Power supply required
GPIO	VCCIO2	Power supply required
GPIO	VCCIO1, VCCIO3, VCCIO4, VCCIO5, and VCCIO6 do not need to be powered	
SARADC	SARADC_AVDD_1V8	Power supply required
OTP	OTP_VDDOTP_0V75	Power supply required
USB3.0 PHY	TYPEC0_DP0_VDD_0V85 _y	Power supply required
	TYPEC0_DP0_VDDA_0V85 _y	
	TYPEC0_DP0_VDDH_1V8	
USB2.0 PHY	TYPEC1_DP1_VDD_0V85 _y	No power supply required
	TYPEC1_DP1_VDDA_0V85 _y	
	TYPEC1_DP1_VDDH_1V8	
USB2.0 PHY	USB20_DVDD_0V75 _y USB20_AVDD_1V8 _y	Power supply required
	USB20_AVDD_3V3	

Module	Power pin	Power supply requirements for the first time
PCIe2.0/SATA3.0 Combo PHY PCIE20_SATA30_0/1_AVDD_0V85	PCIE20_SATA30_0/1_AVDD_1V8	No power supply required
PCIe2.0/SATA3.0/USB3.0 Combo PHY	PCIE20_SATA30_USB30_2_AVDD_0V85 PCIE20_SATA30_USB30_2_AVDD_1V8	No power supply required
PCIe3.0 PHY	PCIE30_PORT0_AVDD0V75, PCIE30_PORT0_AVDD1V8	No power supply required
MIPI CSI RX PHY	MIPI_CSI0_AVDD0V75 MIPI_CSI0_AVCC1V8	No power supply required
MIPI D/C Combo PHY	MIPI_D/C_PHY0/1_VDD MIPI_D/C_PHY0/1_VDD_1V2 MIPI_D/C_PHY0/1_VDD_1V8	No power supply required
HDMI/EDP Combo PHY	HDMI/EDP_TX0/1_VDD_0V75 HDMI/EDP_TX0/1_AVDD_0V75 HDMI/EDP_TX0/1_VDD_IO_1V8 HDMI/EDP_TX0/1_VDD_CMN_1V8	No power supply required
HDMI2.0 RX PHY	HDMI_RX_AVDD_0V75 HDMI_RX_VPH3V3 HDMI_RX_DVDD_3V3	No power supply required

The RK3588 chip supports low-power standby solutions. When entering standby mode, the power supply and power-off conditions are as follows:

Table 2-11 RK3588 standby power supply requirements

Module	Power pin	Standby power requirements
DDR PLL	DDR_CH0/1_PLL_DVDD DDR_CH0/1_PLL_AVDD1V8	No power supply required
SYSPLL	PLL_DVDD0V75 PLL_AVDD1V8	No power supply required
CPU	VDD_CPU_BIG0 VDD_CPU_BIG1	No power supply required
GPU	VDD_GPU	No power supply required
NPU	VDD_NPU	No power supply required
VDENC	VDD_VDENC	No power supply required
Logic	VDD_LOGIC	No power supply required
PMU Logic	PMU_0V75	Power supply required
DDR	DDR_CH0/1_VDDQ_CKE	Power supply required
GPIO	PMUIO1 PMUIO2	Power supply required
GPIO	EMMCIO_1V8	No power supply required
GPIO	VCCIO2	No power supply required
GPIO	VCCIO1, VCCIO3, VCCIO4, VCCIO5, and VCCIO6 do not need to be powered	
SARADC	SARADC_AVDD_1V8	No power supply required
OTP	OTP_VDDOTP_0V75	No power supply required
USB3.0 PHY	TYPEC0_DP0_VDD_0V85 TYPEC0_DP0_VDDA_0V85	No power supply required

Module	Power pin	Standby power requirements
	TYPEC0_DP0_VDDH_1V8 TYPEC1_DP1_VDD_0V85 TYPEC1_DP1_VDDA_0V85 TYPEC1_DP1_VDDH_1V8	
USB2.0 PHY	USB20_DVDD_0V75 USB20_AVDD_1V8 USB20_AVDD_3V3	No power supply required
PCIe2.0/SATA3.0 Combo PHY	SATA30_0/1_AVDD_0V85 PCIE20_SATA30_0/1_AVDD_1V8	No power supply required
PCIe2.0/SATA3.0/USB3.0 Combo PHY	PCIE20_SATA30_USB30_2_AVDD_0V85 PCIE20_SATA30_USB30_2_AVDD_1V8	No power supply required
PCIe3.0 PHY	PCIE30_PORT0_AVDD0V75, PCIE30_PORT0_AVDD1V8	No power supply required
MIPI CSI RX PHY	MIPI_CSI0_AVDD0V75 MIPI_CSI0_AVCC1V8	No power supply required
MIPI D/C Combo PHY	MIPI_D/C_PHY0/1_VDD MIPI_D/C_PHY0/1_VDD_1V2 MIPI_D/C_PHY0/1_VDD_1V8	No power supply required
HDMI/EDP Combo PHY	HDMI/EDP_TX0/1_VDD_0V75 HDMI/EDP_TX0/1_AVDD_0V75 HDMI/EDP_TX0/1_VDD_IO_1V8 HDMI/EDP_TX0/1_VDD_CMN_1V8	No power supply required
HDMI2.0 RX PHY	HDMI_RX_AVDD_0V75 HDMI_RX_DVDD_3V3	No power supply required

This standby solution can only support IO interrupt wakeup of PMUIO1 and PMUIO2.

In standby mode, at least the following power supplies should be kept on (the following are the power pin names):

DDR_CH0/1_VDDQ_CKE: Provides power for DDR self-refresh;

PMU_0V75: Provides power for the logic of PMUIO1 & PMUIO2 power domains;

PMUIO1_1V8: Provides power for PMU1 operation; provides IO power for PMUIO1 power domain to maintain output status and interrupt response.

source;

PMUIO2_1V8: Provides IO power for the PMUIO2 power domain to maintain output status and respond to interrupts.

In standby mode, to support USB HID device wake-up, the USB PHY and VDD_LOG power supplies must not be powered off and must remain powered;

To support IO interrupt wakeup in VCCIO1, VCCIO2, VCCIO3, VCCIO4, VCCIO5, VCCIO6, and EMMCIO_1V8,

Then you need VCCIO1, VCCIO2, VCCIO3, VCCIO4, VCCIO5, VCCIO6, EMMCIO_1V8 power supply and LOGIC power supply.

The power source cannot be cut off and the power supply must be maintained.

2.2.2.2 PLL Power Supply

The RK3588 chip PLL is distributed in two parts, as follows:

Table 2-12 RK3588 internal PLL introduction

	power supply	Standby mode

Inside the PMU unit	PLL_DVDD0V75\PLL_AVDD1V8	Power can be turned off
DDR PLL	DDR_CH0_PLL_DVDD\ DDR_CH0_PLL_AVDD1V8	Power can be turned off

\ PLL_DVDD0V75: Peak current 20mA \ PLL_AVDD1V8: Peak current 40 \

DDR_CH0_PLL_DVDD: Peak current 20mA \

DDR_CH0_PLL_AVDD1V8: Peak current 30 It is recommended to use LDO power supply:

\ 0.75V AC requirement: <20mV; \ 1.8V AC requirement: <50mV A

stable PLL power supply helps improve chip operating stability,

and the decoupling capacitors should be placed close to the pins. For specific capacitor quantity and capacity, refer to

Schematic diagram, please do not adjust it at will.

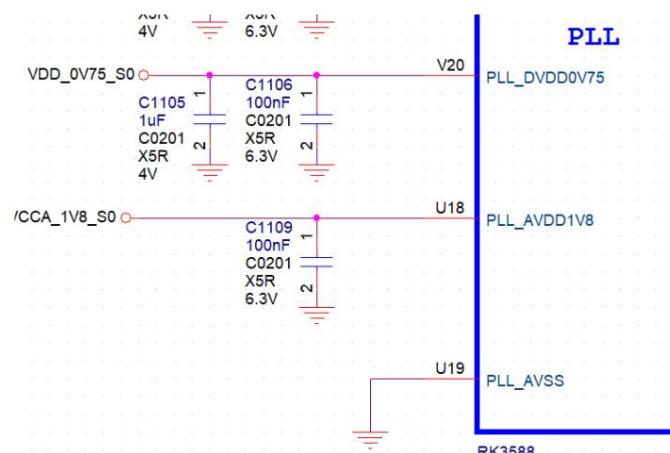


Figure 2-24 RK3588 chip SYS PLL power pin



Figure 2-25 RK3588 chip DDR PLL power pin

2.2.2.3 OSC Power Supply

The power supply OSC_1V8 of the RK3588 chip provides power for the crystal oscillator circuit.

\ OSC_1V8: Peak current <10mA. It is recommended to use

LDO power supply:

\ 1.8V AC requirement: <20mV Stable OSC power supply helps

improve chip working stability, and decoupling capacitors should be placed close to the pins. The specific number and capacity of capacitors are shown in the table below.

Refer to the schematic diagram and do not adjust it arbitrarily. Consider using a separate LDO power supply. For cost reasons, this power supply can be shared with the PLL power supply.

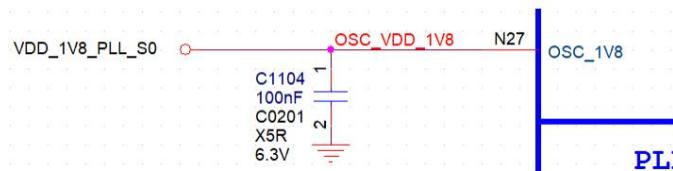


Figure 2-26 Power pins of the RK3588 chip crystal oscillator circuit

2.2.2.4 PMU LOGIC Power Supply

The PMU_0V75 power supply of RK3588 supplies power to the LOGIC of the internal PMU unit. The peak current is TBD. Please do not delete the RK3588 chip.

Decoupling capacitors in the reference design schematic.

Can be powered by DC/DC or LDO.

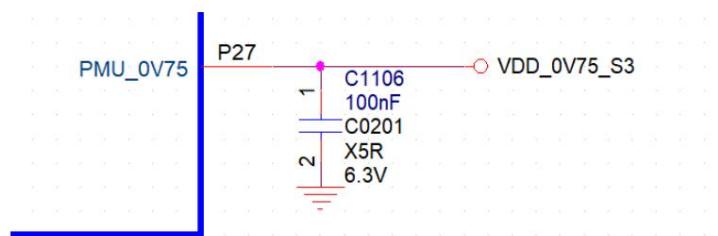


Figure 2-27 RK3588 chip PMU_0V75 power pin

2.2.2.5 VDD_CPU_BIG0 Power Supply

The RK3588's VDD_CPU_BIG0 power supply supplies the A76's CORE1 and CORE2 units. It uses an RK806 BUCK2 or DC/DC power supply, supports dynamic frequency and voltage regulation, and has a default supply voltage of 0.75V. Peak current can reach over 3.5A. Do not delete the decoupling capacitors in the RK3588 chip reference design schematic.

The main requirements for DC/DC BUCK are as follows:

Output current greater than 3.5A with a 20% margin; Output voltage

accuracy required to be $\pm 1.5\%$; BUCK transient

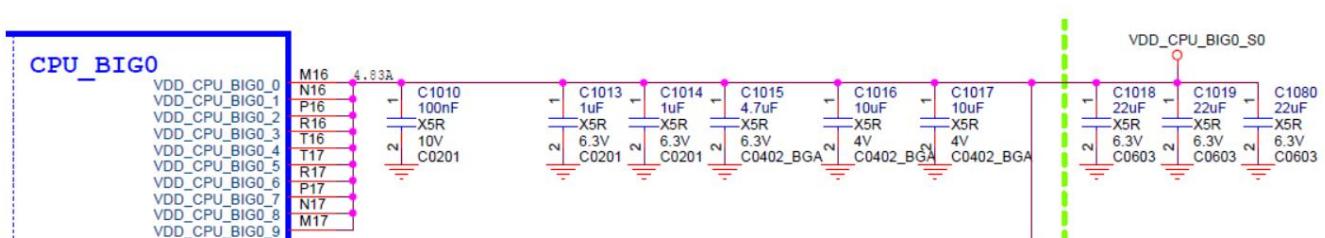
response requirements: $I_{load} = \text{BUCK Max current} * 10\% \sim \text{BUCK Max current} * 80\%$ jump, slope 1A/us, ripple

The wave is required to be within $\pm 3\%$;

If you are sensitive to the power consumption of the entire machine, you also need to consider the efficiency issue.

During layout, place the capacitors between the green line and the chip on the back of the RK3588 chip.

The capacitance must be greater than 150uF to ensure that the power ripple is within 85mV and avoid excessive power ripple under heavy load conditions.



Note: In scenarios where power consumption is not a high priority, VDD_CPU_BIG0_MEM can be combined with VDD_CPU_BIG0 for power supply.

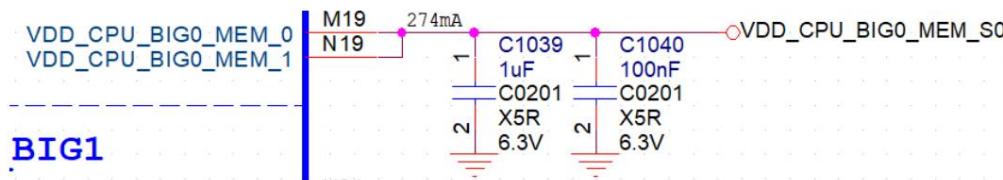


Figure 2-29 RK3588 chip VDD_CPU_BIG0_MEM power supply

2.2.2.6 VDD_CPU_BIG1 Power Supply

The VDD_CPU_BIG1 power supply of RK3588 is used to power the CORE3 and CORE4 units of A76, using the BUCK or

It is powered by a DC/DC power supply and supports dynamic frequency and voltage regulation. The default supply voltage is 0.75V. The peak current can reach more than 4.83A.

Do not delete the decoupling capacitors in the RK3588 chip reference design schematic.

The main requirements for DC/DC BUCK are as follows:

- ŷ Output current is greater than or equal to 3.5A with a 20% margin;
- ŷ Output voltage accuracy is required to be $\pm 1.5\%$;
- ŷ Buck transient response requirements: $I_{load} = \text{Buck Max current} * 10\% \sim \text{Buck Max current} * 80\%$ jump, slope 1A/us, ripple

The wave is required to be within

$\pm 3\%$. If you are sensitive to the power consumption of the whole machine, you also need to consider the efficiency issue.

During layout, place the capacitors between the green line and the chip on the back of the RK3588 chip.

The capacitance must be greater than 150uF to ensure that the power ripple is within 85mV and avoid excessive power ripple under heavy load conditions.

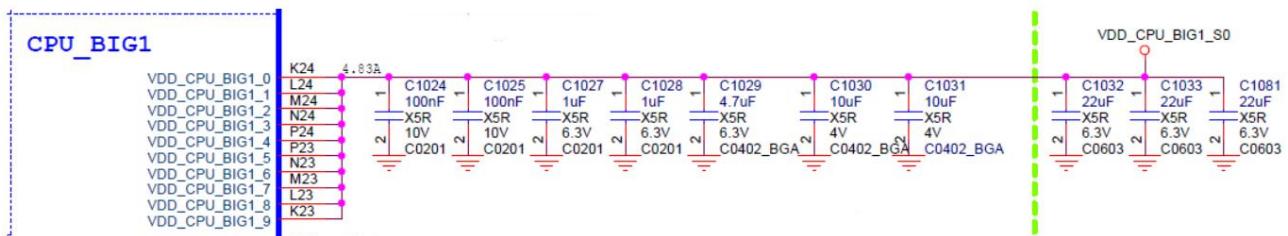


Figure 2-30 RK3588 chip VDD_CPU_BIG1 power pin

VDD_CPU_BIG1_MEM is the memory power supply for A76 CORE3 and CORE4. The current can reach 100mA.

To adjust the voltage, you can use a BUCK power supply. The following two capacitors C1014 and C1015 must be placed under the RK3588 pins.

Note: In scenarios where power consumption is not a high priority, VDD_CPU_BIG1_MEM can be combined with VDD_CPU_BIG1 for power supply.

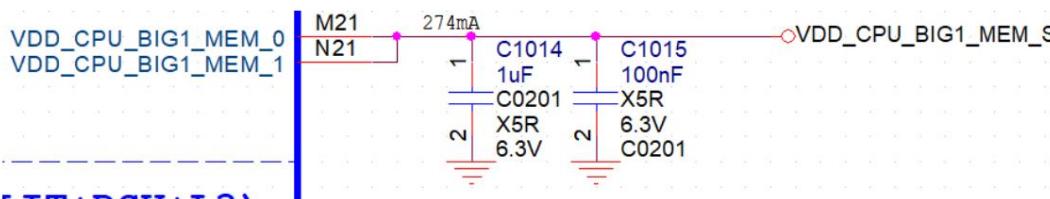


Figure 2-31 RK3588 chip VDD_CPU_BIG1_MEM power supply

2.2.2.7 VDD_CPU_LIT Power Supply

The VDD_CPU_LIT power supply of RK3588 provides power to the internal ARM Cortex-A55 core, DSU logic, control, and L3 cache.

It uses the RK806 BUCK power supply and supports dynamic frequency and voltage regulation. The peak current can reach over 2.5A. Please do not delete the decoupling capacitor in the RK3588 chip reference design schematic.

The main requirements for DC/DC BUCK are as follows:

- ŷ Output current is greater than or equal to 2.5A with a 20% margin;
- ŷ Output voltage accuracy is required to be $\pm 1.5\%$;
- ŷ Buck transient response requirements: $I_{load} = \text{Buck Max current} * 10\% - \text{Buck Max current} * 80\% \text{ jump, slope } 1\text{A/us, ripple}$

The wave is required to be within $\pm 3\%$;

If you are sensitive to the power consumption of the entire machine, you also need to consider the efficiency issue.

During layout, place the capacitors from the green line to the chip position below the RK3588 chip. The total capacitance of the VDD_CPU_LIT power supply must be greater than 150uF (it is recommended to reserve 1-2 22uF capacitors, which can be omitted by default) to ensure that the power supply ripple is within 85mV to avoid large Under load conditions, the power supply ripple is too large.

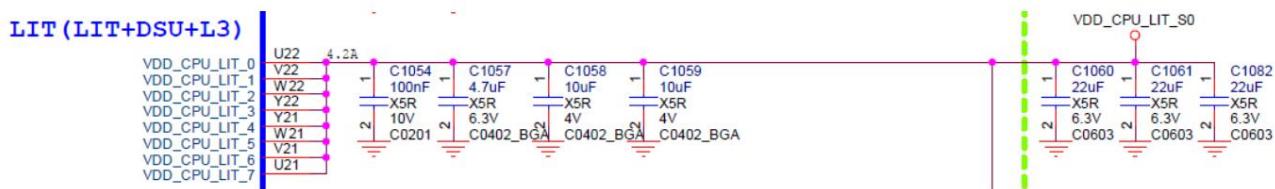


Figure 2-32 VDD_CPU_LIT power supply capacitor

The VDD_CPU_LIT_MEM power supply is the memory power supply for the A55 and DSU. It can draw up to 100mA and requires voltage regulation. It can be powered by a buck converter. The following two capacitors, C1059 and C1060, must be placed below the RK3588 pins.

Note: In scenarios where power consumption is not a high requirement, VDD_CPU_LIT_MEM can be combined with VDD_CPU_LIT for power supply.

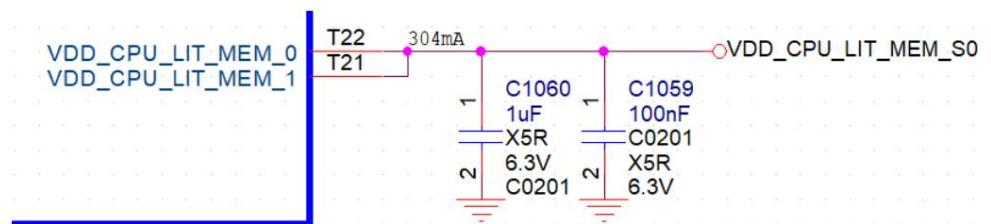


Figure 2-33 RK3588 chip VDD_CPU_LIT_MEM power supply

2.2.2.8 GPU Power Supply

The VDD_GPU power supply of RK3588 supplies power to the internal GPU unit, using BUCK1 of RK806 or RK860 for power supply, supporting dynamic

The peak current can reach 5.6A. Please do not delete the decoupling capacitor in the RK3588 chip reference design schematic.

The main requirements for DC/DC BUCK are as follows:

- ŷ Output current is greater than or equal to 5.6A with a 20% margin;
- ŷ Output voltage accuracy is required to be $\pm 1.5\%$;

$I_{load} = \text{Buck Max current} * 10\% - \text{Buck Max current} * 80\% \text{ jump, slope } 1\text{A/us, ripple}$

The wave is required to be within $\pm 3\%$;

If you are sensitive to the power consumption of the entire machine, you also need to consider the efficiency issue.

During layout, place the capacitors from the green line to the chip position on the back of the RK3588 chip. The total capacitance of the VDD_GPU power supply needs to be Greater than 200uF to ensure that the power ripple is within 100mV and avoid excessive power ripple under heavy load conditions.

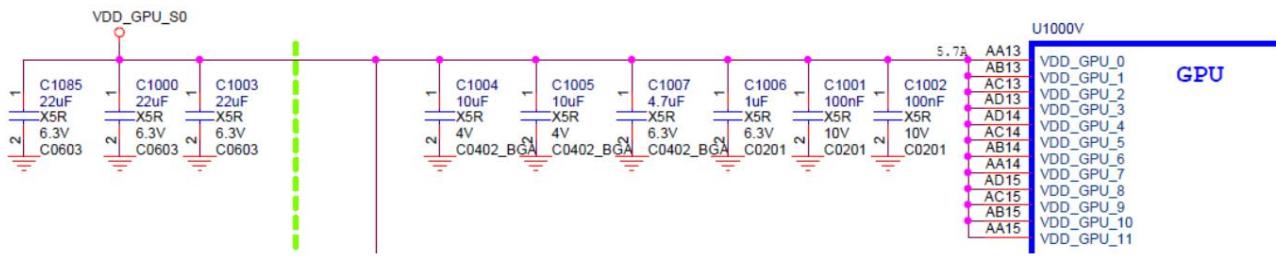


Figure 2-34 RK3588 chip VDD_GPU power pin

VDD_GPU_MEM power supply is the memory power supply of VDD_GPU_MEM. The current can reach 400mA and needs voltage regulation.

The following two capacitors C1012 and C1013 must be placed under the RK3588 pins.

Note: In scenarios where power consumption is not a high priority, VDD_GPU_MEM can be combined with VDD_GPU for power supply.

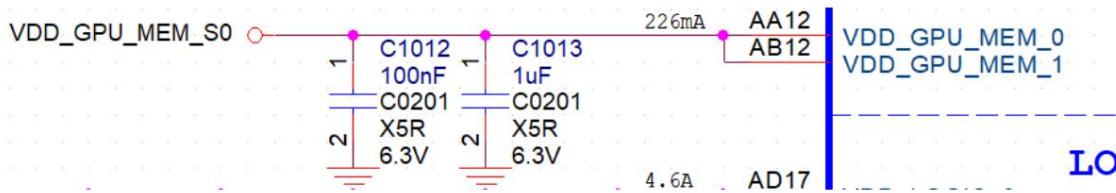


Figure 2-35 RK3588 chip VDD_GPU power pin

2.2.2.9 NPU Power Supply

The VDD_NPU power supply of RK3588 supplies power to the internal NPU unit. It uses a DC/DC power supply and supports dynamic frequency and voltage modulation. The peak current can

reach more than 4A. Please do not delete the decoupling capacitor in the RK3588 chip reference design schematic.

The main requirements for DC/DC BUCK are as follows: δ Output

current is greater than or equal to 4A with a 20% margin; δ Output voltage accuracy is

required to be $\pm 1.5\%$; δ BUCK transient response requirements:

$I_{load} = \text{BUCK Max current} * 10\% \sim \text{BUCK Max current} * 80\%$ jump, slope 1A/us, ripple

The wave is required to be within

$\pm 3\%$. If you are sensitive to the power consumption of the whole machine, you also need to consider the efficiency issue.

During layout, place the capacitors between the green line and the chip on the back of the RK3588 chip. The total capacitance of the VDD_NPU power supply needs to be

Greater than 200uF to ensure that the power ripple is within 100mV and avoid excessive power ripple under heavy load conditions.

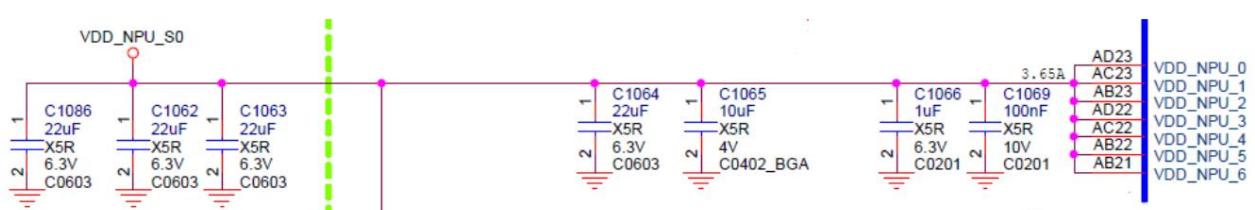


Figure 2-36 RK3588 chip VDD_NPU power pin

VDD_NPU_MEM power supply is the memory power supply of VDD_NPU. The current can reach 100mA. If voltage regulation is required, BUCK can be used.

Power supply. The following two capacitors C1057 and C1058 should be placed under the RK3588 pins.

Note: In scenarios where power consumption is not a high requirement, VDD_NPU_MEM and VDD_NPU can be combined to provide power.

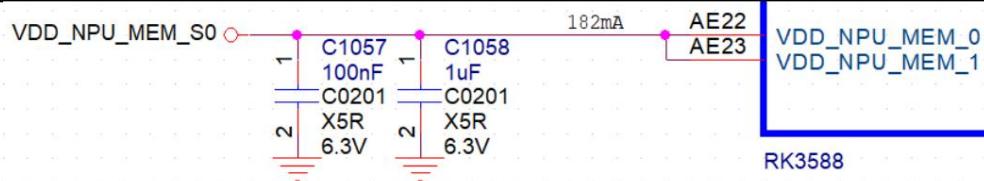


Figure 2-37 RK3588 chip VDD_NPU_MEM power pin

2.2.2.10 Logic Power Supply

The RK3588's VDD_LOGIC power supply provides power to the internal logic unit. It uses an independent DC/DC power supply, supports dynamic frequency and voltage modulation, and defaults to a fixed voltage supply. Peak current can reach over 2A. Do not delete the decoupling capacitors in the RK3588 chip reference design schematic.

The main requirements for DC/DC BUCK are as follows: \dot{y} Output

current greater than or equal to 2A; \dot{y} Output voltage

accuracy is required to be $\pm 1.5\%$; \dot{y} BUCK transient response

requirements: $I_{load} = \text{BUCK Max current} * 10\% - \text{BUCK Max current} * 80\%$ jump, slope 1A/us, ripple

The wave is required to be within

$\pm 3\%$. If you are sensitive to the power consumption of the whole machine, you also need to consider the efficiency issue.

During layout, place the capacitors between the green line and the chip on the back of the RK3588 chip. The total capacitance of the VDD_LOGIC power supply is

The value should be greater than 100uF to ensure that the power ripple is within 75mV and avoid excessive power ripple under heavy load conditions.

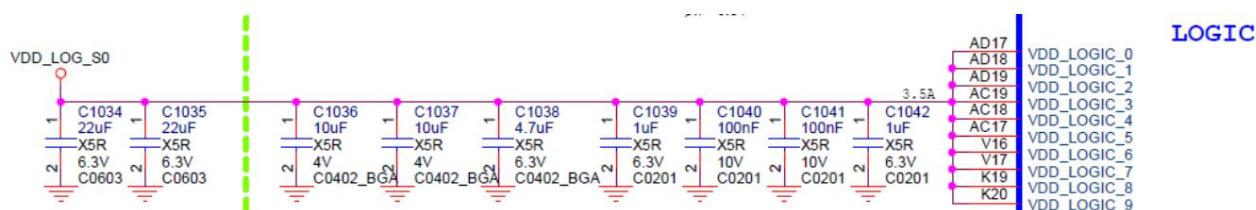


Figure 2-38 RK3588 chip VDD_LOGIC power pin

2.2.2.11 Video Power Supply

The RK3588's VDD_VDENC power supply provides power to the internal video codec logic unit. It uses an independent DC/DC power supply, supports dynamic frequency and voltage modulation, and defaults to a fixed voltage. Peak current can reach over 2A. Do not delete the decoupling capacitors in the RK3588 chip reference design schematic. The main requirements for the DC/DC buck are as follows: \dot{y} Output current greater than or equal to 2A; \dot{y} Output voltage

accuracy within $\pm 1.5\%$; \dot{y} Buck transient response requirements: I_{load}

$= \text{Buck Max current} * 10\% - \text{Buck Max current} * 80\%$,

with a slope of 1A/us and a ripple of 0.

The wave is required to be within $\pm 3\%$;

If you are sensitive to the power consumption of the entire machine, you also need to consider the efficiency issue.

During layout, place the capacitors shown in the figure below on the back of the RK3588 chip. The total capacitance of the VDD_VDENC power supply must be greater than 100uF.

To ensure that the power supply ripple is within 75mV and avoid excessive power supply ripple under heavy load conditions.

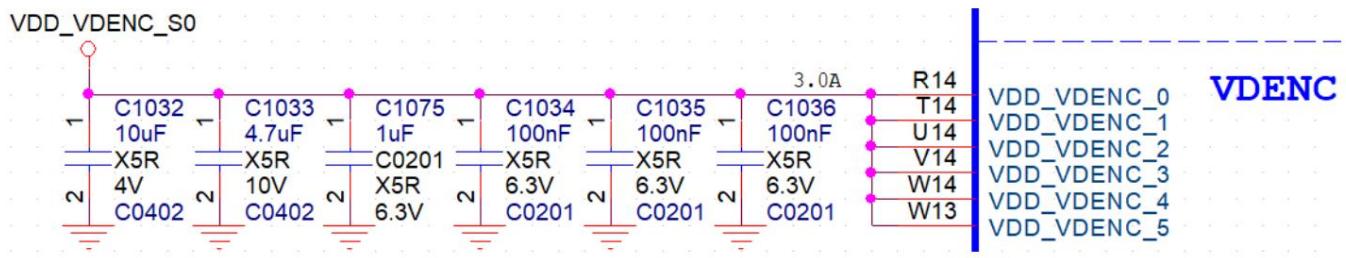


Figure 2-39 RK3588 chip VDD_VDENC power pins

VDD_VDENC_MEM power supply is the memory power supply of VDD_VDENC. The current can reach 100mA and needs voltage regulation.

Use BUCK power supply. The following two capacitors C1043 and C1044 should be placed under the RK3588 pins.

Note: In scenarios where power consumption is not a high requirement, VDD_VDENC_MEM can be combined with VDD_VDENC for power supply.

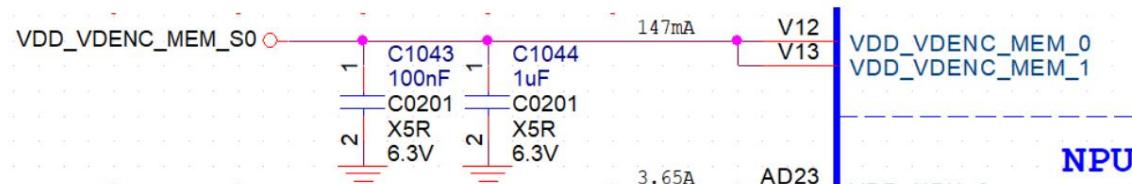


Figure 2-40 RK3588 chip VDD_VDENC power pin

2.2.2.12 DDR Power Supply

The DDR PHY interface of the RK3588 chip supports LPDDR4/LPDDR4x/LPDDR5 level standards, with two channels in total.

6 power supplies, DDR_CH0/1_PLL_DVDD, DDR_CH0/1_PLL_AVDD1V8, DDR_CH0/1_VDD_MIF,

For information about DDR_CH0/1_VDDQ_CKE, DDR_CH0/1_VDDQ_CK, and DDR_CH0/1_VDDQ, see [2.1.7.5 DDR Power Supply Design and Power-On Sequence Requirements](#). When designing your product, ensure that the chip usage meets the design requirements. Similarly, some voltages differ between LPDDR4/4X and LP5 chips. See the drawings for details.

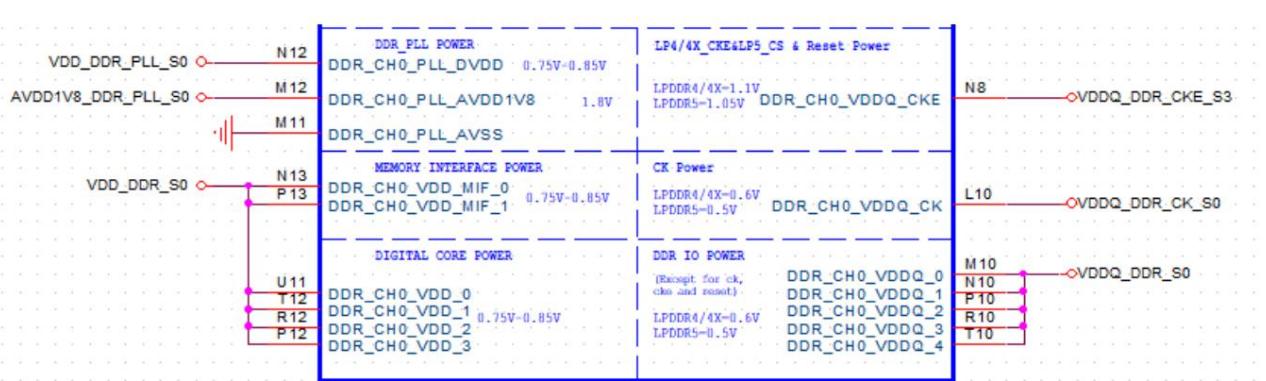


Figure 2-41 DDR power pins of the RK3588 chip in LPDDR4/4X mode

When designing the layout, place the filter capacitor shown in the figure below on the back of the RK3588 chip to ensure that the power ripple is within 80mV and avoid high load conditions.

Under such circumstances, the power supply ripple is too large.

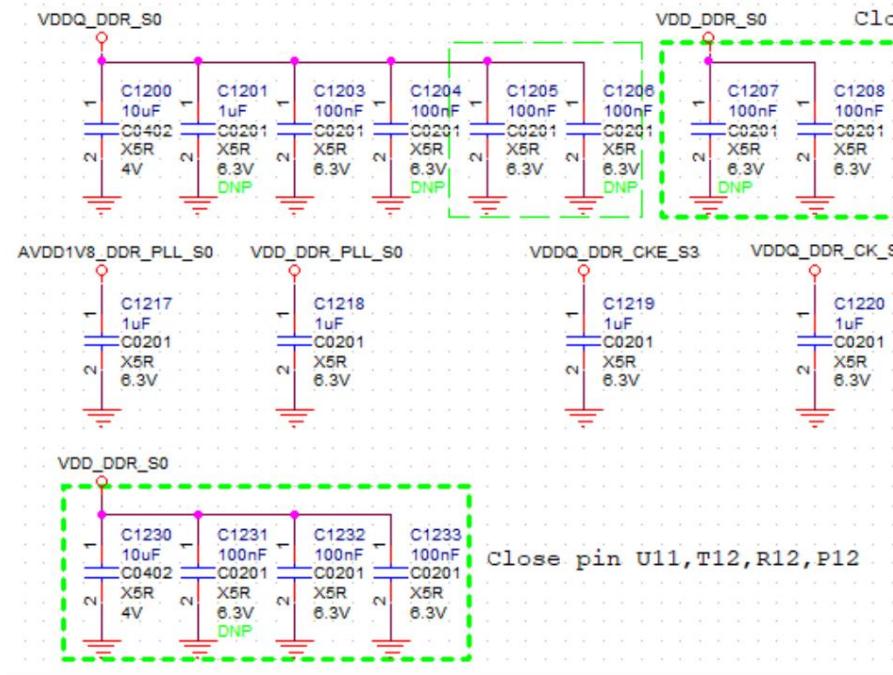


Figure 2-42 Power filter capacitors for the RK3588 chip in LPDDR4/4x mode

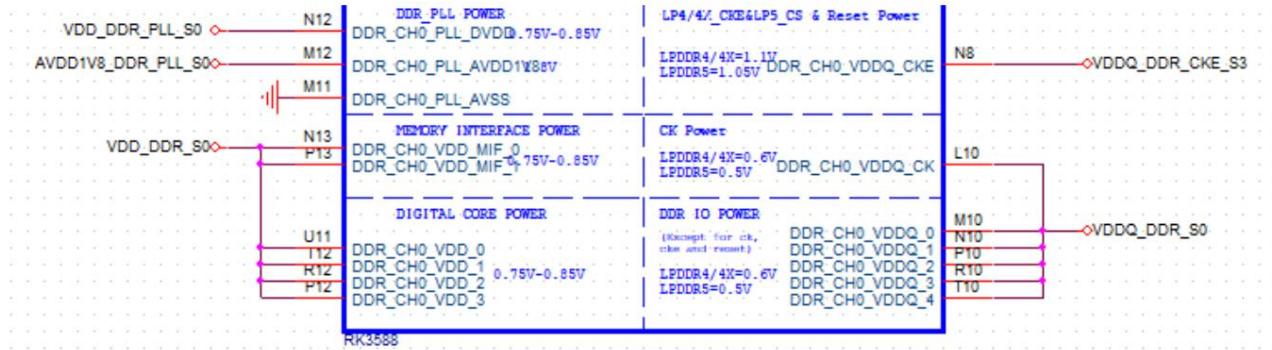


Figure 2-43 DDR power pins of the RK3588 chip in LPDDR5 mode

When designing the layout, place the filter capacitor shown in the figure below on the back of the RK3588 chip to ensure that the power ripple is within 80mV and avoid high load conditions.

Under such circumstances, the power supply ripple is too large

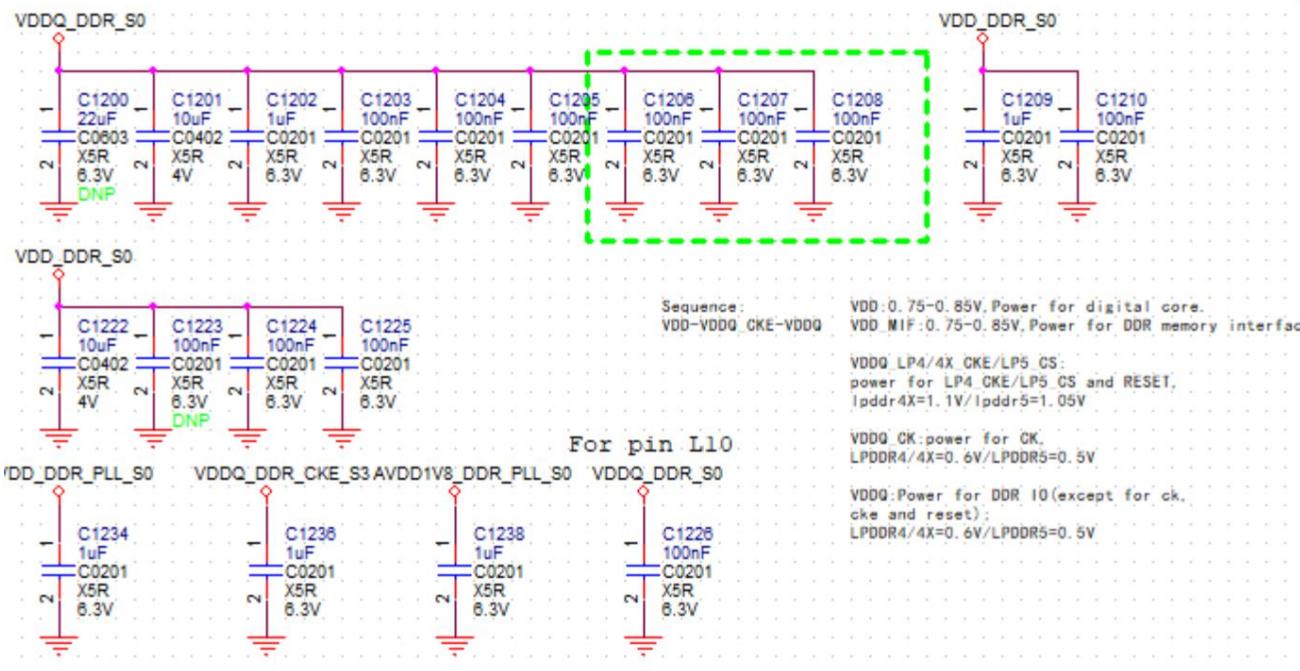


Figure 2-44 Power filter capacitors for the RK3588 chip in LPDDR5 mode

2.2.2.13 USB 2.0 PHY Power Supply

RK3588 has 4 USB2.0 interfaces. For detailed connection methods, please refer to **2.3.4 Introduction to USB2.0/USB3.0 Circuit Unit**.

USB20_DVDD_0V75, **USB20_AVDD_1V8**, **USB20_AVDD_3V3** power is provided to **USB2_HOST0/1_DP/M** and

TYPEC0/1_USB20_OTG_DP/M PHY power supply, please do not delete the decoupling capacitors in the RK3588 chip reference design schematic.

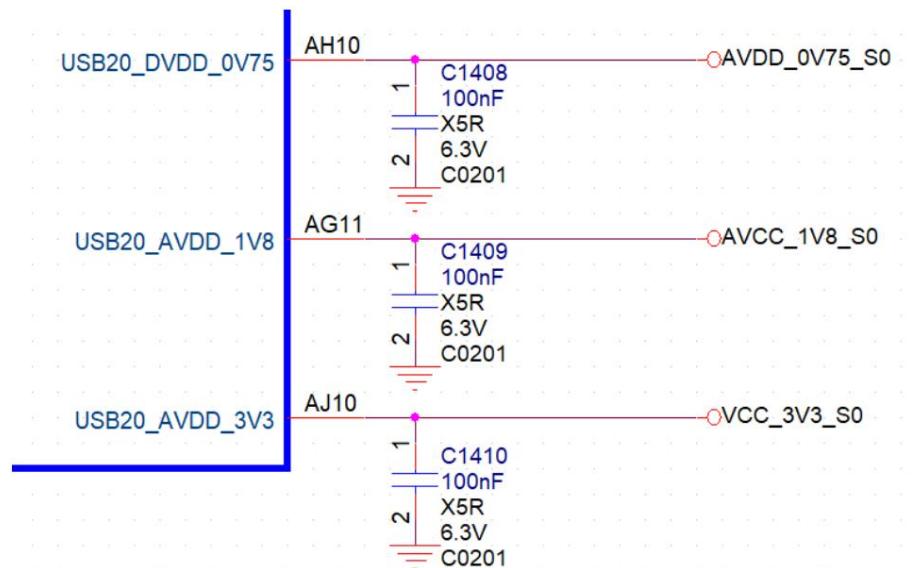


Figure 2-45 RK3588 USB2.0 PHY power pin

ÿ **USB20_DVDD_0V75**: Peak current 30mA ÿ **USB20_AVDD_1V8**:

Peak current 65mA ÿ **USB20_AVDD_3V3**: Peak current 45mA

It is recommended to use LDO power supply:

ÿ 0.75V AC requirement <25mV

ÿ 1.8V AC requirement: <50mV; ÿ 3.3V AC

requirement: <200mV A stable power supply helps

improve chip operating stability, and decoupling capacitors should be placed close to the pins. For the specific number and capacity of capacitors, refer to the principle

Since the **RK3588** chip

firmware must be downloaded from the **TYPEC0_USB20_OTG_DP/M** interface, the first time it is powered on ,

USB20_DVDD_0V75, USB20_AVDD_1V8, USB20_AVDD_3V3 must be powered.

2.2.2.14 USB3.0/DP1.4 Combo Power Supply

RK3588 has two USB30\DP1.4 Combo PHY interfaces: TYPEC0_DP0_VDD_0V85,

TYPEC0_DP0_VDDH_1V8 power supplies are for USB30/DP1.4 Combo0.

Do not delete the decoupling capacitors in the RK3588 chip reference design schematic.

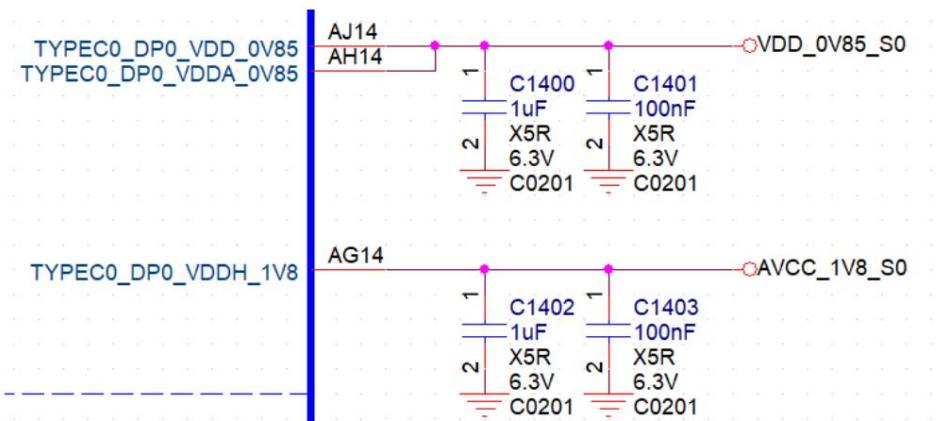


Figure 2-46 RK3588 USB30/DP1.4 Combo0 power pin

TYPEC1_DP1_VDD_0V85, TYPEC1_DP1_VDDH_1V8 power supply is for USB30/DP1.4 Combo1 power supply, please

Do not delete the decoupling capacitors in the RK3588 chip reference design schematic.

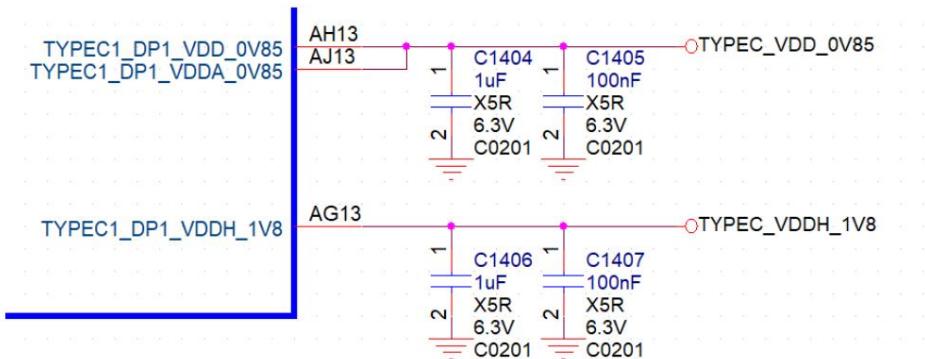


Figure 2-47 RK3588 USB30/DP1.4 Combo1 power pin

TYPEC_VDD_0V85: Peak current 40mA
TYPEC_VDDA_0V85:

Peak current 300mA
TYPEC_VDDH_1V8: Peak current 60mA

(Note: The above peak current is the total current value of the two channels combined, the same below)

It is recommended to use LDO power supply:

0.85V AC requirement <20mV

1.8V AC requirement: <50mV A stable power supply

helps improve chip operating stability, and the decoupling capacitors should be placed close to the pins. For the specific number and capacity of capacitors, refer to the principle

Please do not adjust the picture at will.

When this function is not used, the RK3588 chip firmware must be downloaded from the TYPEC0_USB20_OTG_DP/M interface.

The PHY0 port of USB30 is the same controller and has an internal logical relationship, so the PHY0 port of USB30 must also be powered;

If the USB30 PHY1 port is not used, it can be unpowered.

2.2.2.15 PCIe 2.0 PHY Power Supply

RK3588 has 2 PCIe2.0/SATA30 Combo PHY interfaces and 1 PCIe2.0/SATA30/USB30 Combo PHY.

2 PCIE20_SATA30_0/1_AVDD_0V85 , 2 PCIE20_SATA30_0/1_AVDD_1V8,

PCIE20_SATA30_USB30_2_AVDD_0V85, PCIE20_SATA30_USB30_2_AVDD_1V8, a total of 6 power supplies are used to power PCIe2.0 Combo PHY.

Please do not delete the decoupling capacitors in the RK3588 chip reference design schematic. As shown in the figure below, on the left side of the green dotted line

The capacitor layout needs to be close to the chip pins.

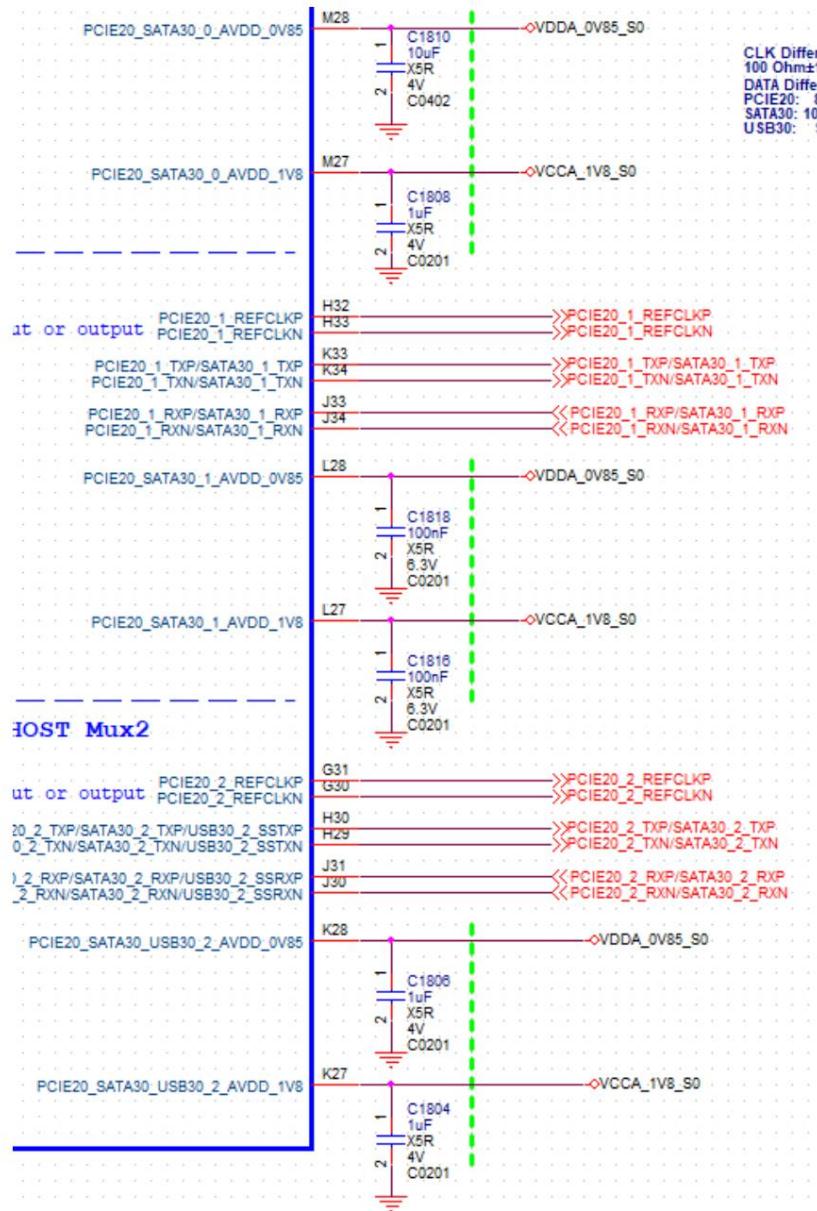


Figure 2-48 RK3588 PCIe2.0 Combo PHY power pin

PCIE20_SATA30_0/1_AVDD_0V85/PCIE20_SATA30_USB30_2_AVDD_0V85: Peak current 140mA

PCIE20_SATA30_0/1_AVDD_1V8/PCIE20_SATA30_USB30_2_AVDD_1V8: Peak current 270mA

It is recommended to use LDO power supply:

0.85V AC requirement <20mV

1.8V AC requirement <50mV

A stable power supply helps improve the working stability of the chip, and the decoupling capacitors should be placed close to the pins. The specific number and capacity of capacitors refer to the principle

Please do not adjust the picture at will.

The 6 power supplies are all independent. The 2 power supplies (0V85 and 1V8) corresponding to the PHY that do not use the PCIE function can be left unpowered and can be left floating.

2.2.2.16 PCIe 3.0 PHY Power Supply

The RK3588 has two PCIe 3.0 PHY interfaces, PCIE30_PORT0/ PORT1_AVDD0V75 and PCIE30_PORT0/ PORT1_AVDD1V8. These four power supplies are used to power the PCIe 3.0 PHY. Do not delete the decoupling capacitors in the RK3588 chip reference design schematic. As shown in the figure below, the capacitor layout on the left side of the green dotted line needs to be close to the chip pins. (The power supply for phy1 is handled the same as for phy0.)

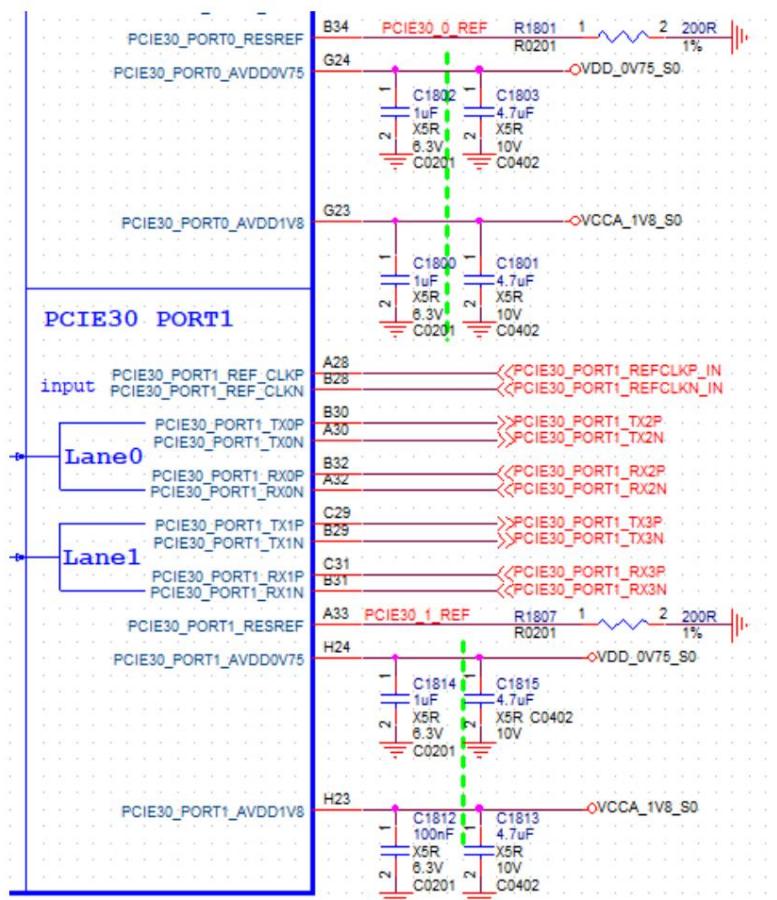


Figure 2-49 RK3588 PCIe3.0 PHY power pin

ÿ PCIE30_PORT0/ PORT1_AVDD0V75: Peak current 230mA ÿ PCIE30_PORT0/ PORT1_AVDD1V8:

Peak current 210mA It is recommended to use LDO power supply:

ÿ 0.75V AC requirement <20mV

ÿ 1.8V AC requirement: <50mV A stable power supply

helps improve chip operating stability, and the decoupling capacitors should be placed close to the pins. For the specific number and capacity of capacitors, refer to the principle

Please do not adjust the picture at will.

If PCIe3.0 functions are not used, then PCIE30_PORT0/1_AVDD0V75, PCIE30_PORT0/1_AVDD1V8

It can be left unpowered, left floating or grounded.

If PORT0 is used and PORT1 is not used, the two power supplies (0V75 and 1V8) of PORT1 must also be powered.

If PORT1 is used and PORT0 is not used, the two power supplies (0V75 and 1V8) of PORT0 must also be powered.

RK3588 PCIE Power		Port0 Not used Port1 Not used	Port0 used Port1 Not used	Port0 Not used Port1 used
Port0	PCIE30_PORT0_AVDD0V75	ÿ	ÿ	ÿ
	PCIE30_PORT0_AVDD1V8	ÿ	ÿ	ÿ
Port1	PCIE30_PORT1_AVDD0V75	ÿ	ÿ	ÿ
	PCIE30_PORT1_AVDD1V8	ÿ	ÿ	ÿ

2.2.2.17 MIPI CSI RX PHY Power Supply

RK3588 has two MIPI CSI RX interfaces. MIPI_CSI0_AVDD0V75 and MIPI_CSI0_AVCC1V8 power supplies are used to power the MIPI CSI RX PHY. Please do not delete the decoupling capacitors in the RK3588 chip reference design schematic. The capacitor on the left of the green line in the figure below needs to be placed under the RK3588 chip, the capacitor on the right should be placed as close to the chip as possible (the power supply of the MIPI_CSI1 port is handled in the same way as the MIPI_CSI0 port).

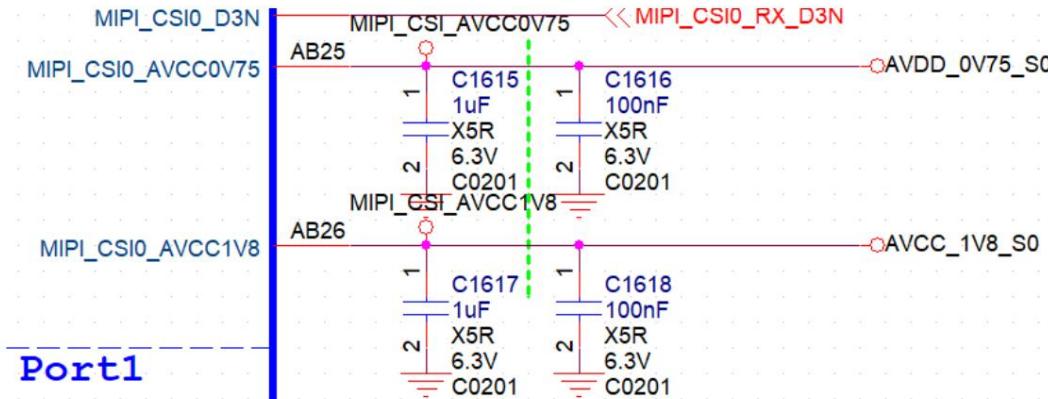


Figure 2-50 RK3588 MIPI CSI RX PHY0 power pin

MIPI_CSI_RX_AVDD_0V9: Peak current 10mA

MIPI_CSI_RX_AVDD_1V8: Peak current 3.3mA

It is recommended to use LDO power supply:

ÿ 0.75V AC requirement<20mV

ÿ 1.8V AC requirement<50mV

A stable power supply helps improve the working stability of the chip, and the decoupling capacitors should be placed close to the pins. The specific number and capacity of capacitors refer to the principle

Please do not adjust the picture at will.

If the MIPI CSI RX function is not used, MIPI_CSI0/1_AVDD_0V75 and MIPI_CSI0/1_ACC1V8 can be omitted.

Electricity, Grounding or Floating are all acceptable.

2.2.2.18 MIPI D/C Combo PHY Power Supply

RK3588 has two MIPI D/C COMBO interfaces.

MIPI_D/C_PHY0_VDD, MIPI_D/C_PHY0_VDD_1V2, MIPI_D/C_PHY0_VDD_1V8 power supplies are for MIPI D/C PHY. Please do not delete the decoupling capacitors in the RK3588 chip reference design schematic. The capacitor on the left of the green line in the figure below needs to be placed on the RK3588.

The capacitor on the right is placed as close to the chip as possible (the power supply of phy1 port is handled the same as that of phy0 port).

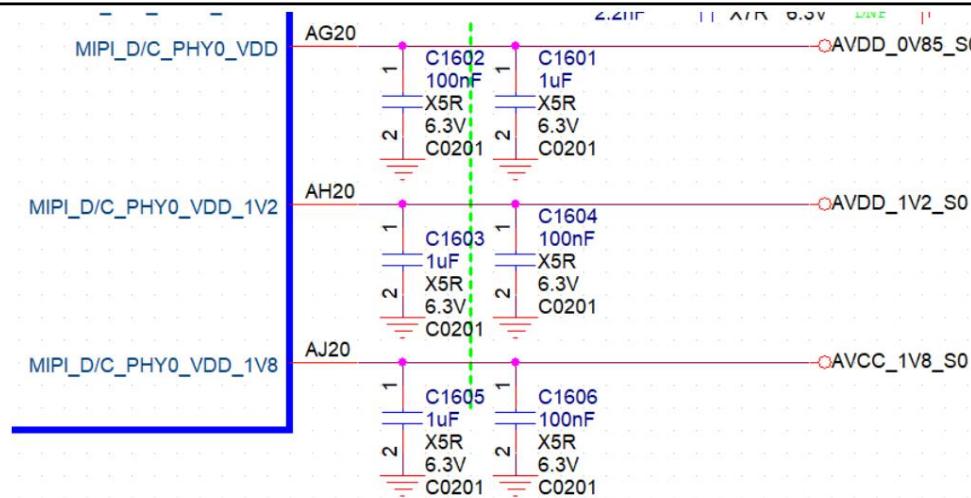


Figure 2-51 RK3588 MIPI D/C Combo PHY0 power pin

MIPI_D/C_PHY_VDD: Peak current 130mA

MIPI_D/C_PHY_VDD_1V2: Peak current 4mA

MIPI_D/C_PHY_VDD_1V8: Peak current 35mA It is recommended to use LDO power supply:

0.9V AC requirement <20mV

1.8V AC requirement: <50mV A stable power supply

helps improve chip operating stability, and the decoupling capacitors should be placed close to the pins. For the specific number and capacity of capacitors, refer to the principle

Please do not adjust the picture at will.

If the MIPI D/C PHY functions are not used, MIPI_D/C_PHY0/1_VDD, MIPI_D/C_PHY0/1_VDD_1V2, and MIPI_D/C_PHY0/1_VDD_1V8 can be left unpowered and connected to ground or floating.

2.2.2.19 HDMI2.1/eDP1.4 Combo Power Supply

RK3588 has two HDMI2.1/eDP Combo PHY interfaces.

HDMI/EDP_TX0_VDD_0V75/HDMI/EDP_TX0_AVDD_0V75/HDMI/EDP_TX0_VDD_IO_1V8

The HDMI/EDP_TX0_VDD_CMN_1V8 power supply is used to power the HDMI2.1/eDP Combo PHY. Please do not delete the decoupling capacitor in the RK3588 chip reference design schematic (the power supply of the phy1 port is handled the same as that of the phy0 port).

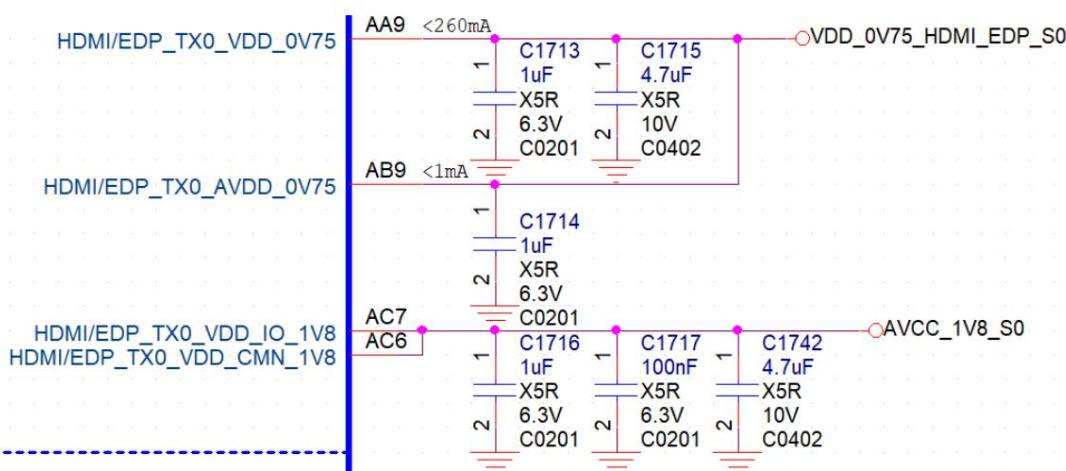


Figure 2-52 RK3588 HDMI2.1/EDP Combo PHY power pin

ÿ HDMI/EDP_TX_VDD_0V75: Peak current 440mA ÿ HDMI/

EDP_TX_AVDD_0V75: Peak current 1mA ÿ HDMI/

EDP_TX_VDD_IO_1V8: Peak current 100mA ÿ HDMI/

EDP_TX_VDD_CMN_1V8: Peak current 100mA It is recommended to use LDO power supply:

ÿ 0.9V AC requirement: <20mV ÿ 1.8V AC requirement:

<50mV A stable power supply helps improve chip

operating stability, and decoupling capacitors should be placed close to the pins. For the specific number and capacity of capacitors, refer to the schematic diagram and do not adjust them at will.

If the HDMI2.1/EDP1.4 TX function is not used, then HDMI/EDP_TX0_VDD_0V75, HDMI/EDP_TX0_AVDD_0V75, HDMI/EDP_TX0_VDD_IO_1V8/HDMI/EDP_TX0_VDD_CMN_1V8 can be unpowered, grounded or left floating.

2.2.2.20 SARADC/OTP Power Supply

RK3588 has 1 SARADC with 8 inputs. SARADC_AVDD_1V8 is used to power SARADC and TSADC.

Delete the decoupling capacitor in the RK3588 chip reference design schematic.

ÿ SARADC_AVDD_1V8: Peak current: 5mA. It is recommended to use LDO power supply:

ÿ 1.8V AC requirement<50mV

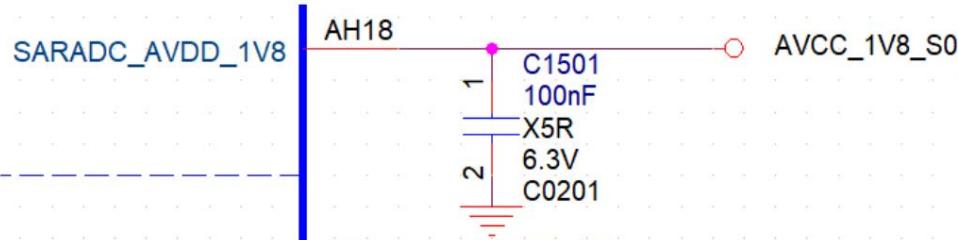


Figure 2-53 RK3588 SARADC power pin

RK3588 has one OTP. OTP_VCC18 is used to power the OTP. Do not delete the capacitor in the RK3588 chip reference design schematic. ÿ OTP_VCCOTP_0V75: Peak current TBD LDO or DC/DC can be used to power the OTP.

A stable power supply helps improve the working stability of the chip, and the decoupling capacitors should be placed close to the pins. The specific number and capacity of capacitors refer to the principle

Please do not adjust the picture at will.

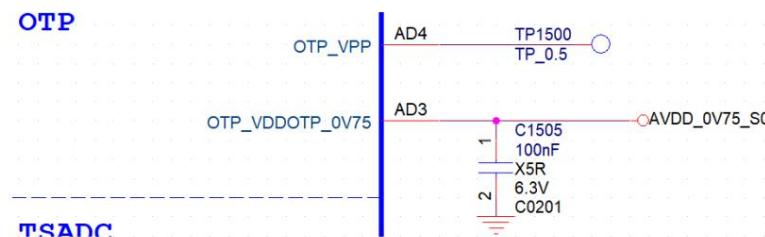


Figure 2-54 RK3588 SARADC power pin

2.2.3 RK806 Solution Introduction

2.2.3.1 RK806 Typical Application Diagram

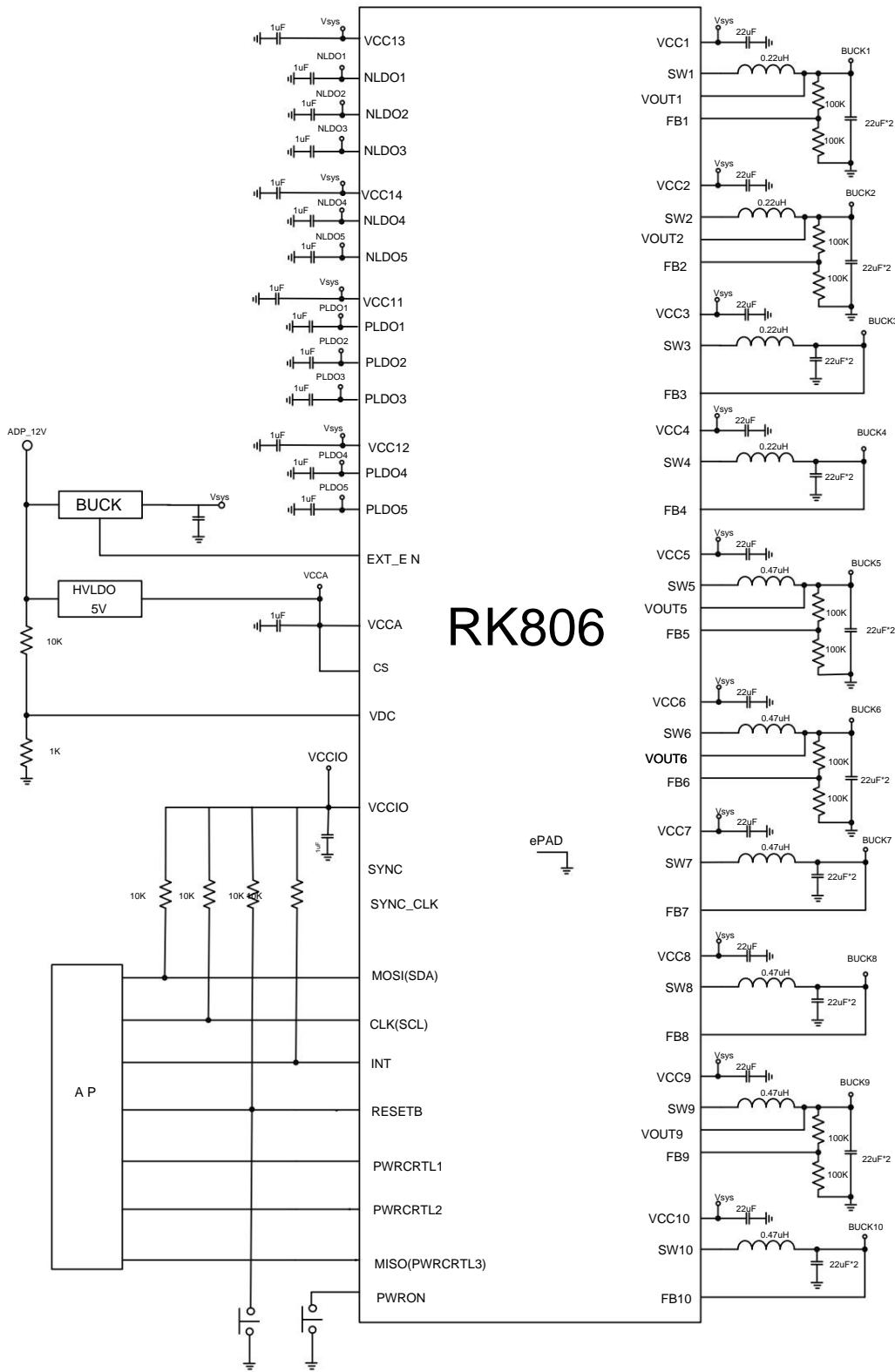


Figure 2-55 RK806 single chip typical application diagram

2.2.3.2 RK806 Features

- ÿ Input range: 2.7V-5.5V; ÿ Ultra-low standby current: 10uA; ÿ Supports I2C and SPI dual communication protocols; ÿ Supports dual-chip collaborative operation; ÿ Ripple control architecture provides excellent transient response;

ÿ Output levels programmable via I2C or SPI

ÿ Optional power startup time

Power channel:

Buck 1: 0.5V-3.4V output, 6.5A max

Busch/2/2/1

Part 1: 5/2/7/8/8/4/2-2, 5V, 2, 4V, 1, 4

NEC041/2/3: 0.8V-3.4V output, 800mA max,

y NEDOS/4. 0.5V-3.4V output, 500mA Max.

0.5V-3.4V output, 500mA max. y PLDU2/3/5/6: 0.5V-3.4

output, 300mA max.

ernal Buck enable co

Package: 7mm x 7mm QFN68.

connected to the EN pin of an external buck), and the other as the slave (EXT_EN is shorted to VCCA for identification). The power-up and power-down timing of the two chips is synchronized by SYNC and SYNC_CLK. When in use, short the VDC, PWRON, and RESET pins of the two PMICs together.

Note: When using a single PMIC, set the PMIC to master mode via EXT_EN and leave SYNC and SYNC_CLK floating.

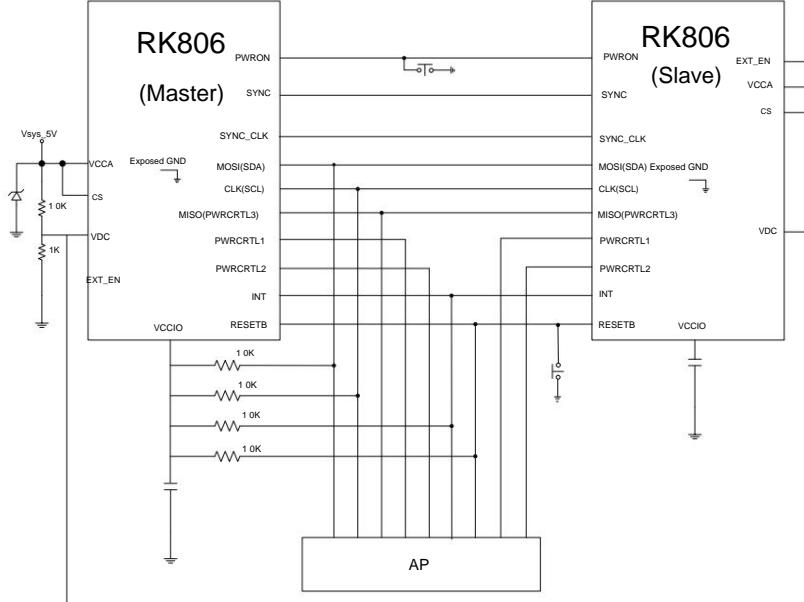


Figure 2-56 RK806 dual-chip (I2C mode) typical application diagram

of RK806 power-on, it is in SPI mode. The figure below shows the dual PMIC working mode of SPI connection.

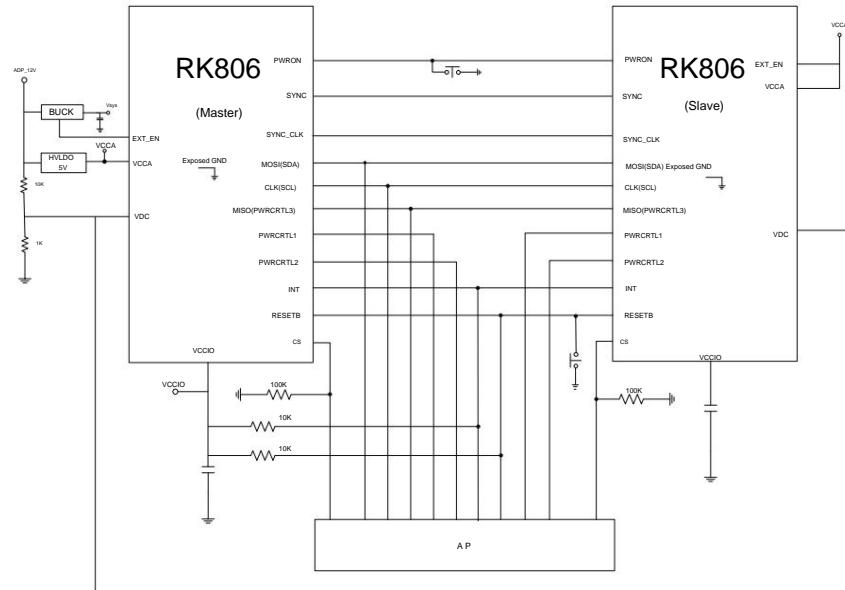


Figure 2-57 RK806 dual-chip (SPI mode) typical application diagram

- ÿ RK806-2 works together: SYNC_CLK and SYNC of the two chips are interconnected, the main chip provides SYNC_CLK clock (frequency close to 32K) received from the chip, SYNC provides synchronization signal, generates synchronization pulses for: power on, power off, reset,
- Power-on and power-off timing.
- ÿ Power on: The PWRON, VDC, and RESET pins of the master and slave are connected together, so the master and slave can receive the same power-on signal. When the power-on signal is valid, the master will provide the SYNC_CLK clock to the slave and pull SYNC high. The master and slave will use the SYNC_CLK clock as the counting clock according to the master-slave timing burned in the on-chip OTP, with a step of about 1ms, to turn on the LDO or BUCK according to the timing.

- ÿ Normal shutdown or restart: RESET remains high and SYNC is pulled low (above 3clk for about 90us);
- ÿ Abnormal shutdown: SYNC and RESET are pulled low at the same time within 22us (the capacitance on the reset line cannot be greater than 0.3uF);
- ÿ Pull RESET low to reset: SYNC is high, pull RESET low (2clk about 60us).

ÿ VCCA (Pin 21) of RK806: It is the power supply pin for the digital logic and some analog control inside the RK806 chip. The design of this pin requires that the power supply voltage must be the highest voltage among all the power supply pins of RK806 or greater than Vmax-0.3V, so VCCA must be

It is powered on first, or powered on together with other power supplies. It is not allowed to have VCCA power off while other power supplies are powered on first.

ÿ RK806 RESETB (Pin 40): This pin outputs the reset signal for the main controller. When pulled high, it also serves as an external reset signal and a synchronous shutdown signal input for the dual PMICs. Because of its input function, a 100nF capacitor is required to improve anti-interference capabilities.

However, the total capacitance on the line cannot exceed 0.3uF (because RESET has a synchronous shutdown function, when the capacitance on the RESET line is too large, the high level rise speed will slow down, resulting in abnormal dual PMIC synchronous shutdown timing detection).

ÿ PLDO6 of RK806 is for CS\ MOSI(SDA)\CLK(SCL)\MISO(SLEEP3)\SLEEP2\SLEEP1

VCCIO power supply, the GPIO power domain connected to these IOs should also be powered by this power supply to achieve level matching and upper and lower Electrical synchronization, etc.

ÿ Pin 32 (VDC) of RK806: It is used to automatically start the machine when connected to an external power supply. The VDC pin's high level is 0.8V, and it is recommended to be greater than 1V and less than or equal to the VCCA voltage. When VDC detects a high level (VCCA\VCC1\VCC2 greater than 3.0V), RK806 will start up, and RK806 cannot be shut down while VDC is high (If you want to start the machine by plugging in an adapter, you need to set the VDC pin.

RC delay is shown in the figure below).

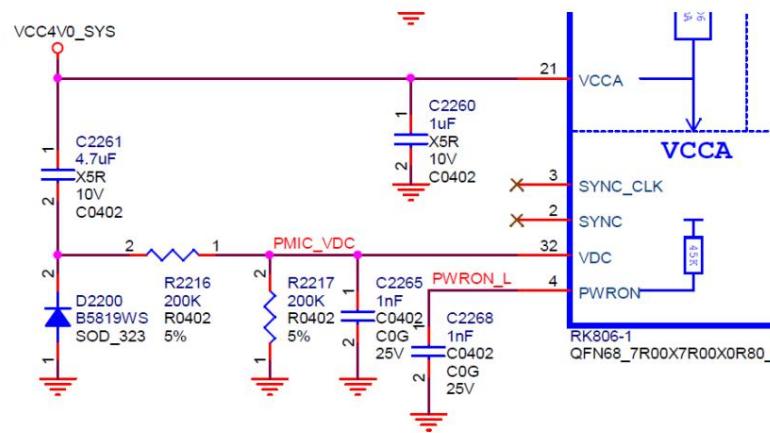


Figure 2-58 RK806 VDC pin

- ÿ Pin 4 (PWRON) of RK806: Connect to the power button. This pin has a 45Kohm resistor inside that pulls it up to VCCA. When the power is off, pull this pin down for 20ms. If the voltage meets the power-on conditions, the power will be turned on (Note: RK806-1 and RK806-2 default to 20ms. If PWRON is pulled down in the power-on state, a short press or long press interrupt will be sent to the main control. If the pull-down time exceeds 6S, the power will be forced to shut down. (6S\8S\10S\12S software optional)).
- ÿ RK806 has three PWRCTRL pins, namely PIN16\61\62 (PWRCTRL3\2\1), which have the same functions except that PWRCTR3 reuses MISO. These pins can control RK806 to enter and exit SLEEP mode, and can also be used to control BUCK or LDO for fast voltage regulation or switching output by configuring the corresponding registers.

ÿ VOUT of RK806 BUCK: VOUT is both the ripple detection input of COT structure BUCK and the feedback voltage input pin.

It is usually connected directly to the positive terminal of the output capacitor (the VOUT line should be kept away from interference from other signals as much as possible).

ÿ FB pin of RK806 BUCK: BUCK1\2\5\6\9 has an additional FB pin compared to other BUCKs. BUCKs with FB pins can choose the voltage feedback pin as VOUT pin or FB pin. The FB reference voltage is 0.5V. When using the FB pin, the recommended voltage divider resistor is between 10K ohm and 1M ohm. The calculation formula is $V_{out} = (R1/R2+1) \cdot 0.5V$. When using an external voltage divider resistor, for better transient response of the system, it is recommended to connect a 100pF bypass capacitor in parallel across the upper voltage divider resistor. Note: Whether FB is enabled by default is set by OTP. Generally, it is only used when the default voltage of the power supply needs to be changed (such as VDD_DDR). FB is used to adjust the default voltage, and the register can be changed after power on to achieve dynamic switching.

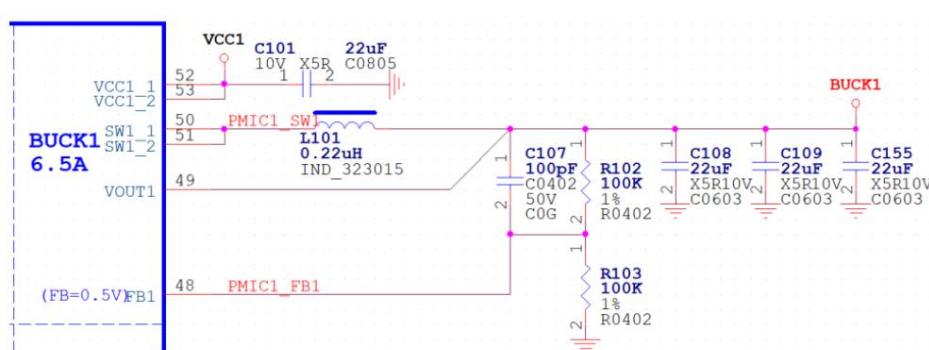


Figure 2-59 RK806 BUCK1

ÿ RK806 BUCK1: Maximum output full load current is 6.5A, input capacitance is 22uF, output capacitance is 66uF, switching frequency is 2MHz

(Typical), the inductor is 0.22uH. The input and output capacitor voltage is recommended to be twice the operating voltage, and the inductor current ripple is About 30% of the full load ripple (saturation current above 9.1A), DCR is less than 20m ohm (in order to achieve better conversion efficiency,

It is recommended to select a DCR of around 15m ohm).

ŷ BUCK2\3\4 of RK806: Maximum output full-load current is 5A, input capacitance is 22uF, output capacitance is 66uF, switching frequency is 2MHz (typical), and inductance is 0.22uH. It is recommended to select the input and output capacitor voltage to be twice the operating voltage, the inductor current ripple is about 30% of the full-load ripple (saturation current is above 7A), and the DCR is less than 20m ohm (in order to achieve better conversion efficiency, it is recommended to select It is recommended to choose a DCR of around 15m ohm).

ŷ RK806 BUCK5\6\7\8\9\10: Maximum output full-load current is 2.A, input capacitance is 10uF, output capacitance is 44uF, switching frequency is 2MHz (typical), inductor inductance is 0.47uH. It is recommended to select the input and output capacitor voltage twice the operating voltage, take the inductor current ripple to be about 30% of the full-load ripple (saturation current is above 4.5A), and DCR is less than 40m ohm (to achieve better conversion efficiency, it is recommended to choose a DCR of around 20m ohm).

ŷ RK806 PLDO: In addition to PLDO6 (VCCIO), the RK806 also provides three PLDOs (PLDO1 and PLDO4) with a load capacity of 300mA and two with a load capacity of 500mA. The input and output capacitors of each PLDO must have a guaranteed capacity of 1uF or more. VCC11 is the power input pin for PLDO1, 2, and 3, and VCC12 is the power input pin for PLDO4 and 5. To ensure the normal voltage regulation efficiency of the PLDO, the minimum input voltage of VCC11 and VCC12 is the highest output voltage of the LDO below it + 0.2V, and the minimum input voltage must not be lower than 2.0V.

ŷ NLDO of RK806: NLDO is an LDO with an N-type transistor as the adjustment tube. Its characteristic is that the input voltage of the adjustment tube can be very low (no PLDO minimum input voltage requirement of 2.0V) and only needs to meet the output voltage +0.2V. However, the maximum output voltage must be 1.5V lower than the VCCA (Pin21) voltage. NLDO also has two power supply pins, VCC13 and VCC14, and also provides 3 load The output capacity is 300mA and the two with load capacity are 500mA (NLDO3\NLDO4). The capacity of each NLDO output capacitor is guaranteed to be 2.2uF or above. Among them, VCC13 is the power supply input pin of NLDO1\2\3, and VCC14 is the power supply input pin of NLDO4\5.

ŷ RK806 power on/off conditions:

ŷ VDC startup process:

- VCCA has power; • VDC pin is higher than 0.8V, the recommended value is about 1.0V; • EXT_EN outputs high level; • VCCA\VCC1\VCC2 voltage exceeds VB_LO_SEL voltage within 100ms of EXT_EN outputting high level (RK806-1/RK806-2 value is 3.0V), otherwise it will not boot;
- Start the power-on process, and power on each DC/DC and LDO in sequence;
- After power on, VDC can be pulled low or kept high without affecting the power on status.

ŷ Power Key startup process: • VCCA has

- power;
- The PWRON pin voltage is pulled from high level (greater than VCCA*0.7) to low level (less than VCCA*0.3V) for a period of time exceeding Over 20ms (20/500ms OTP setting);
- EXT_EN outputs high level; • VCCA\VCC1\VCC2 voltage exceeds 3.0V within 100ms of EXT_EN outputting high level, otherwise it will not start; • Start the power-on process, and each DC/DC and LDO will be powered on according to the timing.

ŷ Shutdown method:

- The voltage of VCC9\VCC1\VCC2 is lower than the voltage set by VB_UV_SEL for undervoltage setting; • The voltage of VCC9\VCC1\VCC2 is lower than the voltage set by VB_LO_SEL for undervoltage setting, and VB_LO_ACT=0; • Write DEV_OFF=1 via I2C or SPI command; • Over-temperature protection shutdown (140/160 degrees); • Press and hold the PowerKey for more than 6 seconds to force shutdown (6/8/10/12 configurable);

- Another PMIC pulls down the SYNC and RESET pins to trigger a coordinated shutdown

For detailed design instructions of RK806, please refer to the RK PMIC related design document "AN_RK806_V1.0".

2.2.4 Introduction to the RK3588 and RK806-2 Dual PMIC Power Solution

2.2.4.1 RK3588+RK806-2 Power Tree

Power Diagram

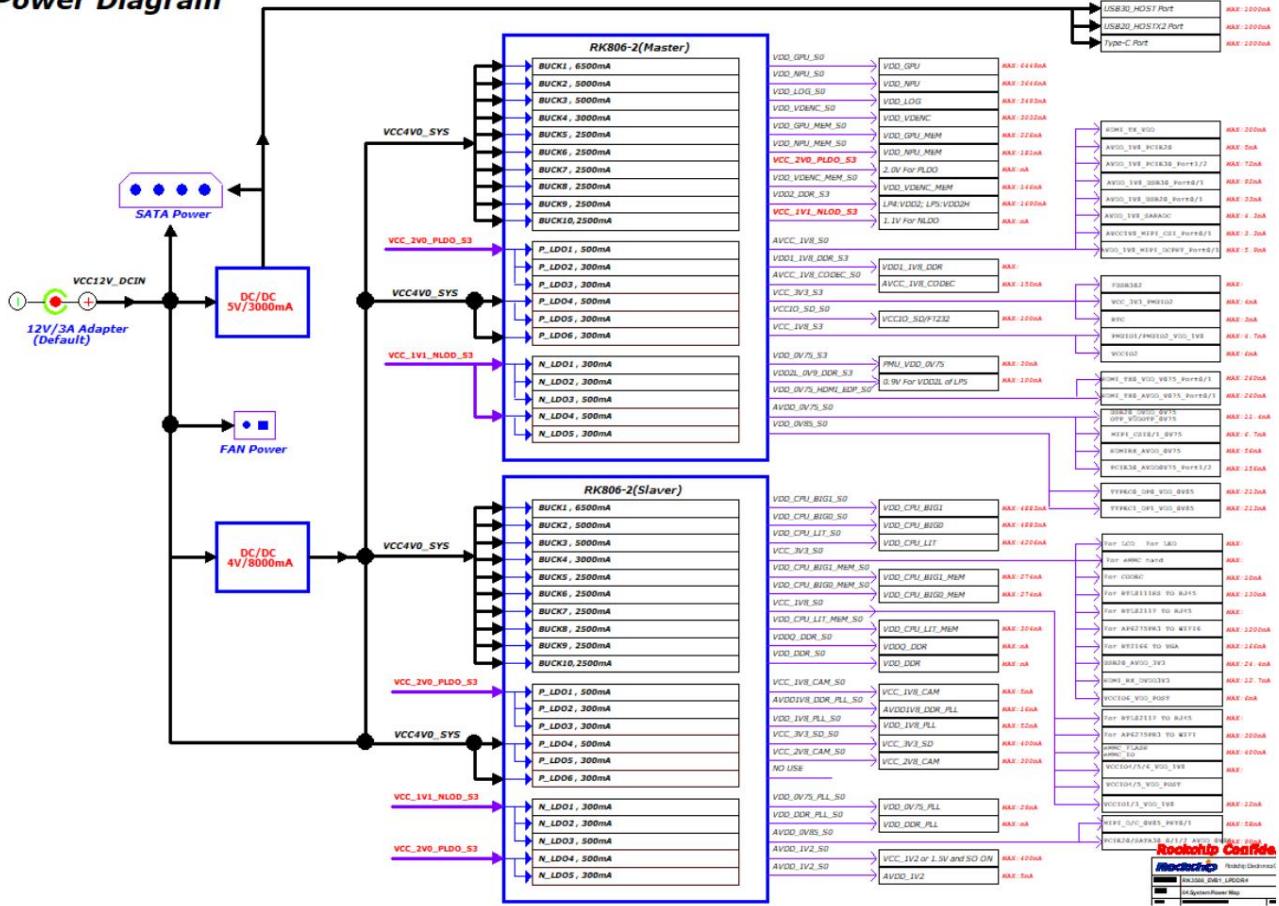


Figure 2-60 RK3588+RK806-2 power supply architecture

2.2.4.2 RK806-2 Power-On Sequence

RK806-2 contains two sets of power-on sequences, Master and Slave, which are already fixed and cannot be replaced by other models such as RK806-1.

RK806-2, also using the single PMIC solution RK806-1 can not be replaced by RK806-2.

Master:

Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Sleep ON/OFF	Peak Current	Sleep Current
VCC4V0_SYS	PMIC1_BUCK1	6.5A	VDD_GPU_S0		0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	PMIC1_BUCK2	5A	VDD_NPU_S0		0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	PMIC1_BUCK3	5A	VDD_LOG_S0		0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	PMIC1_BUCK4	3A	VDD_VDENC_S0		0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	PMIC1_BUCK5	2.5A	VDD_GPU_MEM_S0		0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	PMIC1_BUCK6	2.5A	VDD_NPU_MEM_S0		0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	PMIC1_BUCK7	2.5A	VCC_2V0_PLDO_S3		2.0V	ON	ON	TBD	TBD
VCC4V0_SYS	PMIC1_BUCK8	2.5A	VDD_VDENC_MEM_S0		0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	PMIC1_BUCK9	2.5A	VDD2_DDR_S3		1.1V	ON	ON	TBD	TBD
VCC4V0_SYS	PMIC1_BUCK10	2.5A	VCC_1V1_NLDO_S3		1.1V	ON	ON	TBD	TBD
VCC_2V0_PLDO	PMIC1_PLDO1	0.3A	AVCC_1V8_S0		1.8V	ON	OFF	TBD	TBD
	PMIC1_PLDO2	0.3A	VDD1_1V8_DDR_S3		1.8V	ON	ON	TBD	TBD
	PMIC1_PLDO3	0.5A	AVCC_1V8_CODEC_S0		1.8V	ON	OFF	TBD	TBD
VCC4V0_SYS	PMIC1_PLDO4	0.5A	VCC_3V3_S3		3.3V	ON	ON	TBD	TBD
	PMIC1_PLDO5	0.3A	VCCIO_SD_S0		3.3V	ON	OFF	TBD	TBD
VCC4V0_VCCA	PMIC1_PLDO6	0.3A	VCC_1V8_S3		1.8V	ON	ON	TBD	TBD
VCC_1V1_NLDO	PMIC1_NLDO1	0.3A	VDD_0V75_S3		0.75V	ON	ON	TBD	TBD
	PMIC1_NLDO2	0.3A	VDD2L_0V9_DDR_S3		0.9V	ON	ON	TBD	TBD
	PMIC1_NLDO3	0.5A	VDD_0V75_HDMI_EDP_S0		0.75V	ON	OFF	TBD	TBD
VCC_1V1_NLDO	PMIC1_NLDO4	0.5A	AVDD_0V75_S0		0.75V	ON	OFF	TBD	TBD
	PMIC1_NLDO5	0.3A	VDD_0V85_S0		0.85V	ON	OFF	TBD	TBD

Slave:

VCC4V0_SYS	PMIC2_BUCK1	6.5A	VDD_CPU_BIG1_S0		0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	PMIC2_BUCK2	5A	VDD_CPU_BIG0_S0		0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	PMIC2_BUCK3	5A	VDD_CPU_LIT_S0		0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	PMIC2_BUCK4	3A	VCC_3V3_S0		3.3V	ON	OFF	TBD	TBD
VCC4V0_SYS	PMIC2_BUCK5	2.5A	VDD_CPU_BIG1_MEM_S0		0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	PMIC2_BUCK6	2.5A	VDD_CPU_BIG0_MEM_S0		0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	PMIC2_BUCK7	2.5A	VCC_1V8_S0		1.8V	ON	OFF	TBD	TBD
VCC4V0_SYS	PMIC2_BUCK8	2.5A	VDD_CPU_LIT_MEM_S0		0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	PMIC2_BUCK9	2.5A	VDDQ_DDR_S0		0.6V	ON	OFF	TBD	TBD
VCC4V0_SYS	PMIC2_BUCK10	2.5A	VDD_DDR_S0		0.85V	ON	OFF	TBD	TBD
VCC_2V0_PLDO	PMIC2_PLDO1	0.3A	VCC_1V8_CAM_S0		0V	OFF	OFF	TBD	TBD
	PMIC2_PLDO2	0.3A	AVDD1V8_DDR_PLL_S0		1.8V	ON	OFF	TBD	TBD
	PMIC2_PLDO3	0.5A	VDD_1V8_PLL_S0		1.8V	ON	OFF	TBD	TBD
VCC4V0_SYS	PMIC2_PLDO4	0.5A	VCC_3V3_SD_S0		3.3V	ON	OFF	TBD	TBD
	PMIC2_PLDO5	0.3A	VCC_2V8_CAM_S0		0V	OFF	OFF	TBD	TBD
VCC_1V1_NLDO	PMIC2_NLDO1	0.3A	VDD_0V75_PLL_S0		0.75V	ON	OFF	TBD	TBD
	PMIC2_NLDO2	0.3A	VDD_DDR_PLL_S0		0.85V	ON	OFF	TBD	TBD
	PMIC2_NLDO3	0.5A	AVDD_0V85_S0		0.85V	ON	OFF	TBD	TBD
VCC_2V0_PLDO	PMIC2_NLDO4	0.5A	VCC_1V2_CAM_S0		0V	OFF	OFF	TBD	TBD
	PMIC2_NLDO5	0.3A	AVDD_1V2_S0		1.2V	ON	OFF	TBD	TBD

Figure 2-61 RK806-2 power-on default voltage and timing

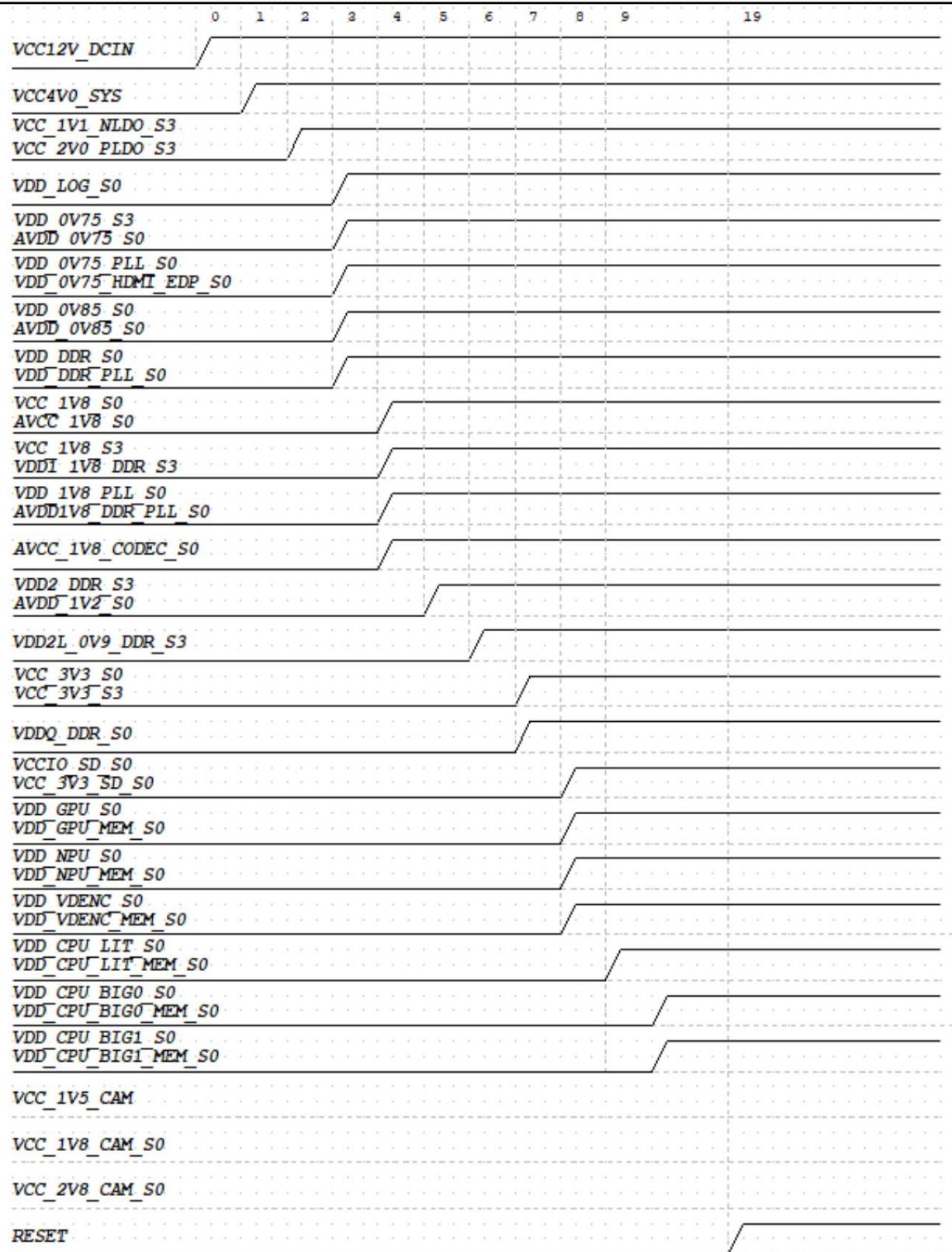


Figure 2-62 RK3588+RK806-2 power-on sequence diagram

2.2.5 Introduction to RK3588 and RK806-1 Single PMIC Power Solution

2.2.5.1 RK3588+RK806-1 Power Tree (AIOT REF)

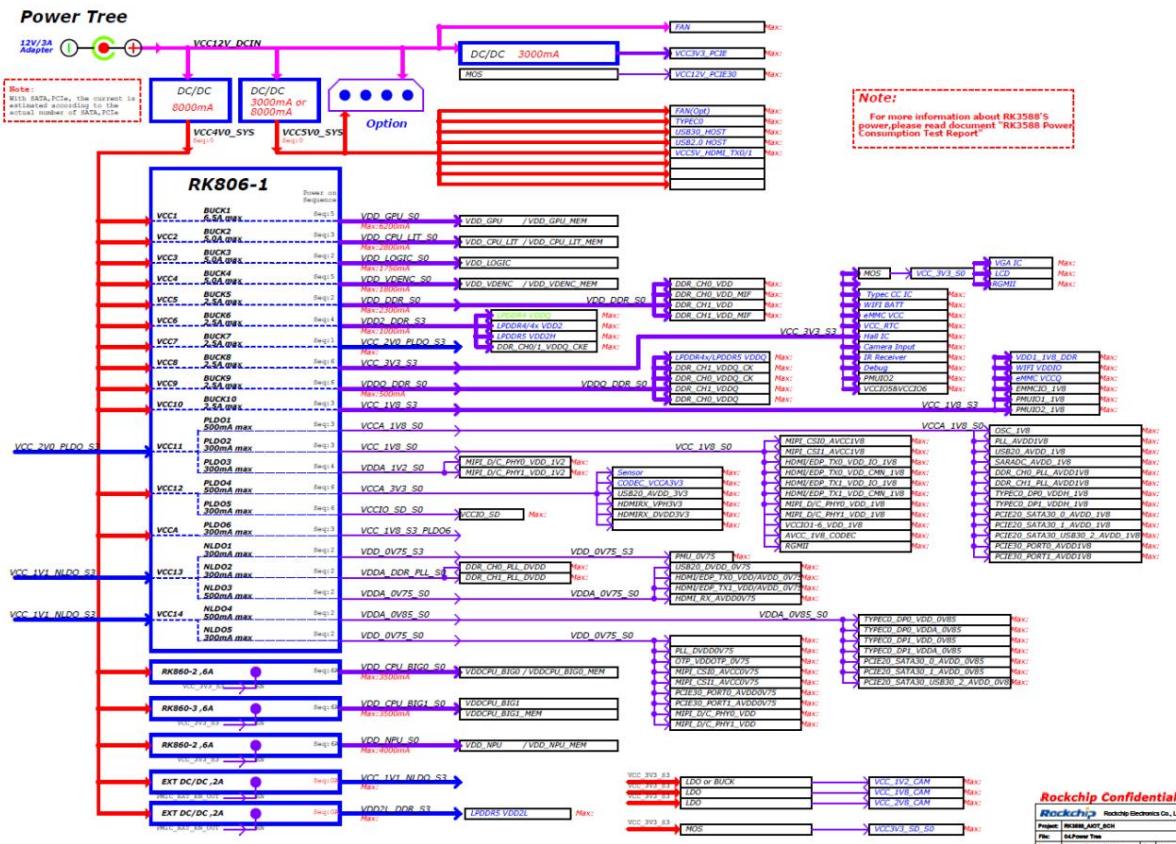


Figure 2-63 RK3588+RK806-1 power supply architecture

2.2.5.2 RK806-1 Power-On Sequence

When RK3588 uses a single PMIC RK806-1, it also needs to add three RK860s to provide auxiliary power for the NPU and two big CPUs of RK3588.

The material numbers of the three RK860s are RK860-2/RK860-3/RK860-2 (respectively connected to two I2C buses).

The EN signal is controlled by the VCC_3V3_S3 power supply. The BIG0 CPU, BIG1_CPU, and NPU (including their respective MEM power supplies) require the default power supply to be on.

Confirm the power supply.

Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Sleep ON/OFF	Peak Current	Sleep Current
VCC4V0_SYS	RK806-1_BUCK1	6.5A	VDD_GPU_S0	Slot:5	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK2	5A	VDD_CPU_LIT_S0	Slot:3	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK3	5A	VDD_LOG_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK4	3A	VDD_VDENC_S0	Slot:5	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK5	2.5A	VDD_DDR_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK6	2.5A	VDD2_DDR_S3	Slot:4	ADJ FB=0.5V	ON	ON	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK7	2.5A	VCC_2V0_PLDO_S3	Slot:1	2.0V	ON	ON	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK8	2.5A	VCC_3V3_S3	Slot:6	3.3V	ON	ON	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK9	2.5A	VDDQ_DDR_S0	Slot:6	ADJ FB=0.5V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK10	2.5A	VCC_1V8_S3	Slot:3	1.8V	ON	ON	TBD	TBD
VCC_2V0_PLDO	RK806-1_PLDO1	0.5A	VCCA_1V8_S0	Slot:3	1.8V	ON	OFF	TBD	TBD
	RK806-1_PLDO2	0.3A	VCC_1V8_S0	Slot:3	1.8V	ON	OFF	TBD	TBD
	RK806-1_PLDO3	0.3A	VDDA_1V2_S0	Slot:4	1.2V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_PLDO4	0.5A	VCCA_3V3_S0	Slot:6	3.3V	ON	OFF	TBD	TBD
	RK806-1_PLDO5	0.3A	VCCIO_SD_S0	Slot:6	3.3V	ON	OFF	TBD	TBD
	RK806-1_PLDO6	0.3A	VCCA1V8_PLDO6_S3	Slot:3	1.8V	ON	ON	TBD	TBD
VCC_1V1_NLDO	RK806-1_NLDO1	0.3A	VDD_0V75_S3	Slot:2	0.75V	ON	ON	TBD	TBD
	RK806-1_NLDO2	0.3A	VDDA_DDR_PLL_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
	RK806-1_NLDO3	0.5A	VDDA_0V75_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC_1V1_NLDO	RK806-1_NLDO4	0.5A	VDDA_0V85_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
	RK806-1_NLDO5	0.3A	VDD_0V75_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	BUCK_RK860-2	6A	VDD_CPU_BIG0_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	BUCK_RK860-3	6A	VDD_CPU_BIG1_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	BUCK_RK860-2	6A	VDD_NPU_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	EXT BUCK	2A	VCC_1V1_NLDO_S3	Slot:1	1.1V	ON	ON	TBD	TBD
VCC4V0_SYS	EXT BUCK	2A	VDD2L_0V9_DDR_S3	Slot:5	0.9V	ON	ON	TBD	TBD
VCC4V0_SYS	EXT BUCK	2.5A	VCC_3V3_SD_S0	Slot:6A	3.3V	ON	OFF	TBD	TBD
VCC_3V3_S3	EXT_BUCK	2A	VCC_1V2_CAM_S0	OFF	1.2V	OFF	OFF	TBD	TBD
VCC_3V3_S3	LDO_PT5108	0.5A	VCC_1V8_CAM_S0	OFF	1.8V	OFF	OFF	TBD	TBD
VCC_3V3_S3	LDO_PT5108	0.5A	VCC_2V8_CAM_S0	OFF	2.8V	OFF	OFF	TBD	TBD

Figure 2-64 RK3588+RK806-1 power-on sequence

Power Sequence

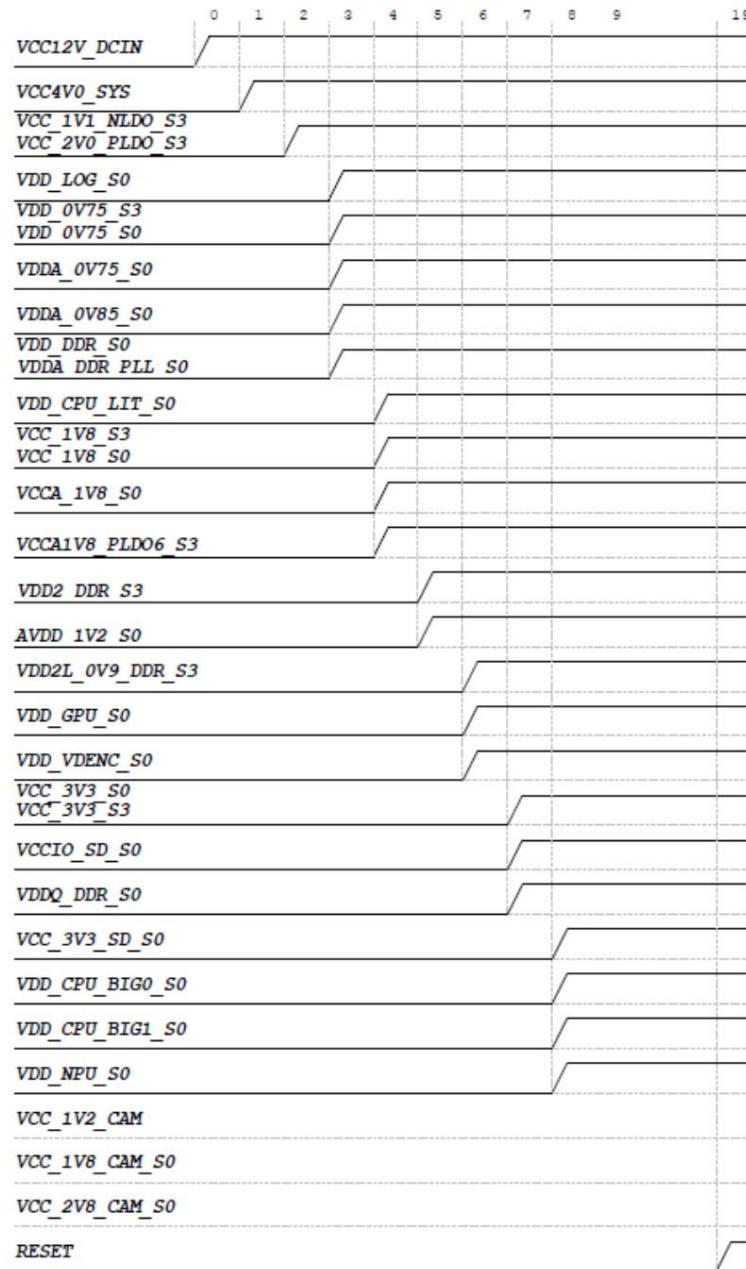


Figure 2-65 RK3588+RK806-1 power-on sequence diagram

2.2.5.3 Core Module Peak Current Meter

The following data is the peak current of each core module, for evaluation of power supply solutions and PCB layout, for reference only.

Note: You cannot simply add up all the peak currents to calculate the SOC. To evaluate the cooling solution, please calculate the average working current based on the actual scenario.

Current conduction.

Table 2-13 RK3588 Peak Current Meter

RK3588 core module current limit				
<p>Environment: room temperature 23°C;</p> <p>Heat dissipation: bare board, no heat sink;</p> <p>Test method: After the development board is stable, run and record for 15 minutes;</p> <p>Operational scenarios: The test results of different modules under their respective extreme operating scenarios are for reference only;</p> <p>Note: The following data is the test data on the internal R&D board, which is for design reference only and does not represent the final capability of the chip.</p> <p>It is highly relevant to international application scenarios. If you need in-depth optimization, you can discuss it with technical support personnel.</p>				
	Power network	Voltage (V)	Peak current mA	Peak power (mW)
Core Module Limiting current	VDD_CPU_BIG0_S0	0.950	3.50	3.33
	VDD_CPU_BIG1_S0	0.950	3.50	3.33
	VDD_CPU_LIT_S0	0.950	3.00	2.85
	VDD_LOG_S0	0.750	2.00	1.50
	VDD_GPU_S0	0.850	6.00	5.27
	VDD_NPU_S0	0.900	4.00	3.60
	VDD_VDENC_S0	0.775	2.00	1.55
	VDD_DDR_S0	0.800	2.50	2.00

2.3 Functional Interface Design Guidelines

2.3.1 SDMMC/SDIO

RK3588 integrates one SDMMC controller and one SDIO controller, both of which support SDIO3.0 protocol and MMC V4.51 protocol.

4-wire data bus width; supports [SDR104](#) mode, with a speed of up to 150MHz.

2.3.1.1 SDMMC Interface

- ÿ The SDMMC interface is multiplexed in the VCCIO2 power domain;
- ÿ Support System Boot, with SD card function assigned by default;
- ÿ SDMMC and JTAG functions are multiplexed together. By default, the function is selected through the SDMMC_DET state. For details, please refer to Section 2.1.5 Description;

ÿ VCCIO2 power supply, requires external 3.3V or 1.8V power supply;

ÿ When connecting an SD card: If only SD2.0 mode is supported: 3.3V power can be directly supplied; if SD3.0 mode is supported, SD2.0 is compatible.

Mode: The default power supply is 3.3V. After negotiating with the SD card to run SD3.0 mode, the power supply voltage needs to be switched to 1.8V.

Or PLDO5 of RK806-1 can supply power to VCCIO2 separately to achieve this process;

ÿ When connected to an SDIO device: supply 1.8V or 3.3V according to the peripheral device and the actual operating mode;

U1000D

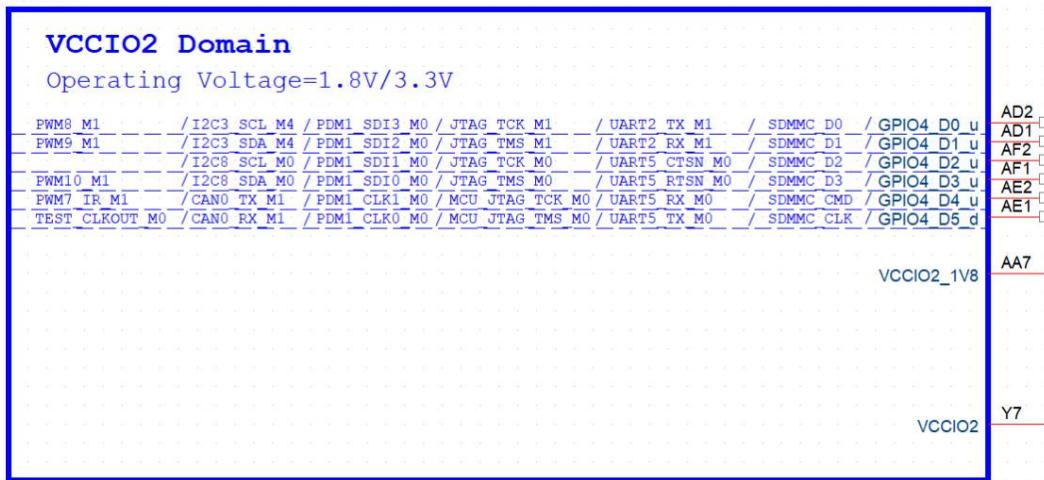


Figure 2-66 RK3588 SDMMC interface pins

When using a connector to connect a board to a board, it is recommended to connect a resistor with a certain resistance (between 220ohm and 1000ohm, depending on the specific resistance).

SI test shall prevail), and TVS devices shall be reserved;

When using an SD card, please pay attention to the following issues:

1) The VDD pin of the SD card has a supply voltage of 3.3V. The decoupling capacitor must not be removed and should be placed close to the card holder during layout.

2) SDMMC_D[3:0], SDMMC_CMD, SDMMC_CLK need to be connected in series with a 220ohm resistor, and SDMMC_DET in series with 100 ohm resistor;

3) SDMMC_D[3:0], SDMMC_CMD, SDMMC_CLK, SDMMC_DET signals are required at the SD card location

Place ESD devices, which need to support SD3.0 mode. The junction capacitance of the ESD device must be less than 1pF. If only SD2.0 is supported,

mode, the junction capacitance of the ESD device can be relaxed to 9pF.

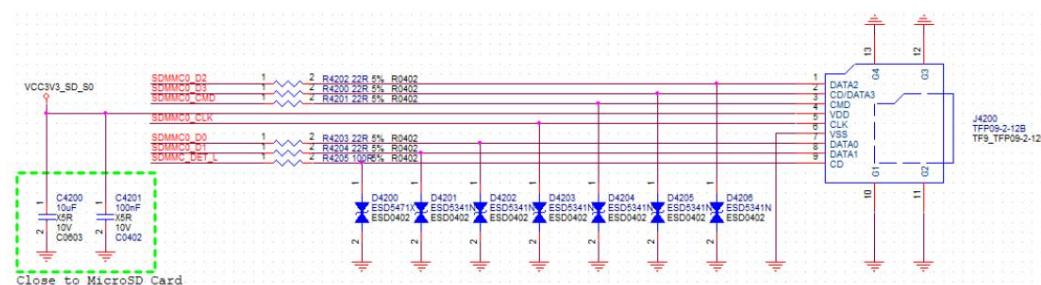


Figure 2-67 SD Card interface circuit

4) The pull-up and matching design recommendations for the SDMMC0 interface are shown in the table below:

Table 2-14 SDMMC0 interface design

Signal	Internal pull-up and pull-down	Connection method	Description (chip side)
SDMMC0_D[3:0]	Pull-up	Connect a 220ohm resistor in series Use the corresponding IO internal pull-up resistor	SD data sending/receiving
SDMMC0_CLK	drop down	Connect a 220ohm resistor in series	SD clock transmission
SDMMC0_CMD	Pull-up	Connect a 220ohm resistor in series Use the corresponding IO internal pull-up resistor	SD command send/receive
SDMMC0_DET	Pull-up	Connect a 100ohm resistor in series Use the corresponding IO internal pull-up resistor	SD card insertion detection

2.3.1.2 SDIO interface

þ The SDIO interface multiplexes two locations, one in the VCCIO3 power domain and the other in the VCCIO5 power domain. Only one of them can be used.

Either all use the VCCIO3 power domain, or all use the VCCIO5 power domain. Some use of the VCCIO3 power domain is not supported.

Some use the VCCIO5 power domain;

þ System Boot is not supported;

þ VCCIO3 power supply is 1.8V only; VCCIO5 power supply is 1.8V or 3.3V. Select the corresponding power supply according to the needs of the peripherals.

Pressure, please make sure it is consistent with the IO of the peripherals.

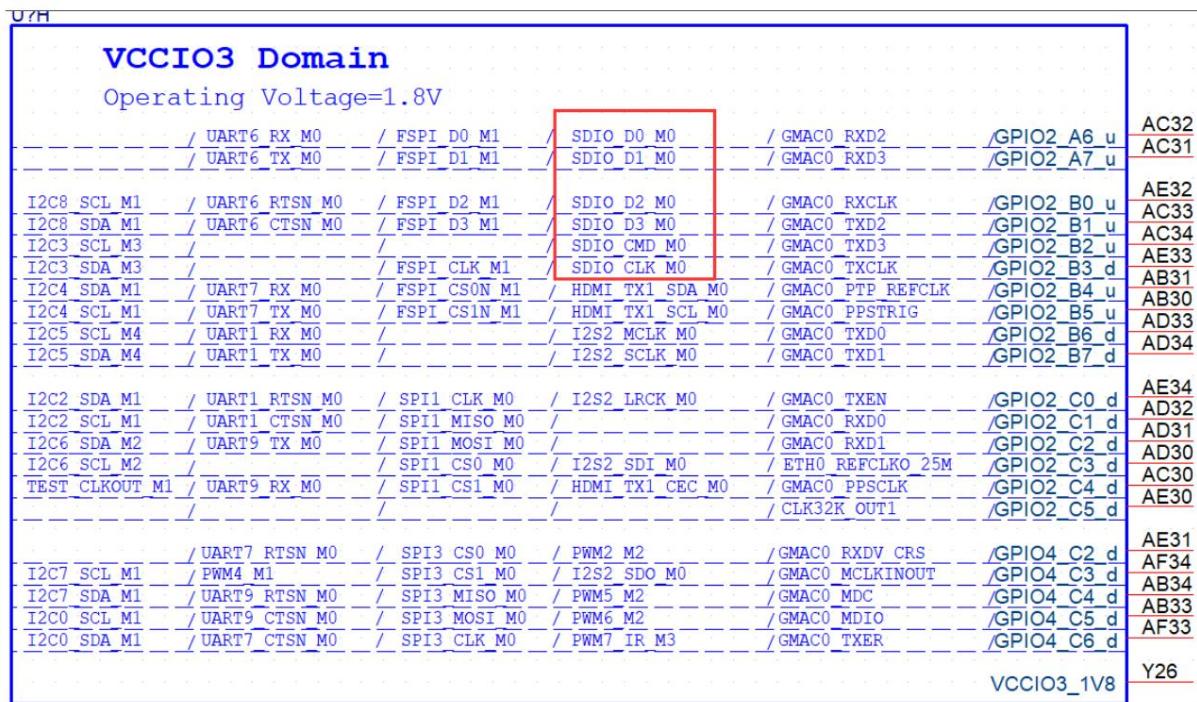


Figure 2-68 RK3588 SDIO interface M0 function pin

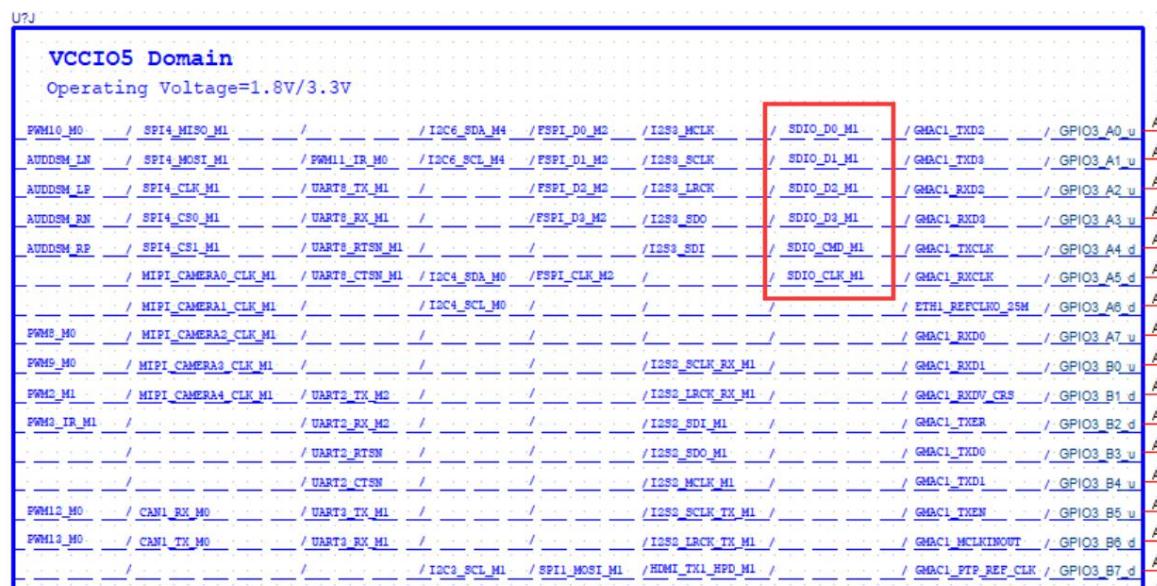


Figure 2-69 RK3588 SDIO interface M1 function pin

ÿ The pull-up and matching design recommendations for the SDIO interface are shown in the table:

Table 2-15 SDIO interface design

Signal	Internal pull-up and pull-down	Connection method	Description (chip side)
SDIO_D[3:0] pull-up		Connect a 22ohm resistor in series, which can be deleted if the trace is short. Use the corresponding IO internal pull-up resistor	SD data sending/receiving
SDIO_CLK	drop down	Connect a 22ohm resistor in series	SD clock transmission
SDIO_CMD	Pull-up	Connect a 22ohm resistor in series, which can be deleted if the trace is short. Use the corresponding IO internal pull-up resistor	SD command send/receive

When using a connector to connect a board to a board, it is recommended to connect a resistor with a certain resistance (between 22ohm and 100ohm, depending on the specific resistance).

Test is subject to the requirements) and TVS devices should be reserved.

2.3.1.3 Notes when connecting SDIO to WIFI

- ÿ Please ensure that the IO level of the module is consistent with the IO level of the CPU, otherwise level matching is required;
- ÿ Please select the crystal load capacitance according to the CL capacitance value of the actual crystal used, and control the frequency tolerance at room temperature within 10ppm;
- ÿ The antenna reserves a γ -type circuit for antenna matching adjustment;
- ÿ Confirm the connection direction of PCM and UART interface, such as IN and OUT, TXD and RXD;
- ÿ If you need to use a module with 32.768k clock input, 32.768k requires a pull-up resistor and you need to pay attention to the clock amplitude meeting the WIFI module

Parameters of the group.

2.3.2 SARADC Circuit

RK3588 integrates a SARADC controller with a resolution of 12 bits, a speed of 1MS/s, and an input voltage range of 0-1.8V.

It can provide 8-way SARADC input.

SARADC_IN0_BOOT is dedicated to the setting of SYSTEM BOOT startup sequence and cannot be used for other functions.

The value obtained by voltage division sampling is used to determine which interface to boot from. The settings are as follows: (Rup/Rdown represent pull-up and pull-down resistors)

Item	Rup(ohm)	Rdown(ohm)	ADC VOL(Unit:V)		BOOT MODE
LEVEL1	DNP	100K	0	0	USB (Maskroom Mode)
LEVEL2	100K	20K	682	0.3	SD Card γ USB
LEVEL3	100K	51K	1365	0.6	EMMC γ USB
LEVEL4	100K	100K	2047	0.9	FSPI_M0 γ USB
LEVEL5	100K	200K	2730	1.2	FSPI_M1 γ USB
LEVEL6	100K	499K	3412	1.5	FSPI_M2 γ USB
LEVEL7	100K	DNP	4095	1.8	FSPI_M2 γ FSPI_M1 γ FSPI_M0 γ EMMC_SD Card γ USB

If Rup=DNP, Rdown=100K; RK3588 device is connected to USB cable, then powered on, the system can directly enter Maskrom.

SARADC_VIN1 is used as the key input sample and multiplexed as the Recovery mode key (cannot be modified).

SARADC_VIN1 is pulled up to VCCA_1V8_S0 through a 10Kohm pull-up resistor. The default is high level (1.8V).

If the system has been powered on and the firmware has been burned, the system will be directly entered after power on. If the Recovery mode button is pressed when the system starts,

That is, keep SARADC_VIN1 at low level (0V), then RK3588 enters Loader programming mode. When the PC recognizes the USB device,

Releasing the button returns SARADC_VIN1 to a high level (1.8V), allowing firmware programming. Therefore, if the product does not have a button, leaving SARADC_VIN1 floating will cause it to become unstable, potentially affecting startup. Therefore, the 10kohm pull-up resistor on SARADC_VIN1 must be retained and not removed to ensure normal startup behavior. For development convenience, it is recommended to reserve a button or test point on SARADC_VIN1.

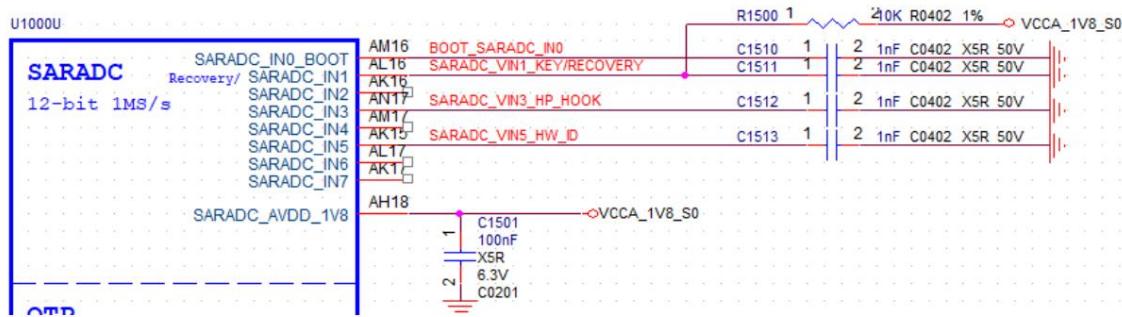


Figure 2-70 SARADC VINO interface

On the RK3588, the key array adopts a parallel type. The input key value can be adjusted by adding or removing keys and adjusting the voltage divider resistor ratio to achieve multi-key input to meet customer product requirements. The design recommends that the key value of any two keys must be greater than +/-35, that is, the center voltage difference must be greater than 123mV.

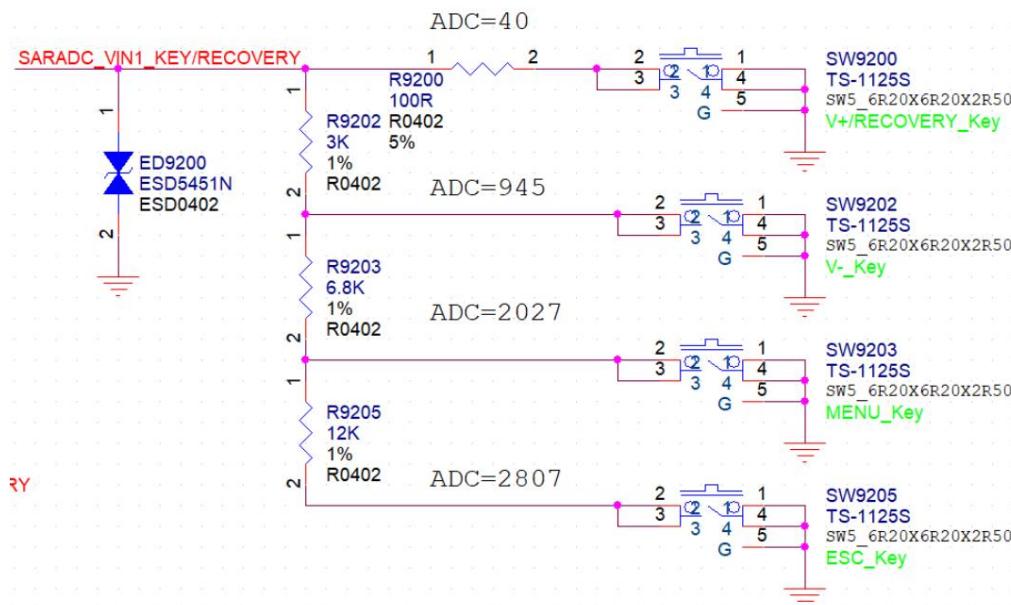


Figure 2-71 RK3588 SARADC key matrix circuit

RK3588 SARADC design considerations:

þ The decoupling capacitor of the SARADC_AVDD_1V8 power supply must not be deleted. During layout, it must be placed close to the RK3588 pin.

þ If SARADC_VIN[7:0] is used, a 1nF capacitor must be added near the pin to eliminate jitter.

þ When used for key acquisition, ESD protection must be done near the key, and a 100ohm resistor must be connected in series with the 0 key value to enhance the anti-static surge capability (if there is only one key, the ESD must be close to the key, first passing through ESD100ohm resistor1nFchip pin).

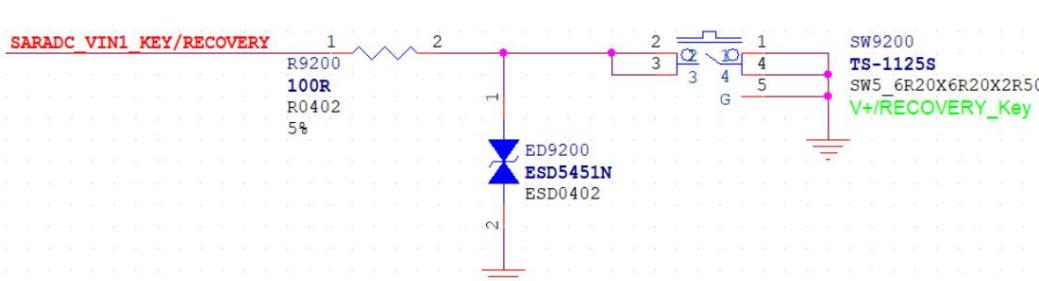


Figure 2-72 RK3588 SARADC single-button circuit

2.3.3 OTP Circuit

RK3588 has 32Kbit internal space and high 4Kbit address non-safe space for programming. Supports programming, reading and idle modes.

In these modes, the OTP_VDDOTP_0V75 pin must be powered.

The decoupling capacitor of the OTP_VDDOTP_0V75 power supply must not be deleted and should be placed close to the RK3588 pin during layout.

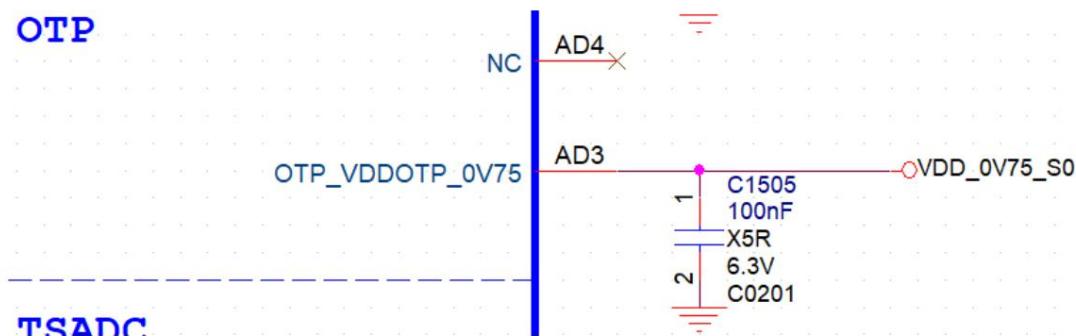


Figure 2-73 RK3588 OTP power pin

2.3.4 USB2.0/USB3.0 Circuit

The RK3588 chip has two built-in USB3.0 OTG controllers (two embedded USB2.0 OTG, shown in green in the figure below), and one USB3.0 HOST Controller, 2 USB2.0 HOST controllers.

The internal multiplexing diagram of these controllers and PHY is as follows:

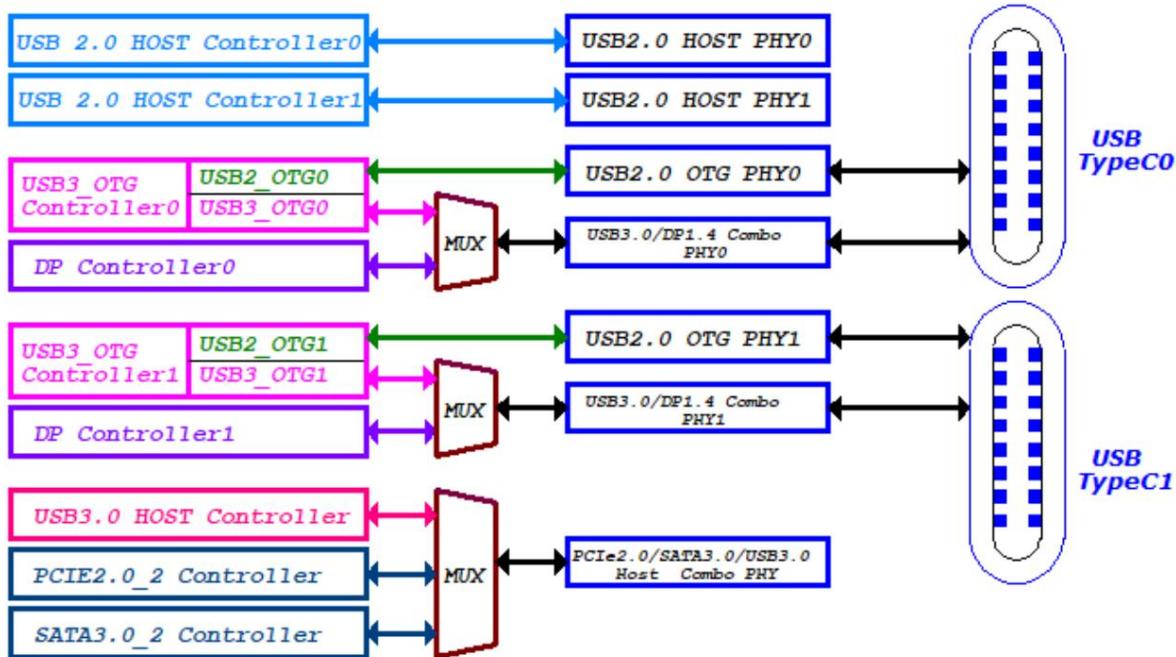


Figure 2-74 Internal multiplexing relationship between USB PHY and USB Controller

The USB3.0 OTG controller supports SS/HS/FS/LS. The embedded USB2.0 (HS/FS/LS) signal uses USB2.0 OTG PHY. The signal name is shown in the red box in the figure below. Currently, RK3588 only supports Fireware Download on this interface. Please make sure to reserve it in your application.

This interface.

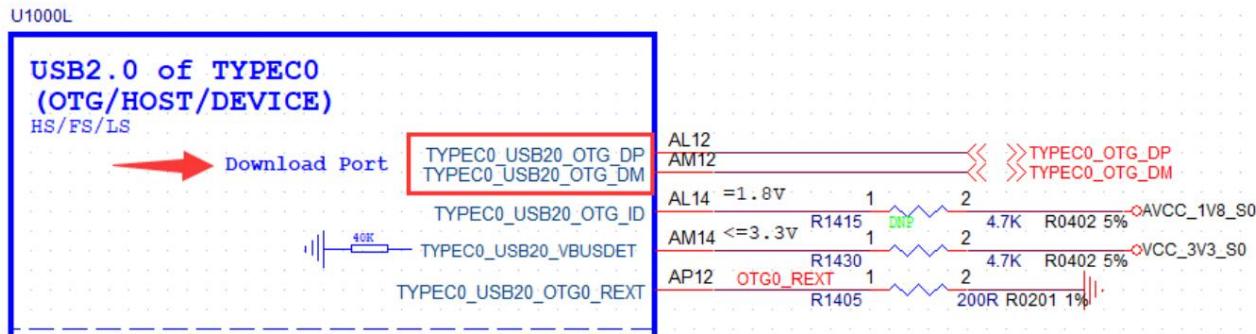


Figure 2-75 TYPEC0 USB2.0 OTG pins



Notice

only TYPEC0_USB2.0_OTG0_DP/TYPEC0_USB2.0_OTG_DM

support Download Firmware

If the product does not use this interface,

This interface must be reserved during the production process. Note: `USB3_OTG0_VBUSDET`

Must be connected too!

The USB 3.0 SS signal (5Gbps) is multiplexed with DP1.4, using the USB/DP Combo PHY; the signal is shown in the red box in the figure below.

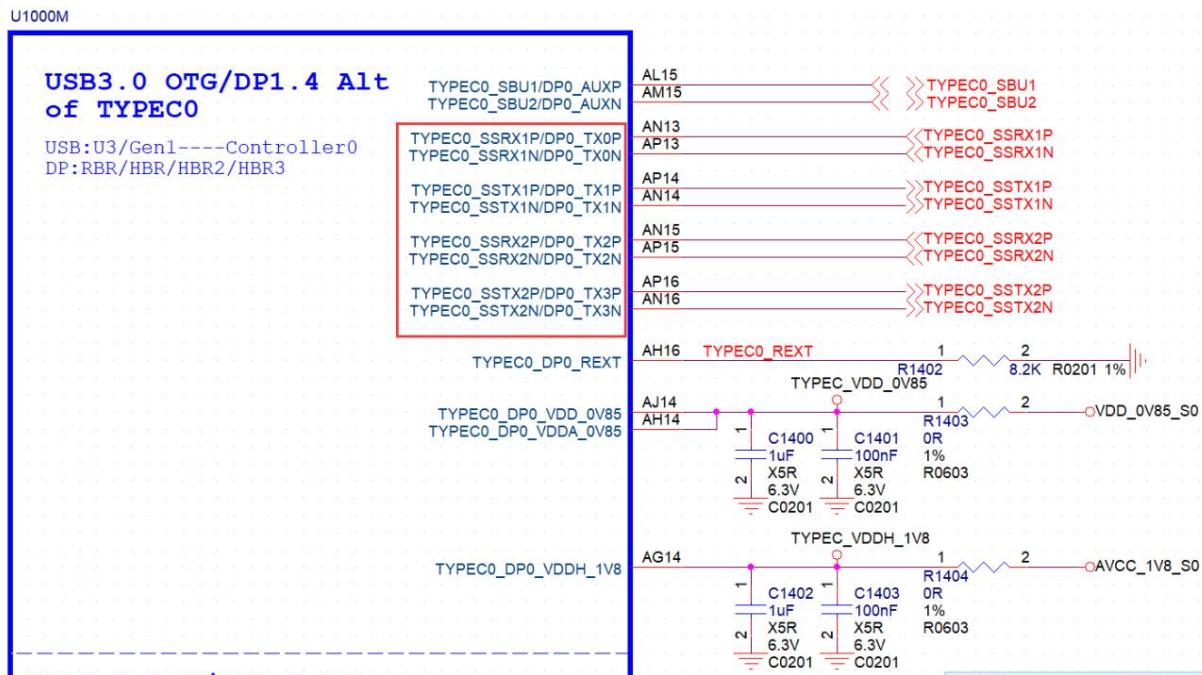


Figure 2-76 TYPEC0 USB3.0 OTG and DP pins

Since USB3.0 OTG and USB2.0 OTG are the same USB3.0 controller, USB3.0 and USB2.0 OTG

It can only be used as a device or a host at the same time. It cannot be used as a host for USB3.0 OTG or a device or a host for USB2.0 OTG.

The OTG of USB2.0 acts as the device and the OTG of USB2.0 acts as the host.

USB3.0 Controller0 and DP1.4 Controller0 are combined into a complete TYPEC through USB3.0/DP1.4 Combo PHY

Port, this Combo PHY supports Display Alter mode, Lane0 and Lane2 do TX in DP mode and do RX in USB mode;

TX and RX share Lane0 and Lane2.

The TYPEC1 port composed of USB3.0 Controller1 and DP1.4 Controller1 is the same as the TYPEC0 port, so it will not be described again. This USB3.0/DP1.4 Combo PHY supports lane swapping (SWAP), so a TYPEC standard port can have the following functions:

The following five configurations:

Configuration 1: Type-C 4Lane (with DP function)

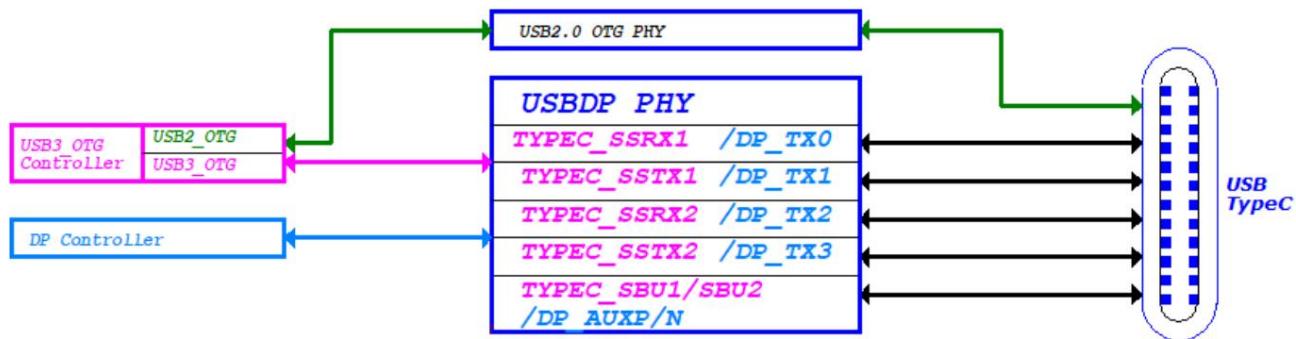


Figure 2-77 Connection diagram between TYPEC0 4Lane and DP

Configuration 2: USB2.0 OTG+DP 4Lane (Swap OFF)

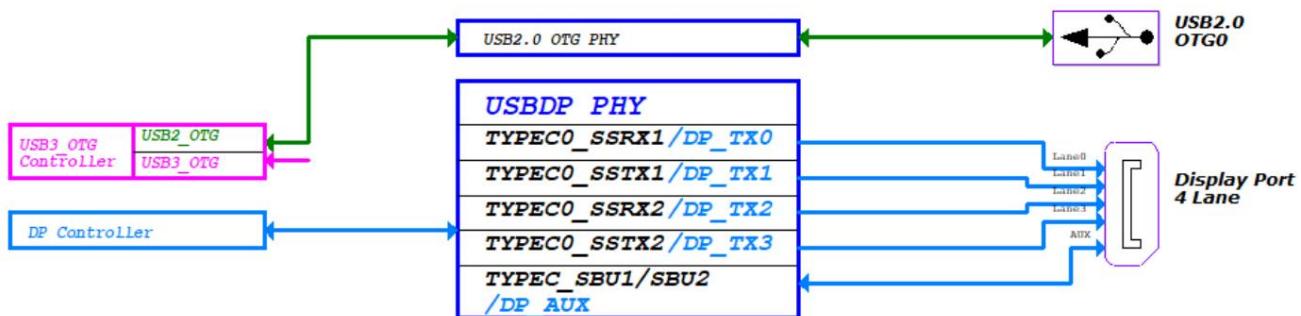


Figure 2-78 USB2.0 OTG+DP 4Lane connection diagram

Configuration 3: USB2.0 OTG+DP 4Lane (Swap ON)

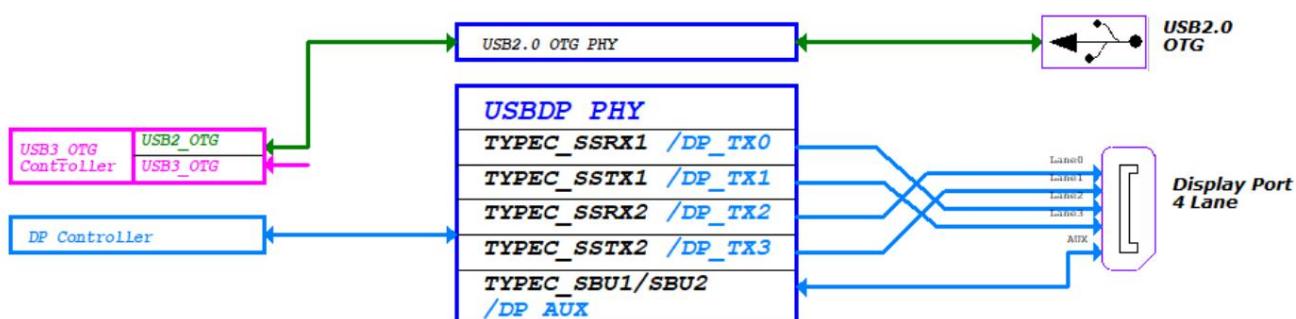


Figure 2-79 USB2.0 OTG+DP 4Lane (Swap ON) connection diagram

Configuration 4: USB 3.0 OTG 0 + DP 2 Lane (Swap OFF)

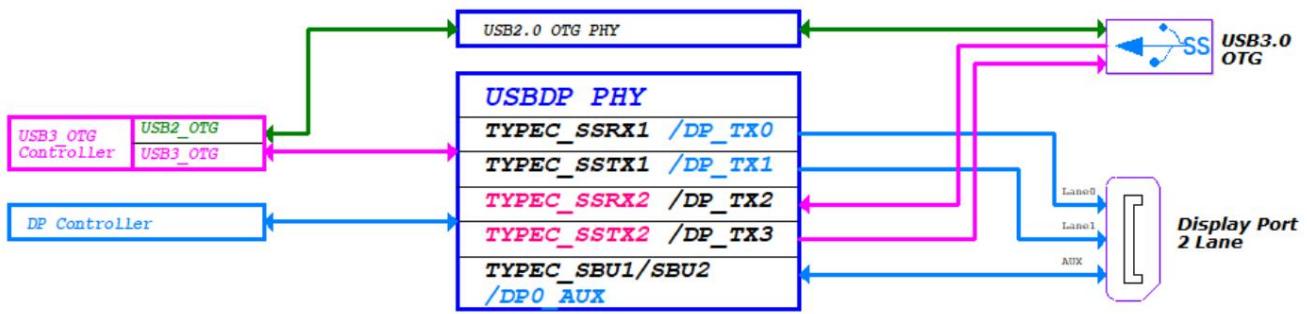


Figure 2-80 USB3.0 OTG0+DP 2Lane (Swap OFF) connection diagram

Configuration 5: USB3.0 OTG+DP 2Lane (Swap ON)

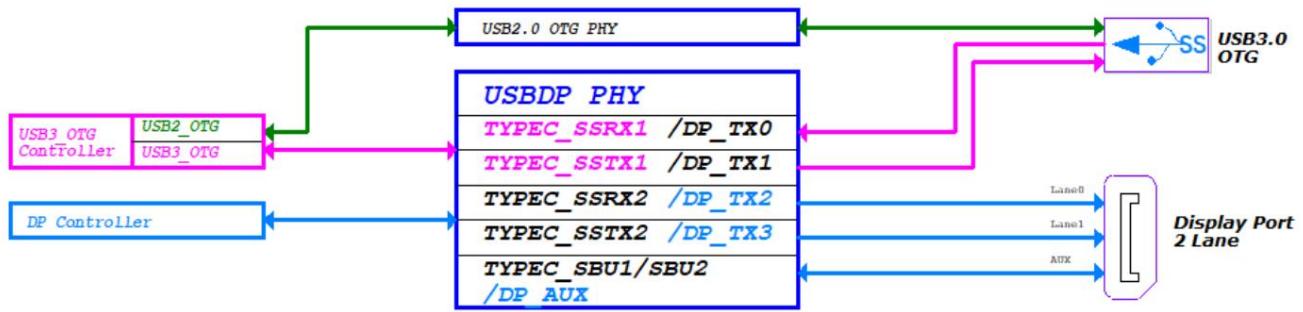


Figure 2-81 USB3.0 OTG0+DP 2Lane (Swap ON) connection diagram

For the pin assignments of the above configurations, please refer to PAGE 07 of the EVB schematic diagram.

The USB3.0 HOST controller only has USB3.0 HOST and no USB2.0 is embedded. If you need to form a complete USB3.0

HOST interface, needs to be combined with USB2.0 HOST Controller1 (configuration one) or USB2.0 HOST Controller0 (configuration two)

A standard USB3.0 HOST. The internal connection diagram is as follows:

Configuration 1: USB3.0 HOST2 + USB2.0 HOST1

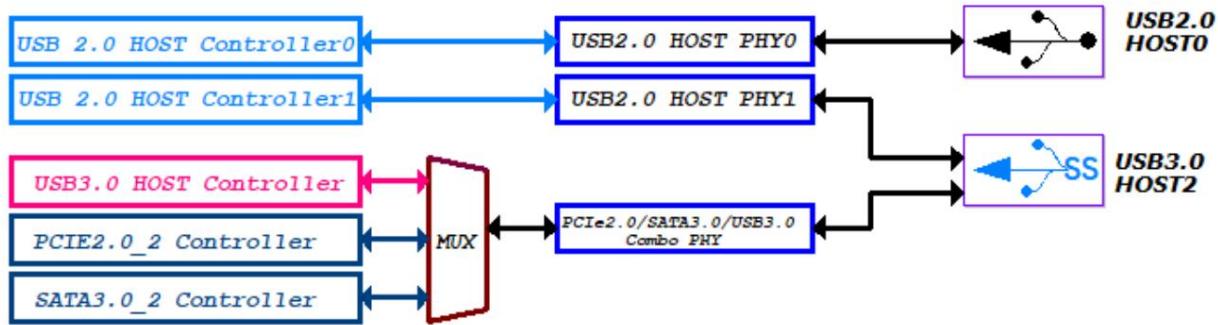


Figure 2-82 Connection diagram of USB3.0 HOST2 + USB2.0 HOST1

Configuration 2: USB3.0 HOST2 + USB2.0 HOST0

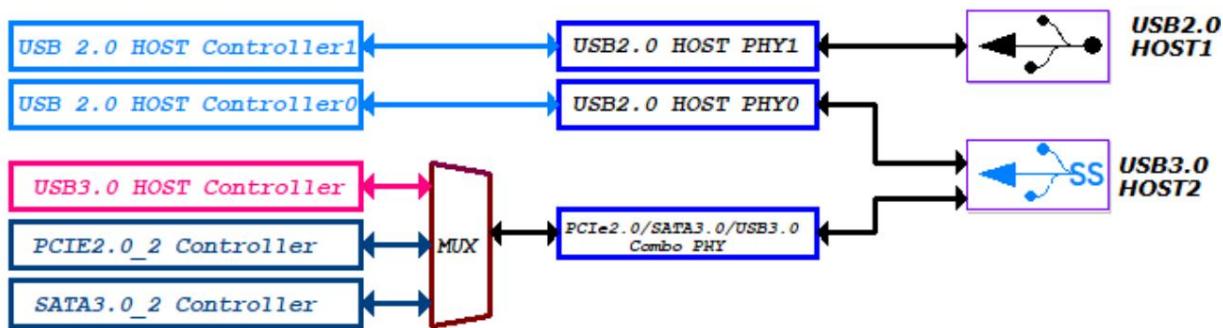


Figure 2-83 Connection diagram of USB3.0 HOST2 + USB2.0 HOST0

The USB2.0 HOST0 controller uses the USB2.0 HOST0 PHY. The signals in the box below constitute the USB2.0 HOST0 interface:

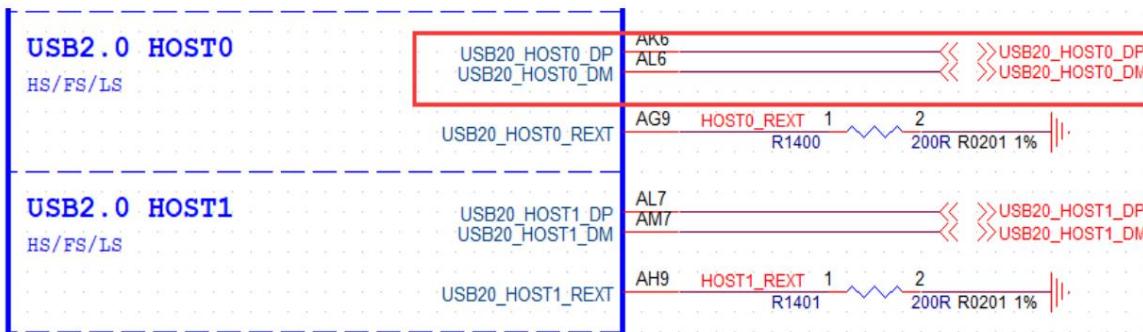


Figure 2-84 USB2.0 HOST0 pins

The USB2.0 HOST1 controller uses the USB2.0 HOST1 PHY. The signals in the following box constitute the USB2.0 HOST1 interface:

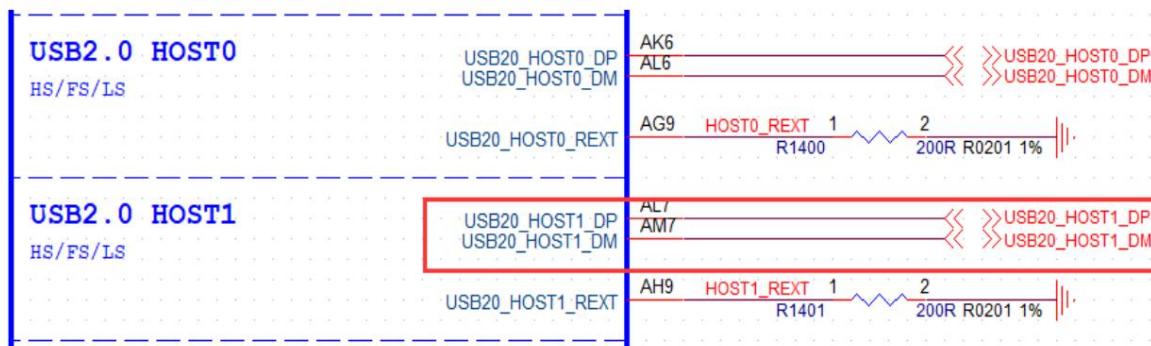


Figure 2-85 USB2.0 HOST1 pins

The internal connection diagram of USB2.0 Controller and PHY is as follows:

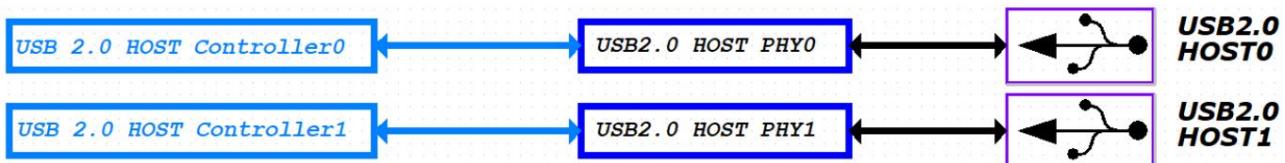


Figure 2-86 Connection diagram of USB2.0 Controller and PHY

Please note the following when designing USB2.0/USB3.0:

TYPEC0_USB20_OTG_DP/TYPEC0_USB20_OTG_DM is the system firmware burning port. If the product does not use this interface, this interface must be reserved during the debugging and production process, otherwise debugging and production firmware burning will not be possible;
 ÿ TYPEC_USB20_OTG0_ID has about 200Kohm resistor inside to pull up to USB20_AVDD_1V8; ÿ TYPEC_USB20_VBUSDET is the OTG and Device mode detection pin, high effective, 2.7-3.3V, TYP: 3.0V, it is recommended to place a 100nF capacitor on the pin.

OTG mode can be set to the following three modes: ÿ OTG

mode: automatically switch to device mode or HOST mode according to the ID pin status, ID high is device, ID low is HOST,

When in device mode, it will also check whether the VBUSDET pin is high (greater than 2.3V). If it is high, DP will be pulled high.

Start enumeration:

ÿ Device mode: When set to this mode, no ID pin is needed. You only need to check whether the VBUSDET pin is high (greater than 2.3V).

If it is high, DP will be pulled high to start enumeration;

ÿ HOST mode: When set to this mode, the ID and VBUSDET status do not need to be concerned. (If the product only needs HOST mode, but since only TYPEC0_USB20_OTG_DP/

TYPEC0_USB20_OTG_DM is the system firmware programming port, this port is needed during debugging and production. When programming and adb debugging, it needs to be set to device mode, so

The TYPEC_USB20/1_VBUSDET signal must also be connected).

Before uboot starts, the default mode is device mode. After entering uboot, you can configure these three modes according to actual needs.

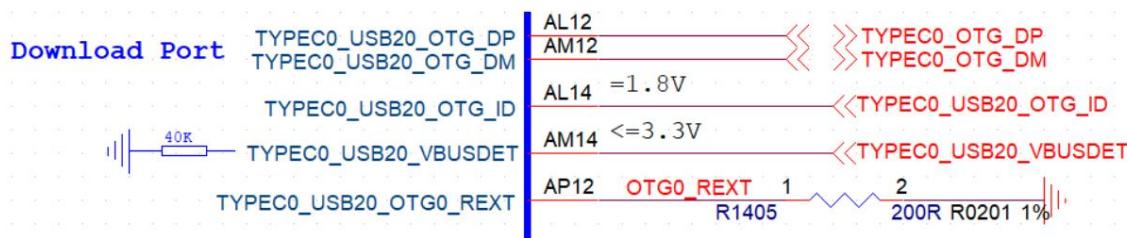


Figure 2-87 RK3588 TYPEC0_USB20_OTG circuit

If the TYPEC interface is used, the pin "TYPEC0_USB20_VBUSDET" can be connected to 1.8V through a 4.7K pull-up resistor;

Using Micro USB2.0 interface, the following circuit is adopted:

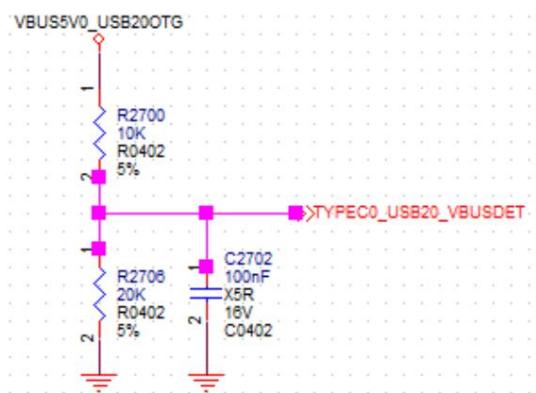


Figure 2-88 TYPEC0_USB20_VBUSDET detection circuit

To improve USB performance, the decoupling capacitors of each PHY power supply must not be removed and should be placed close to the pins during layout.

ÿ To enhance the anti-static and surge capabilities, ESD devices must be reserved for the signal. The ESD parasitic capacitance of the USB2.0 signal must not exceed 3pF. In addition, a

2.2ohm resistor is connected in series with the DP/DM of the USB2.0 signal to enhance the anti-static surge capability. This resistor must not be deleted. See the figure below.

Take USB20_HOST_DP/DM as an example. Other USB2.0 interfaces also need to be processed in the same way.

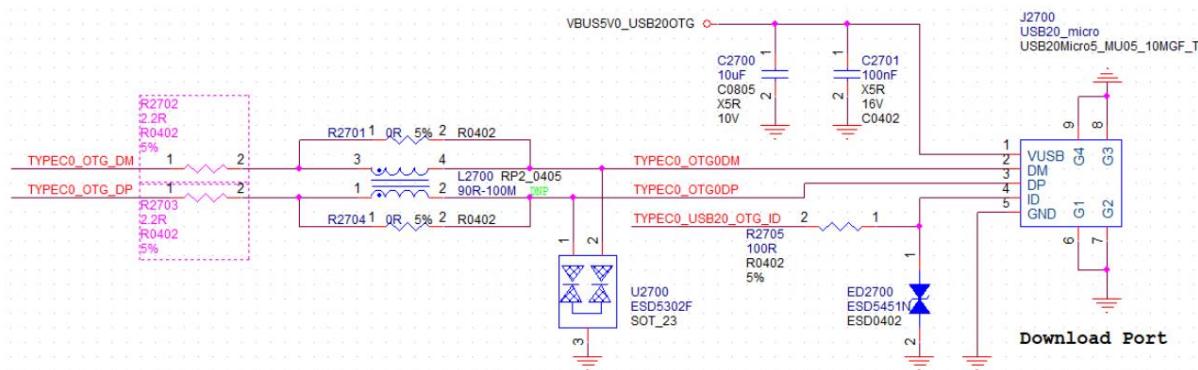


Figure 2-89 USB2.0 signal connected in series with a 2.2ohm resistor circuit

To suppress electromagnetic radiation, consider reserving a common-mode choke on the signal line. During debugging, choose to use a resistor or a common-mode choke based on the actual situation. See the figure below,

which uses USB20_HOST_DP as an example. Other USB2.0 interfaces also require the same treatment.

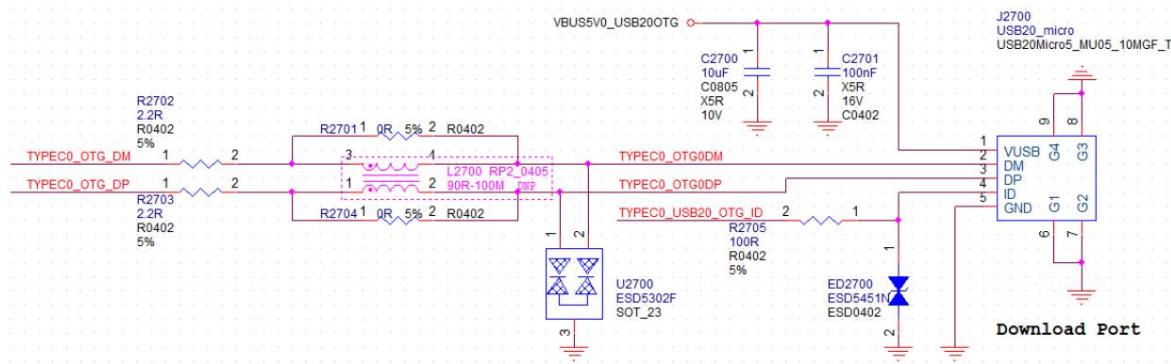


Figure 2-90 USB2.0 signal string common-mode inductor circuit

If the TYPEC_USB20_OTG0/1_ID signal is used, ESD devices must be reserved on the signal to enhance the anti-static and surge capabilities.

And connect a 100ohm resistor in series, do not delete it, see the figure below:

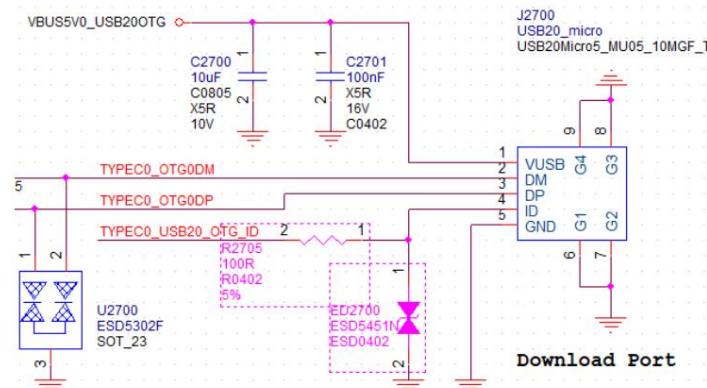


Figure 2-91 TYPEC_USB20_OTG0/1_ID pin circuit

When the HOST function is used, it is recommended to add a current limiting switch to the 5V power supply. The current limiting size can be adjusted according to the application needs. The current limiting switch uses a 3.3V

For GPIO control, it is recommended to add 22uF and 100nF or more capacitors to filter the 5V power supply; if the USB port may be connected to a mobile hard disk, it is recommended to add more filters.

The capacitor should be above 100uF.

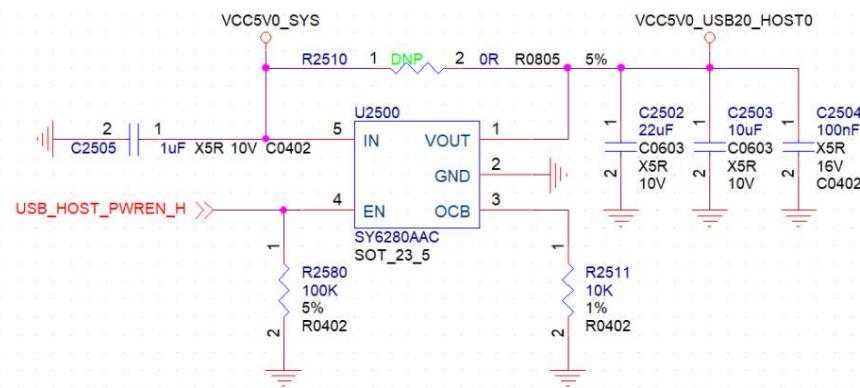


Figure 2-92 USB 5V current limiting circuit

The TYPEC protocol requires adding a 100nF AC coupling capacitor on the SSTXP/N line. The AC coupling capacitor is recommended to use a 0201 package, which is lower.

The ESR and ESL can also reduce the impedance variation on the line.

All signals of TYPEC socket must add ESD devices and be placed close to the USB connector during layout.

Signal, ESD parasitic capacitance shall not exceed 0.3pF.

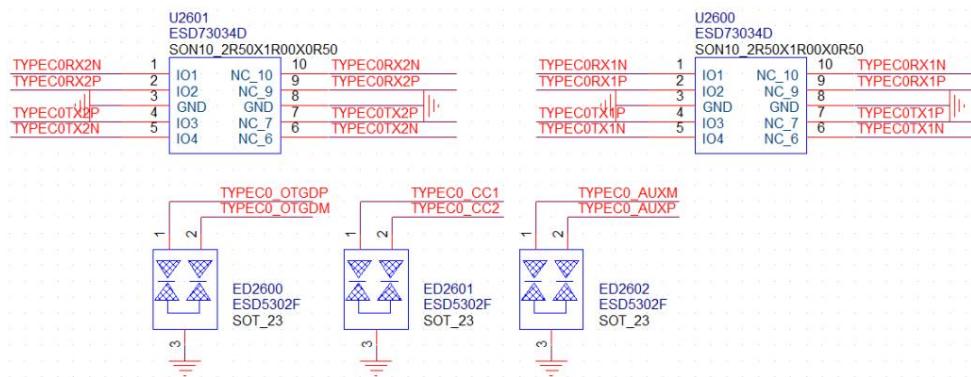


Figure 2-93 TYPEC socket ESD circuit

The recommended USB2.0/USB3.0 interface matching design is shown in the following table:

Table 2-16 RK3588 USB2.0/USB3.0 interface design

Signal	Connection method	illustrate
TYPEC0_USB20_OTG_DP/DM connected in series	with a 2.2ohm resistor	USB HS/FS/LS mode data input/output
TYPEC_SSTXP/SSTXN	Connect a 100nF capacitor in series (0201 package recommended)	USB SS mode data output
TYPEC_SSXP/SSRXN	Connect a 0ohm resistor in series	USB SS mode data input
TYPEC_USB20_OTG_ID	Connect a 100ohm resistor in series (external power supply should be strengthened, power supply superior)	USB OTG ID identification, required for Micro-USB interface use
TYPEC_USB20_VBUSDET resistor voltage divider detection		USB OTG insertion detection
USB30_2_SSTXP/SSTXN	Connect a 100nF capacitor in series (0201 package recommended)	USB SS mode data output
USB30_2_SSXP/SSRXN	Connect a 0ohm resistor in series	USB SS mode data input
HOST0_DP/DM	Connect a 2.2ohm resistor in series	USB HS/FS/LS mode data input/output
HOST1_DP/DM	Connect a 2.2ohm resistor in series	USB HS/FS/LS mode data input/output

2.3.5 SATA 3.0 Circuit

The RK3588 chip has three SATA3.0 controllers, and multiplexes PIPE PHY0/1/2 with PCIe and USB3_HOST2 controllers.

Please see the figure below for the diameter.

- ÿ Support SATA PM function, each port can support 5 devices;
- Supports SATA 1.5Gb/s, SATA 3.0Gb/s, and SATA 6.0Gb/s speeds.
- ÿ Supports eSATA.

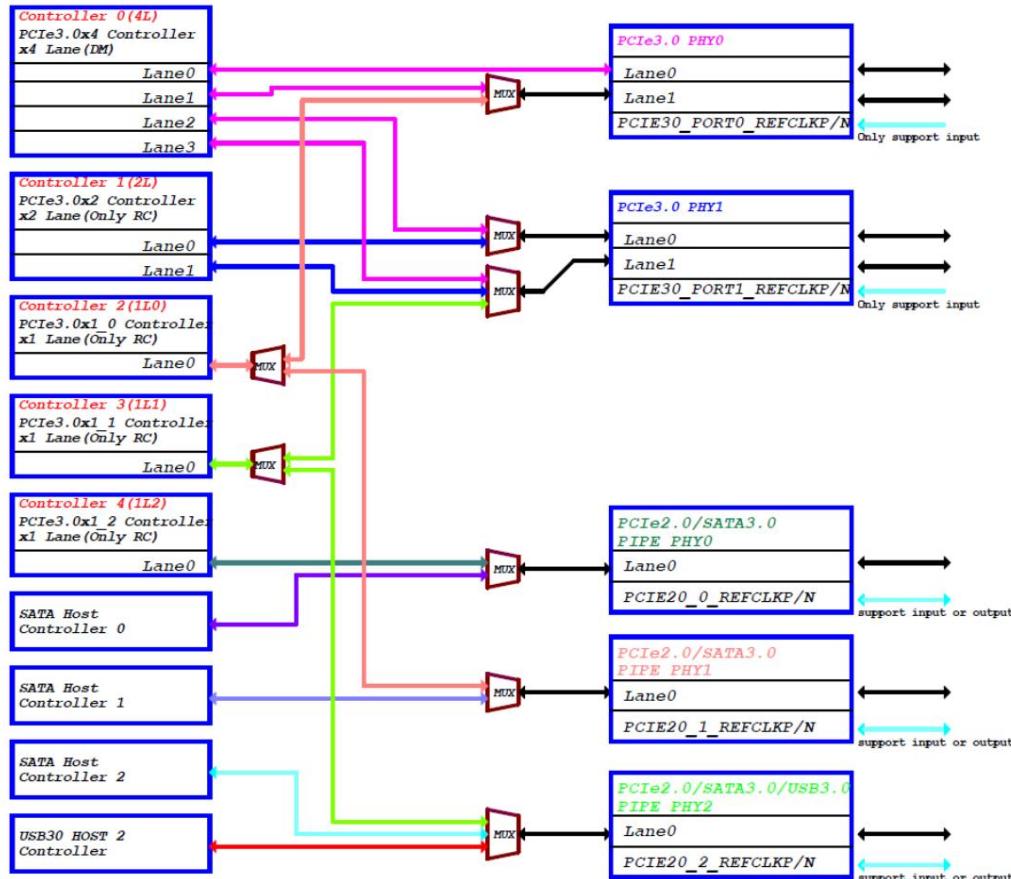
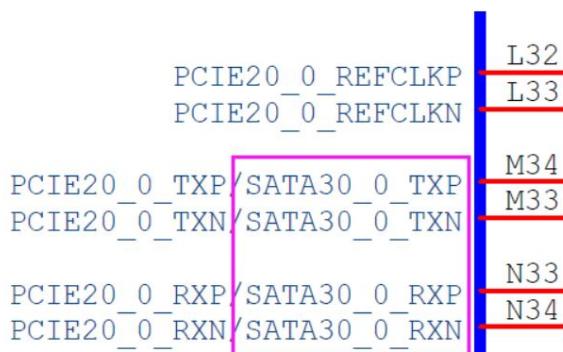
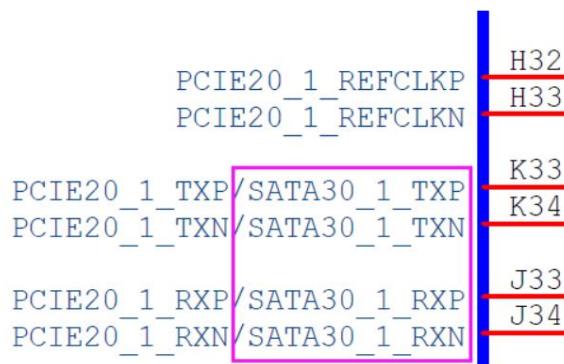


Figure 2-94 PIPE_PHY0/1/2 and SATA 3.0 controller multiplexing relationship

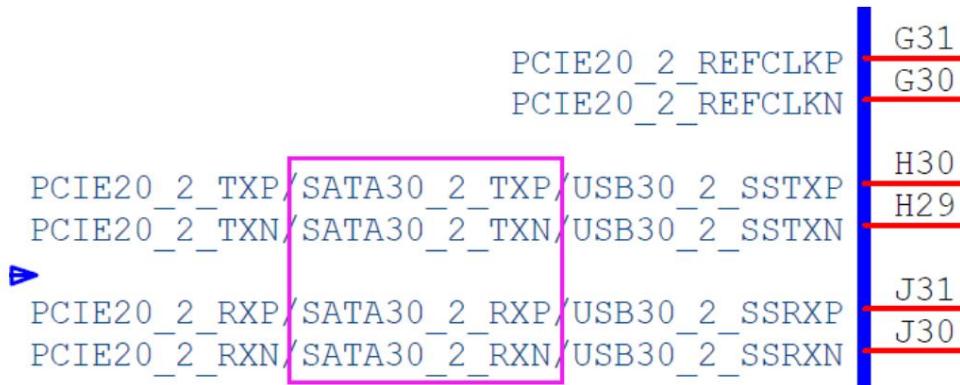
The SATA0 controller uses PIPE_PHY0 (multiplexed with the PCIe3.0x1_2 Controller).



The SATA1 controller uses PIPE_PHY1 (multiplexed with the PCIe3.0x1_0 Controller).



The SATA2 controller uses PIPE_PHY2 (multiplexed with the PCIe3.0x1_1 Controller and USB30 HOST2 Controller).



SATA0/1/2 controller related control IO are

- ÿ SATA0_ACT_LED: SATA0 interface LED flashing control output when data is transmitted;
- ÿ SATA1_ACT_LED: SATA1 interface LED flashing control output when data is transmitted;
- ÿ SATA2_ACT_LED: SATA2 interface LED flashing control output when data is transmitted;
- ÿ SATA_CP_DET: SATA hot-swappable device plug detection input; ÿ
- SATA_MP_SWITCH: SATA hot-swappable device switch detection input; ÿ
- SATA_CP POD: SATA hot-swappable device power switch output; ÿ
- SATA_CP_DET, SATA_MP_SWITCH, SATA_CP POD are SATA0/1/2 common interfaces, which can be controlled by registering
- The memory configuration is SATA0, SATA1 or SATA2, in the PMUIO2 power domain;
- ÿ SATA0_ACT_LED, SATA1_ACT_LED, SATA2_ACT_LED are multiplexed to two locations, one at VCCIO6 power domains, one in the VCCIO4 power domain.

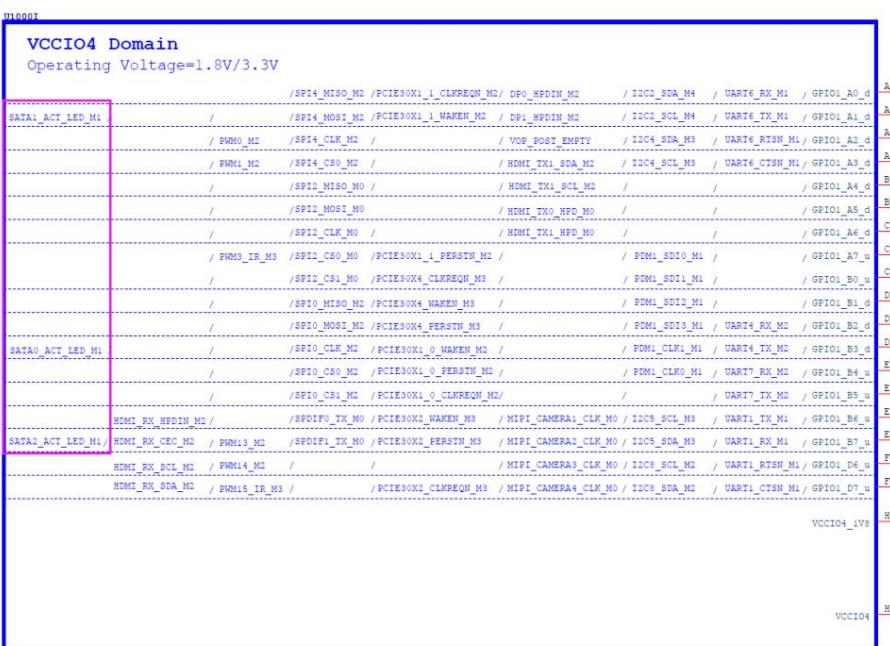


Figure 2-95 SATA0/1/2 related control IO pins

Please note in SATA design: Ѽ

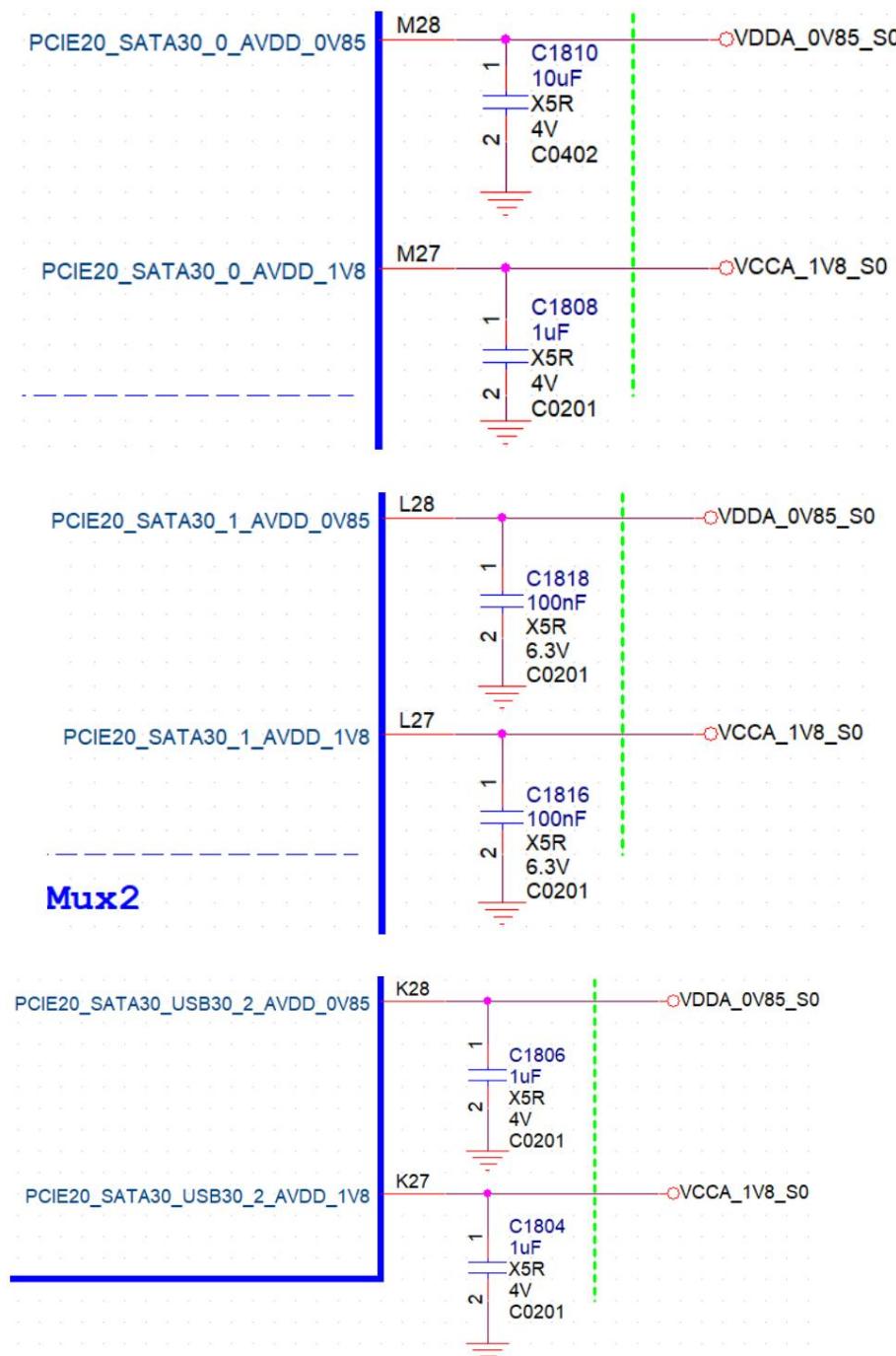
When designing the slot, the peripheral circuit and power supply must meet the Spec

requirements; Ѽ PCIE20_SATA30_0/1_AVDD_0V85/PCIE20_SATA30_USB30_2_AVDD_0V85, these three 0.85V combined power supplies, need to place

1x10uF+1x1uF+1x100nF decoupling capacitors, and place them close to the RK3588 pins during layout.

PCIE20_SATA30_0/1_AVDD_1V8/PCIE20_SATA30_USB30_2_AVDD_1V8 three-way 1.8V combined power supply requires 2x1uF +1x100nF decoupling capacitors.

When laying out, place them close to the RK3588 pins.



Ѡ 10nF AC coupling capacitor connected in series to the TXP/N and RXP/N differential signals of the SATA interface. It is recommended to use 0201 AC coupling capacitor.

Package, lower ESR and ESL, can also reduce impedance changes on the line;

Ѡ All signals of the eSATA interface socket must be equipped with ESD devices and placed close to the socket during layout. The ESD parasitic capacitance must not exceed

0.4pF \ddot{Y}

ŷ SATA interface matching design recommendations are shown in the following table:

Table 2-17 RK3588 SATA interface design

Signal	Connection method	illustrate
SATA30_0_TXP/TXN	Connect a 10nF capacitor in series (0201 package recommended)	SATA data out
SATA30_0_RXP/RXN	Connect a 10nF capacitor in series (0201 package recommended)	SATA data input
SATA30_1_TXP/TXN	Connect a 10nF capacitor in series (0201 package recommended)	SATA data out
SATA30_1_RXP/RXN	Connect a 10nF capacitor in series (0201 package recommended)	SATA data input
SATA30_2_TXP/TXN	Connect a 10nF capacitor in series (0201 package recommended)	SATA data out
SATA30_2_RXP/RXN	Connect a 10nF capacitor in series (0201 package recommended)	SATA data input

2.3.6 PCIe 2.0 and PCIe 3.0 Circuits

The RK3588 chip has five PCIe 3.0 controllers: (DM stands for Dual Mode, RC stands for Root Complex.)

1. Controller 0(4L)ŷPCIe3.0x4 Controller x4 Lane(DM)
2. Controller 1(2L)ŷPCIe3.0x2 Controller x2 Lane(Only RC)
3. Controller 2(1L0)ŷPCIe3.0x1_0 Controller x1 Lane(Only RC)
4. Controller 3(1L1)ŷPCIe3.0x1_1 Controller x1 Lane(Only RC)
5. Controller 4(1L2)ŷPCIe3.0x1_2 Controller x1 Lane(Only RC)

2 PCIe3.0 PHYs, data bit 2Lane, PCIe3.0 PHY0 and PCIe3.0 PHY1.

3 PCIe2.0 Combo PHYs, data bit 1 Lane, PCIe2.0/SATA3.0 Combo PHY0, PCIe2.0/SATA3.0 Combo

PHY1 and PCIe2.0/SATA3.0/USB3.0 HOST Combo PHY2.

Mapping diagram between Controller and PHY:

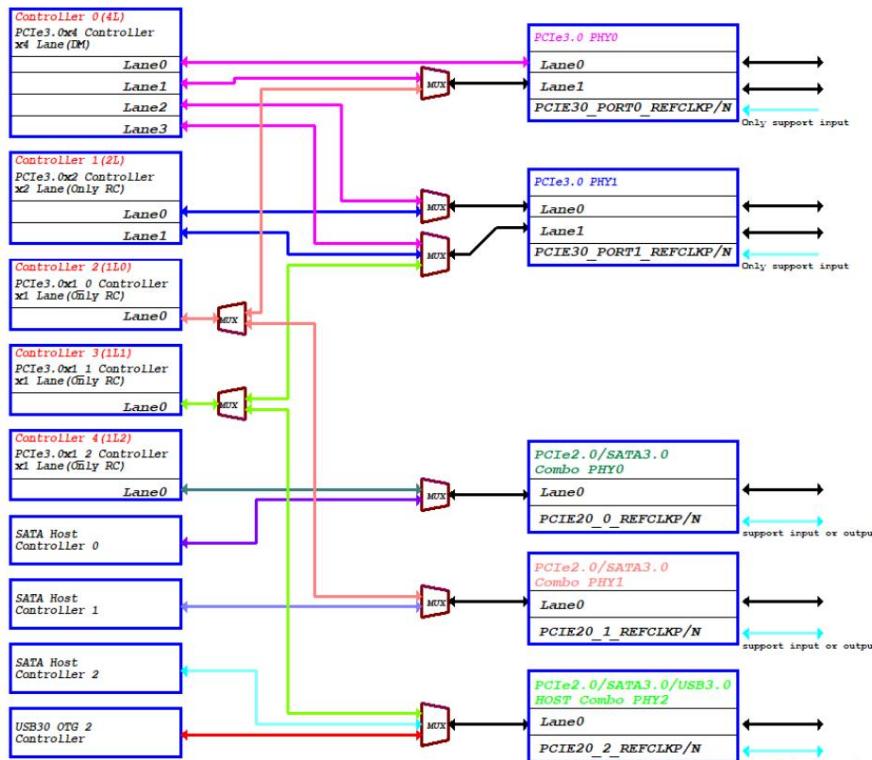


Figure 2-96 RK3588 PCIe 5 Controllers and 5 PHYs mapping diagram

- ÿ Controller 0 (4L) Lane 0 can only be combined with PCIe 3.0 PHY 0 Lane 0;
- ÿ Controller 1(2L) Lane 0 can only be combined with PCIe3.0 PHY1 Lane 0;
- ÿ Controller 1(2L) + PCIe3.0 PHY1, forming 2Lane PCIe3.0 X2Lane RC mode. Compatible with PCIe3.0 X1Lane RC model;

RK3588 PCIE Signal		PCIe3.0 X2Lane RC	PCIe3.0 X1Lane RC
Port1	PCIE30_PORT1_TX0P/N	ÿ	ÿ
	PCIE30_PORT1_RX0P/N	ÿ	ÿ
	PCIE30_PORT1_TX1P/N	ÿ	ÿ
	PCIE30_PORT1_RX1P/N	ÿ	ÿ
	PCIE30_PORT1_REFCLKP/N_IN	ÿ	ÿ

ÿ Controller 0 (4Lane) + PCIe 3.0 PHY0 + PCIe 3.0 PHY1 form 4 lanes of PCIe 3.0 x4Lane RC or EP mode.

Compatible with PCIe3.0 X2Lane RC or EP mode, compatible with PCIe3.0 X1Lane RC or EP mode;

RK3588 PCIE Signal		PCIe3.0 X4Lane RC or EP	PCIe3.0 X2Lane RC or EP	PCIe3.0 X1Lane RC or EP
Port0	PCIE30_PORT0_TX0P/N	ÿ	ÿ	ÿ
	PCIE30_PORT0_RX0P/N	ÿ	ÿ	ÿ
	PCIE30_PORT0_TX1P/N	ÿ	ÿ	ÿ
	PCIE30_PORT0_RX1P/N	ÿ	ÿ	ÿ
	PCIE30_PORT0_REFCLKP/N_IN	ÿ	ÿ	ÿ
Port1	PCIE30_PORT1_TX0P/N	ÿ	ÿ	ÿ
	PCIE30_PORT1_RX0P/N	ÿ	ÿ	ÿ
	PCIE30_PORT1_TX1P/N	ÿ	ÿ	ÿ
	PCIE30_PORT1_RX1P/N	ÿ	ÿ	ÿ
	PCIE30_PORT1_REFCLKP/N_IN	ÿ	ÿ	ÿ

ÿ Controller 4 (1L2) + PCIe2.0/SATA3.0 Combo PHY0, forming 1Lane PCIe2.0 x1Lane RC mode;

ÿ The signal corresponding to this mode is:

RK3588 PCIE Signal		PCIe2.0 X1Lane RC
PCIe2.0/SATA3.0 Combo PHY0	PCIE20_0_TXP/N	ÿ
	PCIE20_0_RXP/N	ÿ
	PCIE20_0_REFCLKP/N	ÿ

ÿ Controller 2 (1L0) + PCIe 3.0 PHY0 Lane 1 forms a 1Lane PCIe 3.0 X1Lane RC, or Controller 2 (1L0) + PCIe 2.0/SATA 3.0 Combo PHY1 forms a PCIe 2.0 X1Lane RC. Therefore, these two modes cannot be used at the same time;

ÿ The signals corresponding to the PCIe3.0 X1Lane RC mode in this mode are:

RK3588 PCIE Signal		PCIe3.0 X1Lane RC
Port0	PCIE30_PORT0_TX1P/N	ÿ
	PCIE30_PORT0_RX1P/N	ÿ
	PCIE30_PORT0_REFCLKP/N_IN	ÿ

ŷ The signals corresponding to the PCIe2.0 X1Lane RC mode in this mode are:

RK3588 PCIE Signal		PCIe2.0 X1Lane RC
PCIe2.0/SATA3.0 Combo PHY1	PCIE20_1_TXP/N	ŷ
	PCIE20_1_RXP/N	ŷ
	PCIE20_1_REFCLKP/N	ŷ

ŷ Controller 3 (1L1) + PCIe3.0 PHY1 Lane 1 forms 1Lane PCIe3.0 X1Lane RC mode, or Controller 3 (1L1) + PCIe2.0/SATA3.0/USB3.0 HOST

Combo PHY2 forms PCIe2.0 X1Lane RC mode, so these two

Modes cannot be used simultaneously.

ŷ The signals corresponding to the PCIe3.0 X1Lane RC mode in this mode are:

RK3588 PCIE Signal		PCIe3.0 X1Lane RC
Port1	PCIE30_PORT1_TXP/N	ŷ
	PCIE30_PORT1_RXP/N	ŷ
	PCIE30_PORT1_REFCLKP/N_IN	ŷ

ŷ The signals corresponding to the PCIe2.0 X1Lane RC mode in this mode are:

RK3588 PCIE Signal		PCIe2.0 X1Lane RC
PCIe2.0/SATA3.0/USB HOST Combo PHY2	PCIE20_2_TXP/N	ŷ
	PCIE20_2_RXP/N	ŷ
	PCIE20_2_REFCLKP/N	ŷ

Based on the above description, multiple modes can be supported. Therefore, if PCIe functions are used, RK3588 can support multiple PCIe modes.

Up to 5 modes can be used simultaneously.

eg1: 1 x PCIe3.0 X4Lane RC or EP
+ 3 x PCIe2.0 X1Lane RC

PCIe3.0 x4Lane	Controller 0 (4L) RC or EP	PCIe3.0 PHY0 Lane0+Lane1 + PCIe3.0 PHY1 Lane0+Lane1
+ PCIe2.0 x1Lane	Controller 4 (1L2) RC	PCIe2.0/SATA3.0 Combo PHY0
+ PCIe2.0 x1Lane	Controller 2 (1L0) RC	PCIe2.0/SATA3.0 Combo PHY1
+ PCIe2.0 x1Lane	Controller 3 (1L1) RC	PCIe2.0/SATA3.0/USB3.0 HOST Combo PHY2

eg2: 1 x PCIe3.0 X2Lane RC or EP
+ 1 x PCIe3.0 X2Lane RC
+ 3 x PCIe2.0 X1Lane RC

PCIe3.0 x2Lane	Controller 0 (4L) RC or EP	PCIe3.0 PHY0 Lane0+Lane1
+ PCIe3.0 x1Lane	Controller 1 (2L) RC	PCIe3.0 PHY1 Lane0
+ PCIe2.0 x1Lane	Controller 4 (1L2) RC	PCIe2.0/SATA3.0 Combo PHY0
+ PCIe2.0 x1Lane	Controller 2 (1L0) RC	PCIe2.0/SATA3.0 Combo PHY1
+ PCIe2.0 x1Lane	Controller 3 (1L1) RC	PCIe2.0/SATA3.0/USB3.0 HOST Combo PHY2

eg3: 1 x PCIe3.0 X2Lane RC or EP
+ 1 x PCIe3.0 X1Lane RC
+ 3 x PCIe2.0 X1Lane RC

PCIe3.0 x2Lane	Controller 0 (4L) RC or EP	PCIe3.0 PHY0 Lane0+Lane1
+ PCIe3.0 x1Lane	Controller 1 (2L) RC	PCIe3.0 PHY1 Lane0
+ PCIe2.0 x1Lane	Controller 4 (1L2) RC	PCIe2.0/SATA3.0 Combo PHY0
+ PCIe2.0 x1Lane	Controller 2 (1L0) RC	PCIe2.0/SATA3.0 Combo PHY1
+ PCIe2.0 x1Lane	Controller 3 (1L1) RC	PCIe2.0/SATA3.0/USB3.0 HOST Combo PHY2

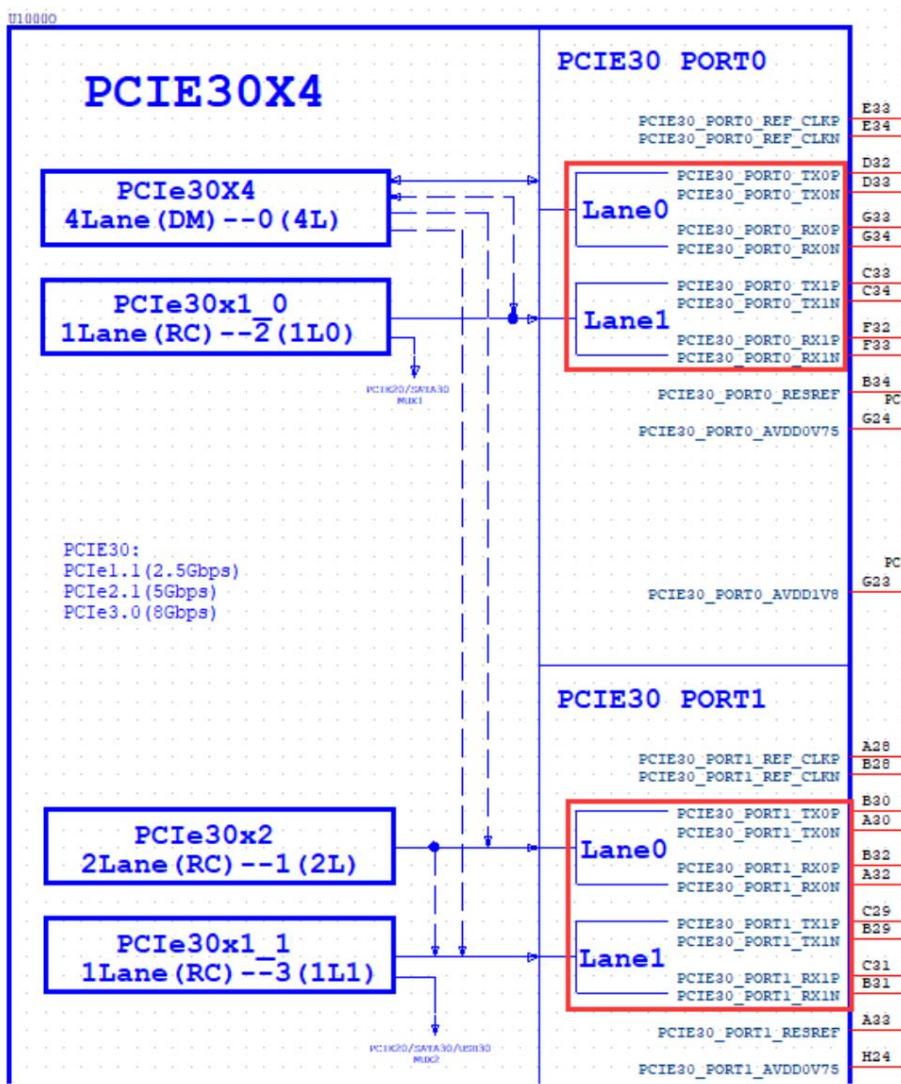
eg4: 4 x PCIe3.0 X1Lane RC
+ 1 x PCIe2.0 X1Lane RC

PCIe3.0 x1Lane	Controller 0 (4L) RC	PCIe3.0 PHY0 Lane0
+ PCIe3.0 x1Lane	Controller 2 (1L0) RC	PCIe3.0 PHY0 Lane1
+ PCIe3.0 x1Lane	Controller 1 (2L) RC	PCIe3.0 PHY1 Lane0
+ PCIe3.0 x1Lane	Controller 3 (1L1) RC	PCIe3.0 PHY1 Lane1
+ PCIe2.0 x1Lane	Controller 4 (1L2) RC	PCIe2.0/SATA3.0 HOST Combo PHY0

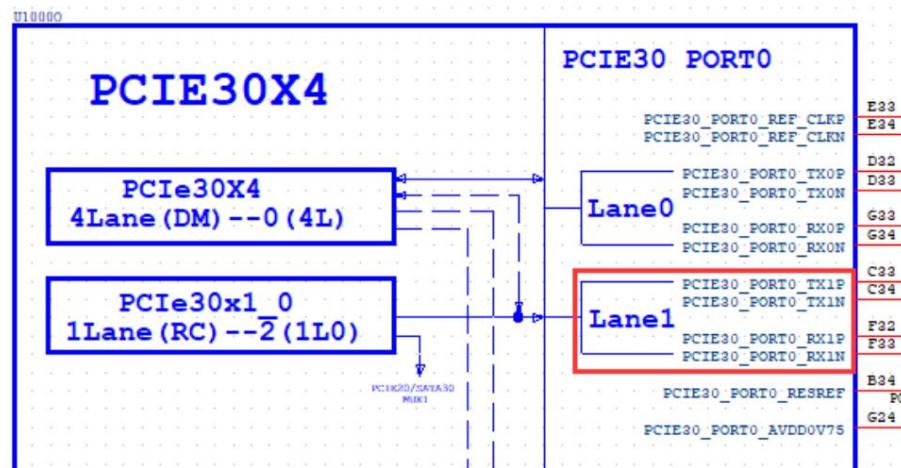
Figure 2-97 RK3588 PCIe multiple mode combinations

The combination of PCIe Controller and PHY is reflected in the schematic module:

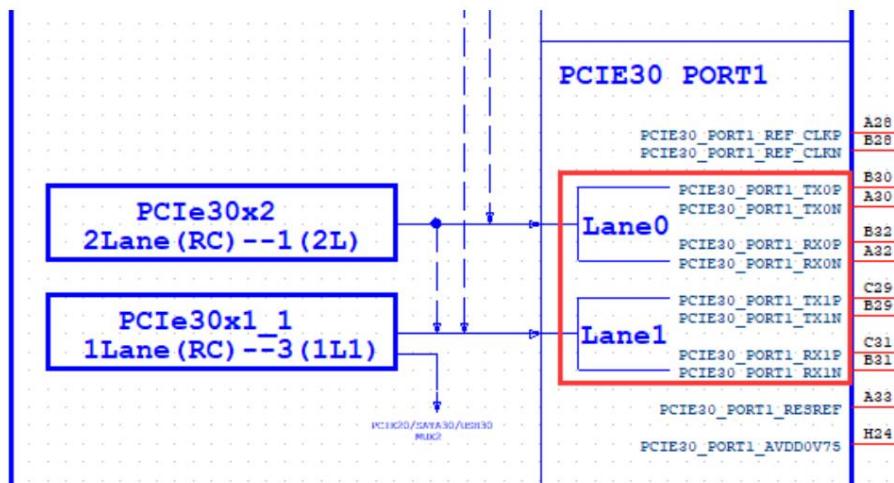
PCIe 3.0 controller Controller 0 (4L) can use PCIe 3.0 PHY0 and PCIe 3.0 PHY1;



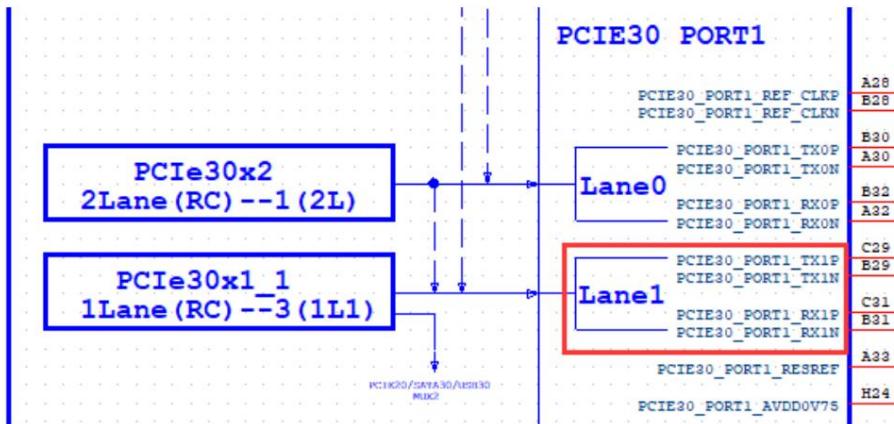
PCIe 3.0 controller 2 (1L0) can use PCIe 3.0 PHY0 Lane 1.



PCIe 3.0 controller 1 (2L) uses PCIe 3.0 PHY1.

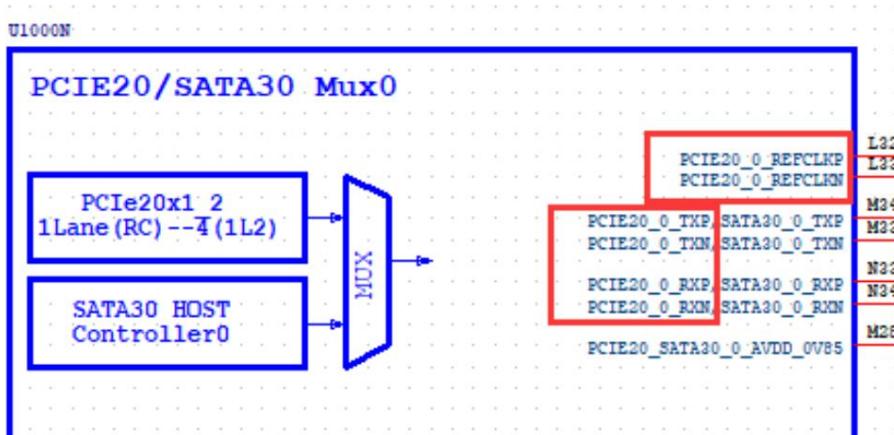


PCIe 3.0 controller 3 (1L1) uses Lane 1 of PCIe 3.0 PHY1.

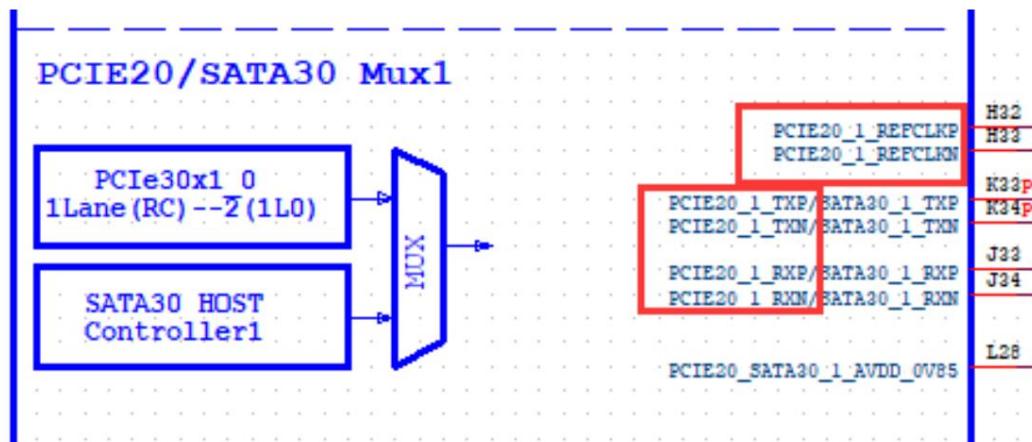


PCIe3.0 controller Controller 4 (1L2) and SATA30 HOST Controller0 controller multiplex PCIe2.0/SATA3.0

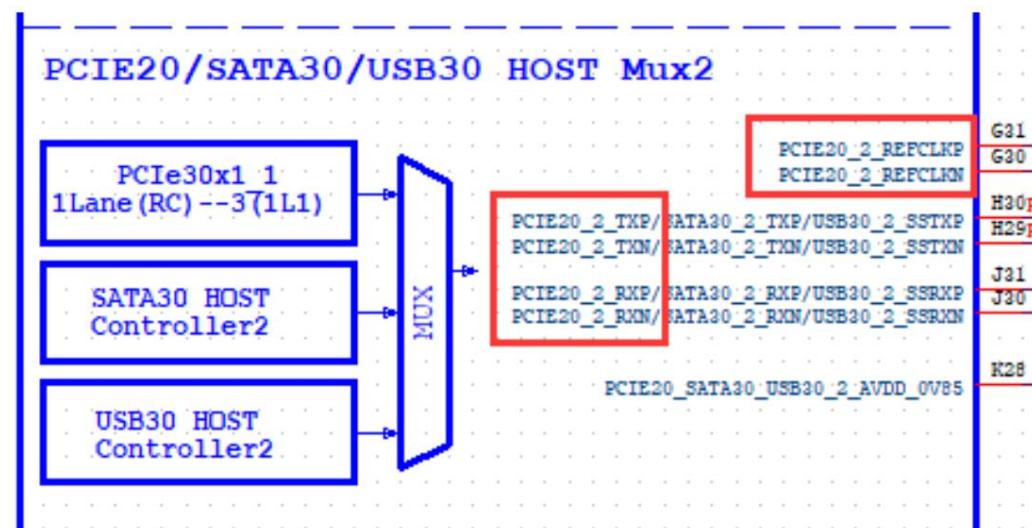
Combo PHY0



þ PCIe3.0 controller Controller 2 (1L0) and SATA30 HOST Controller 1 controller multiplex PCIe2.0/SATA3.0
Combo PHY1



þ PCIe3.0 Controller 3 (1L1), SATA30 HOST Controller2, USB30 OTG Controller2
Use PCIe2.0/SATA3.0/USB3.0 HOST Combo PHY2.



PCIE20_REFCLKP/N can support both output and input. The default output is provided to the EP device.

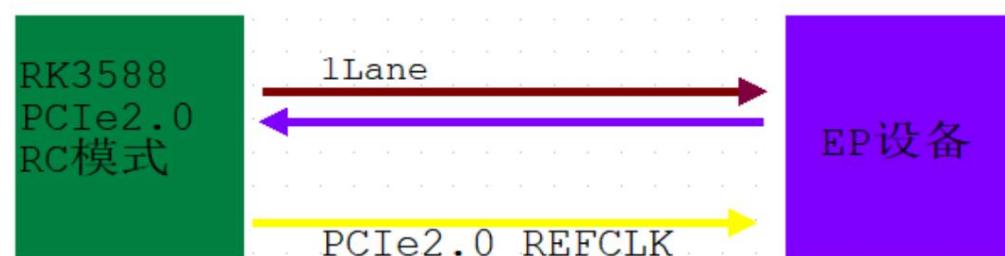


Figure 2-98 RK3588 PCIe2.0 RC mode, reference clock path diagram

Please note the following when designing PCIe 2.0:

- ÿ When designing the slot, the peripheral circuits and power supply must meet the specification requirements;
- ÿ A 100nF AC coupling capacitor is connected in series to the TXP/N differential signal of the PCIe2.0 interface. The AC coupling capacitor is recommended to use a 0201 package.
- Lower ESR and ESL can also reduce impedance changes on the line;
- ÿ PCIE2.0_CLKREQn and PCIE20_WAKEEn must use the function pins and cannot be replaced by GPIO. Special note: When selecting, You must select _M0, _M1 or _M2. You cannot select one _M0 and one _M1.
- ÿ PCIE20_PERSTn can select function pin or use GPIO instead. When selecting function pin, it must be PCIE20_CLKREQn and PCIE20_WAKEEn are in the same group_Mx;
- ÿ Standard PCIe Slot: PCIE20_CLKREQn, PCIE20_WAKEEn, PCIE20_PERSTn are 3.3V level;
- ÿ PCIE20_PRSNT is the Add In Card insertion detection pin, which can use GPIO;
- ÿ When using the PCIE20 function, the reused SATA/USB30 function cannot be used. The corresponding functional modules of SATA/USB30 are described below;
- ÿ PCIe2.0 function module is not used, data lines PCIE20_TXP/TXN, PCIE20_RXP/RXN and reference clock line PCIE20_REFCLKP/REFCLKN can be left floating;

ÿ PCIe2.0 interface matching design recommendations are shown in the following table:

Table 2-18 RK3588 PCIe2.0 interface design

Signal	Connection method	illustrate
PCIE20_0/1/2_TXP/TXN	Connect a 100nF capacitor in series (0201 package recommended) PCIe data output	
PCIE20_0/1/2_RXP/RXN	Direct connection	PCIe data input
PCIE20_0/1/2_REFCLKP/CLKN	Direct connection	PCIe reference clock
PCIE20_CLKREQn	Connect a 0ohm resistor in series	PCIe reference clock request input (RC mode)
PCIE20_WAKEEn	Connect a 0ohm resistor in series	PCIe wake-up input (RC mode)
PCIE20_PERSTn	Connect a 0ohm resistor in series	PCIe global reset output (RC mode)
PCIE20_PRSNT	Connect a 0ohm resistor in series	Add In Card insertion detection input (RC mode)

PCIE30_REF_CLKP/N only supports input:

- ÿ HCSL level clock input is required;
- ÿ Must provide clock requirements that meet PCIe3.0 or higher;
- ÿ RK3588 PCIe3.0 X4Lane RC mode. Compatible with PCIe3.0 X2Lane RC mode and PCIe3.0 X1Lane RC mode.

The reference clock path is shown in the figure below:

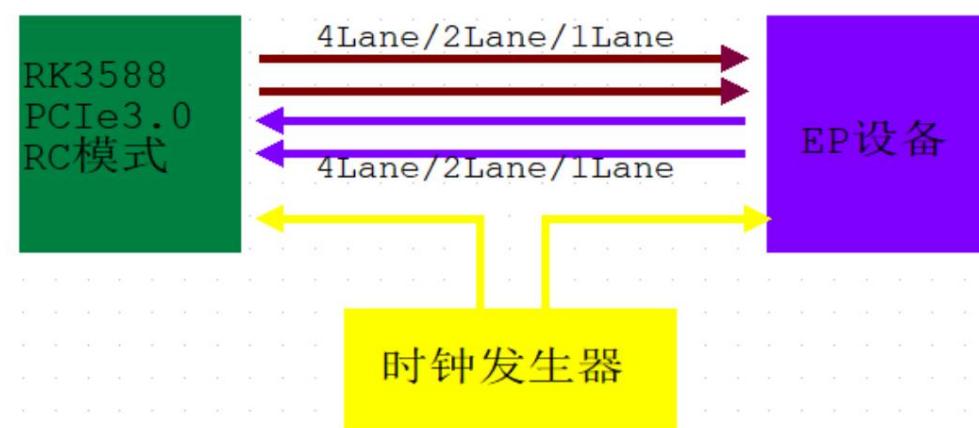


Figure 2-99 RK3588 PCIe3.0 RC mode, reference clock path diagram

ÿ In another case, if two RK3588s are cascaded, it is equivalent to the EP device in the above figure being RK3588. Reference clock path

Consistent, data lane TX connects to RX, RX connects to TX;

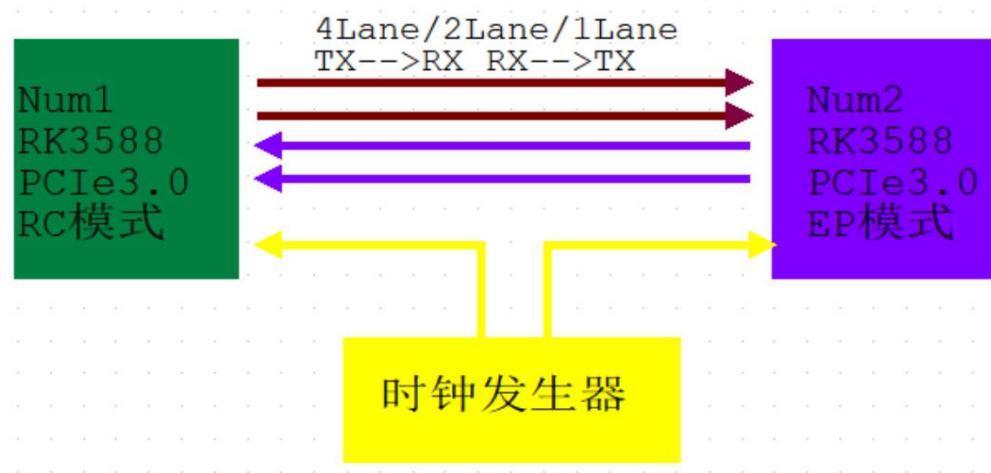


Figure 2-100 RK3588 PCIe 3.0 cascade connection mode, reference clock path diagram

ÿ RK3588 PCIe3.0 x4 Lane EP mode, compatible with PCIe3.0 X2Lane EP mode, and compatible with PCIe3.0 X1Lane EP mode.

The reference clock path is shown in the figure below:

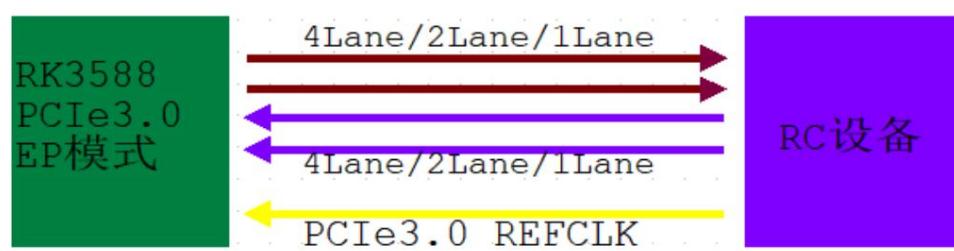


Figure 2-101 RK3588 PCIe3.0 EP mode, reference clock path diagram

Please note the following when

designing PCIe3.0: ÿ When designing the slot, the peripheral circuit and power supply must

meet the Spec requirements; ÿ The 220nF AC coupling capacitor connected in series to the TX0P/N and TX1P/N differential signals of the PCIe3.0 interface is recommended to use

Using 0201 package, lower ESR and ESL, can also reduce the impedance change on the line;

ÿ PCIE_RESREF is the external reference resistor pin of PCIe3.0 PHY. It is connected to a 200ohm resistor with a precision of 1% to ground.

Change the resistor value and place it close to the RK3588 chip pins during layout;

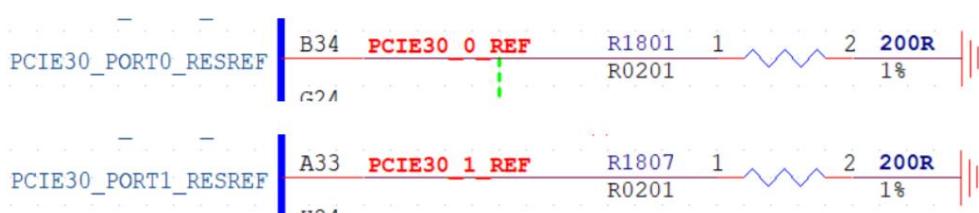


Figure 2-102 PCIe 3.0 PHY RESREF pin

The corresponding relationship between PCIE30_CLKREQn, PCIE30_WAKEn, PCIE30_PERSTn, PCIE30X4_BUTTON_RSTN control signals and controllers is as follows:

PCIe Controller Configure Table

Controller Name	Data & Clk Lane Configure			Control GPIO
	OPTION	CLK LANE	DATA LANE	
PCIE30X4 RC & EP	OPTION1	PCIE30_PORT0_REF_CLKP PCIE30_PORT0_REF_CLKN	PCIE30_PORT0_TX0 PCIE30_PORT0_RX0	PCIE30X4_CLKREQ_M* PCIE30X4_WAKEN_M* PCIE30X4_PERSTN_M* PCIE30X4_BUTTON_RSTN
	OPTION2	PCIE30_PORT0_REF_CLKP PCIE30_PORT0_REF_CLKN	PCIE30_PORT0_TX0 PCIE30_PORT0_RX0 PCIE30_PORT0_TX1 PCIE30_PORT0_RX1	
	OPTION3	PCIE30_PORT0_REF_CLKP PCIE30_PORT0_REF_CLKN PCIE30_PORT1_REF_CLKP PCIE30_PORT1_REF_CLKN	PCIE30_PORT0_TX0 PCIE30_PORT0_RX0 PCIE30_PORT1_TX0 PCIE30_PORT1_RX0 PCIE30_PORT0_RX1 PCIE30_PORT1_RX1	
PCIE30X2 RC	OPTION1	PCIE30_PORT1_REF_CLKP PCIE30_PORT1_REF_CLKN	PCIE30_PORT1_TX0 PCIE30_PORT1_RX0	PCIE30X2_CLKREQ_M* PCIE30X2_WAKEN_M* PCIE30X2_PERSTN_M* PCIE30X2_BUTTON_RSTN
	OPTION2	PCIE30_PORT1_REF_CLKP PCIE30_PORT1_REF_CLKN	PCIE30_PORT1_TX0 PCIE30_PORT1_RX0 PCIE30_PORT1_TX1 PCIE30_PORT1_RX1	
PCIE30X1_0 RC	OPTION1	PCIE30_PORT0_REF_CLKP PCIE30_PORT0_REF_CLKN	PCIE30_PORT0_TX1 PCIE30_PORT0_RX1	PCIE30X1_0_CLKREQ_M* PCIE30X1_0_WAKEN_M* PCIE30X1_0_PERSTN_M* PCIE30X1_0_BUTTON_RSTN
	OPTION2	PCIE20_1_REFCLKP PCIE20_1_REFCLKN	PCIE20_1_TXP PCIE20_1_TXX PCIE20_1_RXP PCIE20_1_RXN	
PCIE30X1_1 RC	OPTION1	PCIE30_PORT1_REF_CLKP PCIE30_PORT1_REF_CLKN	PCIE30_PORT1_TX1 PCIE30_PORT1_RX1	PCIE30X1_1_CLKREQ_M* PCIE30X1_1_WAKEN_M* PCIE30X1_1_PERSTN_M* PCIE30X1_1_BUTTON_RSTN
	OPTION2	PCIE20_2_REFCLKP PCIE20_2_REFCLKN	PCIE20_2_TXP PCIE20_2_TXX PCIE20_2_RXP PCIE20_2_RXN	
PCIE20X1_2 RC	OPTION1	PCIE20_0_REFCLKP PCIE20_0_REFCLKN	PCIE20_0_TXP PCIE20_0_TXX PCIE20_0_RXP PCIE20_0_RXN	PCIE20X1_2_CLKREQ_M* PCIE20X1_2_WAKEN_M* PCIE20X1_2_PERSTN_M* PCIE20X1_2_BUTTON_RSTN

Note:

PCIE30_PORT*_REF_CLKP/N is input gpio

PCIE20_*_REFCLKP/N is output or input gpio

Note:

M*=Mean to M0 or M1, It's the same source, Just multiplex to M0 or M1, So, Only use one at the same time.

Figure 2-103 PCIe Controller and control signal matching relationship

Table 2-19 PCIe control signal multiplexing and corresponding power domain distribution

PCIe control signals	Reuse	Multiplexing power domains
PCIE30X4_CLKREQ_M* PCIE30X4_WAKEN_M* PCIE30X4_PERSTN_M*	M0 M1 M2 M3	M0: PMUIO2 M1: VCCIO6 M2: VCCIO5 M3: VCCIO4
PCIE30X2_CLKREQ_M* PCIE30X2_WAKEN_M* PCIE30X2_PERSTN_M*	M0 M1 M2 M3	M0: PMUIO2 M1: VCCIO6 M2: VCCIO5 M3: VCCIO4
PCIE30X1_0_CLKREQ_M* PCIE30X1_0_WAKEN_M* PCIE30X1_0_PERSTN_M*	M0 M1 M2	M0: PMUIO2 M1: VCCIO6 M2: VCCIO4
PCIE30X1_1_CLKREQ_M* PCIE30X1_1_WAKEN_M* PCIE30X1_1_PERSTN_M*	M0 M1 M2	M0: PMUIO2 M1: VCCIO6 M2: VCCIO4
PCIE20X1_2_CLKREQ_M* PCIE20X1_2_WAKEN_M* PCIE20X1_2_PERSTN_M*	M0, M1	M0: VCCIO5 M1: VCCIO6

Distribution on the schematic:

ŷ There are 4 IOMUXs on the PMUIO2 power domain:

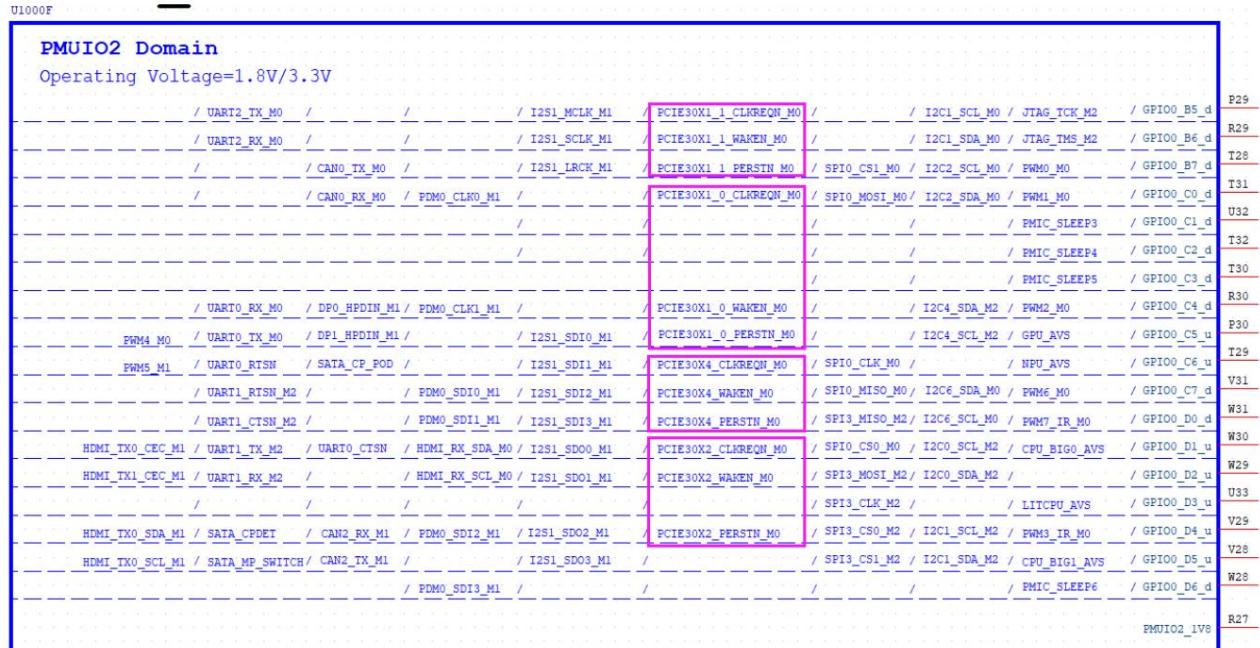


Figure 2-104 PCIE control signal pins on PMUIO2

ŷ There are 5 IOMUXs on the VCCIO6 power domain:

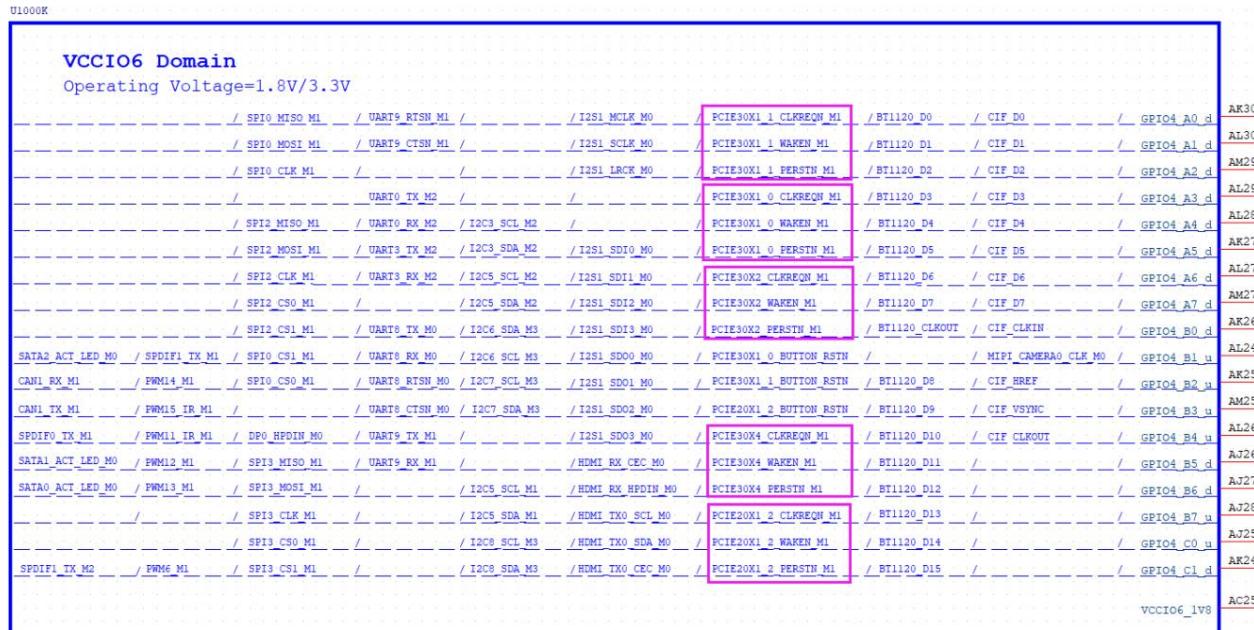


Figure 2-105 PCIE control signal pins on VCCIO6

There are 3 IOMUXs on the VCCIO5 power domain:

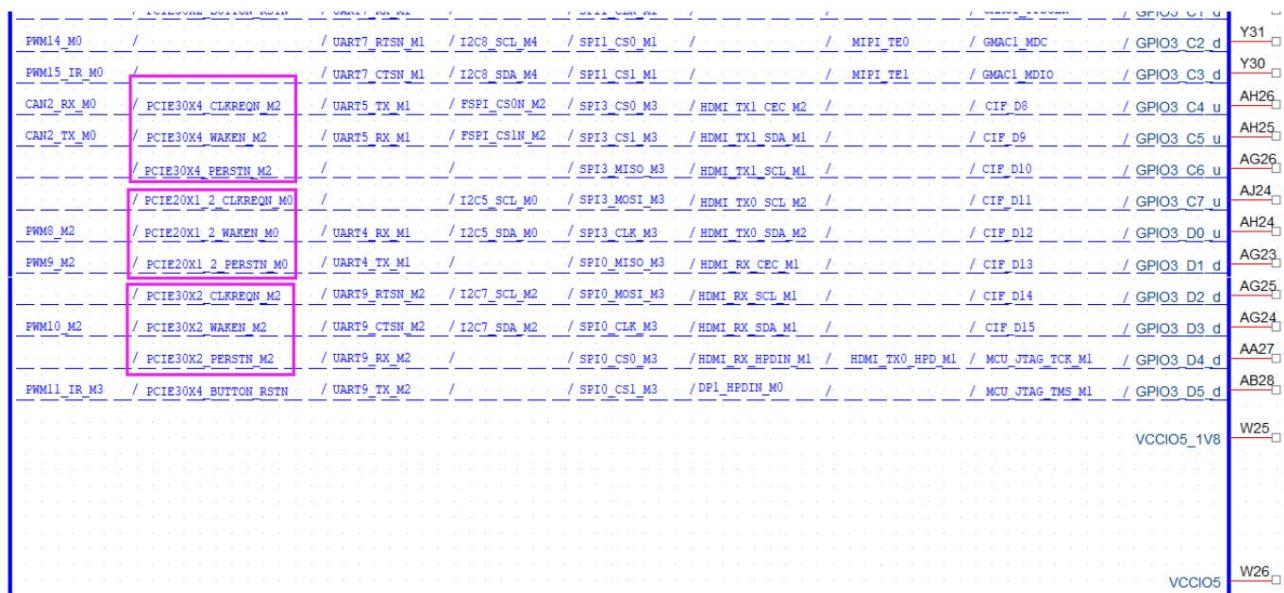


Figure 2-106 PCIE control signal pins on VCCIO5

There are 4 IOMUXs on the VCCIO4 power domain:

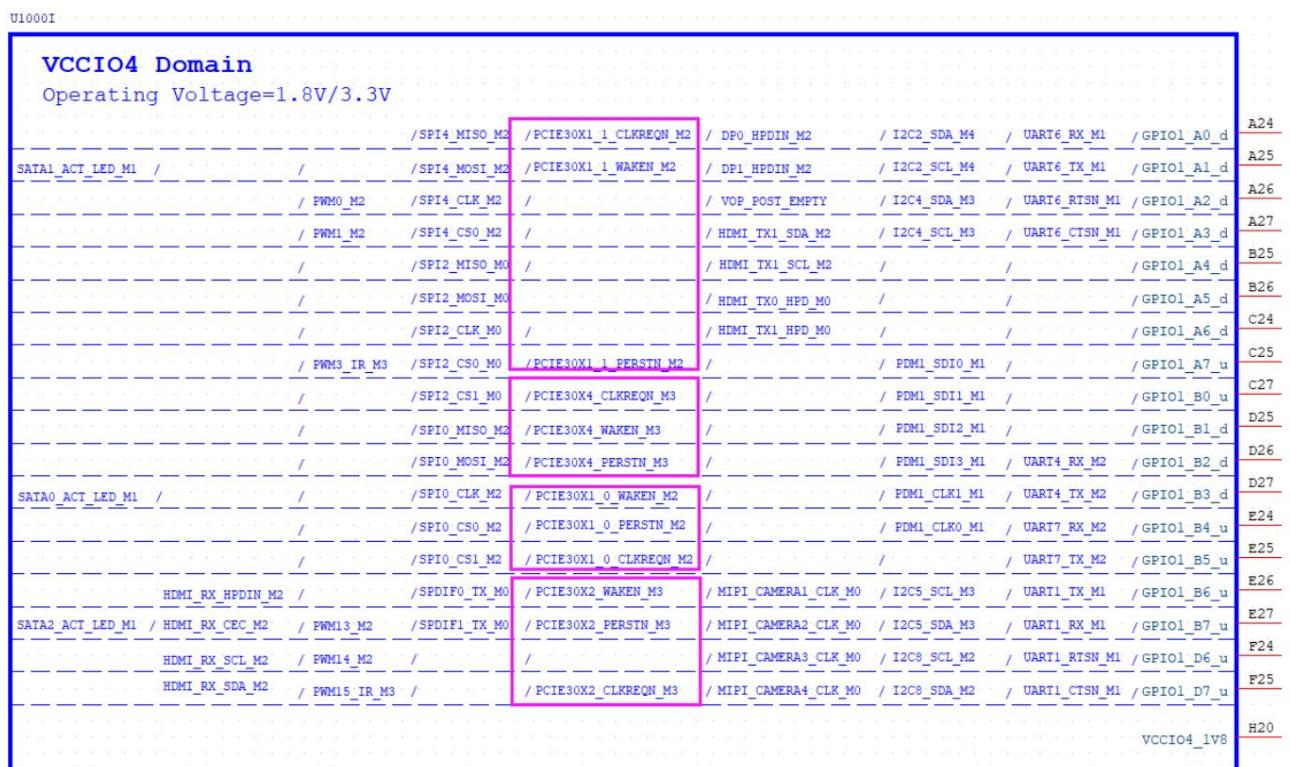


Figure 2-107 PCIE control signal pins on VCCIO4

PCIE30_CLKREQn and PCIE30_WAKEEn must use function pins and cannot be replaced by GPIO. Special note: When selecting,

You must select _M0, _M1 or _M2. You cannot select one _M0 and one _M1.

PCIE30_PERSTn can select function pins or use GPIO instead. When selecting function pins, you must

PCIE30_CLKREQn, PCIE30_WAKEEn same group_Mx;

- ÿ Standard PCIe Slot: PCIE30X2_CLKREQn, PCIE30X1_WAKEEn, PCIE30_PERSTn are 3.3V level;
- ÿ PCIE30_PRSNT is the Add In Card insertion detection pin, which can use GPIO;
- ÿ PCIE30_BUTTON_RSTN is the reset of external hardware and is reserved for future use;
- ÿ 2 RK3588 PCIe cascade connection, data line cross connection, i.e. TX \rightarrow RX, RX \rightarrow TX. Control signal PCIE30_CLKREQn
Connect one to one with PCIE30_PERSTn (for example, Num1 and Num1 represent two RK3588,
Num1_PCIE30_CLKREQn is connected to Num2_PCIE30_CLKREQn and Num1_PCIE30_PERSTn is connected to
Num2_PCIE30_PERSTn). PCIE30_WAKEEn, PCIE30_PRSNT and PCIE30_BUTTON_RSTN
The signal can be left floating;
ÿ The PCIe30 function module is not used, the data lines PCIE30_TXP/TXN and PCIE30_RXP/RXN are suspended, and the reference clock line
PCIE30_REFCLKP/REFCLKN is grounded or left floating;
ÿ PCIe30 PHY and Slot/peripheral REFCLKP/N need to meet the same clock source requirements, such as PHY0/PHY1 in the reference design
The three REFCLKP/N of Slot are output by the same clock generator.

ÿ The PCIe3.0 interface matching design recommendations are shown in the following table:

Table 2-20 RK3588 PCIe3.0 interface design

Signal	Connection method	illustrate
PCIE30_TX0P/TX0N	Connect a 220nF capacitor in series (0201 package recommended)	PCIe data output
PCIE30_RX0P/RX0N	Direct connection	PCIe data input
PCIE30_TX1P/TX1N	Connect a 220nF capacitor in series (0201 package recommended)	PCIe data output
PCIE30_RX1P/RX1N	Direct connection	PCIe data input
PCIE30_REFCLKP_IN/ PCIE30_REFCLKN_IN	Direct connection	PCIe reference clock input
PCIE30_RESREF	200 ohm 1% resistor to ground	External reference resistor for PCIe3.0 PHY
PCIE30_CLKREQn	Connect a 0ohm resistor in series	PCIe reference clock request input (RC mode) PCIe reference clock request output (EP mode)
PCIE30_WAKEEn	Connect a 0ohm resistor in series	PCIe wake-up input (RC mode) PCIe wake-up output (EP mode)
PCIE30_PERSTn	Connect a 0ohm resistor in series	PCIe global reset output (RC mode) PCIe global reset input (EP mode)
PCIE30_PRSNT	Connect a 0ohm resistor in series	Add In Card insertion detection input (RC mode)
PCIE30_BUTTON_RSTN	Connect a 0ohm resistor in series	PCIe external hardware reset output (RC mode) PCIe external hardware reset input (EP mode)

2.3.7 Video Input Interface Circuit

2.3.7.1 MIPI DPHY CSI RX Interface

RK3588 has two MIPI DPHY CSI RXs, both supporting MIPI V1.2, with a maximum data transmission rate of 2.5Gbps per channel.

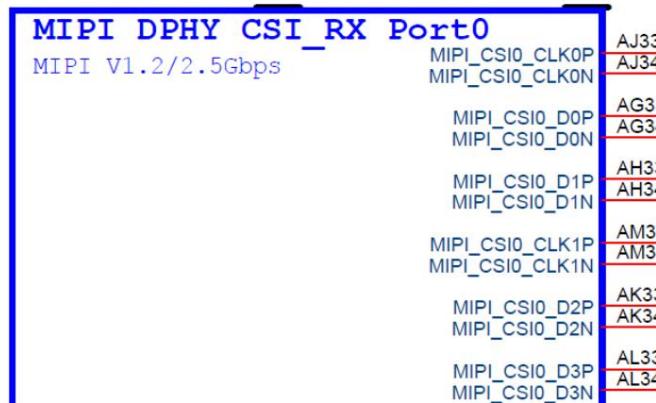


Figure 2-108 RK3588 MIPI DPHY CSI0 RX signal pin

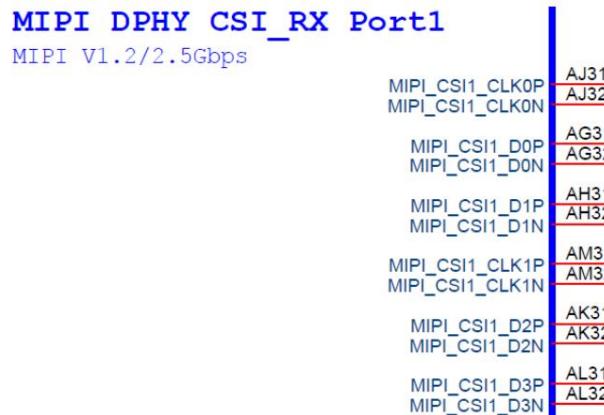


Figure 2-109 RK3588 MIPI DPHY CSI1 RX signal pin

MIPI DPHY CSI0 RX interface mode support:

Support x4Lane mode, MIPI_CSIO_D[3:0] data refers to MIPI_CSIO_CLK0; Support

x2Lane+x2Lane mode:

MIPI_CSIO_D[1:0] data refers to MIPI_CSIO_CLK0. Support

MIPI_CSIO_D[3:2] data refers to MIPI_CSIO_CLK1.

<i>Option1</i>	<i>Sensor1 x4Lane</i>	<i>MIPI_CSII_RX_D0-3</i> <i>MIPI_CSII_RX_CLK0</i>
<i>Option2</i>	<i>Sensor1 x2Lane</i> + <i>Sensor2 x2Lane</i>	<i>MIPI_CSII_RX_D0-1</i> <i>MIPI_CSII_RX_CLK0</i> <i>MIPI_CSII_RX_D2-3</i> <i>MIPI_CSII_RX_CLK1</i>

Figure 2-110 RK3588 MIPI CSI0 operating mode and data and clock distribution

MIPI CSI1 RX interface mode support:
 ÿ Supports x4Lane

mode, MIPI_CSI1_D[3:0] data refers to MIPI_CSI1_CLK0; ÿ Supports x2Lane+x2Lane mode:
 ÿ MIPI1_CSI_D[1:0] data refers
 to MIPI_CSI1_CLK0; ÿ MIPI1_CSI_D[3:2] data refers
 to MIPI_CSI1_CLK1.

<i>Option1</i>	<i>Sensor1 x4Lane</i>	<i>MIPI_CSI_RX_D0-3</i> <i>MIPI_CSI_RX_CLK0</i>
<i>Option2</i>	<i>Sensor1 x2Lane</i> + <i>Sensor2 x2Lane</i>	<i>MIPI_CSI_RX_D0-1</i> <i>MIPI_CSI_RX_CLK0</i> <i>MIPI_CSI_RX_D2-3</i> <i>MIPI_CSI_RX_CLK1</i>

Figure 2-111 RK3588 MIPI CSI1 operating mode and data and clock distribution

Note the following when designing MIPI CSI0/1 RX:

To improve MIPI CSI0/1 RX performance, the decoupling capacitors of each PHY power supply must not be removed and should be placed close to the pins during layout.

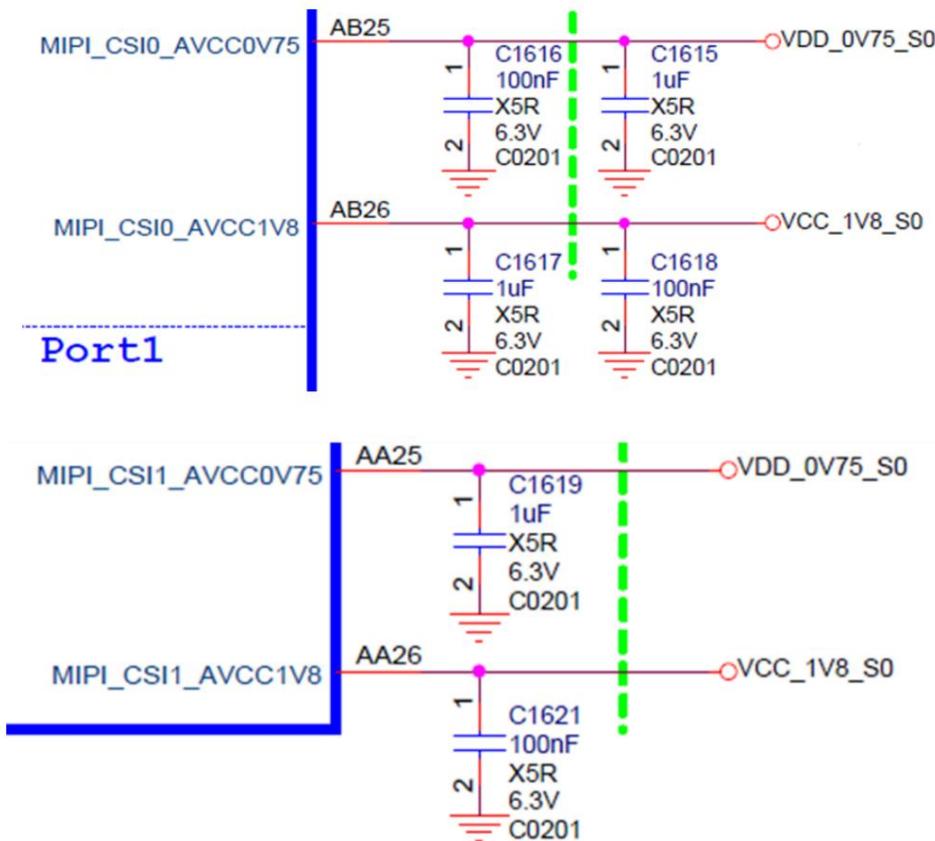


Figure 2-112 MIPI DPHY CSI0/1 RX PHY power decoupling capacitor

The MIPI DPHY CSI0/1 RX interface matching design recommendations are shown in the following table:

Table 2-21 RK3588 MIPI DPHY CSI0/1 RX interface design

Signal	Connection method	illustrate
MIPI_CSIO_D0P/D0N	Direct connection	MIPI CSIO Data Lane 0 Input
MIPI_CSIO_D1P/D1N	Direct connection	MIPI CSIO Data Lane 1 Input
MIPI_CSIO_D2P/D2N	Direct connection	MIPI CSIO Data Lane 2 Input
MIPI_CSIO_D3P/D3N	Direct connection	MIPI CSIO data Lane 3 input
MIPI_CSIO_CLK0P/CLK0N	Direct connection	MIPI CSIO clock 0 input
MIPI_CSIO_CLK1P/CLK1N	Direct connection	MIPI CSIO clock 1 input
MIPI_CS1_D0P/D0N	Direct connection	MIPI CS1 Data Lane 0 Input
MIPI_CS1_D1P/D1N	Direct connection	MIPI CS1 Data Lane 1 Input
MIPI_CS1_D2P/D2N	Direct connection	MIPI CS1 Data Lane 2 Input
MIPI_CS1_D3P/D3N	Direct connection	MIPI CS1 Data Lane 3 Input
MIPI_CS1_CLK0P/CLK0N	Direct connection	MIPI CS1 clock 0 input
MIPI_CS1_CLK1P/CLK1N	Direct connection	MIPI CS1 clock 1 input

2.3.7.2 MIPI_D/CPHY_RX Interface

RK3588 has two MIPI D-PHY/C-PHY CSI RX Combo PHYs

ÿ D-PHY supports version V2.0, D-PHY mode has 0/1/2/3 Lane, and the maximum data transmission rate is 4.5Gbps;

ÿ C-PHY supports V1.1 version. C-PHY mode has 0/1/2 Trio. Each Trio has 3 lines A/B/C. The maximum data transmission rate is

5.7Gbps/Trioÿ2.5Gbpsÿÿ

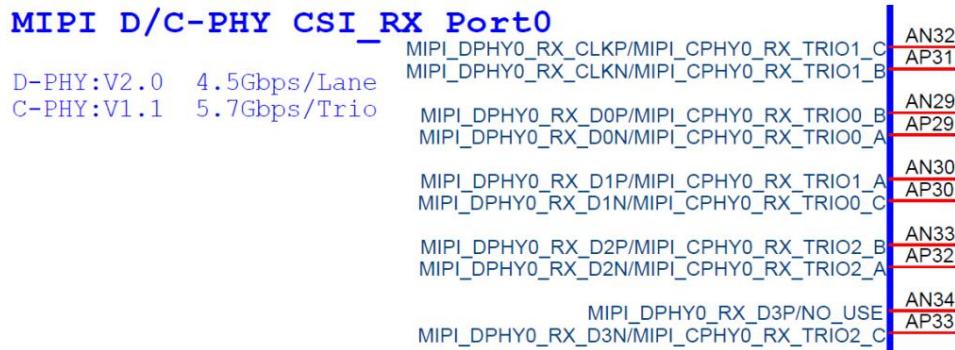


Figure 2-113 RK3588 MIPI D/C-PHY0 RX signal pin

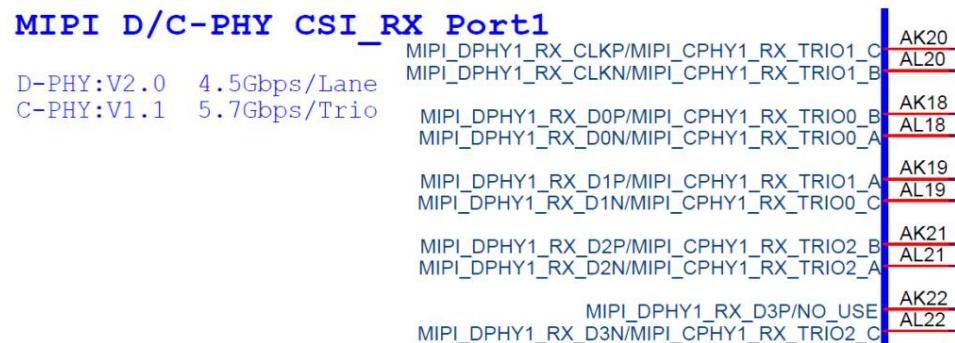


Figure 2-114 RK3588 MIPI D/C-PHY1 RX signal pin

DPHY and CPHY configuration support:

ÿ MIPI D-PHY/C-PHY Combo PHY0 TX and RX can only be configured as DPHY0 TX, DPHY0 RX mode, or as CPHY0 TX, CPHY0 RX mode at the same time. It does not support one configured as DPHY0 TX and the other configured as CPHY0 RX.

CPHY0 RX

ÿ MIPI D-PHY/C-PHY Combo PHY1 TX and RX can only be configured as DPHY1 TX, DPHY1 RX mode at the same time, or configured as CPHY1 TX, CPHY1 RX mode at the same time. It does not support one configured as DPHY1 TX and the other configured as CPHY1 RX

MIPI D/C-PHY0 supports the following modes when working in D-

PHY: ÿ Supports x4Lane mode, MIPI_DPHY0_RX_D[3:0] data refers to MIPI_DPHY0_RX_CLK; ÿ Does not support splitting into x2Lane+x2Lane mode.

MIPI D/C-PHY0 mode support when working in C-PHY: ÿ Support

0/1/2 Trio, each Trio A/B/C 3 lines, MIPI_CPHY0_RX_TRIO[2:0]_A,
MIPI_CPHY0_RX_TRIO[2:0]_B, MIPI_CPHY0_RX_TRIO[2:0]_C

MIPI D/C-PHY1 mode support when working in D-PHY: ÿ

Supports x4Lane mode, MIPI_DPHY1_RX_D[3:0] data refers to MIPI_DPHY1_RX_CLK; ÿ Does not support splitting into x2Lane+x2Lane mode.

MIPI D/C-PHY1 mode support when working in C-PHY: ÿ Support

0/1/2 Trio, each Trio A/B/C 3 lines, MIPI_CPHY1_RX_TRIO[2:0]_A,
MIPI_CPHY1_RX_TRIO[2:0]_B, MIPI_CPHY1_RX_TRIO[2:0]_C

Note the following when designing MIPI D-PHY/C-PHY CSI RX Combo PHY0/1: To

improve the performance of MIPI D-PHY/C-PHY CSI RX Combo PHY0/1, the decoupling capacitors of each PHY power supply must not be removed.

When laying out, please place it close to the pins (note that the MIPI D-PHY/C-PHY CSI RX and MIPI D-PHY/C-PHY DSI TX power supplies are combined into one path);

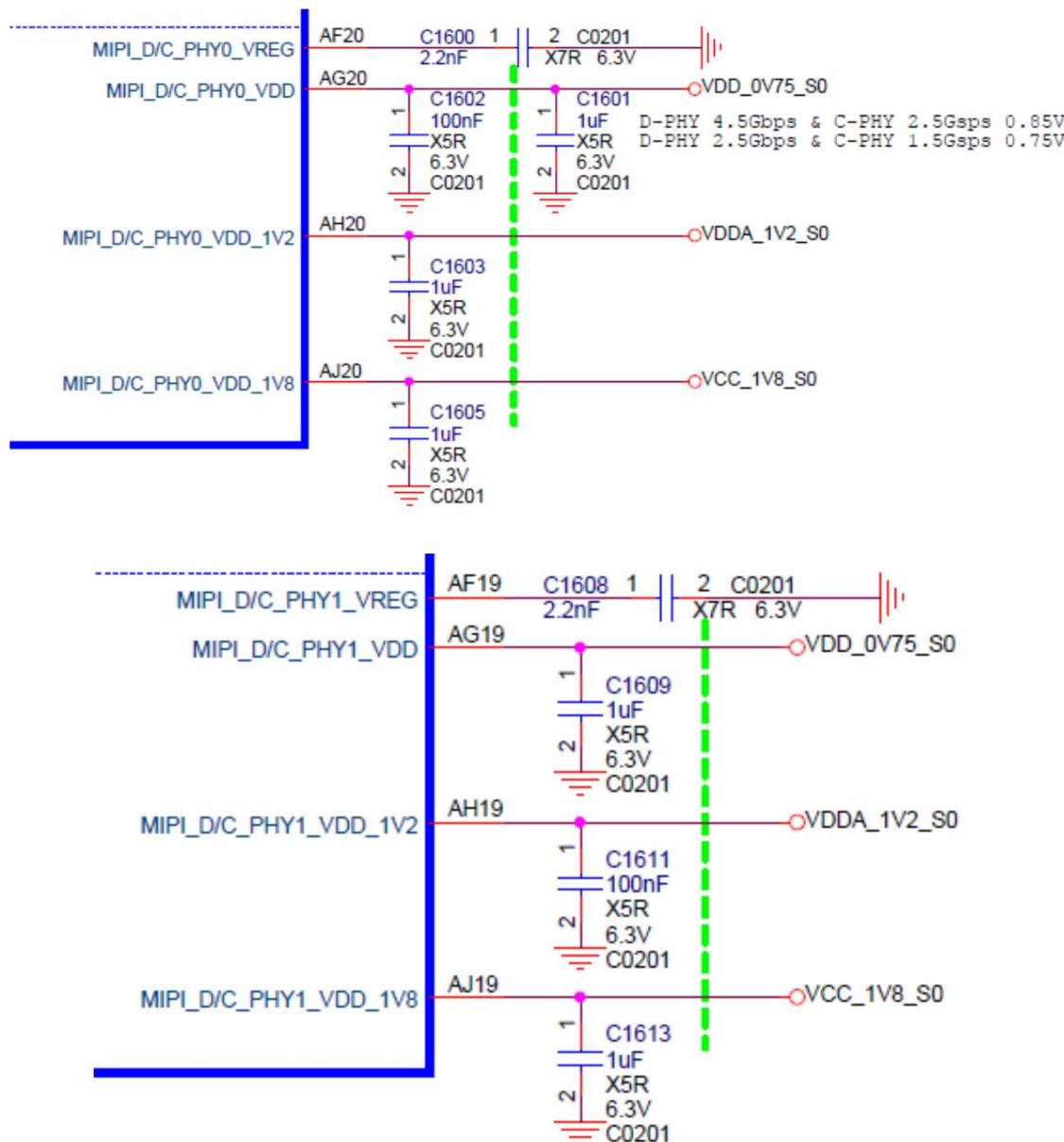


Figure 2-115 MIPI D-PHY/C-PHY CSI RX Combo PHY0/1 power decoupling capacitor

ŷ MIPI_D/C_PHY0_VREG and MIPI_D/C_PHY1_VREG 2.2nF capacitors cannot be deleted and must be placed close to the

Corresponding pin placement;

ŷ MIPI D-PHY/C-PHY Combo PHY0/1 RX matching design recommendations are shown in the following table:

Table 2-22 RK3588 MIPI D-PHY/C-PHY CSI RX Combo PHY0/1 interface design

Signal	Connection method	illustrate
MIPI_DPHY0_RX_D0P/D0N	Direct connection	MIPI_DPHY0_RX Data Lane 0 Input
MIPI_DPHY0_RX_D1P/D1N	Direct connection	MIPI_DPHY0_RX Data Lane 1 Input
MIPI_DPHY0_RX_D2P/D2N	Direct connection	MIPI_DPHY0_RX Data Lane 2 Input
MIPI_DPHY0_RX_D3P/D3N	Direct connection	MIPI_DPHY0_RX Data Lane 3 Input
MIPI_DPHY0_RX_CLKP/CLKN	Direct connection	MIPI_DPHY0_RX clock input
MIPI_CPHY0_RX_TRI0_A/B/C	Direct connection	MIPI_CPHY0_RX_TRI0 input
MIPI_CPHY0_RX_TRI1_A/B/C	Direct connection	MIPI_CPHY0_RX_TRI1 input

Signal	Connection method	illustrate
MIPI_CPHY0_RX_TRI02_A/B/C	Direct connection	MIPI_CPHY0_RX_TRI02 input
MIPI_DPHY1_RX_D0P/D0N	Direct connection	MIPI_DPHY1_RX Data Lane 0 Input
MIPI_DPHY1_RX_D1P/D1N	Direct connection	MIPI_DPHY1_RX Data Lane 1 Input
MIPI_DPHY1_RX_D2P/D2N	Direct connection	MIPI_DPHY1_RX Data Lane 2 Input
MIPI_DPHY1_RX_D3P/D3N	Direct connection	MIPI_DPHY1_RX Data Lane 3 Input
MIPI_DPHY1_RX_CLKP/CLKN	Direct connection	MIPI_DPHY1_RX clock input
MIPI_CPHY1_RX_TRI00_A/B/C	Direct connection	MIPI_CPHY1_RX_TRI00 input
MIPI_CPHY1_RX_TRI01_A/B/C	Direct connection	MIPI_CPHY1_RX_TRI01 input
MIPI_CPHY1_RX_TRI02_A/B/C	Direct connection	MIPI_CPHY1_RX_TRI02 input

2.3.7.3 CIF interface

The CIF interface is distributed on two power domains, namely VCCIO5 and VCCIO6. In actual product design, it is necessary to

The actual IO power supply requirements (1.8V or 3.3V), select the corresponding power supply (the two power domains need to be synchronized), and the I2C pull-up level must be consistent with

Otherwise, the camera may work abnormally or fail to work.

VCCIO6 Domain										
Operating Voltage=1.8V/3.3V										
/ SPI0_MISO_M1	/ UART9_RTSN_M1	/	/ I2S1_MCLK_M0	/ PCIE80X1_1_CLKREQN_M1	/ BT1120_D0	CIF_D0	/ GPIO4_A0_d	AK30		
/ SPI0_MOSI_M1	/ UART9_CTSN_M1	/	/ I2S1_SCLK_RX_M0	/ PCIE80X1_1_WAKEN_M1	/ BT1120_DL	CIF_D1	/ GPIO4_A1_d	AL30		
/ SPI0_CLK_M1	/	/	/ I2S1_LRCK_RX_M0	/ PCIE80X1_0_PERSTN_M1	/ BT1120_DS	CIF_D2	/ GPIO4_A2_d	AM29		
/	UART0_RX_M2	/	/ I2S1_SCLK_RX_M0	/ PCIE80X1_0_WAKEN_M1	/ BT1120_D3	CIF_D3	/ GPIO4_A3_d	AL29		
/ SPI1_MISO_M1	/ UART0_RX_M2	/ I2C3_SDA_M2	/ I2S1_LRCK_RX_M0	/ PCIE80X1_0_WAKEN_M1	/ BT1120_D4	CIF_D4	/ GPIO4_A4_d	AL28		
/ SPI1_MOSI_M1	/ UART3_RX_M2	/ I2C3_SDA_M2	/ I2S1_SD0_M0	/ PCIE80X1_0_PERSTN_M1	/ BT1120_DS	CIF_D5	/ GPIO4_A5_d	AK27		
/ SPI1_CLK_M1	/ UART3_RX_M2	/ I2C5_SCL_M2	/ I2S1_SD1_M0	/ PCIE80X2_CLKREQN_M1	/ BT1120_DL	CIF_D6	/ GPIO4_A6_d	AL27		
/ SPI1_CSO_M1	/	/ I2C5_SDA_M2	/ I2S1_SD2_M0	/ PCIE80X2_WAKEN_M1	/ BT1120_D7	CIF_D7	/ GPIO4_A7_d	AM27		
/ SPI1_CS1_M1	/ UART8_RX_M0	/ I2C6_SDA_M3	/ I2S1_SD3_M0	/ PCIE80X2_PERSTN_M1	/ BT1120_CLKOUT	CIF_CLKIN	/ GPIO4_B0_d	AK26		
SATA0_ACT_LED_M0	/ SPDIF1_TX_M1	/ SPI0_CS1_M1	/ UART8_RX_M0	/ I2C6_SCL_M3	/ I2S1_SD0_M0	/ PCIE80X1_0_BUTTON_RSTN_M0	/ MIPI_CAMERA0_CLK_M0	GPIO4_B1_u	AL24	
PWM14_M1	/ PWM14_CS0_M1	/ UART8_RTSN_M0	/ I2C7_SDA_M3	/ I2S1_SD0_M0	/ PCIE80X1_1_BUTTON_RSTN_M0	CIF_HREF	/ GPIO4_B2_u	AK25		
CAN0_RX_M1	/ PWM15_IR_M1	/	/ UART8_CTSN_M0	/ I2C7_SDA_M3	/ I2S1_SD0_M0	/ PCIE80X1_2_BUTTON_RSTN_M0	/ BT1120_D9	CIF_VSYNC	AM25	
SPDIF0_RX_M1	/ PWM11_IR_M1	/ DPO_HPDIN_M0	/ UART8_RX_M1	/	/ I2S1_SD0_M0	/ PCIE80X4_CLKREQN_M1	/ BT1120_D10	CIF_CLKOUT	/ GPIO4_B4_u	
SATA0_ACT_LED_M0	/ PWM11_M1	/ SPI3_MISO_M1	/ UART9_RX_M1	/	/ I2C5_SCL_M1	/ HDMI_RX_CEC_M0	/ PCIE80X4_WAKEN_M1	/ BT1120_D11	/ GPIO4_B5_d	
SATA0_ACT_LED_M0	/ PWM13_M1	/ SPI3_MOSI_M1	/	/ I2C5_SDA_M1	/ HDMI_RX_HPDIN_M0	/ PCIE80X4_PERSTN_M1	/ BT1120_D12	/ GPIO4_B6_d	AJ27	
/	/ SPI3_CLK_M1	/	/ I2C6_SDA_M1	/ HDMI_RX_SCL_M0	/ PCIE80X1_2_CLKREQN_M1	/ BT1120_D13	/	GPIO4_B7_u	AJ28	
/	/ SPI3_CSO_M1	/	/ I2C8_SCL_M3	/ HDMI_RX_SDA_M0	/ PCIE80X1_2_WAKEN_M1	/ BT1120_D14	/	GPIO4_C0_u	AJ25	
SPDIF1_RX_M2	/ PWM6_M1	/ SPI3_CS1_M1	/	/ I2C8_SDA_M3	/ HDMI_RX_CEC_M0	/ PCIE80X1_2_PERSTN_M1	/ BT1120_D15	/	GPIO4_C1_d	AK24

VCCIO5 Domain										
Operating Voltage=1.8V/3.3V										
PWM10_M0	/ SPI4_MISO_M1	/	/ I2C6_SDA_M4	/ FSPI_D0_M2	/ I2S3_MCLK	/ SDIO_D0_M1	/ GMAC1_TXD2	/ GPIO3_A0_u	AA29	
AUDDSM_LN	/ SPI4_MOSI_M1	/ PWM11_IR_M0	/ I2C6_SCL_M4	/ FSPI_D1_M2	/ I2S3_SCLK	/ SDIO_D1_M1	/ GMAC1_TXD3	/ GPIO3_A1_u	AA30	
AUDDSM_LP	/ SPI4_CLK_M1	/ UART8_RX_M1	/	/ FSPI_D2_M2	/ I2S3_LRCK	/ SDIO_D2_M1	/ GMAC1_RXD2	/ GPIO3_A2_u	AD27	
AUDDSM_RN	/ SPI4_CS0_M1	/ UART8_RX_M1	/	/ FSPI_D3_M2	/ I2S3_SDO	/ SDIO_D3_M1	/ GMAC1_RXD3	/ GPIO3_A3_u	AE27	
AUDDSM_RP	/ SPI4_CS1_M1	/ UART8_RTSN_M1	/	/	/ I2S3_SDI	/ SDIO_CMD_M1	/ GMAC1_RXCLK	/ GPIO3_A4_d	AD28	
/ MIPI_CAMERA0_CLK_M1	/ UART8_CTSN_M1	/ I2C4_SDA_M0	/ FSPI_CLK_M2	/	/	/ SDIO_CLK_M1	/ GMAC1_RXCLK	/ GPIO3_A5_d	AH30	
/ MIPI_CAMERA1_CLK_M1	/	/ I2C4_SCL_M0	/	/	/	/	/ ETH1_REFCLKO_CSM	/ GPIO3_A6_d	AH27	
PWM8_M0	/ MIPI_CAMERA2_CLK_M1	/	/	/	/	/	/ GMAC1_RXDO	/ GPIO3_A7_u	AG29	
PWM9_M0	/ MIPI_CAMERA3_CLK_M1	/	/	/	/ I2S2_SCLK_RX_M1	/	/ GMAC1_RXD1	/ GPIO3_B0_u	AG28	
PWM2_M1	/ MIPI_CAMERA4_CLK_M1	/ UART2_RX_M2	/	/	/ I2S2_LRCK_RX_M1	/	/ GMAC1_RXDV_CRS	/ GPIO3_B1_d	AH29	
PWM3_IR_M1	/	/ UART3_RX_M2	/	/	/ I2S2_SDI_M1	/	/ GMAC1_TXER	/ GPIO3_B2_d	AE28	
/	/ UART3_RTSN	/	/	/	/ I2S2_SDO_M1	/	/ GMAC1_TXDO	/ GPIO3_B3_u	AC28	
/	/ UART3_CTSN	/	/	/	/ I2S2_MCLK_M1	/	/ GMAC1_TXD1	/ GPIO3_B4_u	AC29	
PWM12_M0	/ CAN1_RX_M0	/ UART3_RX_M1	/	/	/ I2S2_SCLK_TX_M1	/	/ GMAC1_TWEN	/ GPIO3_B5_u	AD29	
PWM13_M0	/ CAN1_RX_M0	/ UART3_RX_M1	/	/	/ I2S2_LRCK_TX_M1	/	/ GMAC1_MCLKINOUT	/ GPIO3_B6_d	AE29	
/	/	/ I2C3_SCL_M1	/ SPI1_MOSI_M1	/ HDMI_TX1_HPD_M1	/	/ GMAC1_PTP_REF_CLK	/ GPIO3_B7_d	AA28		
/	/	/ UART7_RX_M1	/ I2C3_SDA_M1	/ SPI1_MISO_M1	/	/ GMAC1_PPSTRIG	/ GPIO3_C0_d	Y29		
/ PCIE80X2_BUTTON_RSTN	/ UART7_RX_M1	/	/ SPI1_CLK_M1	/	/	/ GMAC1_PPCLK	/ GPIO3_C1_d	Y27		
PWM14_M0	/	/ UART7_RTSN_M1	/ I2C8_SCL_M4	/ SPI1_CS0_M1	/	/ MIPI_TE0	/ GMAC1_MDC	/ GPIO3_C2_d	Y31	
PWM15_IR_M0	/	/ UART7_CTSN_M1	/ I2C8_SDA_M4	/ SPI1_CS1_M1	/	/ MIPI_TE1	/ GMAC1_MDIO	/ GPIO3_C3_d	Y30	
CAN2_RX_M0	/ PCIE80X4_CLKREQN_M2	/ UART5_RX_M1	/ FSPI_CS0_M2	/ SPI3_CS0_M3	/ HDMI_RX1_CEC_M2	/	CIF_D8	/ GPIO3_C4_u	AH26	
CAN2_RX_M0	/ PCIE80X4_WAKEN_M2	/ UART5_RX_M1	/ FSPI_CS1_M2	/ SPI3_CS1_M3	/ HDMI_RX1_SDA_M1	/	CIF_D9	/ GPIO3_C5_u	AH25	
/ PCIE80X4_PERSTN_M2	/	/	/ SPI3_MISO_M3	/ HDMI_RX1_SCL_M1	/	/ CIF_D10	/ GPIO3_C6_u	AJ24		
/ PCIE80X4_CLKREQN_M0	/	/ I2C5_SCL_M0	/ SPI3_MOSI_M3	/ HDMI_RX2_SCL_M2	/	/ CIF_D11	/ GPIO3_C7_u	AH24		
PWM8_M2	/ PCIE80X1_2_WAKEN_M0	/ UART4_RX_M1	/ I2C5_SDA_M0	/ SPI3_CLK_M3	/ HDMI_RX2_SDA_M2	/	CIF_D12	/ GPIO3_D0_u	AG23	
PWM9_M2	/ PCIE80X1_2_PERSTN_M0	/ UART4_RX_M1	/	/ SPI0_MISO_M3	/ HDMI_RX_CEC_M1	/	CIF_D13	/ GPIO3_D1_d	AG25	
/ PCIE80X2_CLKREQN_M2	/ UART9_RTSN_M2	/ I2C7_SCL_M2	/ SPI0_MOSI_M3	/ HDMI_RX_SCL_M1	/	CIF_D14	/ GPIO3_D2_d	AG24		
PWM10_M2	/ PCIE80X2_WAKEN_M2	/ UART9_CTSN_M2	/ I2C7_SDA_M2	/ SPI0_CLK_M3	/ HDMI_RX_SDA_M1	/	CIF_D15	/ GPIO3_D3_d	AA27	
/ PCIE80X2_PERSTN_M2	/ UART9_RX_M2	/	/ SPI0_CS0_M3	/ HDMI_RX_HPD_M1 / HDMI_RX_HPD_M1 / MCU_JTAG_TCK_M1	/	/	/ MCU_JTAG_TMS_M1	/ GPIO3_D4_d	AB28	
PWM11_IR_M3	/ PCIE80X4_BUTTON_RSTN	/ UART9_RX_M2	/	/ SPI0_CS1_M3	/ DPL_HPDIN_M0	/	/	/ MCU_JTAG_TMS_M1	/ GPIO3_D5_d	AB28

Figure 2-116 RK3588 CIF function pin

The CIF interface supports the following formats:

- ÿ Support BT601 YCbCr 422 8-bit input;
- ÿ Support BT656 YCbCr 422 8-bit input;
- ÿ Support RAW 8/10/12-bit input;
- ÿ BT1120 YCbCr 422 8/16bit input; single/dual-edge sampling
- ÿ Support 2/4 mixed BT656/BT1120 YCbCr 422 8/16bit input;
- ÿ Support YUYV sequential configuration.

The corresponding relationship of 8/10/12/16-bit data of CIF[15:0] is shown in the following table, using high-bit alignment.

Mode	16bit	12bit	10bit	8bit
<i>CIF_D0</i>	<i>D0</i>	--	--	--
<i>CIF_D1</i>	<i>D1</i>	--	--	--
<i>CIF_D2</i>	<i>D2</i>	--	--	--
<i>CIF_D3</i>	<i>D3</i>	--	--	--
<i>CIF_D4</i>	<i>D4</i>	<i>D0</i>	--	--
<i>CIF_D5</i>	<i>D5</i>	<i>D1</i>	--	--
<i>CIF_D6</i>	<i>D6</i>	<i>D2</i>	<i>D0</i>	--
<i>CIF_D7</i>	<i>D7</i>	<i>D3</i>	<i>D1</i>	--
<i>CIF_D8</i>	<i>D8</i>	<i>D4</i>	<i>D2</i>	<i>D0</i>
<i>CIF_D9</i>	<i>D9</i>	<i>D5</i>	<i>D3</i>	<i>D1</i>
<i>CIF_D10</i>	<i>D10</i>	<i>D6</i>	<i>D4</i>	<i>D2</i>
<i>CIF_D11</i>	<i>D11</i>	<i>D7</i>	<i>D5</i>	<i>D3</i>
<i>CIF_D12</i>	<i>D12</i>	<i>D8</i>	<i>D6</i>	<i>D4</i>
<i>CIF_D13</i>	<i>D13</i>	<i>D9</i>	<i>D7</i>	<i>D5</i>
<i>CIF_D14</i>	<i>D14</i>	<i>D10</i>	<i>D8</i>	<i>D6</i>
<i>CIF_D15</i>	<i>D15</i>	<i>D11</i>	<i>D9</i>	<i>D7</i>

Figure 2-117 RK3588 CIF data correspondence

BT1120 16bit mode data correspondence, supports YC Swap.

Table 2-23 RK3588 BT1120 16-bit mode data correspondence table

Pin Name	Default Mode		Swap Open	
	Pixel #0	Pixel #1	Pixel #0	Pixel #1
CIF_D0	Y0[0]	Y1[0]	Cb0[0]	Cr0[0]
CIF_D1	Y0[1]	Y1[1]	Cb0[1]	Cr0[1]
CIF_D2	Y0[2]	Y1[2]	Cb0[2]	Cr0[2]
CIF_D3	Y0[3]	Y1[3]	Cb0[3]	Cr0[3]
CIF_D4	Y0[4]	Y1[4]	Cb0[4]	Cr0[4]
CIF_D5	Y0[5]	Y1[5]	Cb0[5]	Cr0[5]
CIF_D6	Y0[6]	Y1[6]	Cb0[6]	Cr0[6]
CIF_D7	Y0[7]	Y1[7]	Cb0[7]	Cr0[7]
CIF_D8	Cb0[0]	Cr0[0]	Y0[0]	Y1[0]
CIF_D9	Cb0[1]	Cr0[1]	Y0[1]	Y1[1]
CIF_D10	Cb0[2]	Cr0[2]	Y0[2]	Y1[2]
CIF_D11	Cb0[3]	Cr0[3]	Y0[3]	Y1[3]
CIF_D12	Cb0[4]	Cr0[4]	Y0[4]	Y1[4]
CIF_D13	Cb0[5]	Cr0[5]	Y0[5]	Y1[5]
CIF_D14	Cb0[6]	Cr0[6]	Y0[6]	Y1[6]
CIF_D15	Cb0[7]	Cr0[7]	Y0[7]	Y1[7]

The pull-up and matching design recommendations for the CIF interface are shown in the table below:

Table 2-24 RK3588 CIF interface design

Signal	Internal pull-up and pull-down	Connection method	Description (chip side)
CIF_D[15~0]	drop down	Direct connection, it is recommended to reserve a series resistor CIF data input close to the device end	
CIF_HREF	drop down	Direct connection, it is recommended to reserve a series resistor CIF near the device end.	
CIF_VSYNC	drop down	Direct connection, it is recommended to reserve a series resistor CIF close to the device end Field synchronization input	
CIF_CLKIN	drop down	Connect a 22ohm resistor in series, close to the device end	CIF clock input
CIF_CLKOUT	drop down	Connect a 22ohm resistor in series, close to the chip end	CIF clock output, which can be provided to the device when MCLK working clock

When using a connector to connect a board to a board, it is recommended to connect a resistor with a certain resistance (between 22ohm and 100ohm, depending on the specific resistance).

Test is subject to the requirements) and TVS devices should be reserved.

Notes on MIPI CSI RX/CIF design:

ŷ The DVDD power supply of the camera has different voltages such as 1.2V/1.5V/1.8V. Please provide the correct power supply according to the camera's specifications.

The reference circuit defaults to 1.2V;

ŷ The DVDD current of some cameras is relatively large, exceeding 100mA. It is recommended to use DCDC power supply;

ŷ The power supply of the camera has power-on sequence requirements. Please adjust the power-on sequence according to the camera specification. The default power-on sequence is as shown in the figure.

The power sequence is: 1.8V->1.2V->2.8V;

ŷ When using a camera with a CIF interface, pay attention to the power supply of the camera's DOVDD (IO power) and VCCIO5 and VCCIO6.

The same voltage must be used;

When using two cameras, the power supplies can be separated or combined according to the actual needs. The reference diagram defaults to separation. If the camera has AF function, VCC2V8_AF needs to be powered separately; or if it is shared with AVCC2V8_DVP, a magnetic

Bead isolation;

The decoupling capacitors of all camera power supplies must not be removed and must be retained and placed close to the socket;

The PWDN signal of the Camera must be controlled by GPIO, and the GPIO level must match the Camera IO level; The Reset signal of the Camera is recommended to be controlled by GPIO, and the GPIO level must match the Camera IO level.

The 100nF capacitor must not be removed and should be placed close to the socket to enhance anti-static capability;

Camera's MCLK can be obtained from:

- 1) CIF_CLKOUT
- 2) MIPI_CAMERA0_CLK
- 3) MIPI_CAMERA1_CLK
- 4) MIPI_CAMERA2_CLK
- 5) MIPI_CAMERA3_CLK
- 6) MIPI_CAMERA4_CLK Note: The clock

level must match the Camera IO level. If not, level conversion or resistor voltage division is required to make the levels match.

If the two cameras are of the same model, please pay attention to whether the I2C addresses are the same. If the addresses are the same, then two I2C buses are required.

2.3.7.4 HDMI 2.0 RX Interface

The RK3588 chip supports HDMI2.0 RX and is backward compatible with HDMI1.4b; it supports RGB/YUV444/YUV422/YUV420 formats;

It supports up to 4K@60Hz input.

The HDMI RX TMDS signal is shown in the figure below. A 2.2ohm resistor must be reserved near the HDMI RX connector and must not be removed to enhance the anti-static surge capability.

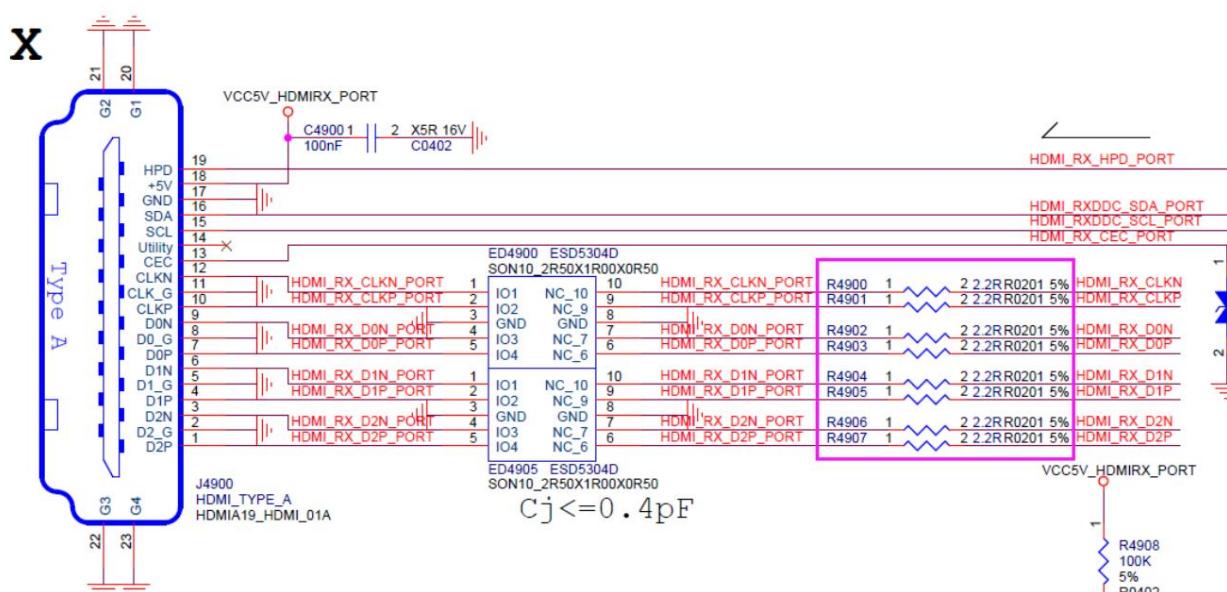


Figure 2-118 RK3588 HDMI RX PHY pins

1uF and 100nF decoupling capacitors must be placed on the HDMI RX PHY power pin and must not be deleted. When laying out, place it close to the RK3588 pin.

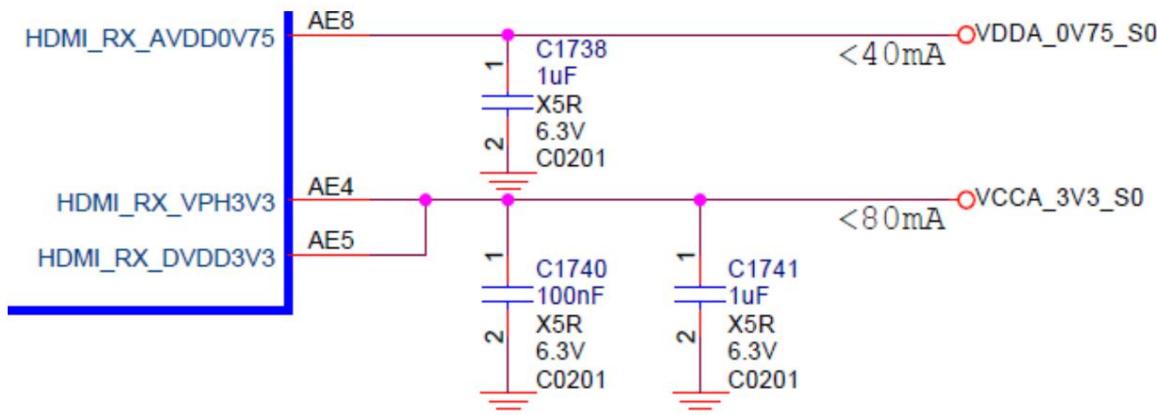


Figure 2-119 RK3588 HDMI RX PHY power decoupling capacitor

HDMI RX REXT is the external reference resistor pin of HDMI RX PHY. It is connected to a 200ohm resistor with a precision of 1% to ground.

Change the resistor value and place it close to the RK3588 chip pins during layout.



Figure 2-120 RK3588 HDMI RX REXT pins

HDMI_RX_HPDOUT is the function of the HDMI RX controller multiplexed to the ordinary GPIO, and the level depends on the power domain voltage;

HDMI_RX_HPDOUT is multiplexed in three different power domains, one on the IO of VCCIO6 power domain, and one on

One is on the IO of the VCCIO5 power domain, and the other is on the IO of the VCCIO4 power domain.

VCCIO6 Domain	
Operating Voltage=1.8V/3.3V	
/ SPI0_MISO_M1 /	/ UART5_PTSN_M1 /
/ SPI0_MOSI_M1 /	/ UART5_CTSN_M1 /
/ SPI0_CLK_M1 /	/ I2S1_SCLK_M0 /
/	/ I2S1_LRCK_M0 /
/ UART0_TX_M2 /	/ I2S1_LRCK_M0 /
/ SPI1_MISO_M1 /	/ UART0_RX_M2 /
/ SPI1_MOSI_M1 /	/ I2C3_SDA_M2 /
/ SPI1_CLK_M1 /	/ I2S3_SD1_M0 /
/ SPI2_MISO_M1 /	/ UART3_TX_M2 /
/ SPI2_MOSI_M1 /	/ I2C3_SDA_M2 /
/ SPI2_CLK_M1 /	/ I2S3_SD1_M0 /
/ SPI2_C80_M1 /	/ I2C5_SDA_M2 /
/ SPI2_C81_M1 /	/ UART3_RX_M0 /
SATA2_ACT_LED_M0 /	/ SPI0_C81_M1 /
CAN1_RX_M1 /	/ UART0_RX_M0 /
CAN1_TX_M1 /	/ PWM15_IR_M1 /
SPDIF0_RX_M1 /	/ PWM11_IR_M1 /
SATA0_ACT_LED_M0 /	/ SPI3_MISO_M1 /
SATA0_ACT_LED_M0 /	/ SPI3_MOSI_M1 /
/	/ SPI3_CLK_M1 /
SPDIF1_RX_M2 /	/ SPI3_C80_M1 /
PWM6_M1 /	/ SPI3_C81_M1 /
HDMI_RX_HPDOUT M0 functional pin	
/ I2S1_MCLK_M0 /	
/ PCIE30X1_1_CKREON_M1 /	
/ BT1120_D0 /	
/ CIF_D0 /	
/ GPIO4_A0_d /	
AL30	
/ I2S1_SCLK_M0 /	
/ PCIE30X1_1_WAKEN_M1 /	
/ BT1120_D1 /	
/ CIF_D1 /	
/ GPIO4_A1_d /	
AM29	
/ I2S1_LRCK_M0 /	
/ PCIE30X1_1_PERSTN_M1 /	
/ BT1120_D2 /	
/ CIF_D2 /	
/ GPIO4_A2_d /	
/ I2S1_LRCK_M0 /	
/ PCIE30X1_0_CKREON_M1 /	
/ BT1120_D3 /	
/ CIF_D3 /	
/ GPIO4_A3_d /	
AL29	
/ I2S1_LRCK_M0 /	
/ PCIE30X1_0_WAKEN_M1 /	
/ BT1120_D4 /	
/ CIF_D4 /	
/ GPIO4_A4_d /	
AL28	
/ I2S1_SCLK_M0 /	
/ PCIE30X1_0_PERSTN_M1 /	
/ BT1120_D5 /	
/ CIF_D5 /	
/ GPIO4_A5_d /	
AK27	
/ I2S1_SD1_M0 /	
/ PCIE30X1_0_PERSTN_M1 /	
/ BT1120_D6 /	
/ CIF_D6 /	
/ GPIO4_A6_d /	
AL27	
/ I2S1_SD1_M0 /	
/ PCIE30X1_0_WAKEN_M1 /	
/ BT1120_D7 /	
/ CIF_D7 /	
/ GPIO4_A7_d /	
AM27	
/ I2S1_SD1_M0 /	
/ PCIE30X2_CKREON_M1 /	
/ BT1120_CLKOUT /	
/ CIF_CLKIN /	
/ GPIO4_B0_d /	
AK26	
/ I2S1_SD0_M0 /	
/ PCIE30X1_0_BUTTON_RSTN /	
/ MIPI_CAMERA0_CLK_M0 /	
/ GPIO4_B1_u /	
AL24	
/ I2S1_SD0_M0 /	
/ PCIE30X1_1_BUTTON_RSTN /	
/ CIF_HREF /	
/ GPIO4_B2_u /	
AK25	
/ I2S1_SD0_M0 /	
/ PCIE30X1_2_BUTTON_RSTN /	
/ CIF_VSYNC /	
/ GPIO4_B3_u /	
AM25	
/ I2S1_SD0_M0 /	
/ PCIE30X4_CKREON_M1 /	
/ BT1120_D10 /	
/ CIF_CLKOUT /	
/ GPIO4_B4_u /	
AL26	
/ HDMI_RX_CCS_M0 /	
/ PCIE30X4_WAKEN_M1 /	
/ BT1120_D11 /	
/ CIF_D11 /	
/ GPIO4_B5_d /	
AJ26	
/ HDMI_RX_HPDOUT_M0 /	
/ PCIE30X4_PERSTN_M1 /	
/ BT1120_D12 /	
/ CIF_D12 /	
/ GPIO4_B6_d /	
AJ27	
/ HDMI_RX_CCS_M0 /	
/ PCIE30X4_WAKEN_M1 /	
/ BT1120_D13 /	
/ CIF_D13 /	
/ GPIO4_B7_u /	
AJ28	
/ HDMI_RX_CCS_M0 /	
/ PCIE30X4_WAKEN_M1 /	
/ BT1120_D14 /	
/ CIF_D14 /	
/ GPIO4_C0_u /	
AJ25	
/ HDMI_RX_CCS_M0 /	
/ PCIE30X1_2_PERSTN_M1 /	
/ BT1120_D15 /	
/ CIF_D15 /	
/ GPIO4_C1_d /	
AJ24	

Figure 2-121 RK3588 HDMI_RX_HPDOUT M0 functional pin

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

PWM10_M0	/ SPI4_MISO_M1	/	/ I2C6_SDA_M4	/ FSPI_D0_M2	/ I2S3_MCLK	/ SDIO_D0_M1	/ GMAC1_RXD2	/ GPIO3_A0_u	AA29
AUDDSM_LN	/ SPI4_MOSI_M1	/ PWM11_IR_M0	/ I2C6_SCL_M4	/ FSPI_DL_M2	/ I2S3_SCLK	/ SDIO_D1_M1	/ GMAC1_RXD3	/ GPIO3_A1_u	AA30
AUDDSM_LP	/ SPI4_CLK_M1	/ UART8_RX_M1	/	/ FSPI_D2_M2	/ I2S3_LRCK	/ SDIO_D2_M1	/ GMAC1_RXD2	/ GPIO3_A2_u	AD27
AUDDSM_RN	/ SPI4_CS0_M1	/ UART8_RX_M1	/	/ FSPI_D3_M2	/ I2S3_SDO	/ SDIO_D3_M1	/ GMAC1_RXD3	/ GPIO3_A3_u	AE27
AUDDSM_RP	/ SPI4_CS1_M1	/ UART8_RTSN_M1	/	/ I2S3_SDI	/ SDIO_CMD_M1	/ GMAC1_RXCLK	/ GPIO3_A4_d	AD28	
	/ MIPI_CAMERA0_CLK_M1	/ UART8_CTSN_M1	/ I2C4_SDA_M0	/ FSPI_CLK_M2	/	/ SDIO_CLK_M1	/ GMAC1_RXCLK	/ GPIO3_A5_d	AH30
	/ MIPI_CAMERA1_CLK_M1	/	/ I2C4_SCL_M0	/	/	/	/ ETH1_REFCLK0_25M	/ GPIO3_A6_d	AH27
PWM8_M0	/ MIPI_CAMERA2_CLK_M1	/	/	/	/	/	/ GMAC1_RXD0	/ GPIO3_A7_u	AG29
PWM9_M0	/ MIPI_CAMERA3_CLK_M1	/	/	/	/	/	/ GMAC1_RXD1	/ GPIO3_B0_u	AG28
PWM2_M1	/ MIPI_CAMERA4_CLK_M1	/ UART2_RX_M2	/	/	/	/	/ GMAC1_RXDV_CRS	/ GPIO3_B1_d	AH29
PWM3_IR_M1	/	/ UART2_RX_M2	/	/	/ I2S2_SDI_M1	/	/ GMAC1_TXER	/ GPIO3_B2_d	AE28
	/	/ UART2_RTSN	/	/	/ I2S2_SDO_M1	/	/ GMAC1_RXD0	/ GPIO3_B3_u	AC28
	/	/ UART2_CTSN	/	/	/ I2S2_MCLK_M1	/	/ GMAC1_RXD1	/ GPIO3_B4_u	AC29
PWM12_M0	/ CAN1_RX_M0	/ UART3_RX_M1	/	/	/ I2S2_SCL_M1	/	/ GMAC1_TXEN	/ GPIO3_B5_u	AD29
PWM13_M0	/ CAN1_TX_M0	/ UART3_RX_M1	/	/	/ I2S2_LRCK_M1	/	/ GMAC1_MCLKINOUT	/ GPIO3_B6_d	AE29
	/	/	/ I2C3_SCL_M1	/ SPI1_MOSI_M1	/ HDMI_RX1_HPD_M1	/	/ GMAC1_PTF_REF_CLK	/ GPIO3_B7_d	AA28
	/	/ UART7_RX_M1	/ I2C3_SDA_M1	/ SPI1_MISO_M1	/	/	/ GMAC1_PPSTRIG	/ GPIO3_C0_d	Y29
	/ PCIE30X2_BUTTON_RSTN	/ UART7_RX_M1	/	/ SPI1_CLK_M1	/	/	/ GMAC1_PPCLK	/ GPIO3_C1_d	Y27
PWM14_M0	/	/ UART7_RTSN_M1	/ I2C8_SCL_M4	/ SPI1_CS0_M1	/	/ MIPI_TE0	/ GMAC1_NDC	/ GPIO3_C2_d	Y31
PWM15_IR_M0	/	/ UART7_CTSN_M1	/ I2C8_SDA_M4	/ SPI1_CS1_M1	/	/ MIPI_TE1	/ GMAC1_MDIO	/ GPIO3_C3_d	Y30
CAN2_RX_M0	/ PCIE30X4_CLKREQN_M2	/ UART8_RX_M1	/ FSPI_CS0N_M2	/ SPI2_CS0_M2	/ HDMI_RX1_CEC_M2	/	/ CIF_D8	/ GPIO3_C4_u	AH26
CAN2_TX_M0	/ PCIE30X4_WAKEN_M2	/ UART8_RX_M1	/ FSPI_CS1N_M2	/ SPI2_CS1_M2	/ HDMI_RX1_SDA_M1	/	/ CIF_D9	/ GPIO3_C5_u	AH25
	/ PCIE30X4_PERSTN_M2	/	/	/ SPI2_MISO_M2	/ HDMI_RX1_SCL_M1	/	/ CIF_D10	/ GPIO3_C6_u	AG28
	/ PCIE30X1_2_CLKREQN_M0	/	/ I2C5_SCL_M0	/ SPI3_MOSI_M2	/ HDMI_RX2_SCL_M2	/	/ CIF_D11	/ GPIO3_C7_u	AJ24
PWM8_M2	/ PCIE30X1_2_WAKEN_M0	/ UART4_RX_M1	/ I2C5_SDA_M0	/ SPI3_CLK_M2	/ HDMI_RX2_SDA_M1	/	/ CIF_D12	/ GPIO3_D0_u	AH24
PWM9_M2	/ PCIE30X1_2_PERSTN_M0	/ UART4_RX_M1	/	/ SPI3_MISO_M2	/ HDMI_RX_CEC_M1	/	/ CIF_D13	/ GPIO3_D1_d	AG23
	/ PCIE30X2_CLKREQN_M2	/ UART9_RTSN_M2	/ I2C7_SCL_M2	/ SPI0_MOSI_M2	/ HDMI_RX_SCL_M1	/	/ CIF_D14	/ GPIO3_D2_d	AG25
PWM10_M2	/ PCIE30X2_WAKEN_M2	/ UART9_CTSN_M2	/ I2C7_SDA_M2	/ SPI0_CLK_M2	/ HDMI_RX_SDA_M1	/	/ CIF_D15	/ GPIO3_D3_d	AG24
	/ PCIE30X2_PERSTN_M2	/ UART9_RX_M2	/	/ SPI0_CS0_M2	/ HDMI_RX_HPDOUT_M1	/ HDMI_RX_HPD_M1 / MCU_JTAG_TCR_M1	/ GPIO3_D4_d	AA27	
PWM11_IR_M2	/ PCIE30X4_BUTTON_RSTN	/ UART9_RX_M2	/	/ SPI0_CS1_M2	/ DP1_HPDIN_M0	/	/ MCU_JTAG_TMS_M1	/ GPIO3_D5_d	AB28

Figure 2-122 RK3588 HDMI_RX_HPDOUT M1 functional pin

VCCIO4 Domain	
Operating Voltage=1.8V/3.3V	
SATA1_ACT_LED_M1 /	/SPI4_MOSI_M2 /PCIE30X1_1_CLKREQN_M2 / DP0_HPDIN_M2 / I2C2_SDA_M4 / UART6_RX_M1 /GPIO1_A0_d A24
/ FWD40_M2	/SPI4_CLK_M2 / VOP_POST_EMPTY / I2C2_SCL_M4 / UART6_TX_M1 /GPIO1_A1_d A25
/ FWD41_M2	/SPI4_CS0_M2 / HDMI_TX1_SDA_M2 / I2C4_SDA_M3 / UART6_RTSN_M1 /GPIO1_A2_d A26
/	/SPI2_MISO_M0 / HDMI_TX1_SCL_M2 / / / GPIO1_A3_d A27
/	/SPI2莫斯I_M0 / HDMI_TX0_HPD_M0 / / / GPIO1_A4_d B25
/	/SPI2_CLK_M0 / HDMI_TX1_HPD_M0 / / / GPIO1_A5_d B26
/ BWM3_IR_M3	/SPI2_CS0_M0 /PCIE30X1_1_PERSTN_M2 / PDM1_SD10_M1 / GPIO1_A7_u C24
/	/SPI2_CS1_M0 /PCIE30X4_CLKREQN_M3 / PDM1_SD11_M1 / GPIO1_B0_u C25
/	/SPI0_MISO_M2 /PCIE30X4_WAKEN_M3 / PDM1_SD12_M1 / GPIO1_B1_d D25
/	/SPI0莫斯I_M2 /PCIE30X4_PERSTN_M3 / PDM1_SD13_M1 / UART4_RX_M2 /GPIO1_B2_d D26
SATA0_ACT_LED_M1 /	/SPI0_CLK_M2 /PCIE30X1_0_WAKEN_M2 / PDM1_CLK1_M1 / UART4_TX_M2 /GPIO1_B3_d D27
/	/SPI0_CS0_M2 /PCIE30X1_0_PERSTN_M2 / PDM1_CLK0_M1 / UART7_RX_M2 /GPIO1_B4_u E24
/	/SPI0_CS1_M2 /PCIE30X1_0_CLKREQN_M2 / / / UART7_TX_M2 /GPIO1_B5_u E25
HDMI_RX_HPDOUT_M2 /	/SPDIFO_TX_M0 /PCIE30X2_WAKEN_M3 / MIPI_CAMERA1_CLK_M0 / I2C5_SCL_M3 / UART1_RX_M1 /GPIO1_B6_u E26
SATA2_ACT_LED_M1 / HDMI_RX_CEC_M2 / FWD41_M2	/SPDIF1_TX_M0 /PCIE30X2_PERSTN_M3 / MIPI_CAMERA2_CLK_M0 / I2C5_SDA_M3 / UART1_RX_M1 /GPIO1_B7_u E27
HDMI_RX_SCL_M2 / FWD41_M2 /	/MIPI_CAMERA3_CLK_M0 / I2C8_SCL_M2 / UART1_RTSN_M1 /GPIO1_D6_u F24
HDMI_RX_SDA_M2 / FWD41_M3 /	/PCIE30X2_CLKREQN_M3 / MIPI_CAMERA4_CLK_M0 / I2C8_SDA_M2 / UART1_CTSN_M1 /GPIO1_D7_u F25

Figure 2-123 RK3588 HDMI_RX_HPDOUT M2 functional pin

Since the HDMI RX controller does not support hardware detection of Source plug-in, it can only be detected by software. The hardware circuit is as follows:

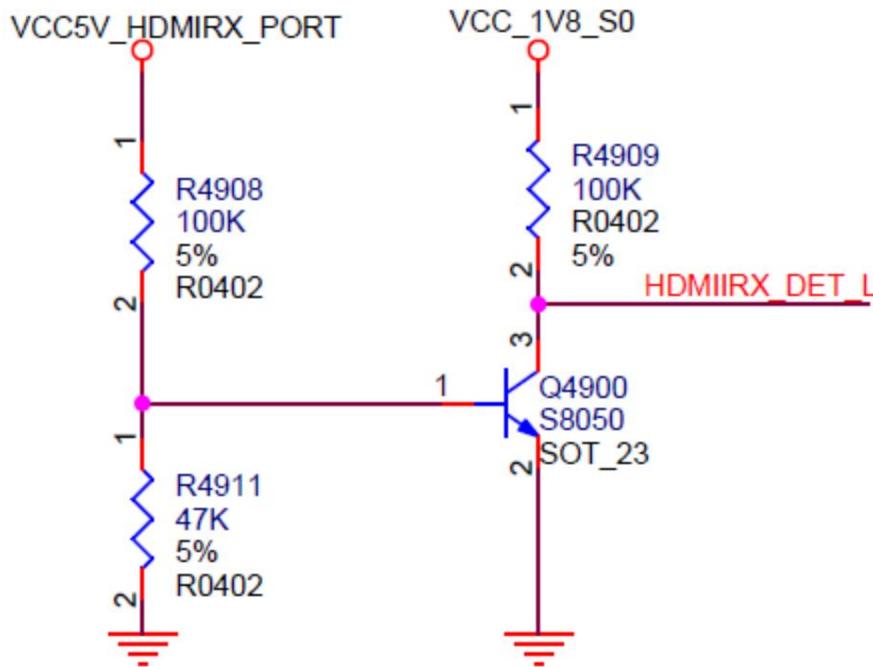


Figure 2-124 RK3588 HDMI_RX_DET circuit

After detecting HDMI RX DET pull-down action,

HDMI RX HPD outputs a high level, Q4900 is turned on,

VCC5V_HDMIRX_PORT sends 5V to the HDMI RX HPD Port to complete the handshake with the Source end.

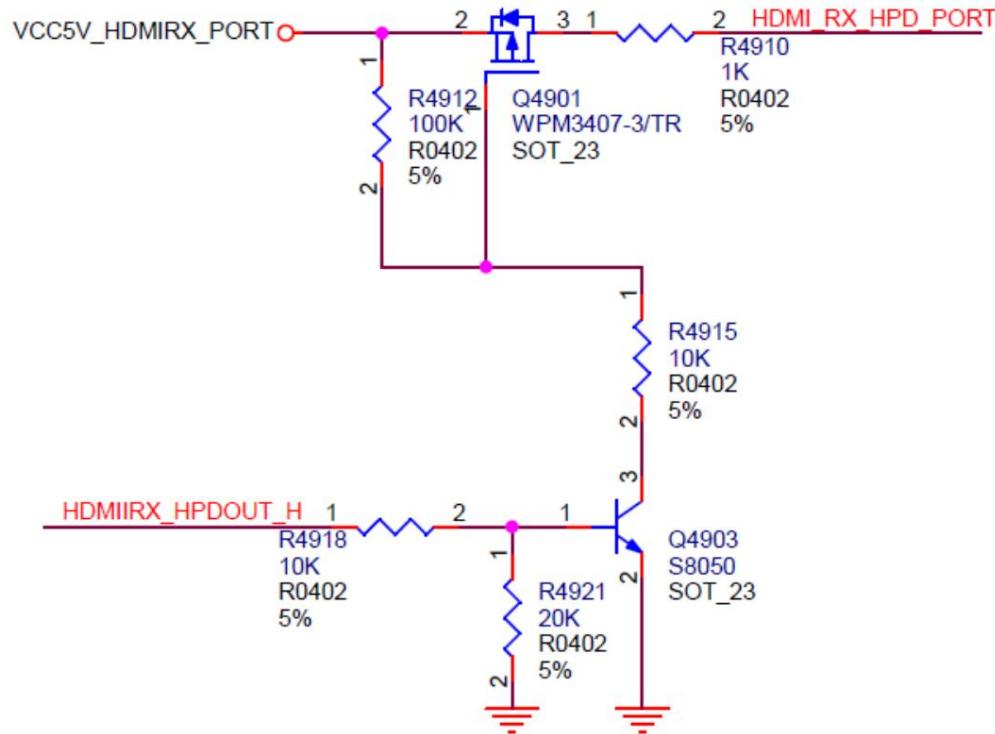


Figure 2-125 RK3588 HDMI_RX_HPD circuit

HDMI_RX_CEC is the HDMI controller CEC function multiplexed to the common GPIO function, the level depends on the power domain voltage, power

If the domain power supply voltage changes, the pull-up resistor power supply of the peripheral circuit must also be adjusted synchronously.

HDMI_RX_CEC reuses 3 locations, one on the IO of the VCCIO6 power domain and one on the IO of the VCCIO5 power domain.

Above, one on the IO in the VCCIO4 power domain.

VCCIO6 Domain							
Operating Voltage=1.8V/3.3V							
/ SPI0_MISO_M1	/ UART9_RTSN_M1	/	/ I2S1_MCLK_M0	/ PCIE30X1_1_CLKREQN_M1	/ BT1120_D0	/ CIP_D0	/ GPIO4_A0_d
/ SPI0_MOSI_M1	/ UART9_CTSN_M1	/	/ I2S1_SDCK_TX_M0	/ PCIE30X1_0_WAREN_M1	/ BT1120_D1	/ CIP_D1	/ GPIO4_A1_d
/ SPI0_CLK_M1	/	/	/ I2S1_LCKC_TX_M0	/ PCIE30X1_1_PERST_M1	/ BT1120_D2	/ CIP_D2	/ GPIO4_A2_d
/	/ UART9_RX_M2	/	/ I2S1_SDCK_RX_M0	/ PCIE30X1_0_CLKREQN_M1	/ BT1120_D3	/ CIP_D3	/ GPIO4_A3_d
/ SPI2_MISO_M1	/ UART0_RX_M2	/ I2C3_SCL_M2	/ I2S1_LCKC_RX_M0	/ PCIE30X1_0_WAREN_M1	/ BT1120_D4	/ CIP_D4	/ GPIO4_A4_d
/ SPI2_MOSI_M1	/ UART3_RX_M2	/ I2C3_SDA_M2	/ I2S1_SDIO_M0	/ PCIE30X1_0_PERSTN_M1	/ BT1120_D5	/ CIP_D5	/ GPIO4_A5_d
/ SPI2_CLK_M1	/ UART3_RX_M2	/ I2C5_SCL_M2	/ I2S1_SD11_M0	/ PCIE30X2_CLKREQN_M1	/ BT1120_D6	/ CIP_D6	/ GPIO4_A6_d
/ SPI2_CS0_M1	/	/ I2C5_SDA_M2	/ I2S1_SD12_M0	/ PCIE30X2_WAREN_M1	/ BT1120_D7	/ CIP_D7	/ GPIO4_A7_d
/ SPI2_CS1_M1	/ UART8_RX_M0	/ I2C6_SDA_M3	/ I2S1_SD13_M0	/ PCIE30X2_PERSTN_M1	/ BT1120_CLKOUT	/ CIP_CLKIN	/ GPIO4_B0_d
SATA0_ACT_LED_M0	/ SPDIF1_RX_M1	/ SPI0_CS1_M1	/	/ PCIE30X1_0_BUTTON_RSTN /	/ MIPI_CAMERA0_CLK_M0	/ GPIO4_B1_u	
CAMI_RX_M1	/ PWM14_M1	/ SPI0_CS0_M1	/ UART8_RTSN_M0	/ I2C7_SCL_M3	/ I2S1_SD01_M0	/ PCIE30X1_1_BUTTON_RSTN /	
CAMI_RX_M1	/ PWM15_IR_M1	/	/ UART8_CTSN_M0	/ I2C7_SDA_M3	/ I2S1_SD02_M0	/ PCIE30X1_2_BUTTON_RSTN /	/ CIP_HREF /
CAMI_TX_M1	/ PWM15_IR_M1	/	/	/	/	/ CIP_VSYNC /	/ GPIO4_B2_u
SAT0_RX_X_M1	/ PWM11_IR_M1	/ DFI_HPDIN_M0	/ UART7_RX_M1	/	/ I2S1_SD03_M0	/ PCIE30X4_CLKREQN_M1	/ BT1120_D10 / CIP_CIRCUIT
SATA0_ACT_LED_M0	/ PWM12_M1	/ SPI3_MISO_M1	/ UART9_RX_M1	/	/ HDMI_RX_CEC_M0	/ PCIE30X4_WAREN_M1	/ BT1120_D11 /
SATA0_ACT_LED_M0	/ PWM13_M1	/ SPI3_MOSI_M1	/	/ I2C5_SCL_M1	/ HDMI_RX_HPDIN_M0	/ PCIE30X4_PERSTN_M1	/ BT1120_D12 /
/	/ SPI3_CLK_M1	/	/ I2C5_SDA_M1	/ HDMI_RX_SCL_M0	/ PCIE30X1_2_CLKREQN_M1	/ BT1120_D13 /	/ GPIO4_B7_u
/	/ SPI3_CS0_M1	/	/ I2C8_SCL_M3	/ HDMI_RX_SDA_M0	/ PCIE30X1_2_WAREN_M1	/ BT1120_D14 /	/ GPIO4_C0_u
SPDIF1_RX_M2	/ PWM6_M1	/ SPI3_CS1_M1	/	/ I2C8_SDA_M3	/ HDMI_RX_CEC_M0	/ PCIE30X1_2_PERSTN_M1	/ BT1120_D15 /

Figure 2-126 RK3588 HDMI_RX_CEC M0 function pin

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

PWM10_M0	/ SPI4_MISO_M1	/	/ I2C6_SDA_M4	/ FSPI_D0_M2	/ I2S8_MCLK	/ SDIO_D0_M1	/ GNAC1_RXD2	/ GPIO3_A0_u	AA29
AUDDSM_LN	/ SPI4_MOSI_M1	/ PWM11_IR_M0	/ I2C6_SCL_M4	/ FSPI_D1_M2	/ I2S8_SCLK	/ SDIO_D1_M1	/ GNAC1_RXD3	/ GPIO3_A1_u	AA30
AUDDSM_LP	/ SPI4_CLK_M1	/ UART8_RX_M1	/	/ FSPI_D2_M2	/ I2S8_LRCK	/ SDIO_D2_M1	/ GNAC1_RXD2	/ GPIO3_A2_u	AD27
AUDDSM_RN	/ SPI4_CS0_M1	/ UART8_RX_M1	/	/ FSPI_D3_M2	/ I2S8_SDO	/ SDIO_D3_M1	/ GNAC1_RXD3	/ GPIO3_A3_u	AE27
AUDDSM_RP	/ SPI4_CS1_M1	/ UART8_RTSN_M1	/	/	/ I2S8_SDI	/ SDIO_CMD_M1	/ GNAC1_RXCLK	/ GPIO3_A4_d	AD28
/ MIPI_CAMERA0_CLK_M1	/ UART8_CTSN_M1	/ I2C4_SDA_M0	/ FSPI_CLK_M2	/	/ SDIO_CLK_M1	/ GNAC1_RXCLK	/ GPIO3_A5_d	AH30	
/ MIPI_CAMERA1_CLK_M1	/	/ I2C4_SCL_M0	/	/	/	/ ETH1_REFCLK0_25M	/ GPIO3_A6_d	AH27	
PWM8_M0	/ MIPI_CAMERA2_CLK_M1	/	/	/	/	/	/ GNAC1_RXD0	/ GPIO3_A7_u	AG29
PWM9_M0	/ MIPI_CAMERA3_CLK_M1	/	/	/	/ I2S2_SCLK_RX_M1	/	/ GNAC1_RXD1	/ GPIO3_B0_u	AG28
PWM2_M1	/ MIPI_CAMERA4_CLK_M1	/ UART2_RX_M2	/	/	/ I2S2_LRCK_RX_M1	/	/ GNAC1_RXDV_CRS	/ GPIO3_B1_d	AH29
PWM3_IR_M1	/	/ UART2_RX_M2	/	/	/ I2S2_SDI_M1	/	/ GNAC1_TXER	/ GPIO3_B2_d	AE28
/	/ UART2_RTSN	/	/	/	/ I2S2_SDO_M1	/	/ GNAC1_TXDO	/ GPIO3_B3_u	AC28
/	/ UART2_CTSN	/	/	/	/ I2S2_MCLK_M1	/	/ GNAC1_TXD1	/ GPIO3_B4_u	AC29
PWM12_M0	/ CAN1_RX_M0	/ UART3_RX_M1	/	/	/ I2S2_SCL_RX_M1	/	/ GNAC1_TXEN	/ GPIO3_B5_u	AD29
PWM13_M0	/ CAN1_RX_M0	/ UART3_RX_M1	/	/	/ I2S2_LRCK_RX_M1	/	/ GNAC1_MCLKINOUT	/ GPIO3_B6_d	AE29
/	/	/ I2C3_SCL_M1	/ SPI1_MOSI_M1	/ HDMI_RX1_HPD_M1	/	/ GNAC1_PTD_REF_CLK	/ GPIO3_B7_d	AA28	
/	/ UART7_RX_M1	/ I2C3_SDA_M1	/ SPI1_MISO_M1	/	/	/ GNAC1_PPSTTRIG	/ GPIO3_C0_d	Y29	
/ PCIE30X2_BUTTON_RSTN	/ UART7_RX_M1	/	/ SPI1_CLK_M1	/	/	/ GNAC1_PPCLK	/ GPIO3_C1_d	Y27	
PWM14_M0	/	/ UART7_RTSN_M1	/ I2C8_SCL_M4	/ SPI1_CS0_M1	/	/ MIPI_TE0	/ GNAC1_HDC	/ GPIO3_C2_d	Y31
PWM15_IR_M0	/	/ UART7_CTSN_M1	/ I2C8_SDA_M4	/ SPI1_CS1_M1	/	/ MIPI_TE1	/ GNAC1_MDIO	/ GPIO3_C3_d	Y30
CAN2_RX_M0	/ PCIE30X4_CLKREQN_M2	/ UART5_RX_M1	/ FSPI_CS0N_M2	/ SPI3_CS0_M3	/ HDMI_RX1_CEC_M2	/	/ CIF_D8	/ GPIO3_C4_u	AH26
CAN2_RX_M0	/ PCIE30X4_WAKEN_M2	/ UART5_RX_M1	/ FSPI_CS1N_M2	/ SPI3_CS1_M3	/ HDMI_RX1_SDA_M1	/	/ CIF_D9	/ GPIO3_C5_u	AH25
/ PCIE30X4_PERSTN_M2	/	/	/ SPI3_MISO_M3	/ HDMI_RX1_SCL_M1	/	/ CIF_D10	/ GPIO3_C6_u	AG26	
/ PCIE30X1_2_CLKREQN_M0	/	/ I2C8_SCL_M0	/ SPI3_MOSI_M3	/ HDMI_RX0_SCL_M2	/	/ CIF_D11	/ GPIO3_C7_u	AJ24	
PWM8_M2	/ PCIE30X1_2_WAKEN_M0	/ UART4_RX_M1	/ I2C6_SDA_M0	/ SPI3_CLK_M3	/ HDMI_RX0_SDA_M2	/	/ CIF_D12	/ GPIO3_D0_u	AH24
PWM9_M2	/ PCIE30X1_2_PERSTN_M0	/ UART4_RX_M1	/	/ SPI0_MISO_M3	HDMI_RX_CEC_M1	/	/ CIF_D13	/ GPIO3_D1_d	AG23
/ PCIE30X2_CLKREQN_M2	/ UART5_RTSN_M2	/ I2C7_SCL_M2	/ SPI0_MOSI_M3	/ HDMI_RX_SCL_M1	/	/ CIF_D14	/ GPIO3_D2_d	AG25	
PWM10_M2	/ PCIE30X2_WAKEN_M2	/ UART5_CTSN_M2	/ I2C7_SDA_M2	/ SPI0_CLK_M3	/ HDMI_RX_SDA_M1	/	/ CIF_D15	/ GPIO3_D3_d	AG24
/ PCIE30X2_PERSTN_M2	/ UART5_RX_M2	/	/ SPI0_CS0_M3	/ HDMI_RX_HPDIN_M1	HDMI_RX_HPD_M1 / MCU_JTAG_TCK_M1	/	/ GPIO3_D4_d	AA27	
PWM11_IR_M3	/ PCIE30X4_BUTTON_RSTN	/ UART5_RX_M2	/	/ SPI0_CS1_M3	/ DPI_HPDIN_M0	/	/ MCU_JTAG_TMS_M1	/ GPIO3_D5_d	AB28

Figure 2-127 RK3588 HDMI_RX_CEC M1 function pin

VCCIO4 Domain

Operating Voltage=1.8V/3.3V

SATA1_ACT_LED_M1	/	/ SPI4_MISO_M2	/ PCIE30X1_1_CLKREQN_M2	/ D0_HPDIN_M2	/ I2C2_SDA_M4	/ UART6_RX_M1	/ GPIO1_A0_d	A24	
/ PWM0_M2	/ SPI4_CLK_M2	/	/ VOF_POST_EMPTY	/ I2C4_SDA_M3	/ UART6_RTSN_M1	/ GPIO1_A2_d	A25		
/ PWM1_M2	/ SPI4_CS0_M2	/	/ HDMI_RX1_SDA_M2	/ I2C4_SCL_M3	/ UART6_CTSN_M1	/ GPIO1_A3_d	A26		
/	/ SPI2_MISO_M0	/	/ HDMI_RX1_SCL_M2	/	/	/	/ GPIO1_A4_d	B25	
/	/ SPI2_MOSI_M0	/	/ HDMI_RX0_HPD_M0	/	/	/	/ GPIO1_A5_d	B26	
/	/ SPI2_CLK_M0	/	/ HDMI_RX1_HPD_M0	/	/	/	/ GPIO1_A6_d	C24	
/ PWM3_IR_M3	/ SPI2_CS0_M0	/ PCIE30X1_1_PERSTN_M2	/	/ PDM1_SD10_M1	/	/	/ GPIO1_A7_u	C25	
/	/ SPI2_CS1_M0	/ PCIE30X4_CLKREQN_M3	/	/ PDM1_SD11_M1	/	/	/ GPIO1_B0_u	C27	
/	/ SPI0_MISO_M2	/ PCIE30X4_WAKEN_M3	/	/ PDM1_SD12_M1	/	/	/ GPIO1_B1_d	D25	
/	/ SPI0_MOSI_M2	/ PCIE30X4_PERSTN_M3	/	/ PDM1_SD13_M1	/ UART4_RX_M2	/	/ GPIO1_B2_d	D26	
SATA0_ACT_LED_M1	/	/ SPI0_CLK_M2	/ PCIE30X1_0_WAKEN_M2	/	/ PDM1_CLK1_M1	/ UART4_TX_M2	/	GPIO1_B3_d	D27
/	/ SPI0_CS0_M2	/ PCIE30X1_0_PERSTN_M2	/	/ PDM1_CLK0_M1	/ UART7_RX_M2	/	/ GPIO1_B4_u	E24	
/	/ SPI0_CS1_M2	/ PCIE30X1_0_CLKREQN_M2	/	/	/	/ UART7_TX_M2	/	/ GPIO1_B5_u	E25
HDMI_RX_HPDIN_M2	/	/ SPDIFO_RX_M0	/ PCIE30X2_WAKEN_M3	/ MIPI_CAMERA1_CLK_M0	/ I2C5_SCL_M3	/ UART1_RX_M1	/ GPIO1_B6_u	E26	
SATA2_ACT_LED_M1	HDMI_RX_CEC_M2	/ PWM13_M2	/ SPDIFI_RX_M0	/ PCIE30X2_PERSTN_M3	/ MIPI_CAMERA2_CLK_M0	/ I2C5_SDA_M3	/ UART1_RX_M1	/ GPIO1_B7_u	E27
HDMI_RX_SCL_M2	/ PWM14_M2	/	/	/ MIPI_CAMERA3_CLK_M0	/ I2C8_SCL_M2	/ UART1_RTSN_M1	/ GPIO1_D6_u	F24	
HDMI_RX_SDA_M2	/ PWM15_IR_M3	/	/ PCIE30X2_CLKREQN_M3	/ MIPI_CAMERA4_CLK_M0	/ I2C8_SDA_M2	/ UART1_CTSN_M1	/ GPIO1_D7_u	F25	

Figure 2-128 RK3588 HDMI_RX_CEC M2 function pin

The CEC protocol specifies a 3.3V level. If the selected IO is a 3.3V IO, then due to protocol requirements, the 27K When a 3.3V voltage is applied to the resistor, the leakage current is not allowed to exceed 1.8uA, and the MOS tube cannot be omitted.

Test ID 7-15: CEC Line Degradation

Reference	Requirement
[HDMI: Table 4-40] CEC line Electrical Specifications for all Configurations	A device with power removed (from the CEC circuitry) shall not degrade communication between other CEC devices (e.g. the line shall not be pulled down by the powered off device). Maximum CEC line leakage current must be $\leq 1.8\mu A$

Figure 2-129 HDMI CEC protocol requirements

When the RK3588 IO Domain is not powered on, if there is voltage on the IO, the IO will leak. For example, if the RK3588 is powered off and the HDMI cable is still connected to the Sink end (TV or monitor), the CEC on the Sink end will have power and will leak to the RK3588 IO through the HDMI cable, causing the CEC leakage to exceed 1.8uA. Therefore, an external isolation circuit is required. The R4813 resistance value cannot be modified arbitrarily and needs to be 27Kohm. The default selection of Q4803 is 2SK3018. If you want to change to other models, the junction capacitance must be equivalent. If the junction capacitance is too large, it will not only affect the work but also fail the certification.

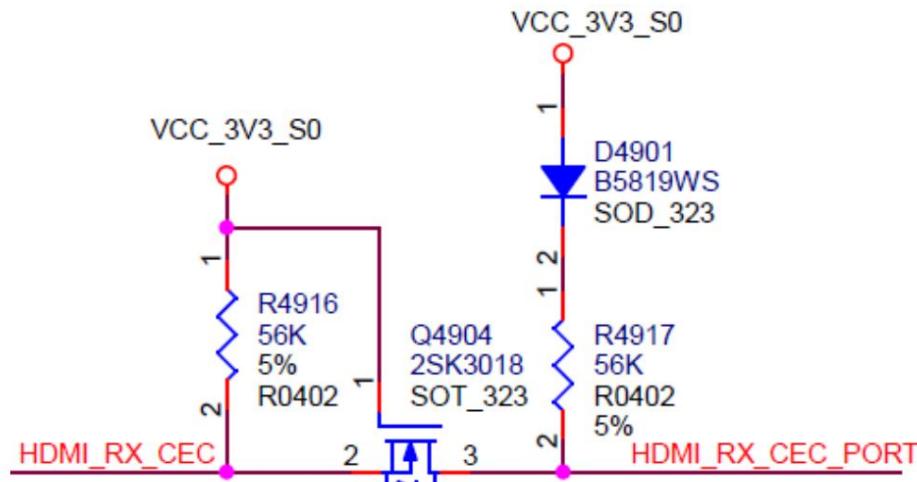


Figure 2-130 HDMI RX CEC isolation circuit

HDMI_RX DDC_SCL/DDC_SDA is the I2C/DDC bus of HDMI RX controller, and its functions are multiplexed to PMUIO2, VCCIO5,

On the IO of the VCCIO4 power domain, the level changes with the voltage of the power domain. If the power domain supply voltage changes, the pull-up resistor power of the peripheral circuit will be They must also be adjusted synchronously.

The DDC_SCL/DDC_SDA protocol specifies a 5V level. RK3588 IO does not support 5V level, so a level conversion circuit must be added.

The default MOS transistor level converter is 2SK3018. If you choose another model, the junction capacitance must be equivalent. Excessively large junction capacitance will not only affect operation but also fail certification. The pull-up resistor is recommended to be kept at the default value and cannot be modified.

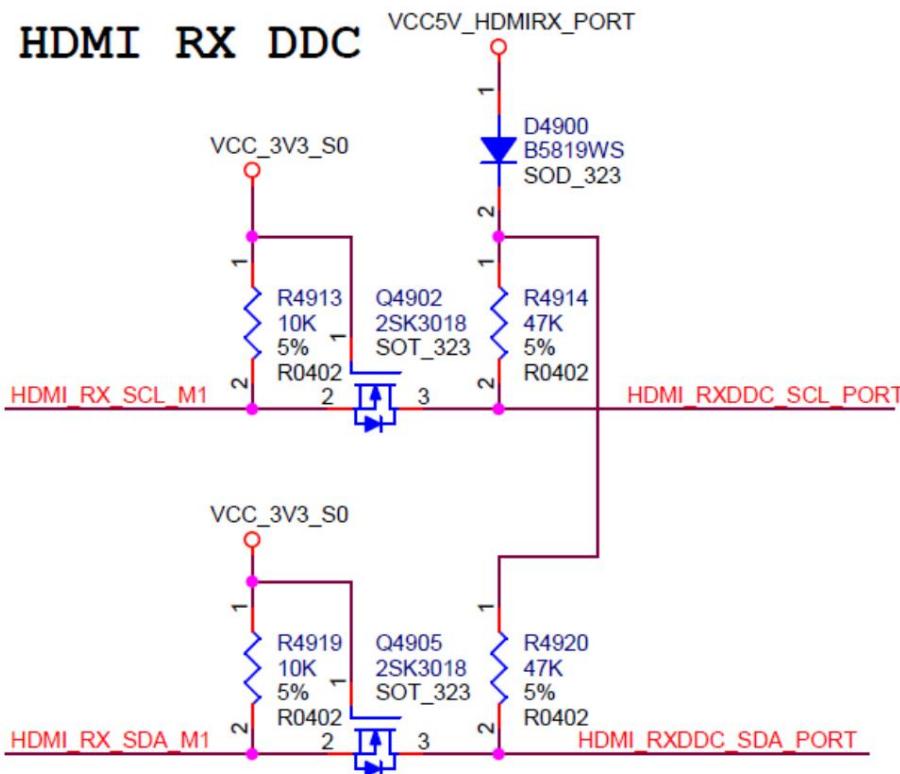


Figure 2-131 HDMI RX DDC level conversion circuit

It is recommended to place a 0.1uF decoupling capacitor on the Pin18 of the HDMI connector. When laying out, place it close to the HDMI connector pin.

ESD devices must be reserved for the signal. The ESD parasitic capacitance of HDMI2.0 signal shall not exceed 0.4pF. The ESD parasitic capacitance of other signals shall not exceed 0.4pF.

It is recommended to use a raw capacitor of no more than 1pF.

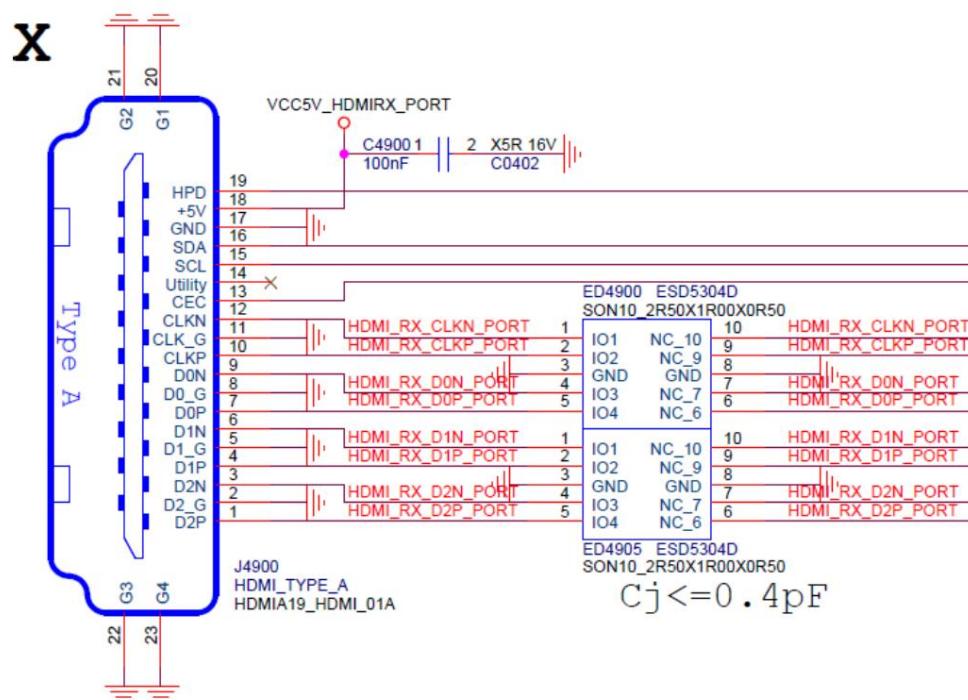


Figure 2-132 HDMI RX connector ESD circuit

The recommended HDMI RX interface matching design is shown in the following table:

Table 2-25 RK3588 HDMI RX interface design

Signal	Connection method	illustrate
HDMI_RX_D0P/D0N	Connect a 2.2ohm resistor in series	TMDS data Lane 0 input
HDMI_RX_D1P/D1N	Connect a 2.2ohm resistor in series	TMDS data Lane 1 input
HDMI_RX_D2P/D2N	Connect a 2.2ohm resistor in series	TMDS data Lane 2 input
HDMI_RX_D3P/D3N	Connect a 2.2ohm resistor in series	TMDS clock input
HDMI_RX_RECT	200 ohm 1% resistor to ground	External reference resistor for HDMI_RX PHY
HDMI_RX_HPD	MOS control circuit	HDMI HPD output
HDMI_RX_CEC	MOS isolation Conversion	HDMI CEC signal
HDMI_RX_SCL	MOS level shifter	HDMI DDC Clock
HDMI_RX_SDA	MOS level shifter	HDMI DDC data input and output

2.3.8 Video output interface circuit

The VOP controller of the RK3588 chip has four port outputs, supporting DP0/DP1/HDMI0/eDP0/HDMI1/eDP1/MIPI DSI0/MIPI DSI1/BT656/BT1120 video interface output.

A maximum of 4 screens are allowed, such as 4K+4K+4K+2K. If 8K is to be supported, only 8K+4K+2K is supported (8K is displayed via Post Process0+ Post Process1 merge implementation).

VOP and video interface output path diagram:

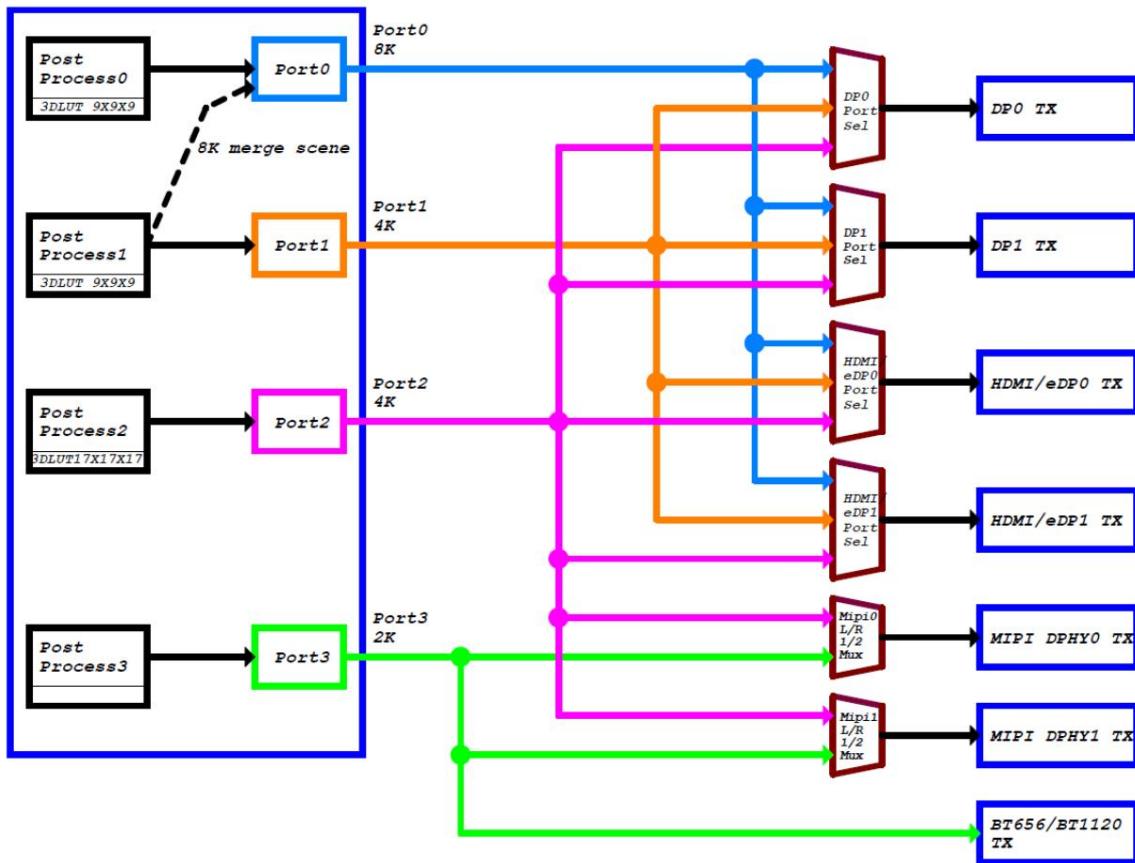


Figure 2-133 RK3588 VOP and video interface output path diagram

2.3.8.1 HDMI2.1/eDP TX Interface

RK3588 has two built-in HDMI/eDP TX Combo PHYs

HDMI/eDP TX Combo PHY supports the following two modes:

- ÿ HDMI TX mode: maximum resolution supports 8K@60Hz, supports RGB/YUV444/YUV420 (Up to 10bit) format;
- ÿ eDP TX mode: supports a maximum resolution of 4K@60Hz and RGB/YUV422 (Up to 10-bit) formats.



Figure 2-134 RK3588 HDMI/eDP Combo PHY0 pins

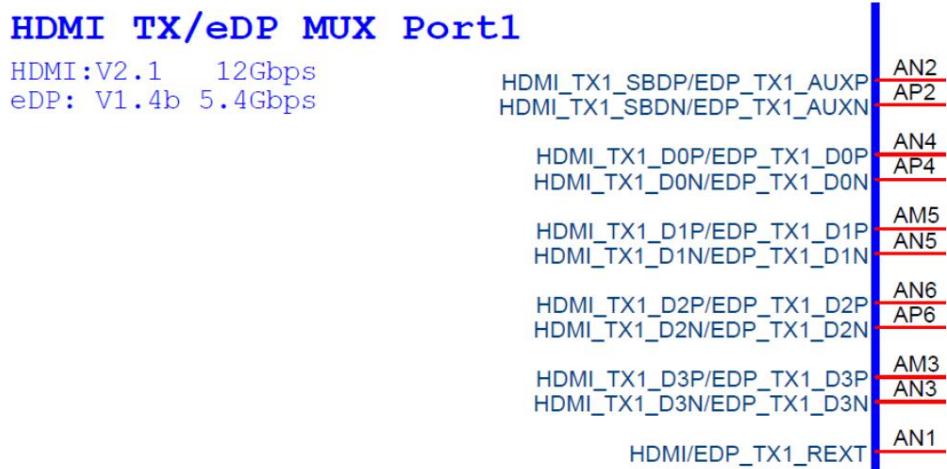


Figure 2-135 RK3588 HDMI/eDP Combo PHY1 pins

HDMI/eDP Combo PHY0/1 power pins need to be placed with 4.7uF, 1uF and 100nF decoupling capacitors. Do not delete them. When laying out, place them close to the RK3588 pin placement.

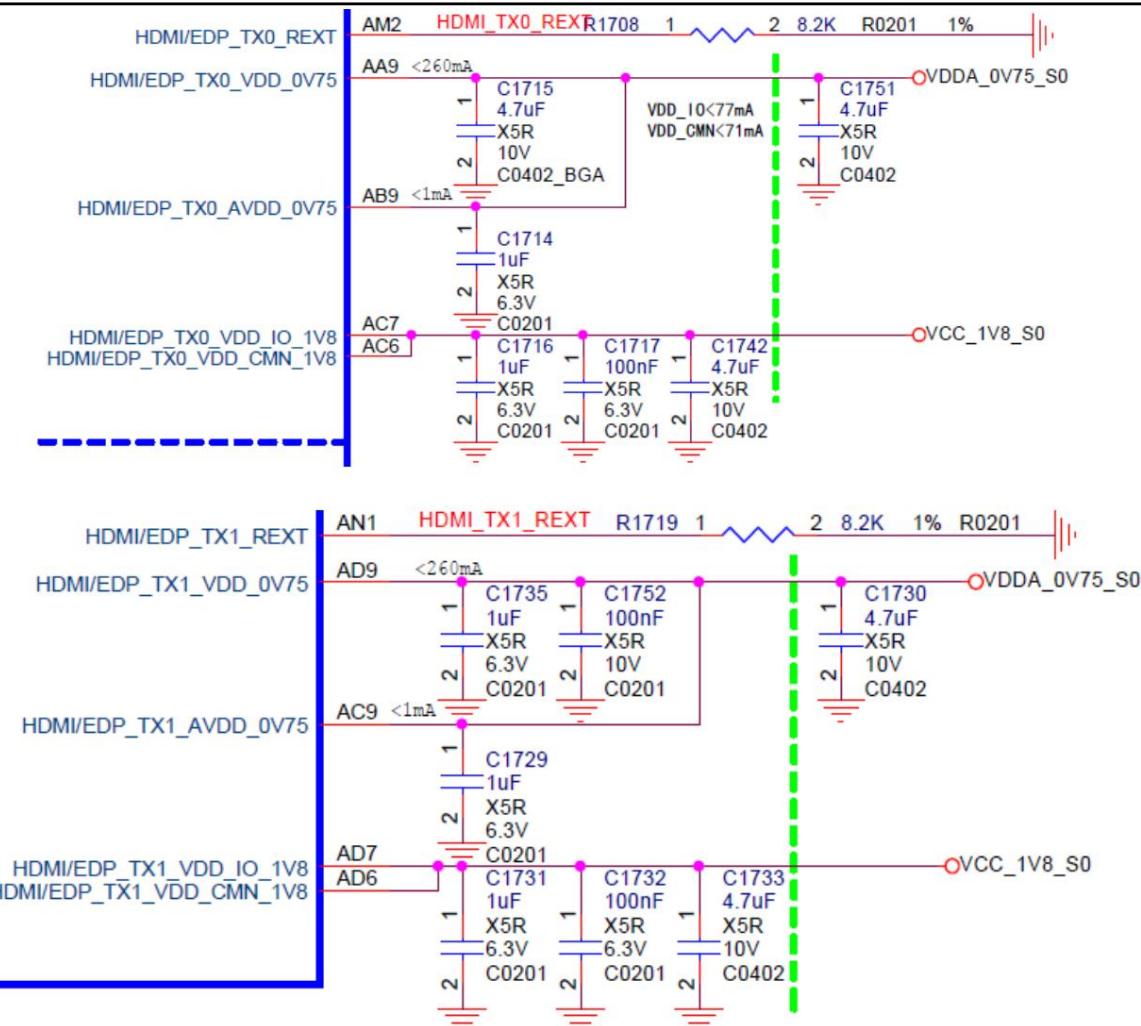


Figure 2-136 HDMI/eDP Combo PHY0/1 power decoupling capacitor

HDMI/EDP_TX0_REXT/HDMI/EDP_TX1_REXT is the external reference resistor pin of HDMI/eDP Combo PHY0/1.

Connect an external 8200ohm resistor with 1% accuracy to ground. Do not change the resistor value. Place it close to the RK3588 chip pins during layout.

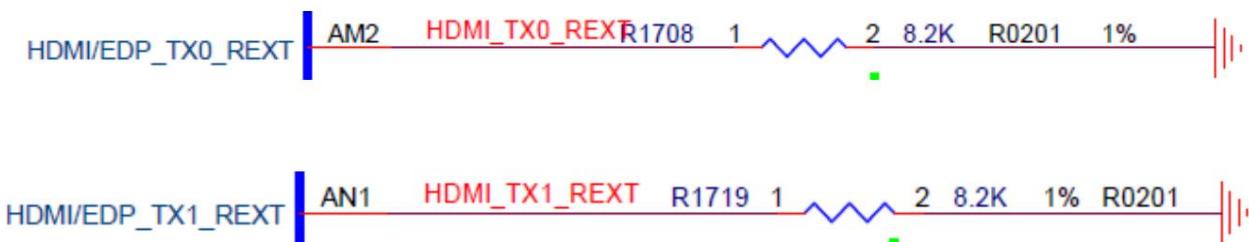


Figure 2-137 RK3588 HDMI/EDP_TX0_REXT/HDMI/EDP_TX1_REXT pins

ÿ HDMI2.1 TX mode

RK3588 supports HDMI2.1 and is compatible with HDMI2.0 and HDMI1.4. Since HDMI2.1 works in FRL mode, when switching to HDMI2.0 and below modes, it works in TMDS mode because it uses AC coupled voltage mode driver.

As shown in the figure below, the AC coupling capacitor uses a capacitance of 220nF and cannot be changed at will. It is recommended to use a 0201 package for AC coupling capacitors, which is lower.

The ESR and ESL can also reduce the impedance variation on the line.

Taking HDMI TX0 as an example, HDMI TX1 is the same as HDMI TX0.

When working in HDMI2.1 mode, HDMI0_TX_ON_H is configured as low level, Q1700, Q1701, Q1702, and Q1703 are not conducting.

When working in HDMI2.0 and below modes, HDMI0_TX_ON_H is configured as high level, Q5007, Q5004, Q5005, Q5006

When it is turned on, the 499ohm resistor to ground and the 50ohm pull-up resistor at the Sink end form a DC bias of about 3V.

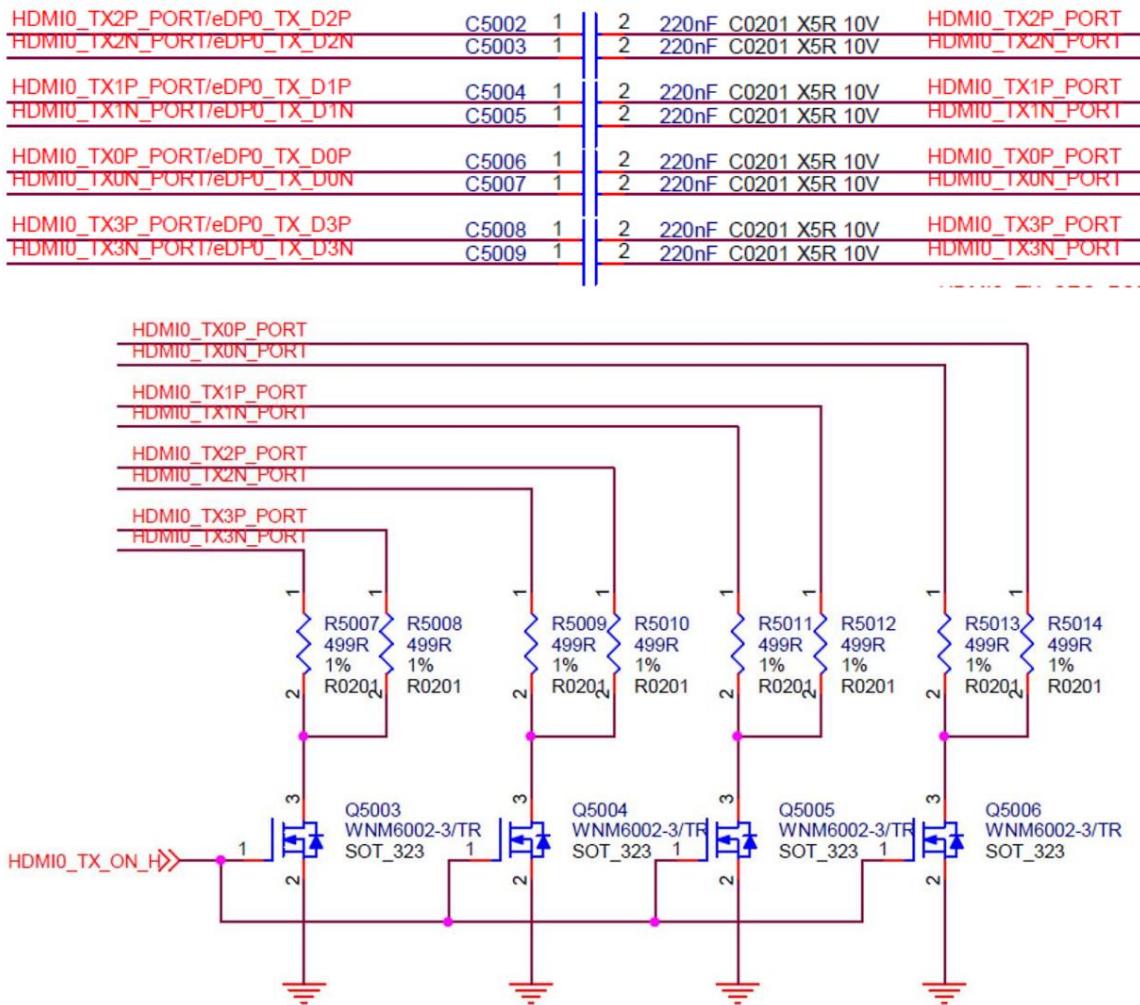


Figure 2-138 RK3588 HDMI TX mode peripheral circuit



Notice

1 : If you only need support HDMI2.0 And the following modes, Q5007 ∨ Q5004 ∨ Q5005 ∨ Q5006 It cannot be omitted. It is necessary to ensure that the pipe is not turned on when the machine is not turned on.

Cannot conduct because HDMI CTS Test ID 7-3 TMDS Voff Test items require I HAVE No power, Wow The voltage must be AVcc+10mV Otherwise, this

Test items failed.

2 : control not Tube Coss It cannot be too large, otherwise it will affect the signal quality. It is recommended to follow the reference figure model or the corresponding Coss value.

FRL mode: In the traditional TMDS architecture, an independent channel is used to transmit the clock, but in the FRL architecture,

The clock is embedded in the data channel and is parsed out through clock recovery at the sink end.

Table 2-26 Relationship between FRL rate and channel

Channel Rate	Number of channels
3Gbps	3
6Gbps	3
6Gbps	4
8Gbps	4
10Gbps	4
12Gbps	4

Supports ARC/eARC, which transmits HDMI0_TX_SBDP/HDMI0_TX_SBDN signals to RK3588 to parse the audio data.

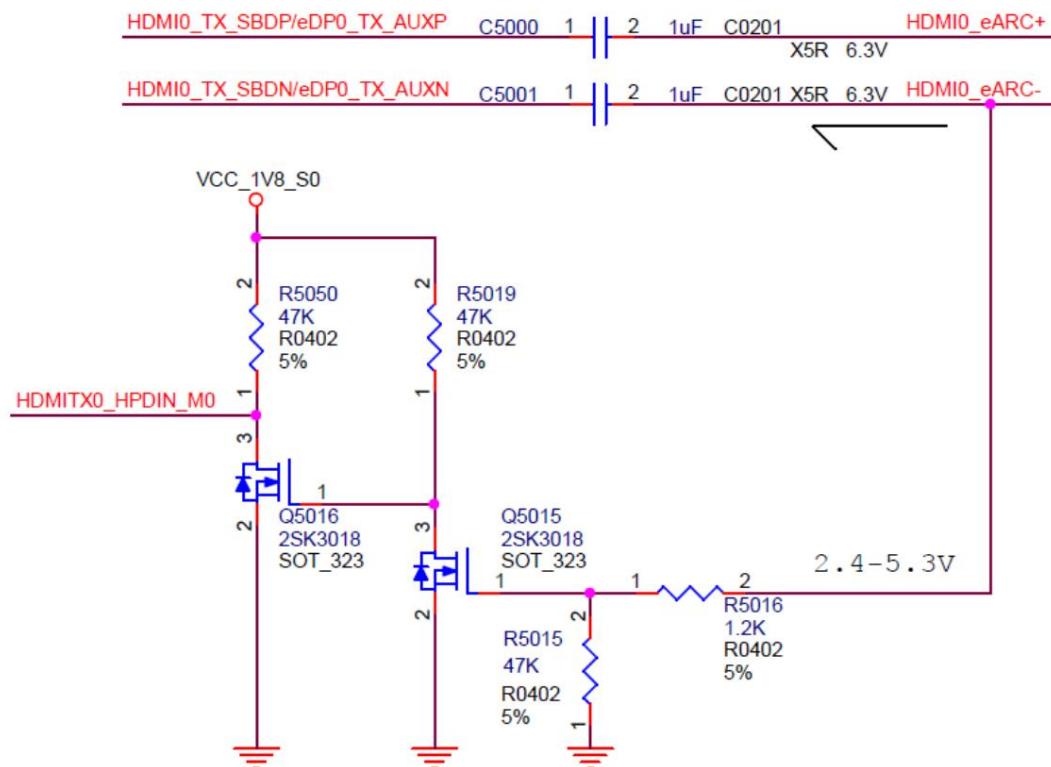


Figure 2-139 RK3588 HDMI TX0 eARC/HPD circuit

HDMI_TX0_HPD is the HDMI TX controller multiplexed to the normal GPIO function, the level depends on the power domain voltage, power domain power supply

If the voltage changes, the pull-up resistor power supply of the peripheral circuit must also be adjusted synchronously.

HDMI_TX0/1_HPD are multiplexed in two different power domains, one on the IO of VCCIO4 power domain and the other on VCCIO5

Above the IO of the power domain.

VCCIO4 Domain

Operating Voltage=1.8V/3.3V

SATA1_ACT_LED_M1 /	/	/SPI4_MOSI_M2 /PCIE30X1_1_CLKREQN_M2 /DPI_HPDIN_M2	/I2C2_SDA_M4 /UART6_RX_M1 /GPIO1_A0_d	A24
/ PWM0_M2	/SPI4_CLK_M2 /	/VOP_POST_EMPTY /	/I2C4_SDA_M3 /UART6_RTSN_M1 /GPIO1_A1_d	A25
/ PWM1_M2	/SPI4_CS0_M2 /	/HDMI_TX1_SDA_M2 /	/I2C4_SCL_M3 /UART6_CTSN_M1 /GPIO1_A2_d	A26
/	/SPI2_MISO_M0 /	/HDMI_TX1_SCL_M2 /	/	A27
/	/SPI2_MOSI_M0	/HDMI_RX0_HPD_M0 /	/	B25
/	/SPI2_CLK_M0 /	/HDMI_RX1_HPD_M0 /	/	B26
/	/	/	/	C24
/ PWM3_IR_M3	/SPI2_CS0_M0 /PCIE30X1_1_PERSTN_M2 /	/PDM1_SDIO_M1 /	/GPIO1_A7_u	C25
/	/SPI2_CS1_M0 /PCIE30X4_CLKREQN_M3 /	/PDM1_SDII_M1 /	/GPIO1_B0_u	C27
/	/SPI0_MISO_M2 /PCIE30X4_WAKEN_M3 /	/PDM1_SDII_M1 /	/GPIO1_B1_d	D25
/	/SPI0_MOSI_M2 /PCIE30X4_PERSTN_M3 /	/PDM1_SDIS_M1 /UART4_RX_M2 /GPIO1_B2_d	D26	
SATA0_ACT_LED_M1 /	/	/SPI0_CLK_M2 /PCIE30X1_0_WAKEN_M2 /	/PDM1_CLK1_M1 /UART4_RX_M2 /GPIO1_B3_d	D27
/	/SPI0_CS0_M2 /PCIE30X1_0_PERSTN_M2 /	/PDM1_CLK0_M1 /UART7_RX_M2 /GPIO1_B4_u	E24	
/	/SPI0_CS1_M2 /PCIE30X1_0_CLKREQN_M2 /	/	/UART7_TX_M2 /GPIO1_B5_u	E25
HDMI_RX_HPDIN_M2 /	/SPDIF0_RX_M0 /PCIE30X2_WAKEN_M3 /	/MIPI_CAMERA1_CLK_M0 /I2C8_SCL_M3 /UART1_RX_M1 /GPIO1_B6_u	E26	
SATA2_ACT_LED_M1 / HDMI_RX_CEC_M2 / PWM13_M2	/SPDIF1_RX_M0 /PCIE30X2_PERSTN_M3 /	/MIPI_CAMERA2_CLK_M0 /I2C8_SDA_M3 /UART1_RTSN_M1 /GPIO1_B7_u	E27	
HDMI_RX_SCL_M2 / PWM14_M2 /	/	/MIPI_CAMERA3_CLK_M0 /I2C8_SCL_M2 /UART1_RTSN_M1 /GPIO1_D6_u	F24	
HDMI_RX_SDA_M2 / PWM15_IR_M3 /	/	/PCIE30X2_CLKREQN_M3 /MIPI_CAMERA4_CLK_M0 /I2C8_SDA_M2 /UART1_CTSN_M1 /GPIO1_D7_u	F25	

Figure 2-140 RK3588 HDMI_TX0/1_HPD M0 functional pin

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

PWM10_M0	/ SPI4_MISO_M1 /	/I2C6_SDA_M4 /FSPI_D0_M2 /I2S8_MCLK	/SDIO_D0_M1 /GNAC1_TxD2 /GPIO3_A0_u	AA29	
AUDDSM_IN	/ SPI4_MOSI_M1 /PWM11_IR_M0 /I2C6_SCL_M4 /FSPI_D1_M2 /I2S8_SCLK	/SDIO_D1_M1 /GNAC1_RXD9 /GPIO3_A1_u	AA30		
AUDDSM_LP	/ SPI4_CLK_M1 /UART8_RX_M1 /	/FSPI_D2_M2 /I2S8_LRCK /SDIO_D2_M1 /GNAC1_RXD2 /GPIO3_A2_u	AD27		
AUDDSM_RN	/ SPI4_CS0_M1 /UART8_RX_M1 /	/FSPI_D3_M2 /I2S8_SDO /SDIO_D3_M1 /GNAC1_RXD3 /GPIO3_A3_u	AE27		
AUDDSM_RP	/ SPI4_CS1_M1 /UART8_RTSN_M1 /	/I2S8_SDI /SDIO_CMD_M1 /GNAC1_RXCLK /GPIO3_A4_d	AD28		
/	/MIPI_CAMERA0_CLK_M1 /UART8_CTSN_M1 /I2C4_SDA_M0 /FSPI_CLK_M2 /	/SDIO_CLK_M1 /GNAC1_RXCLK /GPIO3_A5_d	AH30		
/	/MIPI_CAMERA1_CLK_M1 /	/I2C4_SCL_M0 /	/	ETH1_REFCLKO_25M /GPIO3_A6_d	AH27
PWM8_M0	/MIPI_CAMERA2_CLK_M1 /	/	/	/GNAC1_RXD0 /GPIO3_A7_u	AG29
PWM9_M0	/MIPI_CAMERA3_CLK_M1 /	/	/I2S2_SCLK_RX_M1 /	/GNAC1_RXD1 /GPIO3_B0_u	AG28
PWM2_M1	/MIPI_CAMERA4_CLK_M1 /UART2_RX_M2 /	/	/I2S2_LRCK_RX_M1 /	/GNAC1_RXDV_CRS /GPIO3_B1_d	AH29
PWM3_IR_M1	/	/UART2_RX_M2 /	/I2S2_SDI_M1 /	/GNAC1_RXER /GPIO3_B2_d	AE28
/	/UART2_RTSN /	/	/I2S2_SDO_M1 /	/GNAC1_RXD0 /GPIO3_B3_u	AC28
/	/UART2_CTSN /	/	/I2S2_MCLK_M1 /	/GNAC1_RXD1 /GPIO3_B4_u	AC29
PWM12_M0	/CAN1_RX_M0 /UART3_RX_M1 /	/	/I2S2_SCLK_RX_M1 /	/GNAC1_RXEN /GPIO3_B5_u	AD29
PWM13_M0	/CAN1_RX_M0 /UART3_RX_M1 /	/	/I2S2_LRCK_RX_M1 /	/GNAC1_MCLKINOUT /GPIO3_B6_d	AE29
/	/	/I2C3_SCL_M1 /SPI1_MOSI_M1 /HDMI_TX1_HPD_M1 /	/GNAC1_PTP_REF_CLK /GPIO3_B7_d	AA28	
/	/UART7_RX_M1 /I2C3_SDA_M1 /SPI1_MISO_M1 /	/	/	/GNAC1_PPSTIRG /GPIO3_C0_d	Y29
/ PCIE30X2_BUTTON_RSTN	/UART7_RX_M1 /	/SPI1_CLK_M1 /	/	/GNAC1_PPCLK /GPIO3_C1_d	Y27
PWM14_M0	/	/UART7_RTSN_M1 /I2C8_SCL_M4 /SPI1_CS0_M1 /	/MIPI_TE0 /GNAC1_MDC /GPIO3_C2_d	Y31	
PWM15_IR_M0	/	/UART7_CTSN_M1 /I2C8_SDA_M4 /SPI1_CS1_M1 /	/MIPI_TE1 /GNAC1_MDIO /GPIO3_C3_d	Y30	
CAN2_RX_M0	/PCIE30X4_CLKREQN_M2 /UART5_RX_M1 /FSPI_CS0N_M2 /SPI1_CS0_M3 /HDMI_TX1_CEC_M2 /	/	/CIF_D8 /GPIO3_C4_u	AH26	
CAN2_TX_M0	/PCIE30X4_WAKEN_M2 /UART5_RX_M1 /FSPI_CS1N_M2 /SPI1_CS1_M3 /HDMI_TX1_SDA_M1 /	/	/CIF_D9 /GPIO3_C5_u	AH25	
/PCIE30X4_PERSTN_M2 /	/	/SPI1_MISO_M3 /HDMI_TX1_SCL_M1 /	/CIF_D10 /GPIO3_C6_u	AG26	
/PCIE20X1_2_CLKREQN_M0 /	/I2C5_SCL_M0 /SPI1_MOSI_M3 /HDMI_RX_SCL_M2 /	/CIF_D11 /GPIO3_C7_u	AJ24		
PWM8_M2	/PCIE20X1_2_WAKEN_M0 /UART4_RX_M1 /I2C5_SDA_M0 /SPI1_CLK_M3 /HDMI_RX_SDA_M2 /	/	/CIF_D12 /GPIO3_D0_u	AH24	
PWM9_M2	/PCIE20X1_2_PERSTN_M0 /UART4_RX_M1 /	/SPI0_MISO_M3 /HDMI_RX_CEC_M1 /	/CIF_D13 /GPIO3_D1_d	AG23	
/PCIE30X2_CLKREQN_M2 /UART5_RTSN_M2 /I2C7_SCL_M2 /SPI0_MOSI_M3 /HDMI_RX_SCL_M1 /	/	/CIF_D14 /GPIO3_D2_d	AG25		
PWM10_M2	/PCIE30X2_WAKEN_M2 /UART5_CTSN_M2 /I2C7_SDA_M2 /SPI0_CLK_M3 /HDMI_RX_SDA_M1 /	/	/CIF_D15 /GPIO3_D3_d	AG24	
/PCIE30X2_PERSTN_M2 /UART9_RX_M2 /	/SPI0_CS0_M3 /HDMI_RX_HPDIN_M1 /HDMI_TX0_HPD_M1 /MCU_JTAG_TCK_M1 /GPIO3_D4_d	/	AA27		
PWM11_IR_M3	/PCIE30X4_BUTTON_RSTN /UART5_RX_M2 /	/SPI0_CS1_M3 /DPI_HPDIN_M0 /	/MCU_JTAG_TMS_M1 /GPIO3_D5_d	AB28	

Figure 2-141 RK3588 HDMI_TX0/1_HPD M1 functional pin

HDMI_TX0_CEC is the HDMI controller CEC function multiplexed to the common GPIO function, the level depends on the power domain voltage, power

If the domain power supply voltage changes, the pull-up resistor power supply of the peripheral circuit must also be adjusted synchronously.

HDMI_TX0_CEC multiplexes two locations, one on the IO of VCCIO6 power domain and one on the IO of PMUIO2 power domain.

IO above.

HDMI_TX1_CEC multiplexes three locations, one on the IO of the VCCIO3 power domain, one on the PMUIO2 power domain

IO, and one IO in the VCCIO5 power domain.

VCCIO6 Domain	
Operating Voltage=1.8V/3.3V	
/ SPI0_MISO_M1	/ UART5_RTSN_M1 /
/ SPI0_MOSI_M1	/ UART9_CTSN_M1 /
/ SPI0_CLK_M1	/
/	UART0_RX_M2 /
/ SPI2_MISO_M1	/ UART0_RX_M2 / I2C3_SCL_M2
/ SPI2_MOSI_M1	/ UART3_RX_M2 / I2C3_SDA_M2
/ SPI2_CLK_M1	/ UART3_RX_M2 / I2C5_SCL_M2
/ SPI2_CS0_M1	/
/ SPI2_CS1_M1	/ UART8_RX_M0 / I2C6_SDA_M3
SATA1_ACT_LED_M0	/ SPDIF1_RX_M1 / SPI0_CS1_M1
CAN1_RX_M1	/ PWM14_M1 / SPI0_CS0_M1
CAN1_TX_M1	/ PWM15_IR_M1 /
SPDIF0_RX_M1	/ PWM11_IR_M1 / DPO_HPDIN_M0
SATA1_ACT_LED_M0	/ PWM12_M1 / SPI3_MISO_M1
SATA1_ACT_LED_M0	/ PWM13_M1 / SPI3_MOSI_M1
/	/ SPI3_CLK_M1 /
/	/ I2C3_SDA_M1 /
SPDIF1_RX_M0	/ PWM6_M1 / SPI3_CS1_M1 /
	/ I2C8_SDA_M3 /
	/ HDMI_TX0_CEC_M0 /
	/ PCIE30X1_0_BUTTON_RSTN /
	/ PCIE30X1_1_BUTTON_RSTN / BT1120_D8
	/ PCIE30X1_2_BUTTON_RSTN / BT1120_D9
	/ PCIE30X4_CLREQN_M1 / BT1120_D10
	/ PCIE30X4_WAKEN_M1 / BT1120_D11
	/ PCIE30X4_WAKEN_M1 / BT1120_D12
	/ PCIE30X1_2_WAKEN_M1 / BT1120_D13
	/ PCIE30X1_2_WAKEN_M1 / BT1120_D14
	/ PCIE30X1_2_WAKEN_M1 / BT1120_D15
	/ MIPI_CAMERA0_CLK_M0 / GPIO4_B1_u
	/ CIP_HREF / GPIO4_B2_u
	/ CIP_VSYNC / GPIO4_B3_u
	/ CIP_CLKOUT / GPIO4_B4_u
	/ CIP_HREF / GPIO4_B5_d
	/ CIP_HREF / GPIO4_B6_d
	/ CIP_HREF / GPIO4_B7_u
	/ CIP_HREF / GPIO4_C0_u
	/ CIP_HREF / GPIO4_C1_d

Figure 2-142 RK3588 HDMI_TX0_CEC M0 function pin

VCCIO3 Domain	
Operating Voltage=1.8V	
/ UART6_RX_M0	/ FSPI_D0_M1 / SDIO_D0_M0 / GMAC0_RXD2 / GPIO2_A6_u
/ UART6_TX_M0	/ FSPI_D1_M1 / SDIO_D1_M0 / GMAC0_RXD3 / GPIO2_A7_u
I2C8_SCL_M1	/ UART6_RTSN_M0 / FSPI_D2_M1 / SDIO_D2_M0 / GMAC0_RXCLK / GPIO2_B0_u
I2C8_SDA_M1	/ UART6_CTSN_M0 / FSPI_D3_M1 / SDIO_D3_M0 / GMAC0_RXD2 / GPIO2_B1_u
I2C3_SCL_M3	/
I2C3_SDA_M3	/ FSPI_CLK_M1 / SDIO_CLK_M0 / GMAC0_TXCLK / GPIO2_B3_d
I2C3_SDA_M1	/ UART7_RX_M0 / FSPI_CS0_M1 / HDMI_TX1_SDA_M0 / GMAC0_PTP_REFCLK / GPIO2_B4_u
I2C4_SCL_M1	/ UART7_TX_M0 / FSPI_CS1_M1 / HDMI_TX1_SCL_M0 / GMAC0_PPSTRTG / GPIO2_B5_u
I2C5_SCL_M4	/ UART1_RX_M0 /
I2C5_SDA_M4	/ UART1_TX_M0 / I2S2_MCLK_M0 / GMAC0_RXDO / GPIO2_B6_d
I2C2_SDA_M1	/ UART1_RTSN_M0 / SPI1_CLK_M0 / I2S2_LRCK_RX_M0 / GMAC0_TXEN / GPIO2_C0_d
I2C2_SCL_M1	/ UART1_CTSN_M0 / SPI1_MISO_M0 / I2S2_SCLK_RX_M0 / GMAC0_RXDO / GPIO2_C1_d
I2C6_SDA_M2	/ UART9_RX_M0 / SPI1_MOSI_M0 / I2S2_LRCK_TX_M0 / GMAC0_RXDI / GPIO2_C2_d
I2C6_SCL_M2	/ SPI1_CS0_M0 / I2S2_SDI_M0 / ETH0_REFCLK_25M / GMAC0_RXDO / GPIO2_C3_d
TEST_CLKOUT_M1	/ UART9_RX_M0 / SPI1_CS1_M0 / HDMI_TX1_CEC_M0 / GMAC0_PPCLK / GPIO2_C4_d
	/ CLK32K_OUT1 / GPIO2_C5_d
I2C7_SCL_M1	/ UART7_RTSN_M0 / SPI3_CS0_M0 / PWM2_M2 / GMAC0_RXDV_CRS / GPIO4_C2_d
I2C7_SDA_M1	/ UART7_RTSN_M0 / SPI3_CS1_M0 / I2S2_SDO_M0 / GMAC0_MCLKINOUT / GPIO4_C3_d
I2C7_SDA_M1	/ UART7_RTSN_M0 / SPI3_MISO_M0 / PWM5_M2 / GMAC0_MDC / GPIO4_C4_d
I2C0_SCL_M1	/ UART9_CTSN_M0 / SPI3_MOSI_M0 / PWM6_M2 / GMAC0_MDIO / GPIO4_C5_d
I2C0_SDA_M1	/ UART7_CTSN_M0 / SPI3_CLK_M0 / PWM7_IR_M3 / GMAC0_RXER / GPIO4_C6_d
	Y26
	VCCIO3_1V8

Figure 2-143 RK3588 HDMI_TX1_CEC M0 function pin

PMUIO2 Domain											
Operating Voltage=1.8V/3.3V											
/UART1_RX_M0 /	/	/	/ISI1_MCLK_M1 /	/PCIE30X1_1_CLKREQN_M0 /	/	/ISCI1_SCL_M0 /	/JTAG_TCK_M2	/GPIO0_B5_d	P29		
/UART1_RX_M0 /	/	/	/ISI1_SCLK_RX_M1 /	/PCIE30X1_1_WAKEN_M0 /	/	/ISCI1_SDA_M0 /	/JTAG_TMS_M2	/GPIO0_B6_d	R29		
/	/CAN0_RX_M0 /	/	/ISI1_LRCK_RX_M1 /	/PCIE30X1_1_PERSTN_M0 /	/SPI0_CSI_M0 /	/ISCI2_SCL_M0 /	/PNM0_M0	/GPIO0_B7_d	T28		
/	/CAN0_RX_M0 /	/PEMO_CLK0_M1 /	/ISI1_SCLK_RX_M1 /	/PCIE30X1_0_CLKREQN_M0 /	/SPI0_MOSI_M0 /	/ISCI2_SDA_M0 /	/PNM1_M0	/GPIO0_C0_d	T31		
								/PMIC_SLEEP3	/GPIO0_C1_d	U32	
								/PMIC_SLEEP4	/GPIO0_C2_d	T32	
								/PMIC_SLEEP5	/GPIO0_C3_d	T30	
									/PMIC_SLEEP6	R30	
										P30	
PWM4_M0 /	/UART0_RX_M0 /	/DP1_HPDIN_M1 /	/PEMO_CLK1_M1 /	/ISI1_LRCK_RX_M1 /	/PCIE30X1_0_WAKEN_M0 /	/	/ISCI4_SDA_M0 /	/PNM2_M0	/GPIO0_C4_d	T29	
PWM5_M1 /	/UART0_RX_M0 /	/DP1_HPDIN_M1 /	/ISI1_SDIO_M1 /	/PCIE30X1_0_PERSTN_M0 /	/	/ISCI4_SCL_M0 /	/CPU_AVN	/GPIO0_C5_u	V31		
/UART1_PTSN_M2 /	/	/PEMO_SDIO_M1 /	/ISI1_SDIO_M1 /	/PCIE30X4_CLKREQN_M0 /	/SPI0_CLK_M0 /	/	/NPU_AVN	/GPIO0_C6_u	W31		
/UART1_CTSN_M2 /	/	/PEMO_SDIO_M1 /	/ISI1_SDIO_M1 /	/PCIE30X4_WAKEN_M0 /	/SPI0_MISO_M0 /	/ISCI6_SDA_M0 /	/PNM4_M0	/GPIO0_C7_d	W30		
HDMI_TX0_CEC_M1 /	/UART1_RX_M2 /	/	/HDMI_RX_SCL_M0 /	/ISI1_SDIO_M1 /	/PCIE30X2_CLKREQN_M0 /	/SPI0_CS0_M0 /	/ISCI6_SCL_M0 /	/CPU_BIG0_AVN	/GPIO0_D0_d	W29	
HDMI_TX1_CEC_M1 /	/UART1_RX_M2 /	/	/HDMI_RX_SCL_M0 /	/ISI1_SDIO_M1 /	/PCIE30X2_WAKEN_M0 /	/SPI3_MOSI_M0 /	/ISCI6_SDA_M0 /	/PNM5_IR_M0	/GPIO0_D2_u	U33	
						/SPI3_CLK_M2 /	/	/LTCPU_AVN	/GPIO0_D3_u	V29	
HDMI_TX0_SDA_M1 /	SATA_CPDOT /	/CAN2_RX_M1 /	/PEMO_SDIO_M1 /	/ISI1_SDIO_M1 /	/PCIE30X2_PERSTN_M0 /	/SPI3_CS0_M0 /	/ISCI1_SCL_M0 /	/PNM5_IR_M0	/GPIO0_D4_u	W28	
HDMI_TX0_SCL_M1 /	SATA_MP_SWITCH /	/CAN2_RX_M1 /		/ISI1_SDIO_M1 /			/SPI3_CS1_M2 /	/ISCI1_SDA_M0 /	/CPU_BIG1_AVN	/GPIO0_D5_u	P28
								/PMIC_SLEEP6	/GPIO0_D6_d		

Figure 2-144 RK3588 HDMI_TX0/1_CEC M1 function pin

VCCIO5 Domain									
Operating Voltage=1.8V/3.3V									
PWM10_M0 /	/SPI4_MISO_M1 /	/	/I2C6_SDA_M4 /	/FSPI_D0_M2 /	/I2S3_MCLK /	/SDIO_D0_M1 /	/GNA1_TXD2	/GPIO3_A0_u	AA29
AUDDSM_IN /	/SPI4_MOSI_M1 /	/PWM11_IR_M0 /	/I2C6_SCL_M4 /	/FSPI_D1_M2 /	/I2S3_SCLK /	/SDIO_D1_M1 /	/GNA1_RXD3	/GPIO3_A1_u	AA30
AUDDSM_LP /	/SPI4_CLK_M1 /	/UART8_RX_M1 /	/	/FSPI_D2_M2 /	/I2S3_LRCK /	/SDIO_D2_M1 /	/GNA1_RXD2	/GPIO3_A2_u	AD27
AUDDSM_RN /	/SPI4_CS0_M1 /	/UART8_RX_M1 /	/	/FSPI_D3_M2 /	/I2S3_SDO /	/SDIO_D3_M1 /	/GNA1_RXD3	/GPIO3_A3_u	AE27
AUDDSM_RP /	/SPI4_CS1_M1 /	/UART8_RTSN_M1 /	/	/	/I2S3_SDI /	/SDIO_CMD_M1 /	/GNA1_RXCLK	/GPIO3_A4_d	AD28
/MIPI_CAMERA0_CLK_M1 /	/UART8_CTSN_M1 /	/I2C4_SDA_M0 /	/FSPI_CLK_M2 /	/	/	/SDIO_CLK_M1 /	/GNA1_RXCLK	/GPIO3_A5_d	AH30
/MIPI_CAMERA1_CLK_M1 /	/	/I2C4_SCL_M0 /	/	/	/	/	/ETH1_REFCLK0_28N	/GPIO3_A6_d	AH27
PWM8_M0 /	/MIPI_CAMERA2_CLK_M1 /	/	/	/	/	/	/GNA1_RXD0	/GPIO3_A7_u	AG29
PWM8_M0 /	/MIPI_CAMERA3_CLK_M1 /	/	/	/	/I2S2_SCLK_RX_M1 /	/	/GNA1_RXD1	/GPIO3_B0_u	AG28
PWM2_M1 /	/MIPI_CAMERA4_CLK_M1 /	/UART2_RX_M2 /	/	/	/I2S2_LRCK_RX_M1 /	/	/GNA1_RXDV_CRS	/GPIO3_B1_d	AH29
PWM3_IR_M1 /	/	/UART2_RX_M2 /	/	/	/I2S2_SDI_M1 /	/	/GNA1_RXER	/GPIO3_B2_d	AE28
	/	/UART2_RTSN /	/	/	/I2S2_SDO_M1 /	/	/GNA1_RXD0	/GPIO3_B3_u	AC28
	/	/UART2_CTSN /	/	/	/I2S2_MCLK_M1 /	/	/GNA1_RXD1	/GPIO3_B4_u	AC29
PWM12_M0 /	CAN1_RX_M0 /	/UART3_RX_M1 /	/	/	/I2S2_SCLK_RX_M1 /	/	/GNA1_RXEN	/GPIO3_B5_u	AD29
PWM12_M0 /	CAN1_RX_M0 /	/UART3_RX_M1 /	/	/	/I2S2_LRCK_RX_M1 /	/	/GNA1_RXLINKOUT	/GPIO3_B6_d	AE29
			/I2C3_SCL_M1 /	/SPI1_MOSI_M1 /	/HDMI_TX1_HPD_M1 /	/	/GNA1_PTP_REF_CLK	/GPIO3_B7_d	AA28
			/I2C3_SDA_M1 /	/SPI1_MOSI_M1 /	/HDMI_TX1_MOSI_M1 /	/	/GNA1_PPSTRIG	/GPIO3_C0_d	Y29
			/PCIE30X2_BUTTON_RSTN /	/UART7_RX_M1 /	/SPI1_CLK_M1 /	/	/GNA1_PPCLK	/GPIO3_C1_d	Y27
PWM14_M0 /	/	/UART7_RTSN_M1 /	/I2C6_SCL_M4 /	/SPI1_CS0_M1 /	/	/MIPI_TE0 /	/GNA1_MDC	/GPIO3_C2_d	Y31
PWM15_IR_M0 /	/	/UART7_CTSN_M1 /	/I2C6_SDA_M4 /	/SPI1_CSI_M1 /	/	/MIPI_TE1 /	/GNA1_MDIO	/GPIO3_C3_d	Y30
CAN2_RX_M0 /	/PCIE30X4_CLKREQN_M2 /	/UART5_RX_M1 /	/FSPI_CS0_M2 /	/SPI3_CS0_M3 /	HDMI_TX1_CEC_M2 /	/	/CIF_D8	/GPIO3_C4_u	AH26
CAN2_RX_M0 /	/PCIE30X4_WAKEN_M2 /	/UART5_RX_M1 /	/FSPI_CS1_M2 /	/SPI3_CS1_M3 /	/HDMI_TX1_SDA_M1 /	/	/CIF_D9	/GPIO3_C5_u	AH25
	/PCIE30X4_PERSTN_M2 /	/	/	/SPI3_MISO_M3 /	/HDMI_TX1_SCL_M1 /	/	/CIF_D10	/GPIO3_C6_u	AG26
	/PCIE30X4_CLKREQN_M2 /	/	/I2C5_SCL_M0 /	/SPI3_MOSI_M3 /	/HDMI_TX0_SCL_M2 /	/	/CIF_D11	/GPIO3_C7_u	AJ24
PWM8_M2 /	/PCIE20X1_2_WAKEN_M0 /	/UART4_RX_M1 /	/I2C5_SDA_M0 /	/SPI3_CLK_M3 /	/HDMI_RX_SDA_M2 /	/	/CIF_D12	/GPIO3_D0_u	AH24
PWM8_M2 /	/PCIE20X1_2_PERSTN_M0 /	/UART4_RX_M1 /	/	/SPI0_MISO_M3 /	/HDMI_RX_CEC_M1 /	/	/CIF_D13	/GPIO3_D1_d	AG23
	/PCIE30X2_CLKREQN_M2 /	/UART9_RTSN_M2 /	/I2C7_SCL_M2 /	/SPI0_MOSI_M3 /	/HDMI_RX_SCL_M1 /	/	/CIF_D14	/GPIO3_D2_d	AG25
PWM10_M2 /	/PCIE30X2_WAKEN_M0 /	/UART9_RX_M2 /	/	/SPI0_CLK_M3 /	/HDMI_RX_SDA_M1 /	/	/CIF_D15	/GPIO3_D3_d	AG24
	/PCIE30X2_PERSTN_M2 /	/UART9_RX_M2 /	/	/SPI0_CS0_M3 /	/HDMI_RX_HPD_M1 /	/HDMI_TX0_HPD_M1 /	/MCU_JTAG_TCK_M1	/GPIO3_D4_d	AA27
PWM11_IR_M3 /	/PCIE30X4_BUTTON_RSTN /	/UART9_RX_M2 /	/	/SPI0_CSI_M3 /	/DP1_HPDIN_M0 /	/	/MCU_JTAG_TMS_M1	/GPIO3_D5_d	AB28

Figure 2-145 RK3588 HDMI_TX1_CEC M2 function pin

The CEC protocol specifies a 3.3V level, but the protocol requires that a 3.3V voltage be added to the CEC pin through a 27K resistor, and leakage current is not allowed to exceed

Over 1.8uA.

Test ID 7-15: CEC Line Degradation

Reference	Requirement
[HDMI: Table 4-40] CEC line Electrical Specifications for all Configurations	A device with power removed (from the CEC circuitry) shall not degrade communication between other CEC devices (e.g. the line shall not be pulled down by the powered off device). Maximum CEC line leakage current must be $\leq 1.8\mu A$

Figure 2-146 HDMI CEC protocol requirements

When the RK3588 IO Domain is not powered on, if there is voltage on the IO, the IO will have leakage. For example, if the RK3588 is powered off, then

The HDMI cable is also connected to the Sink end (TV or monitor). At this time, the CEC on the Sink end has power, which will leak to the RK3588 IO through the HDMI cable, causing the CEC leakage to exceed 1.8uA. Therefore, an external isolation circuit is required. The resistance value of R5008 cannot be modified arbitrarily. 27Kohm must be used. The default selection of Q5002 is 2SK3018. If you want to change to other models, the junction capacitance must be equivalent. If the junction capacitance is too large, it will not only affect the work but also fail the certification.

HDMI TX CEC

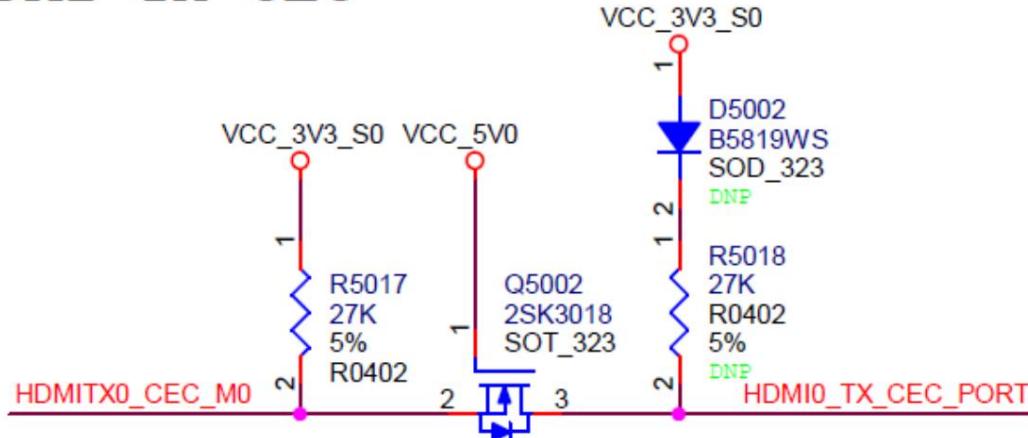


Figure 2-147 HDMI TX CEC isolation circuit

HDMI_TX0/1 DDC_SCL/DDC_SDA is the I2C/DDC bus of HDMI TX0/1 controller, and its function is multiplexed to VCCIO3.

On the IO of VCCIO5 and VCCIO4 power domains, the level varies with the voltage of the power domain. If the power domain voltage changes, the pull-up of the peripheral circuit will be affected.

The resistor power supply must also be adjusted synchronously.

The DDC_SCL/DDC_SDA protocol specifies a 5V level. RK3588 IO does not support 5V level, so a level conversion circuit must be added.

The default MOS transistor level converter is 2SK3018. If you choose a different model, the junction capacitance must be equivalent. Excessively large junction capacitance will not only affect operation but also fail certification. For the pull-up resistor, it is recommended to use the default value

and do not modify it.

The D5000 diode must not be deleted. It is used to prevent the Sink terminal from leaking to VCC_5V0.

The SDA signal level conversion MOS gate and power supply are connected in series with a 1K resistor. The old version has a 100pF capacitor connected between the MOS gate and source.

Timing, cannot be deleted.

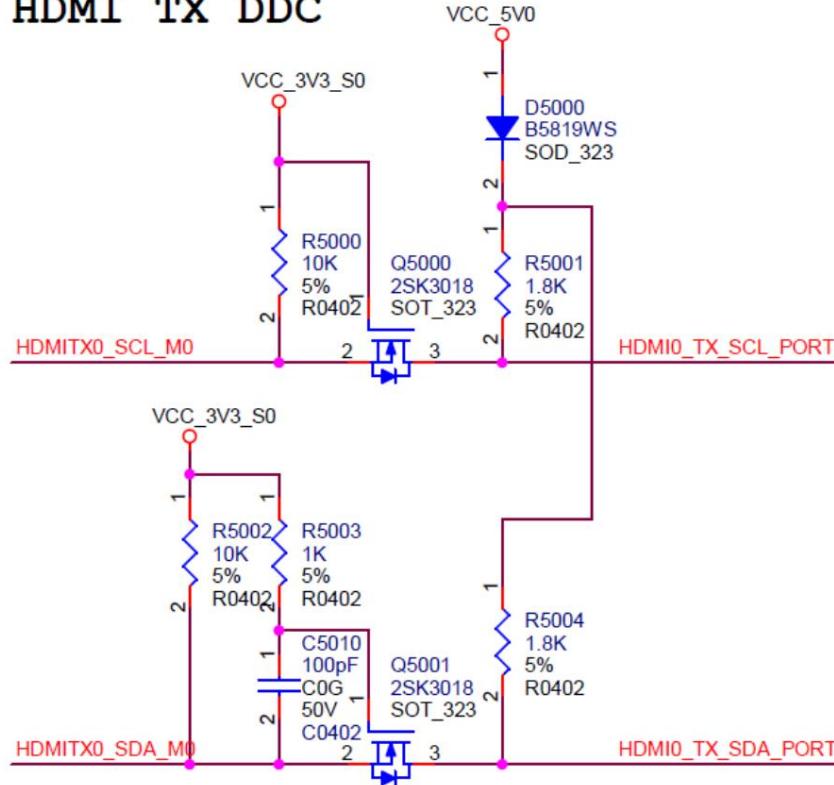
HDMI TX DDC

Figure 2-148 HDMI TX DDC level conversion circuit

The voltage of Pin18 of HDMI socket should be kept between 4.8-5.3V, and 1uF decoupling capacitor should be placed on the pin. It should not be deleted.

Placed near the HDMI connector pins.

To enhance the anti-static capability, ESD devices must be reserved for the signal. The ESD parasitic capacitance of the HDMI2.1 signal must not exceed 0.2pF.

It is recommended that the ESD parasitic capacitance of other signals should not exceed 1pF.

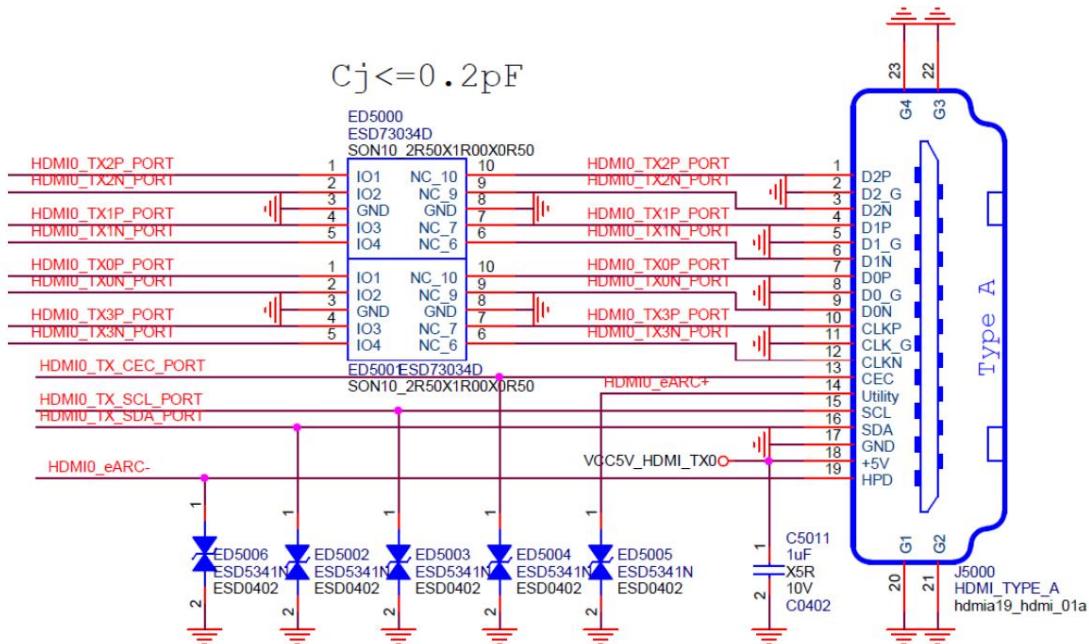


Figure 2-149 HDMI TX connector ESD circuit

The following table shows the recommended HDMI TX interface matching design.

Table 2-27 RK3588 HDMI TX port design

Signal	Connection method	illustrate
HDMI_TX0_D0P/D0N series 220nF capacitor (0201 package), 499ohm resistor to ground RFL mode Lane0/TMDS data Lane0 output		
HDMI_TX0_D1P/D1N series 220nF capacitor (0201 package), 499ohm resistor to ground RFL mode Lane1/TMDS data Lane1 output		
HDMI_TX0_D2P/D2N: 220nF capacitor in series (0201 package), 499ohm resistor to ground RFL mode Lane 2/TMDS data Lane 2 output		
HDMI_TX0_D3P/D3N: 220nF capacitor in series (0201 package), 499ohm resistor to ground RFL mode Lane3/TMDS clock output		
HDMI_TX0_SBDP/SBDN series with a 1uF capacitor (0201 package)		ARC/eARC channel
HDMI/EDP_TX0_REXT 8200 ohm 1% resistor to ground		External reference resistor for HDMI/EDP_TX0 PHY
HDMI_TX0_HPD	Transistor conversion	HDMI insertion detection
HDMI_TX0_CEC	MOS Isolation Conversion	HDMI CEC signal
HDMI_TX0_SCL	MOS level shifter	HDMI DDC Clock
HDMI_TX0_SDA	MOS level shifter	HDMI DDC data input and output
HDMI_TX1_D0P/D0N series 220nF capacitor (0201 package), 499ohm resistor to ground RFL mode Lane0/TMDS data Lane0 output		
HDMI_TX1_D1P/D1N 220nF capacitor in series (0201 package), 499ohm resistor to ground RFL mode Lane 1/TMDS data Lane 1 output		
HDMI_TX1_D2P/D2N: 220nF capacitor in series (0201 package), 499ohm resistor to ground RFL mode Lane2/TMDS data Lane2 output		
HDMI_TX1_D3P/D3N: 220nF capacitor in series (0201 package), 499ohm resistor to ground RFL mode Lane3/TMDS clock output		
HDMI_TX1_SBDP/SBDN series with a 1uF capacitor (0201 package)		ARC/eARC channel
HDMI/EDP_TX1_REXT 8200 ohm 1% resistor to ground		External reference resistor for HDMI/EDP_TX1 PHY
HDMI_TX1_HPD	Transistor conversion	HDMI insertion detection
HDMI_TX1_CEC	MOS Isolation Conversion	HDMI CEC signal
HDMI_TX1_SCL	MOS level shifter	HDMI DDC Clock
HDMI_TX1_SDA	MOS level shifter	HDMI DDC data input and output

ÿ eDP TX mode

Supports eDP V1.3 version, a total of 4 Lanes, eDP TX maximum output resolution up to 4K@60Hz

- ÿ Each lane can support 1.62/2.7/5.4Gbps rate;
- ÿ Support 1Lane, 2Lane or 4Lane mode;
- ÿ Support AUX channel with a rate of up to 1Mbps.

Taking eDP TX0 as an example, eDP TX1 is the same as eDP TX0.

eDP_TX0_D0P/DON, eDP_TX0_D1P/D1N, eDP_TX0_D2P/D2N, eDP_TX0_D3P/D3N need to be connected in series with a 220nF

AC coupling capacitors, it is recommended to use 0201 package, which has lower ESR and ESL, and can also reduce the impedance change on the line.

When the board is in use, place it close to the RK3588 pins.

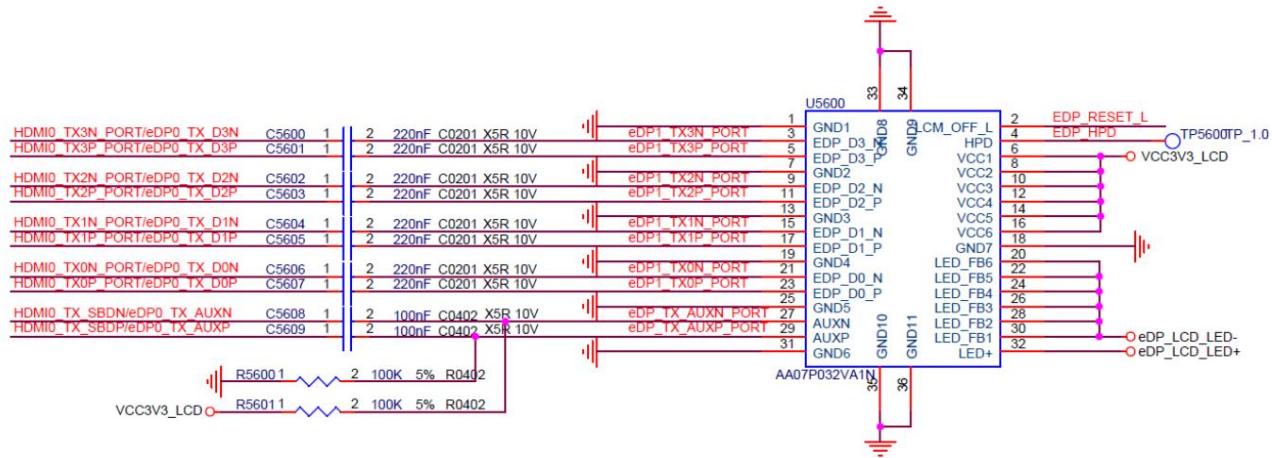


Figure 2-150 RK3588 eDP TX0 signal AC coupling capacitor

eDP_TX0_AUXP/AUXN requires a 100nF AC coupling capacitor to be connected in series close to the interface end, and AUXP needs to reserve a 100Kohm capacitor to ground.

AUXN is reserved for a 100K resistor to pull up to 3.3V.

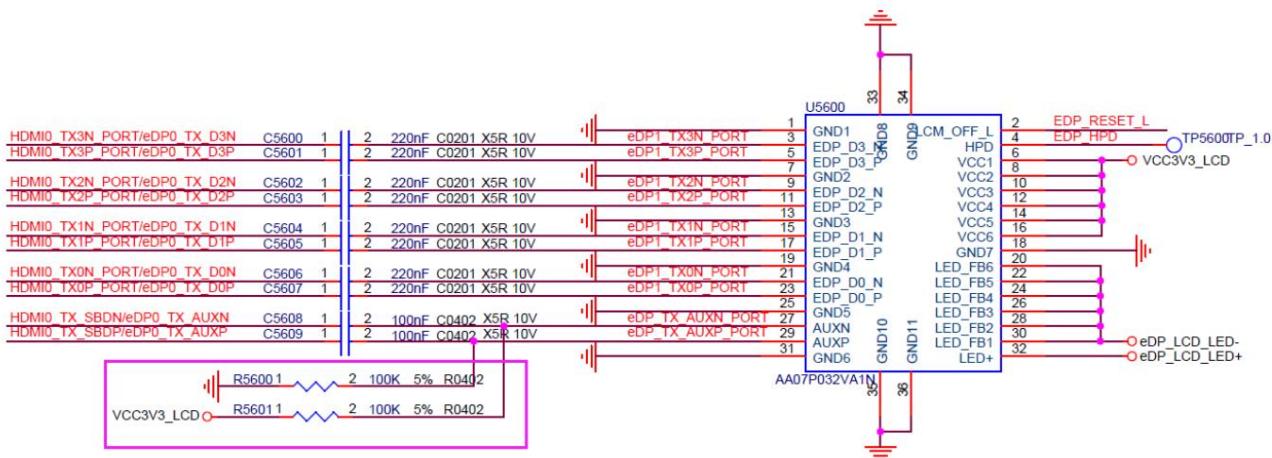


Figure 2-151 RK3588 eDP TX0 AUX signal AC coupling capacitor

The following table shows the recommended matching design for the eDP TX0/1 PHY interface:

Table 2-28 RK3588 eDP TX0/1 PHY interface design

Signal	Connection method	illustrate
eDP_TX0_D0P/D0N	Connect a 220nF capacitor in series (0201 package recommended) eDP data Lane 0 output	
eDP_TX0_D1P/D1N	Connect a 220nF capacitor in series (0201 package recommended) eDP data Lane 1 output	
eDP_TX0_D2P/D2N	Connect a 220nF capacitor in series (0201 package recommended) eDP data Lane 2 output	
eDP_TX0_D3P/D3N	Connect a 220nF capacitor in series (0201 package recommended) eDP data Lane 3 output	
eDP_TX0_AUXP/AUXN	Connect a 100nF capacitor in series	eDP AUX channel
eDP_TX1_D0P/D0N	Connect a 220nF capacitor in series (0201 package recommended) eDP data Lane 0 output	
eDP_TX1_D1P/D1N	Connect a 220nF capacitor in series (0201 package recommended) eDP data Lane 1 output	
eDP_TX1_D2P/D2N	Connect a 220nF capacitor in series (0201 package recommended) eDP data Lane 2 output	
eDP_TX1_D3P/D3N	Connect a 220nF capacitor in series (0201 package recommended) eDP data Lane 3 output	

Signal	Connection method	illustrate
eDP_TX1_AUXP/AUXN	Connect a 100nF capacitor in series	eDP AUX channel

2.3.8.2 MIPI_D/CPHY_TX Interface

RK3588 has two MIPI D-PHY/C-PHY Combo PHY TXs:

- ÿ D-PHY supports version V2.0, D-PHY mode has 0/1/2/3 Lane, and the maximum data transmission rate is 4.5Gbps;
- ÿ C-PHY supports V1.1 version. C-PHY mode has 0/1/2 Trio. Each Trio has 3 lines A/B/C. The maximum data transmission rate is 5.7Gbps/Trioÿ2.5Gbpsÿ

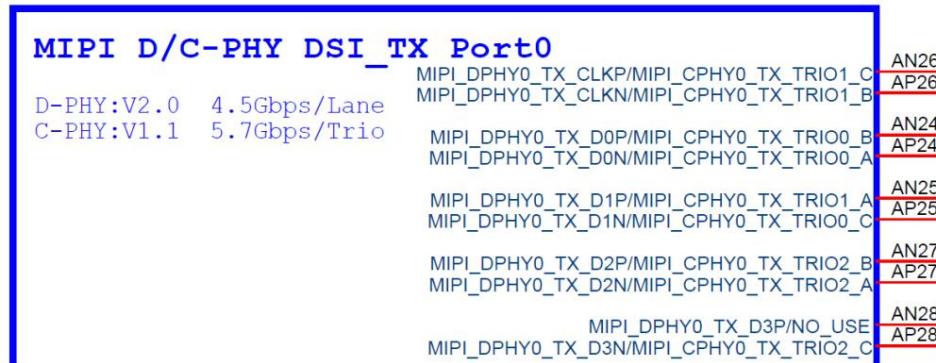


Figure 2-152 RK3588 MIPI D/C-PHY0 TX signal pin

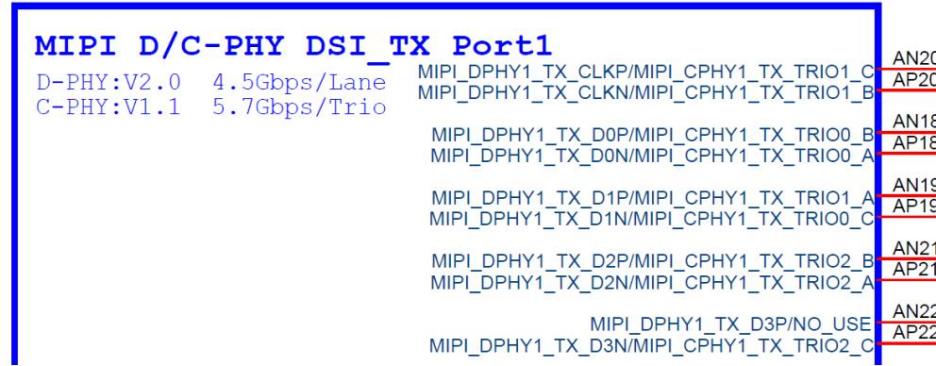


Figure 2-153 RK3588 MIPI D/C-PHY1 TX signal pin

DPHY and CPHY configuration support:

- ÿ MIPI D-PHY/C-PHY Combo PHY0 TX and RX can only be configured as DPHY0 TX, DPHY0 RX mode at the same time.
mode, or configured as CPHY0 TX, CPHY0 RX mode at the same time. It does not support one configured as DPHY0 TX and one configured as CPHY0 RX
- ÿ MIPI D-PHY/C-PHY Combo PHY1 TX and RX can only be configured as DPHY1 TX, DPHY1 RX mode at the same time.
mode, or configured as CPHY1 TX, CPHY1 RX mode at the same time. It does not support one configured as DPHY1 TX and one configured as CPHY1 RX

MIPI D/C-PHY0 mode support when working in D-PHY:

- ÿ Support x4Lane mode, MIPI_DPHY0_TX_D[3:0] data refers to MIPI_DPHY0_TX_CLK.

MIPI D/C-PHY0 mode support when working in C-PHY:

Support 0/1/2 Trio, each Trio A/B/C 3 lines, MIPI_CPHY0_TX_TRIO[2:0]_A,

MIPI_CPHY0_TX_TRIO[2:0]_B, MIPI_CPHY0_TX_TRIO[2:0]_C

MIPI D/C-PHY1 mode support when working in D-PHY:

Supports x4Lane mode. MIPI_DPHY1_TX_D[3:0] data refers to MIPI_DPHY1_TX_CLK.

MIPI D/C-PHY1 mode support when working in C-PHY:

Support 0/1/2 Trio, each Trio A/B/C 3 lines, MIPI_CPHY1_TX_TRIO[2:0]_A,

MIPI_CPHY1_TX_TRIO[2:0]_B, MIPI_CPHY1_TX_TRIO[2:0]_C.

Please note the following when designing MIPI D-PHY/C-PHY Combo PHY0/1 TX:

To improve the MIPI D-PHY/C-PHY Combo PHY0/1 RX performance, the decoupling capacitors of each PHY power supply must not be removed. Place them close to the pins during layout (RX and TX are Combo PHYs and share the same power supply).

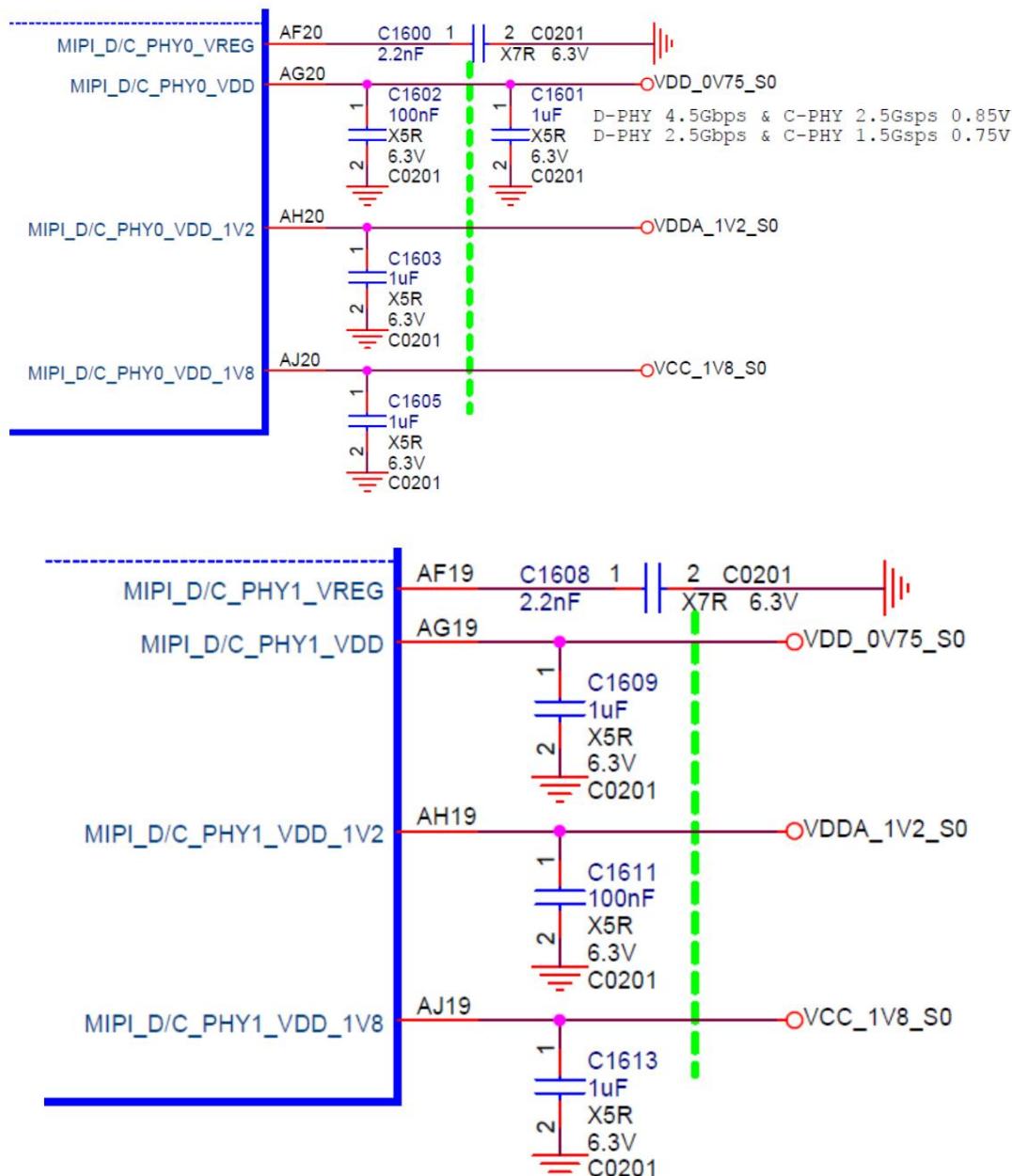


Figure 2-154 MIPI D-PHY/C-PHY Combo PHY0/1 TX power supply decoupling capacitor

ÿ MIPI D-PHY/C-PHY Combo PHY0/1 TX matching design recommendations are shown in the following table:

Table 2-29 RK3588 MIPI D-PHY/C-PHY Combo PHY0/1 TX interface design

Signal	Connection method	illustrate
MIPI_DPHY0_TX_D0P/D0N	Direct connection, to suppress electromagnetic radiation, reserve common mode inductor MIPI_DPHY0_TX data Lane0 output	
MIPI_DPHY0_TX_D1P/D1N	Direct connection, to suppress electromagnetic radiation, reserve common mode inductor MIPI_DPHY0_TX data Lane 1 output	
MIPI_DPHY0_TX_D2P/D2N	Direct connection, to suppress electromagnetic radiation, reserve common mode inductor MIPI_DPHY0_TX data Lane 2 output	
MIPI_DPHY0_TX_D3P/D3N	Direct connection, to suppress electromagnetic radiation, reserve common mode inductor MIPI_DPHY0_TX data Lane3 output	
PUBLIC_DPHY0_TX_CLKP/CLKN	Direct connection, to suppress electromagnetic radiation, reserve common mode inductor MIPI_DPHY0_TX clock output	
MIPI_CPHY0_TX_TRI00_A/B/C	are directly connected. To suppress electromagnetic radiation, a common mode inductor is reserved for MIPI_CPHY0_TX_TRI00 output.	
MIPI_CPHY0_TX_TRI01_A/B/C	are directly connected. To suppress electromagnetic radiation, a common-mode inductor is reserved for MIPI_CPHY0_TX_TRI01 output.	
MIPI_CPHY0_TX_TRI02_A/B/C	are directly connected. To suppress electromagnetic radiation, a common-mode inductor is reserved for MIPI_CPHY0_TX_TRI02 output.	
MIPI_DPHY1_TX_D0P/D0N	Direct connection, to suppress electromagnetic radiation, reserve common mode inductor MIPI_DPHY1_TX data Lane0 output	
MIPI_DPHY1_TX_D1P/D1N	Direct connection, to suppress electromagnetic radiation, reserve common mode inductor MIPI_DPHY1_TX data Lane 1 output	
MIPI_DPHY1_TX_D2P/D2N	Direct connection, to suppress electromagnetic radiation, reserve common mode inductor MIPI_DPHY1_TX data Lane 2 output	
MIPI_DPHY1_TX_D3P/D3N	Direct connection, to suppress electromagnetic radiation, reserve common mode inductor MIPI_DPHY1_TX data Lane3 output	
PUBLIC_DPHY1_TX_CLKP/CLKN	Direct connection, to suppress electromagnetic radiation, reserve common mode inductor MIPI_DPHY1_TX clock output	
MIPI_CPHY1_TX_TRI00_A/B/C	are directly connected. To suppress electromagnetic radiation, a common-mode inductor is reserved for MIPI_CPHY1_TX_TRI00 output.	
MIPI_CPHY1_TX_TRI01_A/B/C	are directly connected. To suppress electromagnetic radiation, a common-mode inductor is reserved for MIPI_CPHY1_TX_TRI01 output.	
MIPI_CPHY1_TX_TRI02_A/B/C	are directly connected. To suppress electromagnetic radiation, a common-mode inductor is reserved for MIPI_CPHY1_TX_TRI02 output.	

2.3.8.3 DP TX Interface

RK3588 supports two DP1.4 TX PHYs (and USB3.0 Combo), with a maximum output resolution of 8K@30Hz

- ÿ Each lane can support 1.62/2.7G/5.4/8.1Gbps rate;
- ÿ Support 1Lane, 2Lane or 4Lane mode;
- ÿ Support RGB/YUV (Up to 10bit) format;
- ÿ Support Single Stream Transport (SST).

USB3.0 OTG/DP1.4 Alt of TYPEC0

USB:U3/Gen1----Controller0
DP:RBR/HBR/HBR2/HBR3

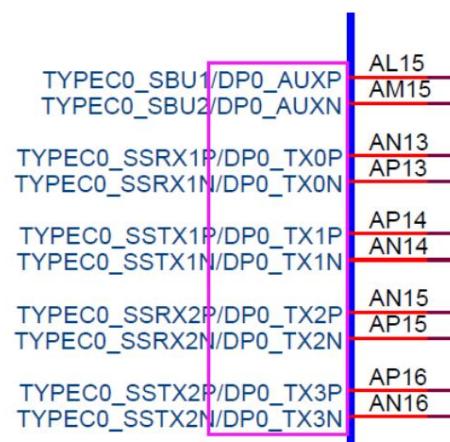


Figure 2-155 RK3588 DP0 TX pin

USB3.0 OTG/DP1.4 Alt of TYPEC1

USB:U3/Gen1----Controller1
DP:RBR/HBR/HBR2/HBR3

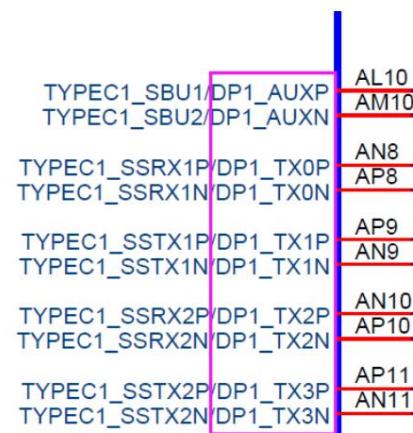


Figure 2-156 RK3588 DP1 TX pin

Note the following when designing DP0/1 TX PHY:

ÿ To improve the performance of DP0/1 TX PHY, the decoupling capacitors of each PHY power supply must not be removed and should be placed close to the pins during layout.

TYPEC0_DP0_VDD_0V85, TYPEC0_DP0_VDDA_0V85, TYPEC0_DP0_VDDH_1V8 these three power supplies

Even if the TYPEC0 function is not used, it must be powered;

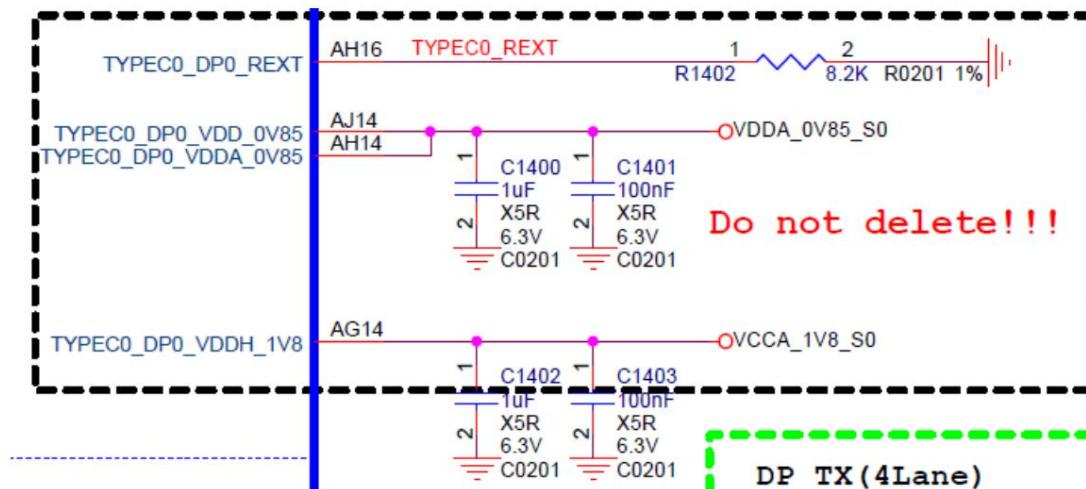


Figure 2-157 RK3588 DP0 TX PHY power decoupling capacitor

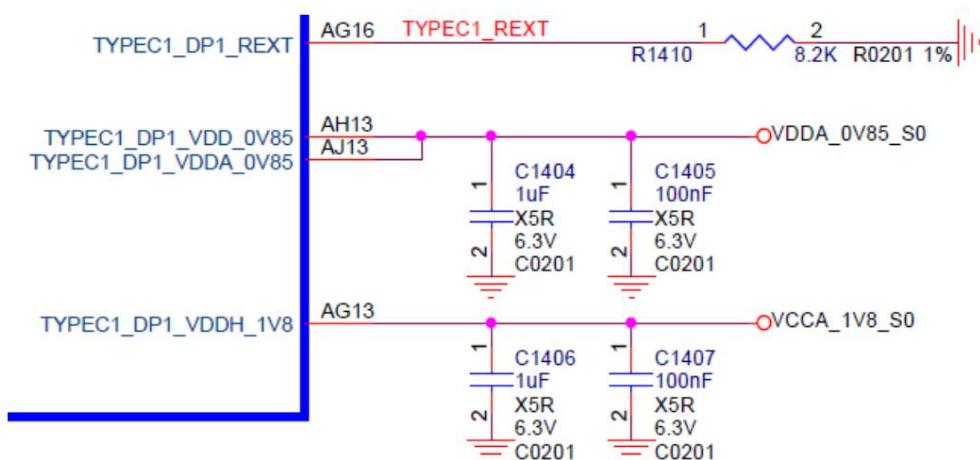


Figure 2-158 RK3588 DP1 TX PHY power decoupling capacitor

DP0_TX_D0P/DON, DP0_TX_D1P/D1N, DP0_TX_D2P/D2N, and DP0_TX_D3P/D3N require 100nF AC coupling capacitors in series. It is recommended to use 0201 packages for AC coupling capacitors, which have lower ESR and ESL and can also reduce impedance changes on the line. During layout, place them close to the RK3588 pins.

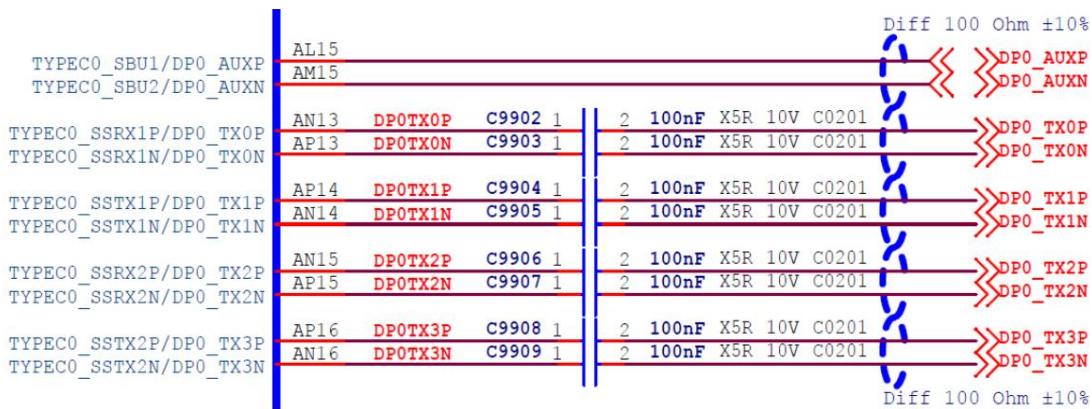


Figure 2-159 RK3588 DP0 TX signal AC coupling capacitor

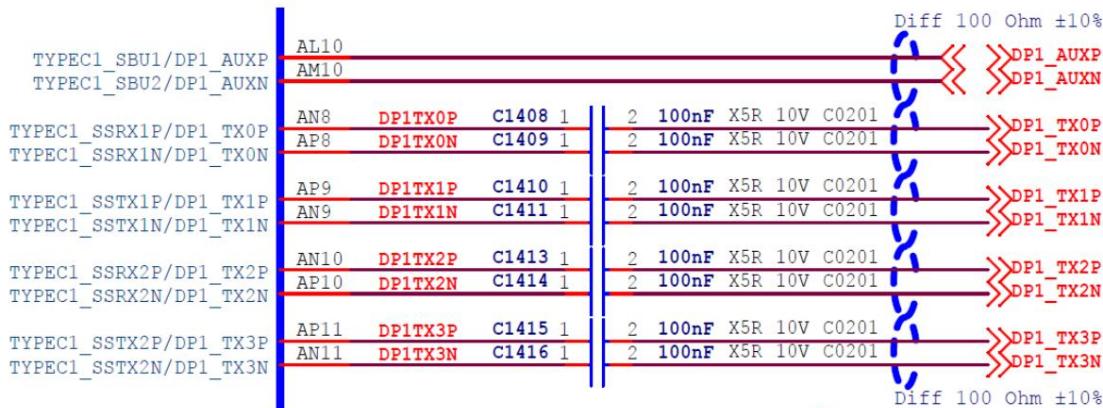


Figure 2-160 RK3588 DP1 TX signal AC coupling capacitor

TYPEC0_DP0_REXT and TYPEC1_DP1_REXT are the external reference resistor pins for USB DP Combo PHY0/1. Connect an 8200-ohm 1% resistor to ground. Do not change the resistor value. Place them close to the RK3588 chip pins during layout. The resistor for the TYPEC0_DP0_REXT pin must be connected even if the TYPEC0 function is not used.



Figure 2-161 RK3588 DP0_TX_REXT pin



Figure 2-162 RK3588 DP1_TX_REXT pin

The DP0/1 TX PHY interface matching design recommendations are shown in the following table:

Table 2-30 RK3588 DP0/1 TX PHY interface design

Signal	Connection method	illustrate
DP0_TX_D0P/D0N	Connect a 100nF capacitor in series (0201 package recommended) DP0 data Lane 0 output	
DP0_TX_D1P/D1N	Connect a 100nF capacitor in series (0201 package recommended) DP0 data Lane 1 output	
DP0_TX_D2P/D2N	Connect a 100nF capacitor in series (0201 package recommended) DP0 data Lane 2 output	
DP0_TX_D3P/D3N	Connect a 100nF capacitor in series (0201 package recommended) DP0 data Lane 3 output	
DP0_TX_AUXP/AUXN	Connect a 100nF capacitor in series	DP0 AUX channel
TYPEC0_DP0_REXT	8200 ohm 1% resistor to ground	External reference resistor for USB/DP0 PHY
DP1_TX_D0P/D0N	Connect a 100nF capacitor in series (0201 package recommended) DP1 Data Lane 0 output	
DP1_TX_D1P/D1N	Connect a 100nF capacitor in series (0201 package recommended) DP1 Data Lane 1 output	
DP1_TX_D2P/D2N	Connect a 100nF capacitor in series (0201 package recommended) DP1 Data Lane 2 output	
DP1_TX_D3P/D3N	Connect a 100nF capacitor in series (0201 package recommended) DP1 data Lane 3 output	
DP1_TX_AUXP/AUXN	Connect a 100nF capacitor in series	DP1 AUX channel
TYPEC1_DP1_REXT	8200 ohm 1% resistor to ground	External reference resistor for USB/DP1 PHY

2.3.8.4 BT1120 TX Interface

RK3588 supports 16-bit BT1120 output interface, with a maximum output resolution of 1920X1080@60Hz; compatible with 8-bit BT656 interface,

Supports PAL and NTSC.



Figure 2-163 RK3588 VOP BT1120 functional pins

The multiplexing relationship between BT1120 and BT656 is shown in the following table:

Table 2-31 RK3588 BT1120 and BT656 relationship table

Pin Name	BT656(8bit)	BT1120(16bit)
BT1120_CLKOUT	CLKOUT	CLKOUT
BT1120_D15		D15
BT1120_D14		D14
BT1120_D13		D13
BT1120_D12		D12
BT1120_D11		D11
BT1120_D10		D10
BT1120_D9		D9
BT1120_D8		D8
BT1120_D7	D7	D7
BT1120_D6	D6	D6
BT1120_D5	D5	D5
BT1120_D4	D4	D4
BT1120_D3	D3	D3
BT1120_D2	D2	D2
BT1120_D1	D1	D1
BT1120_D0	D0	D0

BT1120 output interface data correspondence, supports YC Swap.

Table 2-32 RK3588 BT1120 output format list

Pin Name	Default Mode		Swap Open	
	Pixel #0	Pixel #1	Pixel #0	Pixel #1
BT1120_D0	Y0[0]	Y1[0]	Cb0[0]	Cr0[0]
BT1120_D1	Y0[1]	Y1[1]	Cb0[1]	Cr0[1]
BT1120_D2	Y0[2]	Y1[2]	Cb0[2]	Cr0[2]
BT1120_D3	Y0[3]	Y1[3]	Cb0[3]	Cr0[3]
BT1120_D4	Y0[4]	Y1[4]	Cb0[4]	Cr0[4]
BT1120_D5	Y0[5]	Y1[5]	Cb0[5]	Cr0[5]
BT1120_D6	Y0[6]	Y1[6]	Cb0[6]	Cr0[6]
BT1120_D7	Y0[7]	Y1[7]	Cb0[7]	Cr0[7]
BT1120_D8	Cb0[0]	Cr0[0]	Y0[0]	Y1[0]
BT1120_D9	Cb0[1]	Cr0[1]	Y0[1]	Y1[1]
BT1120_D10	Cb0[2]	Cr0[2]	Y0[2]	Y1[2]
BT1120_D11	Cb0[3]	Cr0[3]	Y0[3]	Y1[3]
BT1120_D12	Cb0[4]	Cr0[4]	Y0[4]	Y1[4]
BT1120_D13	Cb0[5]	Cr0[5]	Y0[5]	Y1[5]
BT1120_D14	Cb0[6]	Cr0[6]	Y0[6]	Y1[6]

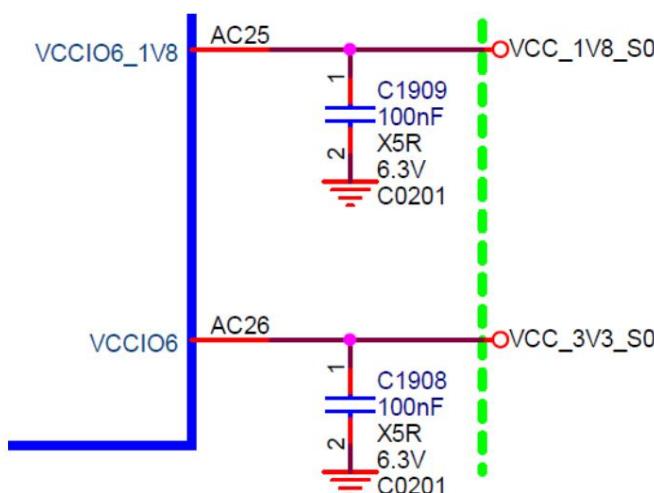
BT1120_D15	Cb0[7]	Cr0[7]	Y0[7]	Y1[7]
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Please note the following when designing the BT1120 output interface:

ŷ The BT1120 output interface power domain is powered by VCCIO6. In actual product design, it is necessary to adjust the power supply according to the actual IO power requirements of the peripherals.

(1.8V or 3.3V) Select the corresponding power supply and it must be consistent;

ŷ To improve the performance of the BT1120 output interface, the decoupling capacitor of the VCCIO6 power supply must not be removed and should be placed close to the pin during layout.



The pull-up and pull-down and matching design recommendations for the BT1120 output interface are shown in the table below:

Table 2-33 RK3588 BT1120 output interface design

Signal	Internal pull-up and pull-down	Connection method	Description (chip side)
BT1120_D[15:0]	drop down	Direct connection, if possible, it is recommended to reserve a series resistor BT1120 close to the chip end Data output	
BT1120_CLK	drop down	Connect a 22ohm resistor in series, close to the device end	BT1120 clock output

ŷ When using a connector to connect a board to a board, it is recommended to connect a resistor with a certain resistance (between 22ohm and 100ohm, depending on the specific resistance).

SI test shall prevail) and TVS devices shall be reserved.

2.3.8.5 LCD and touch screen design considerations

ŷ For the FB-terminal current-limiting resistor of the LED backlight boost IC, please use a 1% precision resistor and select the appropriate package size according to the power requirements;

ŷ For the EN/PWM pin of the LED backlight boost IC, select the internal pull-down GPIO and connect an external pull-down resistor to avoid flickering when powering on.

Screen phenomenon:

ŷ For the LED backlight driving voltage output, please select a filter capacitor with a suitable rated voltage;

ŷ For the Schottky diode in the LED backlight boost circuit, please select the appropriate model according to the operating current and pay attention to the reverse breakdown voltage of the diode.

Pressure to avoid reverse breakdown when no-load;

ŷ The inductor of the LED backlight boost circuit should be matched according to the actual model, including inductance, saturation current, DCR, etc.

The signal levels of the screen and touch screen must match the IO drive levels of the chip, such as RST/Stand by signals;

ŷ The screen's power supply must be controllable. When powered on, it is not provided by default.

ŷ The decoupling capacitors of the screen and touch screen must not be deleted and must be retained;

ŷ The I2C bus of TP must be pulled up to VCC3V3_TP power supply with 2.2K. It is recommended not to share the bus with other devices.

Shared, pay attention to whether the pull-up power supply and address conflict;

ŷ For TP ICs with charge pumps, please pay attention to the rated voltage of the capacitor;

ŷ For the screen, when connecting to the board through FPC, it is recommended to connect a resistor with a certain resistance (between 22ohm-100ohm, the specific resistance should be

SI test shall prevail), and TVS devices shall be reserved;

ŷ It is recommended to reserve common-mode inductance at the interface of the serial interface screen;

2.3.8.6 VGA Interface Design Notes

RK3588 itself does not support direct VGA OUT, and requires an external conversion chip. You can choose RGB888, HDMI, MIPI, eDP, etc.

Interface to VGA output, here mainly describes the relevant points based on IT6516BFN:

ŷ The decoupling capacitors of each power pin must not be deleted and must be retained;

ŷ Pay attention to the power-on sequence requirements;

ŷ The LVTTL signal level of VGADDCSDA and VGADDCCCLK of IT6516BFN Pin12 and Pin13 is 5V, so it is necessary to

Pull to 5V level;

ŷ For the HPD signal of Pin 26 of IT6516BFN, the default ground resistor must not be deleted or the default pull-down GPIO must be used;

ŷ The IT6516BFN peripheral circuit must directly refer to the reference design circuit;

ŷ IVDDO (Pin 25) is the Regulator output 1.8V, providing power to the chip's I/O, DP Analog front end, and DAC/Voltage.

ŷ VGA_R/G/B needs to be pulled down by a 75ohm resistor with an accuracy of 1%. Do not delete it.

ŷ The VGA_R/G/B filter circuit needs to refer to the requirements of each conversion chip;

ŷ TVS tubes must be added to all signals of the VGA socket, and the TVS device should be placed as close to the VGA connector as possible.

2.3.9 Audio-related circuit design

RK3588 provides a total of 11 I2S interfaces, 2 PDM interfaces, 6 SPDIF TX interfaces, 3 SPDIF RX interfaces and 1

Set up DSM PWM Audio interface.

It provides 4 sets of standard I2S interfaces, 2 sets of PDM interfaces, 2 SPDIF TX interfaces and 1 set of DSM PWM Audio.

The IO domain multiplexing of these interfaces and the power domains they belong to are shown in the following table for users to flexibly allocate and select.

Table 2-34 RK3588 external audio interface and IO multiplexing

External interface	The first multiplexing (M0), the second multiplexing (M1), and the third multiplexing (M2) belong to the	internal power domain	
I2S0	VCCIO1	PD_AUDIO	
I2S1	VCCIO6	PD_PMU1	
I2S2	VCCIO3	PD_AUDIO	
I2S3	VCCIO5	PD_AUDIO	
PDM0	VCCIO1	PD_PMU1	
PDM1	VCCIO2	PD_AUDIO	
SPDIFO_TX	VCCIO4 GPIO1_B6	PD_AUDIO	
SPDIF1_TX	VCCIO4 GPIO1_B7	VCCIO6 GPIO4_B1 GPIO4_C1	PD_AUDIO
DSM PWM Audio	VCCIO5	PD_AUDIO	

The remaining unlead audio interfaces are used in conjunction with the video input/output interfaces. Their internal allocation correspondence is described in the box in Section 2.3.9.1.

The internal power domains of these audio interfaces are as follows, which are consistent with the power domains of their corresponding video interfaces:

I2S4 and I2S8 belong to PD_VO0;

I2S5, I2S6, I2S7, I2S9, and I2S10 belong to PD_VO1;

SPDIF2_TX and SPDIF5_TX belong to PD_VO0; SPDIF3_RX and SPDIF4_RX belong to PD_VO1; SPDIF_RX0, SPDIF_RX1 and SPDIF_RX2 belong to PD_VO1.

2.3.9.1 Audio Subsystem Block Diagram

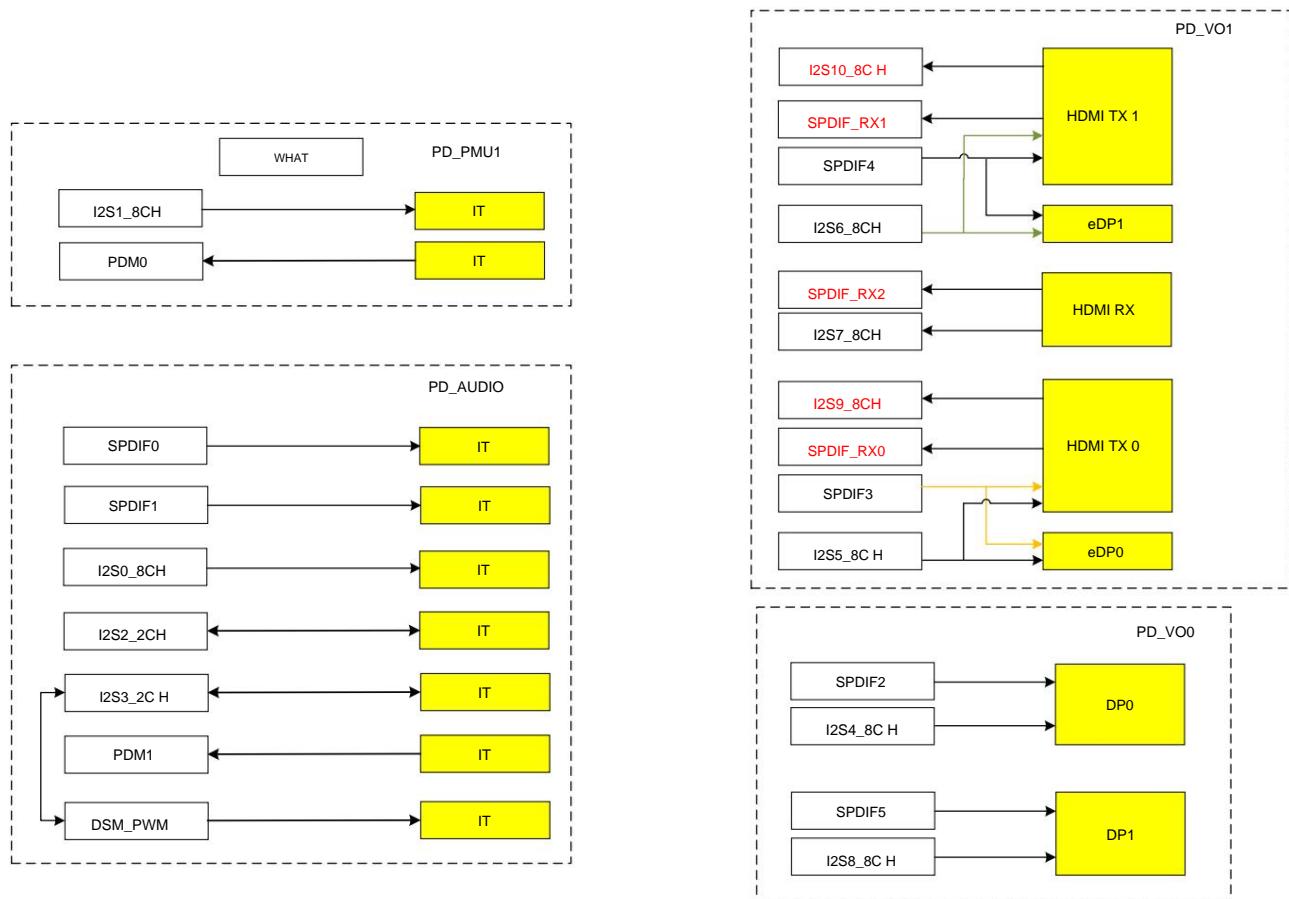


Figure 2-164 RK3588 audio subsystem block diagram

2.3.9.2 I2S Digital Audio Interface

RK3588 provides a total of 11 I2S interfaces, 4 of which are externally connected. I2S is the most widely used digital audio interface.

It can communicate with peripherals such as audio ADC, audio DAC, audio Codec, DSP, etc., and can also provide integrated audio input and output support for video input/output interfaces.

I2S0 and I2S1 are standard I2S interfaces supporting 8-channel input/output and I2S/PCM/TDM modes. I2S2 and I2S3 are standard I2S interfaces supporting 2-channel input/output and I2S/PCM modes. The formats and timings of these modes are detailed in the TRM document.

These four I2S interfaces can support master and slave modes, bit widths from 16 to 32 bits, and sampling rates up to 192kHz.

2.3.9.2.1 I2S0 Digital Audio Interface

The I2S0 interface contains 8 independent channels of output and 8 independent channels of input. For output data SDOx and input data SDIx, both refer to the same Group bit/frame clock SCLK/LRCK.

The I2S0 interface supports master-slave working mode and is software configurable. It supports 3 I2S formats (normal, left-aligned, right-aligned); supports 4

PCM format (early, late1, late2, late3); supports 5 TDM formats (normal, 1/2 cycle left shift, 1 cycle left shift,

2 cycle left shift/right shift)

This group of I2S pins has only one multiplexing, in VCCIO1, where there are two SDOx and SDIx signals with multiplexing conflicts.

At the same time, the IO level of the I2S peripheral needs to be checked to match the corresponding IO power domain.

The recommended pull-up and pull-down and matching designs for the I2S0 interface are shown in the table.

Table 2-35 RK3588 I2S0 interface signal description

Signal	Default pull-up and pull-down	Connection method	Description (chip side)
I2S0_MCLK	drop down	Connect a 22ohm resistor in series	I2S system clock output
I2S0_SCLK	drop down	Connect a 22ohm resistor in series	I2S Continuous Serial Clock, Bit Clock
I2S0_LRCK	drop down	Connect a 22ohm resistor in series	I2S frame clock for channel selection
I2S0_SDO0	drop down	Direct connection	I2S serial data 0 output
I2S0_SDO1	drop down	Direct connection	I2S serial data 1 output
I2S0_SDO2/I2S0_SDID3	drop down	Direct connection	I2S serial data 2 output/serial data 3 input
I2S0_SDO3/I2S0_SDID2	drop down	Direct connection	I2S serial data 3 output/serial data 2 input
I2S0_SDID0	drop down	Direct connection	I2S serial data 0 input
I2S0_SDID1	drop down	Direct connection	I2S serial data 1 input

To improve I2S interface performance, the decoupling capacitors corresponding to the VCCIO power domain must not be removed and should be placed close to the pins during layout.

When using a connector to connect a board to a board, it is recommended that a resistor with a certain resistance value (between 22ohm and 100ohm) be connected in series with the clock/control/signal.

The specific time is subject to whether it can meet the SI test) and TVS devices are reserved.

2.3.9.2.2 I2S1 Digital Audio Interface

The I2S1 interface contains 8 independent channels of output and 8 independent channels of input. For output data SDOx and input data SDIx, both refer to the same

Group bit/frame clock SCLK/LRCK.

The I2S1 interface supports master-slave working mode and is software configurable. It supports 3 I2S formats (normal, left-aligned, right-aligned); supports 4 PCM format (early, late1, late2, late3); supports 5 TDM formats (normal, 1/2 cycle left shift, 1 cycle left shift, 2 cycle left shift/right shift)

This group of I2S pins is multiplexed in two different power domains, I2S1_M0 is multiplexed in VCCIO6, I2S1_M1 is multiplexed in PMUIO2, and the two

All signals can be led out in a complete group. Two multiplexing locations cannot be used at the same time, and only one group can be used at a time.

level to match the corresponding IO power domain.

The pull-up and pull-down and matching design recommendations for the I2S1 interface are shown in the table:

Table 2-36 RK3588 I2S1 interface signal description

Signal	Default pull-up and pull-down	Connection method	Description (chip side)
I2S1_MCLK_M0	drop down	Connect a 22ohm resistor in series	I2S system clock output
I2S1_SCLK_M0	drop down	Connect a 22ohm resistor in series	I2S Continuous Serial Clock, Bit Clock
I2S1_LRCK_M0	drop down	Connect a 22ohm resistor in series	I2S frame clock for channel selection
I2S1_SDO0_M0	Pull-up	Direct connection	I2S serial data 0 output
I2S1_SDO1_M0	Pull-up	Direct connection	I2S serial data 1 output
I2S1_SDO2_M0	Pull-up	Direct connection	I2S serial data 2 output
I2S1_SDO3_M0	Pull-up	Direct connection	I2S serial data 3 output

Signal	Default pull-up and pull-down	Connection method	Description (chip side)
I2S1_SDIO_M0	drop down	Direct connection	I2S serial data 0 input
I2S1_SD1_M0	drop down	Direct connection	I2S serial data 1 input
I2S1_SD2_M0	drop down	Direct connection	I2S serial data 2 input
I2S1_SD3_M0	drop down	Direct connection	I2S serial data 3 input
I2S1_MCLK_M1	drop down	Connect a 22ohm resistor in series	I2S system clock output
I2S1_SCLK_M1	drop down	Connect a 22ohm resistor in series	I2S Continuous Serial Clock, Bit Clock
I2S1_LRCK_M1	drop down	Connect a 22ohm resistor in series	I2S frame clock for channel selection
I2S1_SDO0_M1	Pull-up	Direct connection	I2S serial data 0 output
I2S1_SDO1_M1	Pull-up	Direct connection	I2S serial data 1 output
I2S1_SDO2_M1	Pull-up	Direct connection	I2S serial data 2 output
I2S1_SDO3_M1	Pull-up	Direct connection	I2S serial data 3 output
I2S1_SDIO_M1	Pull-up	Direct connection	I2S serial data 0 input
I2S1_SD1_M1	Pull-up	Direct connection	I2S serial data 1 input
I2S1_SD2_M1	drop down	Direct connection	I2S serial data 2 input
I2S1_SD3_M1	drop down	Direct connection	I2S serial data 3 input

To improve I2S interface performance, the decoupling capacitors corresponding to the VCCIO power domain must not be removed and should be placed close to the pins during layout.

When using a connector to connect a board to a board, it is recommended that a resistor with a certain resistance value (between 22ohm and 100ohm) be connected in series with the clock/control/signal.

The specific time is subject to whether it can meet the SI test) and TVS devices are reserved.

2.3.9.2.3 I2S2 Digital Audio Interface

The I2S2 interface includes two independent channels of output and two independent channels of input. For output data SDOx and input data SDIx, both refer to the same

Group bit/frame clock SCLK/LRCK.

The I2S2 interface supports master-slave working mode and is software configurable. It supports 3 I2S formats (normal, left-aligned, right-aligned); supports 4

PCM formats (early, late1, late2, late3).

This group of I2S pins is multiplexed in two different power domains, I2S2_M0 is multiplexed in VCCIO3, I2S2_M1 is multiplexed in VCCIO5, and the two

All signals can be led out in a complete group. Two multiplexing locations cannot be used at the same time, and only one group can be used at a time.

level to match the corresponding IO power domain.

The pull-up and pull-down and matching design recommendations for the I2S2 interface are shown in the table:

Table 2-37 RK3588 I2S2 interface signal description

Signal	Default pull-up and pull-down	Connection method	Description (chip side)
I2S2_MCLK_M0	drop down	Connect a 22ohm resistor in series	I2S system clock output
I2S2_SCLK_M0	drop down	Connect a 22ohm resistor in series	I2S Continuous Serial Clock, Bit Clock
I2S2_LRCK_M0	drop down	Connect a 22ohm resistor in series	I2S frame clock for channel selection
I2S2_SDO_M0	drop down	Direct connection	I2S serial data 0 output
I2S2_SD1_M0	drop down	Direct connection	I2S serial data 0 input
I2S2_MCLK_M1	Pull-up	Connect a 22ohm resistor in series	I2S system clock output
I2S2_SCLK_M1	Pull-up	Connect a 22ohm resistor in series	I2S Continuous Serial Clock, Bit Clock
I2S2_LRCK_M1	drop down	Connect a 22ohm resistor in series	I2S frame clock for channel selection
I2S2_SDO_M1	Pull-up	Direct connection	I2S serial data 0 output

I2S2_SD1_M1	drop down	Direct connection	I2S serial data 0 input
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To improve I2S interface performance, the decoupling capacitors corresponding to the VCCIO power domain must not be removed and should be placed close to the pins during layout.

When using a connector to connect a board to a board, it is recommended that a resistor with a certain resistance value (between 22ohm and 100ohm) be connected in series with the clock/control/signal.

The specific time is subject to whether it can meet the SI test) and TVS devices are reserved.

2.3.9.2.4 I2S3 Digital Audio Interface

The I2S3 interface includes two independent channels of output and two independent channels of input. For output data SDOx and input data SDIx, both refer to the same

Group bit/frame clock SCLK/LRCK.

The I2S3 interface supports master-slave working mode and is software configurable. It supports 3 I2S formats (normal, left-aligned, right-aligned); supports 4 PCM formats (early, late1, late2, late3).

This group of I2S pins has only one multiplexing, at VCCIO5. You need to check the IO level of the I2S peripheral to match the corresponding IO power domain.

powered by.

The pull-up and pull-down and matching design recommendations for the I2S3 interface are shown in the table:

Table 2-38 RK3588 I2S3 interface design

Signal	Default pull-up and pull-down	Connection method	Description (chip side)
I2S3_MCLK	Pull-up	Connect a 22ohm resistor in series	I2S system clock output
I2S3_SCLK	Pull-up	Connect a 22ohm resistor in series	I2S Continuous Serial Clock, Bit Clock
I2S3_LRCK	Pull-up	Connect a 22ohm resistor in series	I2S frame clock for channel selection
I2S3_SDO	Pull-up	Direct connection	I2S serial data 0 output
I2S3_SD1	drop down	Direct connection	I2S serial data 0 input

To improve I2S interface performance, the decoupling capacitors corresponding to the VCCIO power domain must not be removed and should be placed close to the pins during layout.

When using a connector to connect a board to a board, it is recommended that a resistor with a certain resistance value (between 22ohm and 100ohm) be connected in series with the clock/control/signal.

The specific time is subject to whether it can meet the SI test) and TVS devices are reserved.

2.3.9.3 PDM digital audio interface

RK3588 provides 2 sets of PDM interfaces, both of which are externally connected.

Both PDM groups work in master receive mode (i.e. RK3588 provides PDM clock and receives data) and support 8

Channel input capability, bit width from 16 to 32 bits, sampling rate up to 192kHz.

The PDM interface is usually used to connect a digital microphone, or to record the analog microphone through the analog audio ADC of the PDM interface.

The following figure shows the data format of the PDM interface. PDM_DATA consists of Data(R) and Data(L). PDM is a 1-bit sampling interface.

Data(L) and Data(R) are sampled on the rising and falling edges of CLK, that is, each PDM_SD1x data line can transmit two channels of audio data.