

I2S2_SDI_M1	drop down	Direct connection	I2S serial data 0 input
-------------	-----------	-------------------	-------------------------

To improve I2S interface performance, the decoupling capacitors corresponding to the VCCIO power domain must not be removed and should be placed close to the pins during layout.

When using a connector to connect a board to a board, it is recommended that a resistor with a certain resistance value (between 22ohm and 100ohm) be connected in series with the clock/control/signal.

The specific time is subject to whether it can meet the SI test) and TVS devices are reserved.

2.3.9.2.4 I2S3 Digital Audio Interface

The I2S3 interface includes two independent channels of output and two independent channels of input. For output data SDOx and input data SDIx, both refer to the same

Group bit/frame clock SCLK/LRCK.

The I2S3 interface supports master-slave working mode and is software configurable. It supports 3 I2S formats (normal, left-aligned, right-aligned); supports 4 PCM formats (early, late1, late2, late3).

This group of I2S pins has only one multiplexing, at VCCIO5. You need to check the IO level of the I2S peripheral to match the corresponding IO power domain.

powered by.

The pull-up and pull-down and matching design recommendations for the I2S3 interface are shown in the table:

Table 2-38 RK3588 I2S3 interface design

Signal	Default pull-up and pull-down	Connection method	Description (chip side)
I2S3_MCLK	Pull-up	Connect a 22ohm resistor in series	I2S system clock output
I2S3_SCLK	Pull-up	Connect a 22ohm resistor in series	I2S Continuous Serial Clock, Bit Clock
I2S3_LRCK	Pull-up	Connect a 22ohm resistor in series	I2S frame clock for channel selection
I2S3_SDO	Pull-up	Direct connection	I2S serial data 0 output
I2S3_SD1	drop down	Direct connection	I2S serial data 0 input

To improve I2S interface performance, the decoupling capacitors corresponding to the VCCIO power domain must not be removed and should be placed close to the pins during layout.

When using a connector to connect a board to a board, it is recommended that a resistor with a certain resistance value (between 22ohm and 100ohm) be connected in series with the clock/control/signal.

The specific time is subject to whether it can meet the SI test) and TVS devices are reserved.

2.3.9.3 PDM digital audio interface

RK3588 provides 2 sets of PDM interfaces, both of which are externally connected.

Both PDM groups work in master receive mode (i.e. RK3588 provides PDM clock and receives data) and support 8

Channel input capability, bit width from 16 to 32 bits, sampling rate up to 192kHz.

The PDM interface is usually used to connect a digital microphone, or to record the analog microphone through the analog audio ADC of the PDM interface.

The following figure shows the data format of the PDM interface. PDM_DATA consists of Data(R) and Data(L). PDM is a 1-bit sampling interface.

Data(L) and Data(R) are sampled on the rising and falling edges of CLK, that is, each PDM_SDIx data line can transmit two channels of audio data.

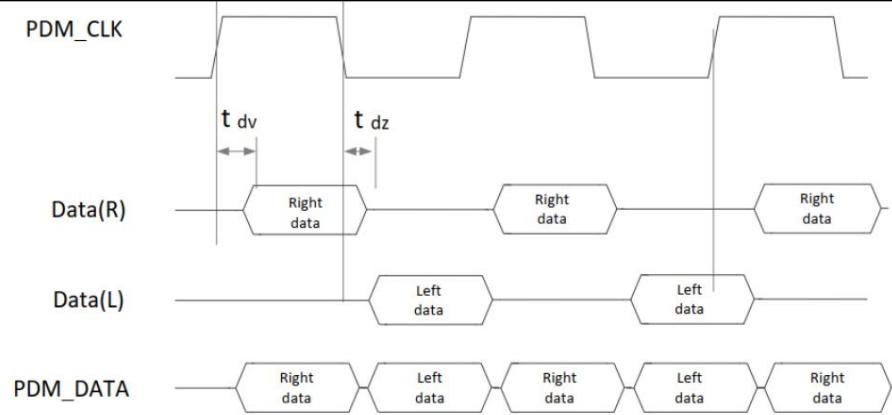


Figure 2-165 RK3588 PDM interface data format

The corresponding relationship between common sampling rates and PDM_CLK is shown in the following table, which can be used as a reference during hardware commissioning:

Table 2-39 RK3588 PDM_CLK frequency and sampling rate comparison table

PDM_CLK frequency	Sampling rate
3.072MHz	12kHz, 24kHz, 48kHz, 96kHz, 192kHz
2.8224MHz	11.025kHz, 22.05kHz, 44.1kHz, 88.2kHz, 176.4kHz
2.048MHz	8kHz, 16kHz, 32kHz, 64kHz, 128kHz

2.3.9.3.1 PDM0 Digital Audio Interface

The PDM0 pin is multiplexed in two different power domains, PDM0_M0 is multiplexed in VCCIO1, and PDM0_M1 is multiplexed in PMUIO2.

Multiplexing cannot be used at the same time, only one group can be used at a time. It is necessary to check the IO level of the PDM peripheral to match the corresponding IO power domain.

electricity.

The pull-up and pull-down and matching design recommendations for the PDM0 interface are shown in the table. To improve the impact of PCB traces on the clock, two co-source and co-phase

PDM clocks, PDM_CLK0 and PDM_CLK1, can be allocated according to layout routing requirements to avoid single CLK routing.

The impact of branches.

Table 2-40 RK3588 PDM0 interface signal description

Signal	Default pull-up and pull-down	Connection method	Description (chip side)
PDM0_CLK0_M0	drop down	Connect a 22ohm resistor in series	PDM Clock 0
PDM0_CLK1_M0	drop down	Connect a 22ohm resistor in series	PDM Clock 1
PDM0_SDIO_M0	drop down	Direct connection	PDM data input 0
PDM0_SD11_M0	drop down	Direct connection	PDM data input 1
PDM0_SD12_M0	drop down	Direct connection	PDM Data Input 2
PDM0_SD13_M0	drop down	Direct connection	PDM Data Input 3
PDM0_CLK0_M1	drop down	Connect a 22ohm resistor in series	PDM Clock 0
PDM0_CLK1_M1	drop down	Connect a 22ohm resistor in series	PDM Clock 1
PDM0_SDIO_M1	drop down	Direct connection	PDM data input 0
PDM0_SD11_M1	drop down	Direct connection	PDM data input 1
PDM0_SD12_M1	Pull-up	Direct connection	PDM Data Input 2
PDM0_SD13_M1	drop down	Direct connection	PDM Data Input 3

To improve PDM interface performance, decoupling capacitors corresponding to the VCCIO power domain must not be removed and should be placed close to the pins during layout.

When using a connector to connect a board to a board, it is recommended that a resistor with a certain resistance value (between 22ohm and 100ohm) be connected in series with the clock/control/signal.

The specific time is subject to whether it can meet the SI test) and TVS devices are reserved.

2.3.9.3.2 PDM1 Digital Audio Interface

The PDM1 pins are multiplexed in two different power domains, PDM1_M0 is multiplexed in VCCIO2, and PDM1_M1 is multiplexed in VCCIO4.

Multiplexing cannot be used at the same time, only one group can be used at a time. It is necessary to check the IO level of the PDM peripheral to match the corresponding IO power domain.

electricity.

The pull-up and pull-down and matching design recommendations for the PDM1 interface are shown in the table. To improve the impact of PCB traces on the clock, two co-source and co-phase

PDM clocks, PDM_CLK0 and PDM_CLK1, can be allocated according to layout routing requirements to avoid single CLK routing.

The impact of branches.

Table 2-41 RK3588 PDM1 interface signal description

Signal	Default pull-up and pull-down	Connection method	Description (chip side)
PDM1_CLK0_M0	drop down	Connect a 22ohm resistor in series	PDM Clock 0
PDM1_CLK1_M0	Pull-up	Connect a 22ohm resistor in series	PDM Clock 1
PDM1_SDIO_M0	Pull-up	Direct connection	PDM data input 0
PDM1_SDID1_M0	Pull-up	Direct connection	PDM data input 1
PDM1_SDID2_M0	Pull-up	Direct connection	PDM Data Input 2
PDM1_SDID3_M0	Pull-up	Direct connection	PDM Data Input 3
PDM1_CLK0_M1	Pull-up	Connect a 22ohm resistor in series	PDM Clock 0
PDM1_CLK1_M1	drop down	Connect a 22ohm resistor in series	PDM Clock 1
PDM1_SDIO_M1	Pull-up	Direct connection	PDM data input 0
PDM1_SDID1_M1	Pull-up	Direct connection	PDM data input 1
PDM1_SDID2_M1	drop down	Direct connection	PDM Data Input 2
PDM1_SDID3_M1	drop down	Direct connection	PDM Data Input 3

To improve the performance of the PDM interface, the decoupling capacitors corresponding to the VCCIO power domain must not be removed and should be placed close to the pins during layout.

When using a connector to connect a board to a board, it is recommended that a resistor with a certain resistance value (between 22ohm and 100ohm) be connected in series with the clock/control/signal.

time, the specific time shall be subject to whether it can meet the SI test) and

2.3.9.4 SPDIF TX digital audio interface

2.3.9.4.1 SPDIF0_TX Digital Audio Interface

The SPDIF0_TX pin is multiplexed in two different power domains, and SPDIF0_TX_M0 is multiplexed in VCCIO4 and GPIO1_B6;

SPDIF0_TX_M1 is multiplexed on VCCIO6, GPIO4_B4. You need to check the IO level of the SPDIF_TX peripheral to match the corresponding IO

Power domains are powered.

The pull-up and pull-down and matching design recommendations for the SPDIF interface are shown in the table:

Table 2-42 RK3588 SPDIF0_TX interface signal description

Signal and multiplexing are pulled up and down by default	Connection method	Power domain
SPDIF0_TX_M0	Pull-up	Connect a 22ohm resistor in series
SPDIF0_TX_M1	Pull-up	Connect a 22ohm resistor in series

To improve the performance of the SPDIF interface, the decoupling capacitors corresponding to the VCCIO power domain must not be removed and should be placed close to the pins during layout.

When using a connector to connect a board to a board, it is recommended that a resistor with a certain resistance value (between 22ohm and 100ohm) be connected in series with the clock/control/signal.

The specific time is subject to whether it can meet the SI test) and TVS devices are reserved.

2.3.9.4.2 SPDIF1_TX Digital Audio Interface

The SPDIF1_TX pin is multiplexed in three places, in two different power domains. SPDIF1_TX_M0 is multiplexed in VCCIO4 and GPIO1_B7.

SPDIF1_TX_M1 is multiplexed on VCCIO6, GPIO4_B1; SPDIF1_TX_M2 is multiplexed on VCCIO6, GPIO4_C1. Need to check

The IO level of the SPDIF_TX peripheral is matched to the corresponding IO power domain.

The pull-up and pull-down and matching design recommendations for the SPDIF interface are shown in the table:

Table 2-43 RK3588 SPDIF1_TX interface signal description

Signal and multiplexing are pulled up and down by default	Connection method	Power domain
SPDIF1_TX_M0	Pull-up	Connect a 22ohm resistor in series
SPDIF1_TX_M1	Pull-up	Connect a 22ohm resistor in series
SPDIF1_TX_M2	drop down	Connect a 22ohm resistor in series

To improve the performance of the SPDIF interface, the decoupling capacitors corresponding to the VCCIO power domain must not be removed and should be placed close to the pins during layout.

When using a connector to connect a board to a board, it is recommended that a resistor with a certain resistance value (between 22ohm and 100ohm) be connected in series with the clock/control/signal.

The specific time is subject to whether it can meet the SI test) and TVS devices are reserved.

2.3.9.5 DSM PWM Audio Interface

DSM PWM Audio refers to the direct bit stream digital encoding (Direct Stream Digital) conversion output of audio PCM data.

1-bit signal stream data, in the design that is not equipped with high-performance audio DAC and needs voice audio output, this interface can be low-pass through a first-order RC

The audio signal is obtained by filtering, as shown in the figure below. The output digital signal is filtered to obtain the audio signal.

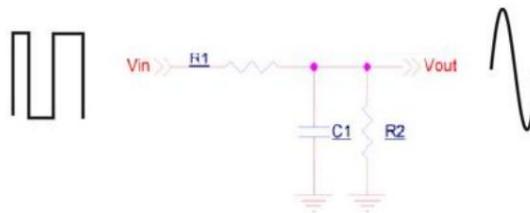


Figure 2-166 RK3588 DSM PWM Audio low-pass filter diagram

This group of interfaces provides two pairs of differential outputs to meet stereo requirements. For a detailed introduction to the interface and calculation of RC low-pass filter parameters, please refer to

Refer to the document "DSMAUDIO Audio Interface Circuit Design".

Table 2-44 RK3588 DSM PWM Audio interface signal description

Signal and multiplexing are pulled up and down by default	Connection method	Power domain
AUDDSM_LN	Pull-up	Series RC low-pass filter
AUDDSM_LP	Pull-up	Series RC low-pass filter
AUDDSM_RN	Pull-up	Series RC low-pass filter
AUDDSM_RP	drop down	Series RC low-pass filter

To improve the performance of the DSM PWM Audio interface, the decoupling capacitors corresponding to the VCCIO power domain must not be deleted. When laying out, place them close to the tube.

foot placement;

When using a connector to connect a board to a board, it is recommended that a resistor with a certain resistance value (between 22ohm and 100ohm) be connected in series with the clock/control/signal.

The specific time is subject to whether it can meet the SI test) and TVS devices are reserved.

2.3.9.6 Audio Peripheral Design Reference

In most cases, the digital audio interface mentioned above cannot be used directly and requires related peripherals to realize specific audio functions.

This section provides design suggestions for common audio scenarios for your reference.

2.3.9.6.1 Sound playback equipment, headphones, and speakers

For the speaker playback requirement, the implementation scheme is as follows: RK3588 connects to the audio DAC via I2S to achieve analog output, and then passes through the audio amplifier

Realize power amplification to drive the speaker:

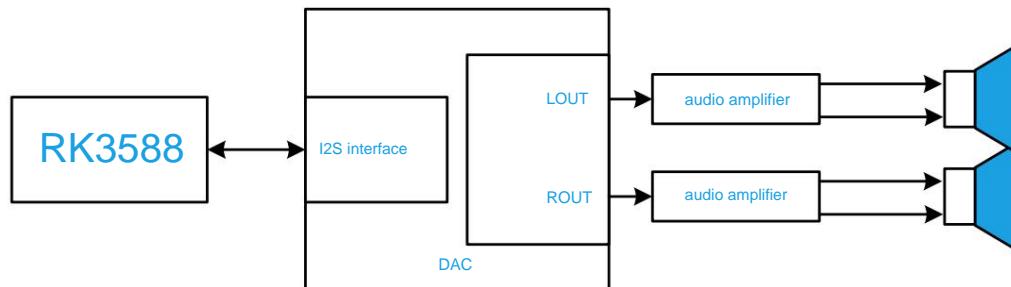


Figure 2-167 RK3588 speaker output diagram

For scenarios with low requirements for sound quality and strict cost, the output path through DSM PWM Audio is shown below.

It is recommended to evaluate audio quality, for example for simple speech announcements:

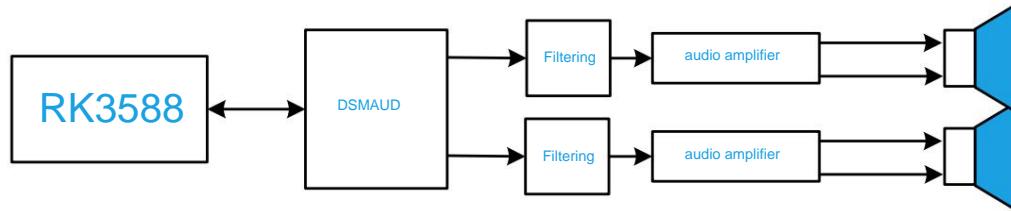


Figure 2-168 RK3588 low-cost speaker output diagram

2.3.9.6.2 Recording equipment, microphone

In tablets, laptops and other application scenarios, in addition to playback, there is also a need for recording. In this case, a Codec with integrated ADC and DAC is usually used.

To achieve the relevant functions, as shown in the figure below, for more complex design references with 4G calling, Bluetooth calling and other functions, please contact RK at this stage

Get:

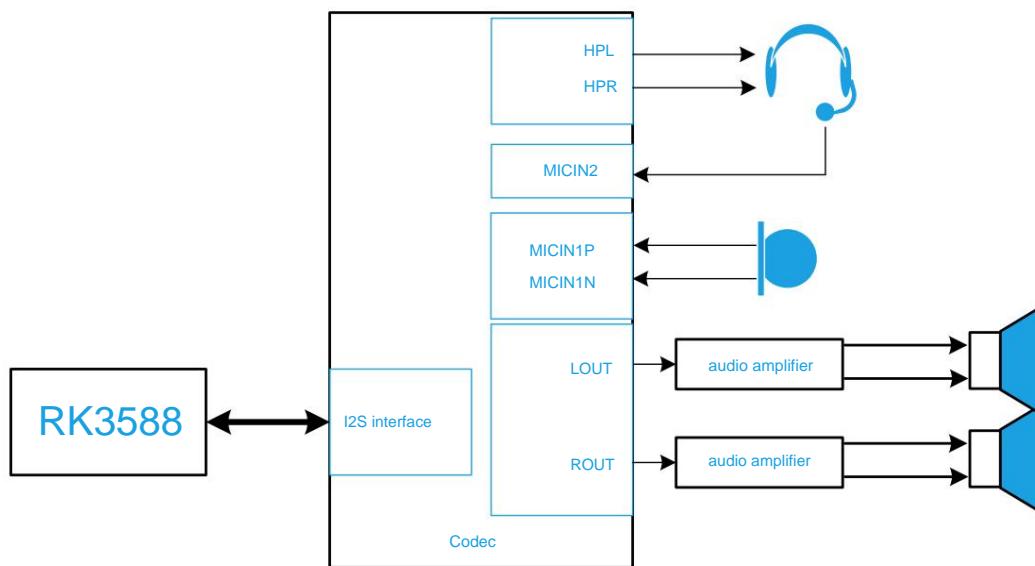


Figure 2-169 RK3588 typical audio solution diagram

2.3.9.6.3 Introduction to Multi-Microphone Solutions

For scenarios with multiple microphone inputs (microphone arrays, far-field recognition), more microphones need to be connected. Common expansion methods are:

There are three solutions as follows. If none of them can meet your specific needs, please contact RK to discuss feasibility:

Method 1: Use the Codec of the I2S interface to realize the input acquisition of multiple microphones and speakers; Method 2: Use the Codec of the PDM interface to realize the input acquisition of multiple microphones and speakers; Method 3: Use the microphone of the PDM interface to realize recording, and use the Codec of the PDM interface to realize the input acquisition of the speaker; If there are not enough channels, you can use multiple SDI signal lines to realize multiple groups of input, or use the TDM module of the I2S interface to realize multiple groups of input.

Cascade input is achieved by simply stacking the same circuits in hardware.

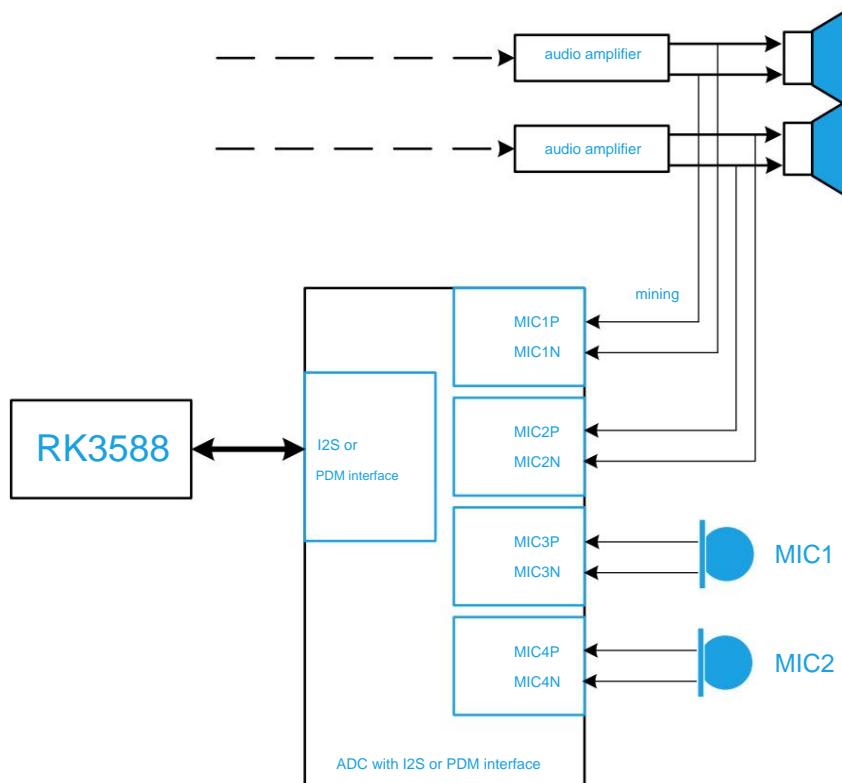


Figure 2-170 RK3588 multi-microphone solution diagram

2.3.10 GMAC Interface Circuit

The RK3588 chip has two GMAC controllers, providing RMII or RGMII interface to connect to external Ethernet PHY

The GMAC controller supports the following functions:

Method 1: Use the Codec of the I2S interface to realize the input acquisition of multiple microphones and speakers; Method 2: Use the Codec of the PDM interface to realize the input acquisition of multiple microphones and speakers; Method 3: Use the microphone of the PDM interface to realize recording, and use the Codec of the PDM interface to realize the input acquisition of the speaker; If there are not enough channels, you can use multiple SDI signal lines to realize multiple groups of input, or use the TDM module of the I2S interface to realize multiple groups of input.

The RGMII/RMII interface of GMAC0 is multiplexed in the VCCIO3 power domain.

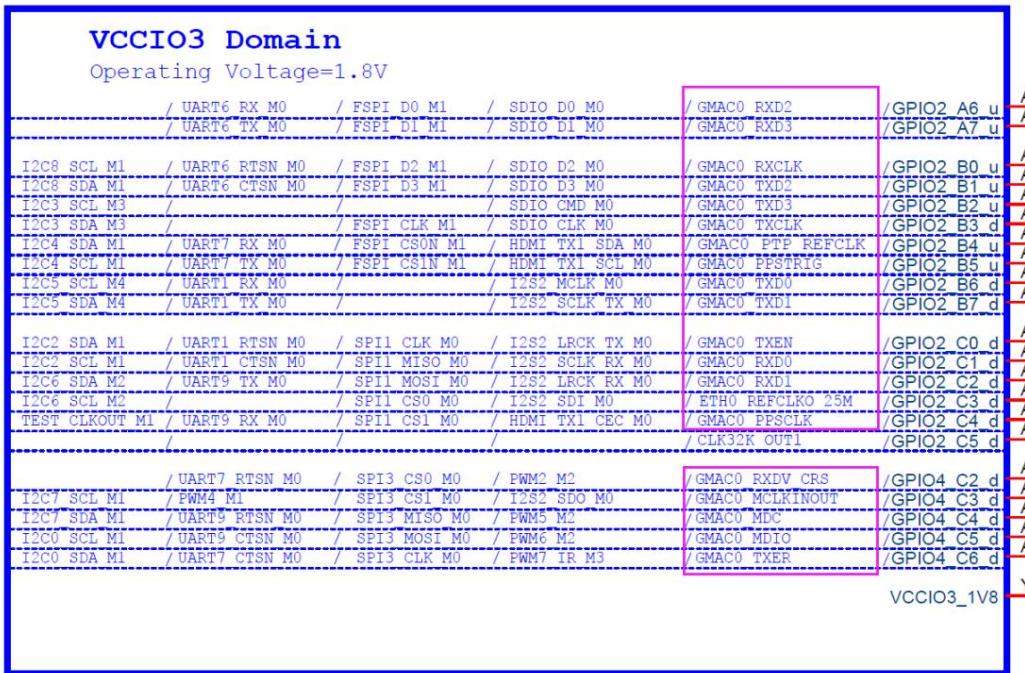


Figure 2-171 RK3588 GMAC0 functional pins

The RGMII/RMII interface of GMAC1 is multiplexed in the VCCIO5 power domain.

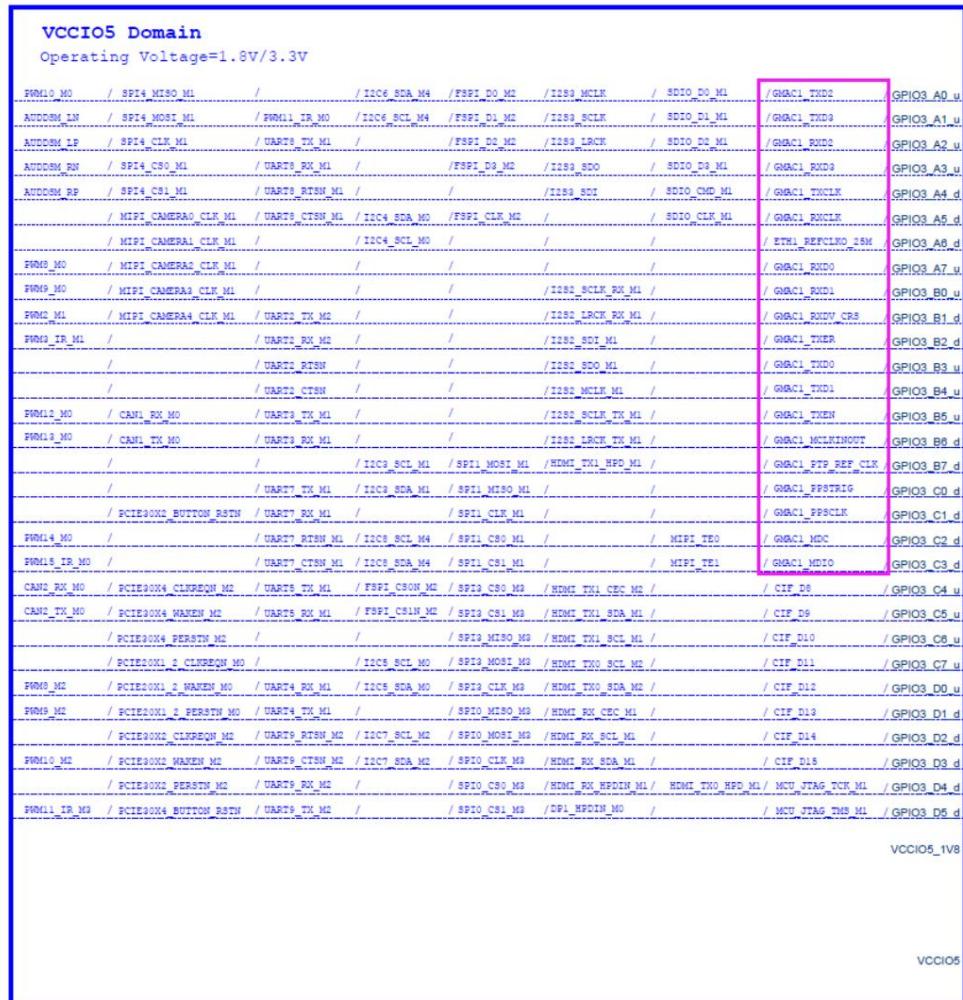


Figure 2-172 RK3588 GMAC1 functional pins

Please note the following when designing the RGMII/

RMII interface: \diamond GMAC0 is multiplexed in the VCCIO3 power domain and only supports 1.8V

level; \diamond GMAC1 is multiplexed in the VCCIO5 power domain and can support 1.8V or 3.3V level, which is determined by VCCIO5 (Pin W26). Pin W26 is connected to a 1.8V

power supply for 1.8V level, and Pin W26 is connected to a 3.3V power supply for 3.3V level (note that Pin W25 is fixed to a 1.8V power supply).

source);

\diamond It is recommended that RGMII/RMII use 1.8V level to obtain better signal quality. \diamond To improve the performance of RGMII/

RMII interface, the decoupling capacitor of the VCCIOx power supply must not be removed. Please place it close to the pin during layout. \diamond ETH0_REFCLKO_25M needs

to be reserved for series connection with a 0 ohm resistor at the RK3588 end. The signal quality can be improved according to the actual situation. \diamond ETH1_REFCLKO_25M

needs to be reserved for series connection with a 0 ohm resistor at the RK3588 end. The signal quality can be improved according to the actual situation. \diamond TXD0-TXD3,

TXCLK, TXEN need to be reserved for series connection with a 0 ohm resistor at the RK3588 end. The signal quality can be improved according to the actual situation.

Signal quality;

\diamond RXD0-RXD3, RXCLK, RXDV need to be connected in series with a 22 ohm resistor at the PHY end to improve signal quality; \diamond The pull-up and

matching design recommendations on the RGMII/RMII interface are as shown in the table:

Table 2-45 RK3588 RGMII/RMII interface design

Signal	IO type (chip side)	Connection method	RGMII interface	Signal Description	RMII interface	Signal Description
GMACx_TXD[3:0]	Output	Reserve a 0ohm resistor in series, close to The RK3588	RGMIIx_TXD[3:0]	Data transmission	RMIIx_TXD[1:0]	Data transmission
GMACx_TXCLK output		terminal is reserved for connecting a 0ohm resistor in series, close to The RK3588	RGMIIx_TXCLK	Data transmission reference clock	-	-
GMACx_TXEN output		terminal is reserved for connecting a 0ohm resistor in series, close to The RK3588 side	RGMIIx_TXEN	Data transmission enable (rising edge) and data transmission error (falling edge)	RMIIx_TXEN	Data sent using signals
GMACx_RXD[3:0]	enter	Connect a 22ohm resistor in series, close to the PHY end.	RGMIIx_RXD[3:0]	Data Reception	RMIIx_RXD[1:0]	Data Reception
GMACx_RXCLK input		Connect a 22ohm resistor in series, close to the PHY end.	RGMIIx_RXCLK	Data receiving reference clock	-	-
GMACx_RXDV input		Connect a 22ohm resistor in series, close to the PHY end	RGMIIx_RXDV	Data reception valid (rising edge) and reception error (falling edge)	RMIIx_RXDV_CRS	Data reception valid and carrier sense
GMACx_MCLKI NOTE	Input/Output	Output mode: Reserved to connect 0ohm resistor in series, close to RK3588 end Input mode: Reserved to connect 22ohm resistor	RGMIIx_MCLKIN_125M	PHY sends 125MHz to MAC, optional	RMII_MCLKIN_50M or RMII_MCLKOUT_50M	RMII data transmission and data reception reference clock
ETHx_REFCLKO_25M	Output	in series, close to PHY end Reserved to connect 0ohm resistor	ETHx_REFCLKO_25M	RK3588 provides 25MHz clock replacement PHY Crystal	ETHx_REFCLKO_25M	RK3588 provides 25MHz clock replaces PHY crystal
GMACx_MDC Output		in series, close to RK3588 end Reserved to connect 0ohm resistor	RGMIIx_MDC	manages the data clock.	-	-
GMACx_MDIO	Input/Output	in series, close to RK3588 end External pull-up resistor 1.5K-1.8Kohm	RGMIIx_MDIO	Manage data import/export	RMIIx_MDIO	Manage data import/export

When using a connector to connect a board to a board, it is recommended to connect a resistor with a certain resistance (between 22ohm and 100ohm, depending on the specific resistance).

SI test shall prevail), and TVS devices shall be reserved;

RGMII connection diagram 1, please see the reference diagram for the specific circuit (GEPHY working clock uses an external 25MHz crystal):

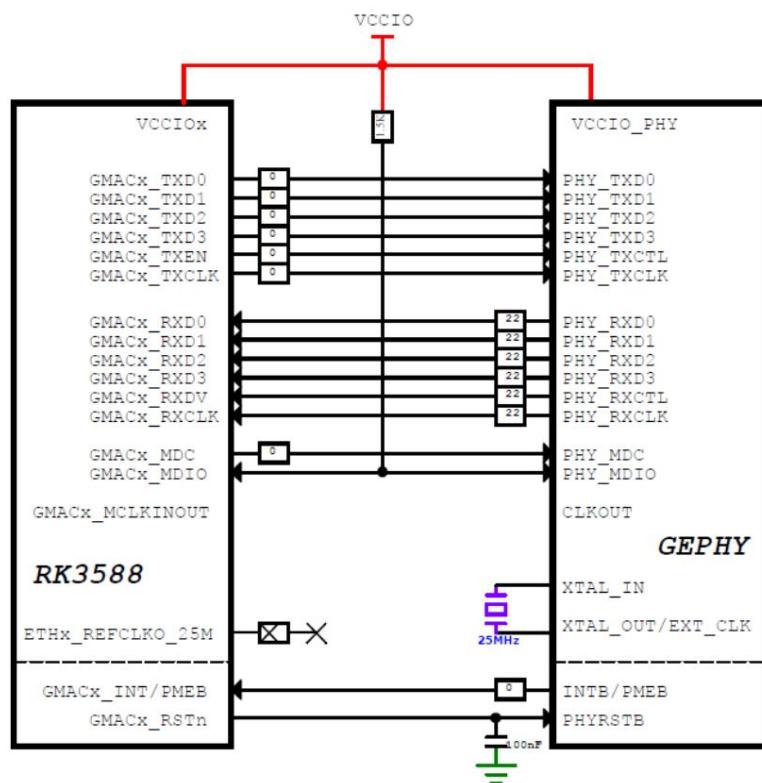


Figure 2-173 RGMII connection diagram 1

RGMII connection diagram 2, please see the reference diagram for the specific circuit (GEPHY working clock uses 25MHz provided by RK3588):

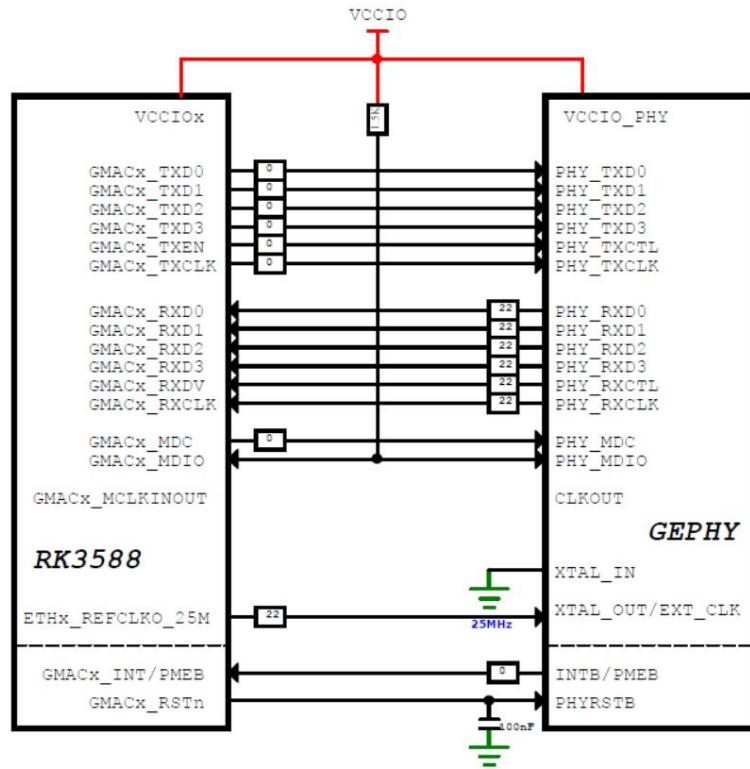


Figure 2-174 RGMII connection diagram 2

For RMII connection diagram 1, please refer to the reference diagram for the specific circuit (GMACx_MCLKINOUT uses output mode, that is, when FEPHY is working)

It is used as the clock and also as the reference clock of the RMII interface. Some FEPHYS do not support this mode, so please note:

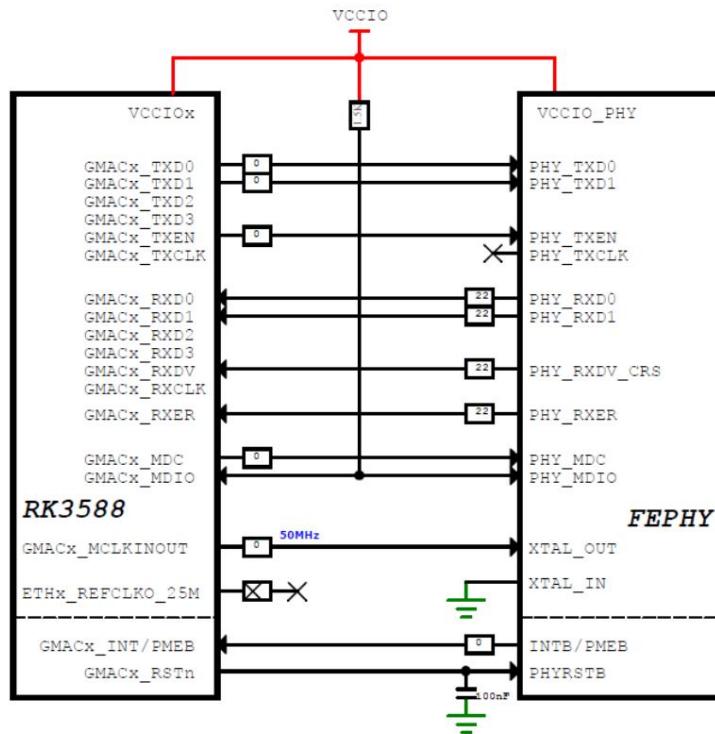


Figure 2-175 RMII connection diagram 1

For RMII connection diagram 2, please see the reference diagram for the specific circuit (FEPHY working clock uses 25MHz crystal,

GMACx_MCLKINOUT uses output mode. When the reference clock of RMII interface, TXCLK of FEPHY needs to be configured as

Input Mode):

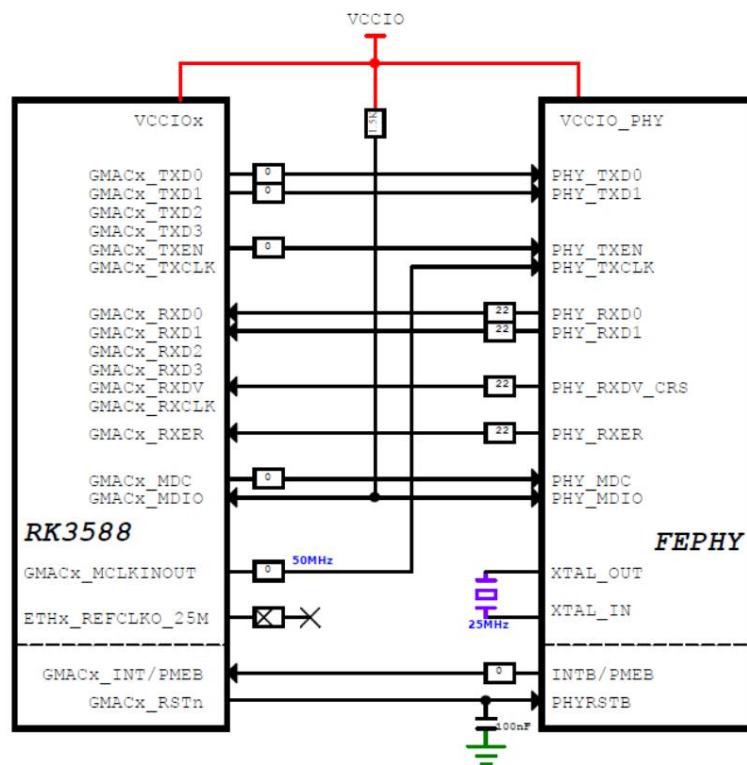


Figure 2-176 RMII connection diagram 2

For RMII connection diagram 3, please see the reference diagram for the specific circuit (use the 25MHz provided by RK3588 to replace the FEPHY crystal,

GMACx_MCLKINOUT uses output mode. When the reference clock of RMII interface, **TXCLK** of FEPHY needs to be configured as

Input Mode):

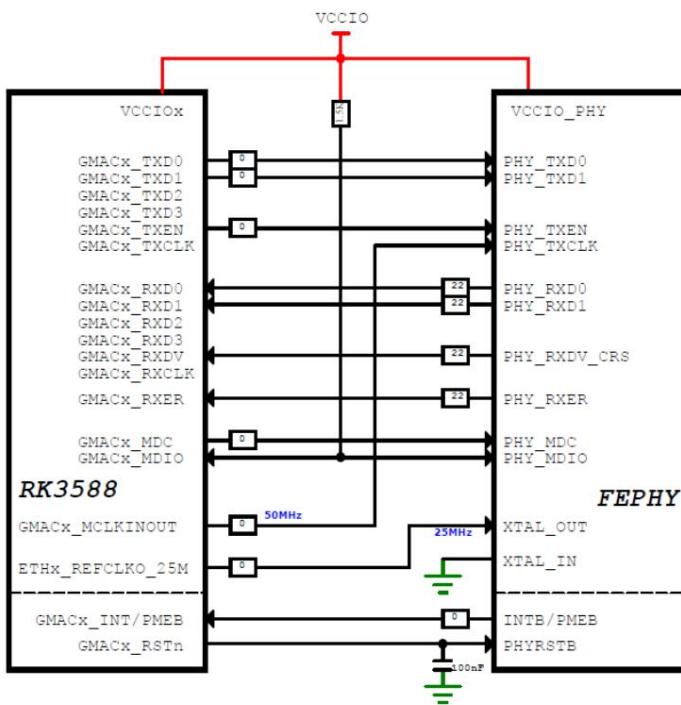


Figure 2-177 RMII connection diagram 3

RMII connection diagram 4, please see the reference diagram for the specific circuit (FEPHY working clock uses an external 25MHz crystal,

GMACx_MCLKINOUT uses input mode. The reference clock of RMII interface is provided by FEPHY. TXCLK of FEPHY

Need to be configured as output mode):

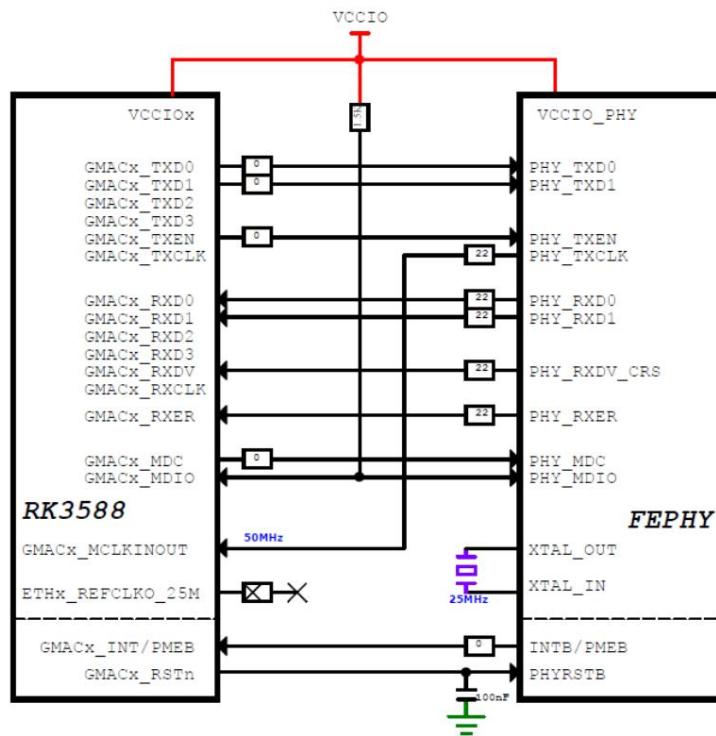


Figure 2-178 RMII connection diagram 4

RMII connection diagram 5, please see the reference diagram for the specific circuit (use the 25MHz provided by RK3588 to replace the FEPHY crystal,

GMACx_MCLKINOUT uses input mode. The reference clock of RMII interface is provided by FEPHY. TXCLK of FEPHY

Need to be configured as output mode):

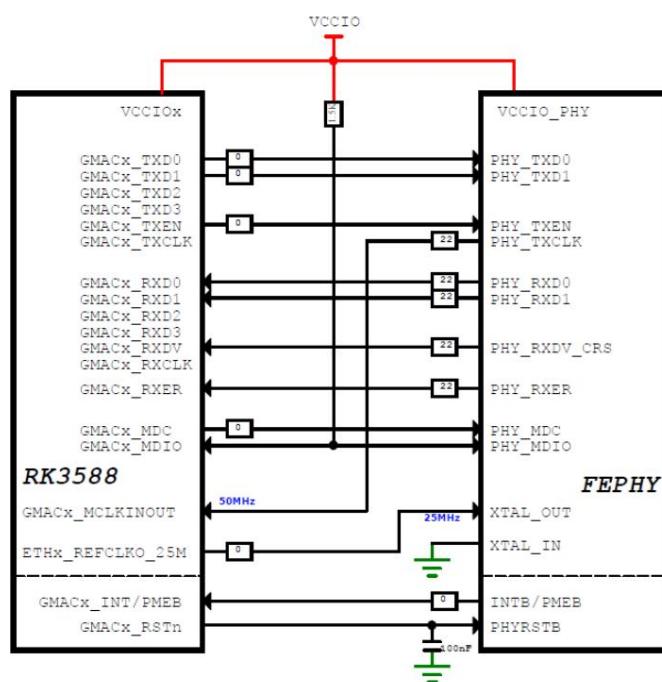


Figure 2-179 RMII connection diagram 5

ÿ In RGMII mode, the TX/RX clock path inside the RK3588 chip integrates delayline and supports adjustment; the default configuration of the reference diagram is: the timing between

TXCLK and data is controlled by MAC, and the timing between RXCLK and data is controlled by PHY (such as using RTL8211F/FI, RXCLK is enabled with 2nS delay by

default, other PHYs should pay attention to this configuration); ÿ The Reset signal of Ethernet PHY needs to be controlled by GPIO, and the GPIO level must match the PHY IO level, close to the PHY

A 100nF capacitor must be added to the pin to enhance anti-static capability. Note: The reset pin of RTL8211F/FI only supports 3.3V level;

ÿ INTB/PMEB of RTL8211F/FI is an open-drain output, and an external pull-up resistor must be added; ÿ When using an external crystal for PHY, the crystal capacitor should be selected according to the load capacitance of the actual crystal used, and the frequency deviation should be controlled within +/-20ppm

Within:

ÿ The external resistor connected to the RSET pin of RTL8211F/FI is 2.49K ohm with an accuracy of 1%. It cannot be modified at will. ÿ MDIO must be connected to an external pull-up resistor. 1.5-1.8Kohm is recommended. The pull-up power supply must be consistent with the IO power supply.

ÿ The connection of the center tap of the transformer of RTL8211F/FI must be made according to the reference diagram. If you use other Ethernet PHY, the transformer

For the connection of the center tap of the Ethernet PHY, it is recommended to refer to the reference design of each Ethernet PHY manufacturer, because different PHY manufacturers have different connection methods.

ÿ It is recommended to use a high-voltage safety capacitor for the 1000pF isolation capacitor, with sufficient electrical clearance to ensure safety from lightning strikes. ÿ

It is recommended to use a 0805 or larger package for the 75 ohm resistor on the high-voltage side of the network transformer.

ÿ Lightning protection level above 4KV requires the addition of lightning arrester tubes. Ordinary isolation transformers can only meet the 2KV level requirement.

If there is a requirement for lightning differential testing, TVS diodes need to be added between the MDI differential pairs;

ÿ Make sure the RJ45 package is consistent with the schematic diagram. RJ45 has Tab down and Tab up, and the signal order is exactly the opposite.

If using RTL8211F/FI, it is recommended to use Tab down, and the MDI order is forward;

ÿ The initial hardware configuration of PHY must match the actual requirements.

2.3.11 UART interface circuit

The RK3588 chip has 10 UART controllers and supports the following functions:

ÿ Both contain two 64-byte FIFOs for data reception and transmission;

ÿ Supports 115.2Kbps, 460.8Kbps, 921.6Kbps, 1.5Mbps, 3Mbps, 4Mbps; ÿ Supports programmable baud rate and non-integer clock

divider;

Supports interrupt-based and DMA-based modes; supports 5- to 8-bit

wide transfers. To accommodate the flexibility

of various product applications, the 10 UARTs are multiplexed across several different power domains, with the suffixes _M0/_M1/_M2 used to distinguish the multiplexing locations.

_M0, _M1, and _M2 cannot be used simultaneously; only one of these groups can be selected during allocation. It is not possible to select M0 for some signals, M1 for others, and M2 for others. This feature is not supported.

RK3588 UART interface distribution:

Table 2-46 RK3588 UART interface distribution

UART Number	Reuse	Multiplexing power domains
UART0	M0ÿM1ÿM2	M0ÿPMUIO2 M1ÿPMUIO1 M2ÿVCCIO6
UART1	M0ÿM1ÿM2	M0ÿVCCIO3 M1ÿVCCIO4 M2ÿPMUIO2

UART Number	Reuse	Multiplexing power domains
UART2	M0＼M1＼M2	M0＼PMUIO2 M1＼VCCIO2 M2＼VCCIO5
UART3	M0＼M1＼M2	M0＼VCCIO1 M1＼VCCIO5 M2＼VCCIO6
UART4	M0＼M1＼M2	M0＼VCCIO1 M1＼VCCIO5 M2＼VCCIO4
UART5	M0＼M1＼M2	M0＼VCCIO2 M1＼VCCIO5 M2＼EMMCIO
UART6	M0＼M1＼M2	M0＼VCCIO3 M1＼VCCIO4 M2＼VCCIO1
UART7	M0＼M1＼M2	M0＼VCCIO3 M1＼VCCIO5 M2＼VCCIO4
UART8	M0, M1	M0＼VCCIO6 M1＼VCCIO5
UART9	M0＼M1＼M2	M0＼VCCIO3 M1＼VCCIO6 M2＼VCCIO5

Table 2-47 RK3588 UART flow control interface distribution

UART Number	Reuse	Multiplexing power domains
UART0_RTSN UART0_CTSN	none	none
UART1_RTSN UART1_CTSN	M0 M1 M2	M0 VCCIO3 M1 VCCIO4 M2 PMUIO2
UART2_RTSN UART2_CTSN	none	VCCIO5
UART3_RTSN UART3_CTSN	none	VCCIO1
UART4_RTSN UART4_CTSN	none	VCCIO1
UART5_RTSN UART5_CTSN	M0, M1	M0 VCCIO2 M1: EMMCIO
UART6_RTSN UART6_CTSN	M0, M1	M0 VCCIO3 M1 VCCIO4
UART7_RTSN UART7_CTSN	M0, M1	M0 VCCIO3 M1 VCCIO5
UART8_RTSN UART8_CTSN	M0, M1	M0 VCCIO6 M1 VCCIO5
UART9_RTSN UART9_CTSN	M0 M1 M2	M0 VCCIO3 M1 VCCIO6 M2 VCCIO5

UART2 M0 is the Debug UART of RK3588 by default.

Adjust the power supply of the corresponding power domain according to the IO level of the UART peripheral and they must remain consistent.

The pull-up and matching design recommendations for the UART interface are shown in the table:

Table 2-48 RK3588 UART interface design

Signal	Connection method	Description (chip side)
UARTx_RX	Direct connection	UART data input
UARTx_TX	Direct connection	UART data output
UARTx_CTSn	Direct connection	UART clear to send signal
UARTx_RTScn	Direct connection	UART request to send signal

When implementing board-to-board connections through connectors, TVS devices should be reserved.

2.3.12 SPI interface circuit

In addition to the FSPI controller, the RK3588 chip also has five general-purpose SPI controllers that support the following functions:

- ÿ Supports both master and slave modes;
- ÿ Support 4, 8, and 16-bit serial data transmission;
- ÿ Supports full-duplex and half-duplex mode transmission.

Considering the flexibility of different product applications, the five SPIs are multiplexed in several different power domains, and the suffixes _M0/_M1/_M2/_M3 are used to distinguish them.

Same as multiplexing position. _M0/_M1/_M2/_M3 cannot be used at the same time. Only one group can be selected when allocating. It is not possible to select M0 for some signals and M1 for others.

Select M1, this function is not supported.

RK3588 SPI interface distribution:

Table 2-49 RK3588 SPI interface distribution

SPI number	Reuse	Multiplexing power domains
SPI0	M0 M1 M2 M3	M0 PMUIO2 M1 VCCIO6 M2 VCCIO4 M3 VCCIO5
SPI1	M0 M1 M2	M0 VCCIO3 M1 VCCIO5 M2 VCCIO1
SPI2	M0 M1 M2	M0 VCCIO4 M1 VCCIO6 M2 PMUIO1
SPI3	M0 M1 M2 M3	M0 PMUIO3 M1 VCCIO6 M2 PMUIO2 M3 VCCIO5
SPI4	M0 M1 M2	M0 VCCIO1 M1 VCCIO5 M2 VCCIO4

Adjust the power supply of the corresponding power domain according to the IO level of the SPI peripheral and they must be consistent.

SPI2 is assigned to PMIC by default for software convenience and is not recommended to be changed.

The pull-up and matching design recommendations for the SPI interface are shown in the table below:

Table 2-50 RK3588 SPI interface design

Signal	Connection method	Description (chip side)
SPIx_CLK	Direct connection	SPI clock
SPIx_MOSI	Direct connection	SPI data output (Master)
SPIx_MISO	Direct connection	SPI data input (Master)
SPIx_CS0	Direct connection	SPI Chip Select 0
SPIx_CS1	Direct connection	SPI chip select 1

When implementing board-to-board connections through connectors, TVS devices should be reserved.

2.3.13 CAN interface circuit

The RK3588 chip has three CAN controllers and supports the following functions:

- ÿ Support CAN 2.0B protocol;
- ÿ Supports 1Mbps and 8Mbps.

Considering the flexibility of different product applications, the three CANs are reused in several different power domains, and the suffixes _M0/_M1 are used to distinguish different reuses.

_M0/_M1 cannot be used at the same time. Only one of the two groups can be selected during allocation. For example, if CAN_M0 is selected, CAN_M1 cannot be selected.

RK3588 CAN interface distribution:

Table 2-51 RK3588 CAN interface distribution

CAN Number	Reuse	Multiplexing power domains
CAN0	M0, M1	M0PMUIO2 M1VCCIO2
CAN1	M0, M1	M0VCCIO5 M1VCCIO6
CAN2	M0, M1	M0VCCIO5 M1VCCIO2

Adjust the power supply of the corresponding power domain according to the IO level of the CAN peripheral and they must be consistent.

The recommended pull-up and pull-down and matching designs for the CAN interface are shown in the table below:

Table 2-52 RK3588 CAN interface design

Signal	Connection method	Description (chip side)
CANx_RX	Direct connection	CAN data input
CANx_TX	Direct connection	CAN data output

When using a connector to connect a board to a board, it is recommended to connect a resistor with a certain resistance (between 22ohm and 100ohm, depending on the specific resistance).

Test is subject to the requirements) and TVS devices should be reserved.

2.3.14 I2C Interface Circuit

The RK3588 chip has 12 I2C controllers and supports the following functions:

- ÿ Support I2C bus master mode;
- ÿ Support software programmable clock frequency and transmission rate up to 400Kbit/s;
- ÿ Supports 7-bit and 10-bit addressing modes.

Considering the flexibility of different product applications, 12 I2Cs are reused in several different power domains, with suffixes _M0/_M1/_M2/_M3/_M4

Differentiate between different multiplexing positions. _M0/_M1/_M2/_M3/_M4 cannot be used at the same time. Only one group can be selected when allocating. For example, you cannot select

I2C1_M0 was selected, and I2C1_M1 or other M* was selected.

The distribution of RK3588 I2C interfaces is shown in the following table:

Table 2-53 RK3588 I2C interface distribution

I2C Numbering	Reuse	Multiplexing power domains
I2C0	M0 M1 M2	M0PMUIO1 M1VCCIO3 M2PMUIO2
I2C1	M0 M1 M2 M3 M4	M0PMUIO2 M1PMUIO1 M2PMUIO2 M3EMMCIO M4VCCIO1
I2C2	M0 M1 M2 M3 M4	M0PMUIO2 M1VCCIO3 M2EMMCIO M3VCCIO1 M4VCCIO4
I2C3	M0 M1 M2 M3 M4	M0VCCIO1 M1VCCIO5 M2VCCIO6 M3VCCIO3 M4VCCIO2

I2C Numbering	Reuse	Multiplexing power domains
I2C4	M0~M1~M2~M3~M4	M0~VCCIO5 M1~VCCIO3 M2~PMUIO2 M3: VCCIO4 M4~VCCIO1
I2C5	M0~M1~M2~M3~M4	M0~VCCIO5 M1~VCCIO6 M2~PMUIO6 M3: VCCIO4 M4~VCCIO3
I2C6	M0~M1~M2~M3~M4	M0~PMUIO2 M1~VCCIO1 M2~PMUIO3 M3~VCCIO6 M4~VCCIO5
I2C7	M0~M1~M2~M3	M0~VCCIO1 M1~VCCIO3 M2~PMUIO5 M3~VCCIO6
I2C8	M0~M1~M2~M3~M4	M0~VCCIO2 M1~VCCIO3 M2~PMUIO4 M3~VCCIO6 M4~VCCIO5
HDMI_TX0_I2C	M0~M1~M2	M0~VCCIO6 M1~PMUIO2 M2~VCCIO5
HDMI_TX1_I2C	M0~M1~M2	M0~VCCIO3 M1~VCCIO5 M2~VCCIO4
HDMI_RX_I2C	M0~M1~M2	M0~PMUIO2 M1~VCCIO5 M2~VCCIO4

HDMI_TXx_SCL/HDMI_Txx_SDA/ HDMI_RX_SCL/HDMI_RX_SDA is the I2C/DDC of HDMI TX controller

Bus is a dedicated bus.

Adjust the power supply of the corresponding power domain according to the IO level of the I2C peripheral and they must be consistent.

I2C signals SCL and SDA require external pull-up resistors. Depending on the bus load, select resistors of different resistance values. 2.2kohm is recommended.

Pull-up resistor.

The addresses of the devices on the I2C bus should not conflict, and the pull-up power supply must be consistent with the power supply.

The pull-up and matching design recommendations for the I2C interface are shown in the table below:

Table 2-54 RK3588 I2C interface design

Signal	Connection method	Description (chip side)
I2Cx_SCL	Direct connection	I2C clock
I2Cx_SDA	Direct connection	I2C data output/input

When implementing board-to-board connections through connectors, TVS devices should be reserved.

2.3.15 PWM Interface Circuit

The RK3588 chip has integrated 4 independent PWM controllers, each controller has 4 channels, and can have up to 16 PWM channels.

Channel, supports the following functions:

Support capture mode;

Support continuous mode or one-time mode;

Optimized for infrared applications of PWM3, PWM7, PWM11 and PWM15;

Each channel has two clock input options, one is a fixed frequency from the crystal oscillator, and the other is a frequency divided from the PLL bus.

Configurable.

Considering the flexibility of different product applications, 16 PWMs are multiplexed in several different power domains, and the suffixes _M0/_M1 are used to distinguish different multiplexed domains.

Use location.

The distribution of RK3588 PWM interfaces is shown in the following table:

Table 2-55 RK3588 PWM interface distribution

PWM number	Reuse	Multiplexing power domains
PWM0	M0 M1 M2	M0:PMUIO2 M1:VCCIO1 M2:VCCIO4
PWM1	M0 M1 M2	M0:PMUIO2 M1:VCCIO1 M2:VCCIO4
PWM2	M0 M1 M2	M0:PMUIO2 M1:VCCIO5 M2:VCCIO3
PWM3_IR	M0 M1 M2 M3	M0:PMUIO2 M1:VCCIO5 M2:VCCIO1 M3: VCCIO4
PWM4	M0, M1	M0:PMUIO2 M1:VCCIO3
PWM5	M0 M1 M2	M0:PMUIO1 M1:PMUIO2 M2:VCCIO3
PWM6	M0 M1 M2	M0:PMUIO2 M1:VCCIO6 M2:VCCIO3
PWM7_IR	M0 M1 M2 M3	M0:PMUIO2 M1:VCCIO2 M2:VCCIO1 M3:VCCIO3
PWM8	M0 M1 M2	M0:VCCIO5 M1:VCCIO2 M2:VCCIO2
PWM9	M0 M1 M2	M0:VCCIO5 M1:VCCIO1 M2:VCCIO5
PWM10	M0 M1 M2	M0:VCCIO5 M1:VCCIO2 M2:VCCIO5
PWM11_IR	M0 M1 M2 M3	M0:VCCIO5 M1:VCCIO6 M2:VCCIO1 M3:VCCIO3

PWM number	Reuse	Multiplexing power domains
PWM12	M0, M1	M0_VCCIO5 M1_VCCIO6
PWM13	M0_M1_M2	M0_VCCIO5 M1_VCCIO6 M2_VCCIO4
PWM14	M0_M1_M2	M0_VCCIO5 M1_VCCIO6 M2_VCCIO4
PWM15_IR	M0_M1_M2	M0_VCCIO5 M1_VCCIO6 M2_VCCIO1

According to the IO level of the PWM peripheral, adjust the power supply of the corresponding power domain and keep it consistent;

When using a connector to connect a board to a board, it is recommended to connect a resistor with a certain resistance (between 22ohm and 100ohm, depending on the specific resistance).

SI test shall prevail), and TVS devices shall be reserved;

When the infrared receiver signal is input, please pay attention to the following:

In standby mode, to support the infrared receiver head wake-up, and considering low power consumption (i.e. VDD_LOGIC power supply power-off solution), only

Select PWM3 as the infrared receiver input;

The infrared receiver needs to be powered by VCC3V3_PMU;

The power supply of the infrared receiver requires a 22-100ohm resistor and a capacitor of 10uF or more for RC filtering;

The infrared receiver uses 38KHz by default. If you change to other frequencies, the software needs to be adjusted accordingly.

The output level of the infrared receiver must match the IO level of RK3588;

It is recommended to connect a 22 ohm resistor and a 1nF capacitor to the infrared receiver output pin, and then connect it to RK3588 to enhance the anti-static surge capability.

force;

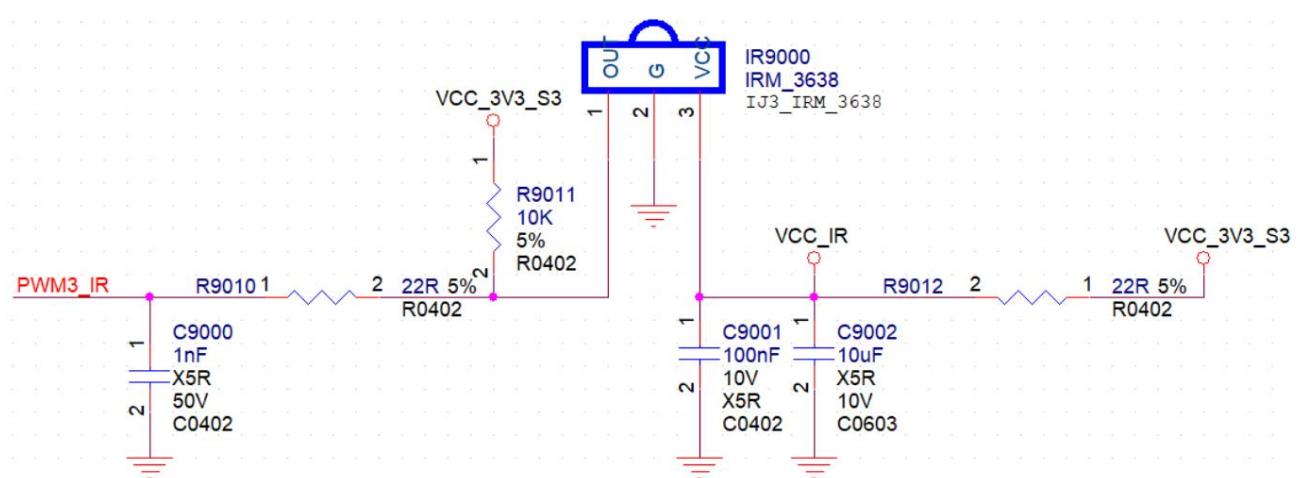


Figure 2-180 Infrared receiver circuit

When arranging the infrared receiver, it should be kept away from the wireless module antenna, such as the WiFi antenna, to avoid affecting the infrared when transmitting wireless data.

Signal reception;

The infrared receiver should be placed away from direct light from the LED light source on the board to prevent the LED flickering frequency from affecting infrared reception;

It is recommended that the IR signal be ground-enclosed throughout the entire process. If ground-enclosed processing is not possible, it is recommended that the spacing between it and other signals be greater than or equal to 2 times the line width.

2.3.16 How to handle the pins of unused modules in RK3588

Please see the document "RK3588 Methods for Processing Unused Pins_V1.0_20211228".

3 PCB Design Recommendations

3.1 PCB stackup design

In order to reduce reflections during high-speed signal transmission, impedance matching must be maintained at the signal source, receiver, and transmission line.

The specific impedance of a single-ended signal line depends on its line width and its relative position to the reference plane.

The line width/line spacing depends on the selected PCB stacking structure. Since the minimum line width and minimum line spacing depend on the PCB type and cost requirements,

To meet this limitation, the selected PCB stackup structure must be able to achieve all impedance requirements on the board, including inner and outer layers, single-ended and differential lines, etc.

Layer definition design principles:

The adjacent layer of the main chip is the ground plane, which provides a reference plane for device surface wiring;

ŷ All signal layers should be as close to the ground plane as possible;

ŷ Avoid placing two signal layers directly adjacent to each other;

ŷ The main power supply should be as close to it as possible;

ŷ In principle, a symmetrical structure design should be adopted. The meaning of symmetry includes: dielectric layer thickness and type, copper foil thickness, pattern distribution type

(large copper foil layer, circuit layer) symmetry.

PCB layer definition recommendation: When setting up specific PCB layers, you should flexibly follow the above principles and determine the appropriate layers based on actual needs.

When setting the layers, avoid blindly copying them. The following are some common layer arrangement recommendations for your reference.

The crosstalk between layers can be reduced by increasing the spacing between adjacent wiring layers.

Consider the ground level or provide necessary bridging measures.

RK3588 currently uses 10 layers of 1st order, 10 layers of 2nd order, 8 layers of through-hole PCB stacking. The following stacking structure is used as an example to provide customers with

If you choose other types of stack-up structures, please re-check the specifications given by the PCB manufacturer.

New calculated impedance.

3.1.1 10 -layer 1- step HDI board stackup

In a 10-layer, 1-step stackup design, the reference plane for the top signal L1 is L2, and the reference plane for the bottom signal L10 is L9.

The stackup is TOP-Signal/Gnd/Gnd/Power-Signal-Gnd/Power-Gnd/Power-Gnd/Power-Signal-Gnd-Bottom. For L1, L2, L9, and L10, 1oz is recommended, and other inner layers use HoZ. The figure below shows a reference stackup and characteristic impedance trace width for a 1.6mm thick board.

Customer Name:				Total Thickness:	1.6 +/- 0.10mm		
Customer P/N:				Measure from	SM-SM		
Layer No.	sig/pln	Copper thk. before process (oz)	Construction	Finished thikness (um)	Finished thikness (mil)	Tolerance	Dk (1GHz)
S/M				25.40	1.00	+/-10	3.5
0 1	Top	1	PP 1080X1(RC65%)	30.48	1.20	+/-10	
1 2	Sig/Gnd	1	PP 1080X1(RC65%)	69.00	2.72	+/-10	4
2 3	Gnd/Pow	H	Core	30.48	1.20	+/-10	
3 4	Sig	H	PP 1080X1(RC65%)	69.00	2.72	+/-10	4
4 5	Gnd/Pow	H	Core	15.24	0.60	+/-10	
5 6	Sig	H	PP 1080X1(RC65%)	115.00	4.53	+/-10	4.2
6 7	Gnd/Pow	H	Core	69.00	2.72	+/-10	
7 8	Sig	H	PP 1080X1(RC65%)	15.24	0.60	+/-10	4
8 9	Gnd	1	Core	698.50	27.50	+/-10	4.2
9 10	Bottom	1	PP 1080X1(RC65%)	69.00	2.72	+/-10	
10 S/M			PP 1080X1(RC65%)	115.00	4.53	+/-10	4.2
				15.24	0.60	+/-10	
				69.00	2.72	+/-10	4
				30.48	1.20	+/-10	
				69.00	2.72	+/-10	4
				30.48	1.20	+/-10	
				25.40	1.00	+/-10	3.5
				总计：	1606.65	63.25	

Figure 3-1 10-layer 1-step HDI board stackup

特性阻抗

阻抗控制层	阻抗参考层		阻抗值 (OHM)		阻抗值控制范围	原始阻抗		调整后阻抗		
	TOP	BOT	原要求阻值	调整后阻值		mil		mil		
						线宽	线宽	线宽	线宽	
L2	L1	L3	40	40	+/-5ohm	3.50		3.20		
L4	L3	L5	40	40	+/-5ohm	3.28		4.00		
L8	L7	L9	40	40	+/-5ohm	4.30		4.00		
L1		L2	50	50	+/-5ohm	4.00		4.30		
L1		L3	50	50	+/-5ohm	20.00		12.00		
L4	L3	L5	50	50	+/-5ohm	4.00		2.50		
L8	L7	L9	50	50	+/-5ohm	4.00		2.50		
L10	L9		50	50	+/-5ohm	4.00		4.30		

差分阻抗

阻抗控制层	阻抗参考层		阻抗值 (OHM)		阻抗值控制范围	原始阻抗			调整后阻抗			
	TOP	BOT	原要求阻值	调整后阻值		mil			mil			
						线宽	/	间距	线宽	/	间距	
L1		L2	100	100	+/-10ohm	3.40	/	4.60	3.30	/	4.70	
L4	L3	L5	100	100	+/-10ohm	2.55	/	5.45	2.50	/	5.50	
L8	L7	L9	100	100	+/-10ohm	2.70	/	5.30	2.50	/	5.50	
L10	L9		100	100	+/-10ohm	3.40	/	4.60	3.30	/	4.70	
L1		L2	90	90	+/-10ohm	4.00	/	4.00	4.00	/	4.00	
L4	L3	L5	90	90	+/-10ohm	3.15	/	4.85	2.80	/	5.00	
L8	L7	L9	90	90	+/-10ohm	3.30	/	4.70	2.80	/	5.00	
L10	L9		90	90	+/-10ohm	4.00	/	4.00	4.00	/	4.00	
L1		L2	85	85	+/-10ohm	5.00	/	4.00	4.60	/	4.40	
L10	L9		85	85	+/-10ohm	5.00	/	4.00	4.60	/	4.40	
L2	L1	L3	80	80	+/-10ohm	3.65	/	5.70	3.00	/	6.35	
L8	L7	L9	80	80	+/-10ohm	3.80	/	4.00	3.60	/	4.40	

Figure 3-2 Impedance reference values for a 10-layer, first-order HDI board

3.1.2 10 -layer 2- stage HDI board stackup

In a 10-layer, 2-step stackup design, the reference plane for the top signal L1 is L2, and the reference plane for the bottom signal L10 is L9.

The stack is TOP-Gnd-Signal-Gnd-Power-Signal/Pow -Gnd-Signal-Gnd-Bottom, where L1, L2, L3, L8, L9, L10,

It is recommended to use 1oz and HoZ for other inner layers. The figure below shows the reference stackup and characteristic impedance line width for a 1.6mm thick board.

Customer Name:				Total Thickness:	1.6 +/- 0.10mm			
Customer P/N:				Measure from	SM~SM			
Layer No.	sig/pln	Copper thk. before process (oz)	Construction		Finished thikness (um)	Finished thikness (mil)	Tolerance	Dk (1GHz)
S/M					25.40	1.00	+/-10	3.5
1	Top	1		PP 1080X1(RC65%)	30.48	1.20	+/-10	
2	Gnd	1		PP 1080X1(RC70%)	66.00	2.60	+/-10	4
3	Sig	1		PP 1080X1(RC70%)	30.48	1.20	+/-10	
4	Gnd	H		PP 1080X1(RC70%)	82.00	3.23	+/-10	4
5	Pow	H	Core		15.24	0.60	+/-10	
6	Pow/Sig	H	PP 1080X1(RC70%)		400.00	15.75	+/-10	4.2
7	Gnd	H	Core		15.24	0.60	+/-10	
8	Sig	1	PP 1080X1(RC70%)		82.00	3.23	+/-10	
9	Gnd	1	PP 1080X1(RC70%)		30.48	1.20	+/-10	
10	Bottom	1	PP 1080X1(RC65%)		66.00	2.60	+/-10	4
S/M					30.48	1.20	+/-10	
					25.40	1.00	+/-10	3.5
					总计:	1636.63	64.43	

Figure 3-3 10-layer 2-stage HDI board stackup

特性阻抗

阻抗控制层	阻抗参考层		阻抗值 (OHM)		阻抗值控制范围	原始阻抗		调整后阻抗		
	TOP	BOT	原要求阻值	调整后阻值		mil		mil		
						线宽	线宽	线宽	线宽	
L3	L2	L4	45	45	+/-5ohm	3.00		3.10		
L8	L7	L9	45	45	+/-5ohm	3.00		3.10		
L1		L3	50	50	+/-5ohm	20.00		12.00		
L1		L2	50	50	+/-5ohm	4.0/4.7		4.20		
L3	L2	L4	50	50	+/-5ohm	2.4/4.0		2.60		
L6	L5	L7	50	50	+/-5ohm	3.90		3.90		

差动阻抗

阻抗控制层	阻抗参考层		阻抗值 (OHM)		阻抗值控制范围	原始阻抗		调整后阻抗		
	TOP	BOT	原要求阻值	调整后阻值		mil		mil		
						线宽	间距	线宽	间距	
L1		L2	85	85	+/-10ohm	4.40	/ 3.00	4.20	/ 3.50	
L8	L7	L9	85	85	+/-10ohm	3.30	/ 4.70	3.20	/ 4.80	
L1		L2	90	90	+/-10ohm	4.00	/ 3.60	3.80	/ 3.80	
L3	L2	L4	90	90	+/-10ohm	2.70	/ 5.50	2.90	/ 5.30	
L3	L2	L4	90	90	+/-10ohm	2.40	/ 4.40	2.70	/ 4.10	
L1		L2	100	100	+/-10ohm	3.50	/ 4.50	3.30	/ 4.70	
L10	L9		100	100	+/-10ohm	3.50	/ 4.50	3.30	/ 4.70	
L3	L2	L4	100	100	+/-10ohm	2.20	/ 5.80	2.50	/ 5.50	
L8	L7	L9	100	100	+/-10ohm	2.20	/ 5.80	2.50	/ 5.50	

Figure 3-4 Impedance reference values for a 10-layer, second-order HDI board

3.1.3 8-layer PTH board stackup

In the 8-layer PTH board stackup design, the reference plane of the top layer signal L1 is L2, and the reference plane of the bottom layer signal L8 is L7.

It is TOP-Gnd-Power-Power/Signal-Gnd-Signal-Gnd-Bottom, and it is recommended to use 1oz for all.

The figure below shows the reference stackup and characteristic impedance line width for a 1.6mm thick board.

8层通孔1.6+-0.16mm				Impedance	40 ohm	50 ohm	80 ohm	85 ohm	90 ohm	100 ohm
Layer	Mother Board	Typical layer thickness (mil)	Dielectric Constant	DF	Reference Layer	Design W(mil)				
L1	Solder Mask	1.10			L1->L2	5	3.4	4->4	3.7->4.3	3.3->4.7
	1/3oz+plating	1.20			L1->L3		22			3->8
	Prepreg (106)	2.10	4.00	0.019						
L2	copper	1.20								
	Core	10.00	4.2	0.015						
L3	copper	1.20								
	Prepreg (1080)	2.70	4.00	0.019						
L4	copper	1.20			L4->L3/L5	5.5	3.5	3.8->4.2	3.5->4.5	3.1->4.9
	Core	22.00	4.2	0.015						3->8
L5	copper	1.20								
	Prepreg (1080)	2.70	4.00	0.019						
L6	copper	1.20			L6->L5/L7	5	3.2	3.8->4.2	3.4->4.6	3.0->5.0
	Core	10.00	4.2	0.015						3->10
L7	copper	1.20								
	Prepreg (106)	2.10	4.00	0.019						
L8	1/3oz+plating	1.20			L8->L7	5	3.4	4->4	3.7->4.3	3.3->4.7
	Solder Mask	1.10								3->8
		63.40								
		1.61								

Figure 3-5 8-layer PTH board stackup

Impedance	40 ohm	50 ohm	80 ohm	85 ohm	90 ohm	100 ohm
Reference Layer	Design W(mil)					
L1->L2	5	3.4	4->4	3.7->4.3	3.3->4.7	3->8
L1->L3		22				
L4->L3/L5	5.5	3.5	3.8->4.2	3.5->4.5	3.1->4.9	3->8
L6->L5/L7	5	3.2	3.8->4.2	3.4->4.6	3.0->5.0	3->10
L8->L7	5	3.4	4->4	3.7->4.3	3.3->4.7	3->8

Figure 3-6 Impedance reference values for an 8-layer PTH board

The following figure shows the reference stackup and characteristic impedance line width for a 1.0mm thick board:

8层通孔 1.0+/-0.1mm				
Layer	Mother Board	Typical layer thickness (mil)	Dielectric Constant	DF
	Solder Mask	1.10		
L1	1/3oz+plating	1.20		
	Prepreg (106)	2.10	4.00	0.019
L2	copper	1.20		
	Core	5.00	4.2	0.015
L3	copper	1.20		
	Prepreg (2116)	3.50	4.00	0.019
L4	copper	1.20		
	Core	8.00	4.2	0.015
L5	copper	1.20		
	Prepreg (2116)	3.50	4.00	0.019
L6	copper	1.20		
	Core	5.00	4.2	0.015
L7	copper	1.20		
	Prepreg (106)	2.10	4.00	0.019
L8	1/3oz+plating	1.20		
	Solder Mask	1.10		
		41.00		
		1.04		

Figure 3-7 8-layer PTH board stackup

Impedance	40 ohm	50 ohm	80 ohm	85 ohm	90 ohm	100 ohm
Reference Layer	Design W(mil)					
L1->L2	5	3.4	4->4	3.7->4.3	3.3->4.7	3->8
L1->L3		13				
L4->L3/L5	5.5	3.8	4.1->3.9	3.7->4.3	3.4->4.6	3.2->7.8
L6->L5/L7	5	3	3.9->4.1	3.5->4.5	3.2->4.8	3->10
L8->L7	5	3.4	4->4	3.7->4.3	3.3->4.7	3->8

Figure 3-8 Impedance reference values for an 8-layer PTH board

3.1.4 RK3588 Fan-Out Design

Ball fan-out design of the outer two circles

The signal of the second circle can be routed out from the middle of the two balls with a 4mil line width.

It is recommended to set up a grid and run the line out from the middle of the two balls.

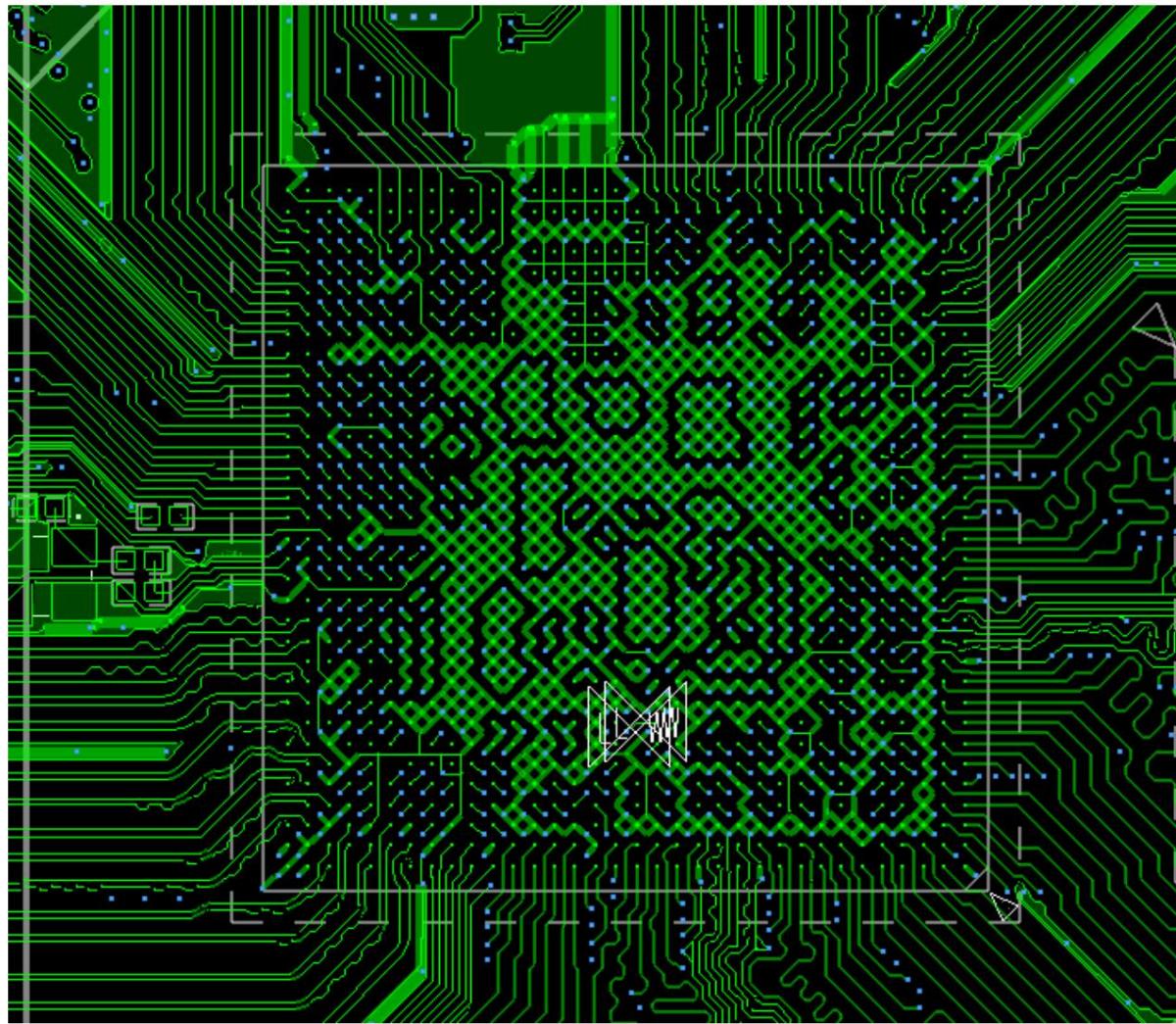


Figure 3-9 RK3588 fan-out diagram 1

Inner circle ball fan-out design

If the first and second circle signals are used, then starting from the third circle, you need to change the layer to the inner layer. Be sure to change the layer via rules and build

It is recommended to place 2-4 rows of layer-changing vias, and leave one row empty without placing layer-changing vias, leaving as large a channel as possible for the ground plane and the power plane.

As shown in the figure below, the ground plane has copper cladding, with multiple channels connected to the outside ground, which is beneficial to SI/PI and heat dissipation.

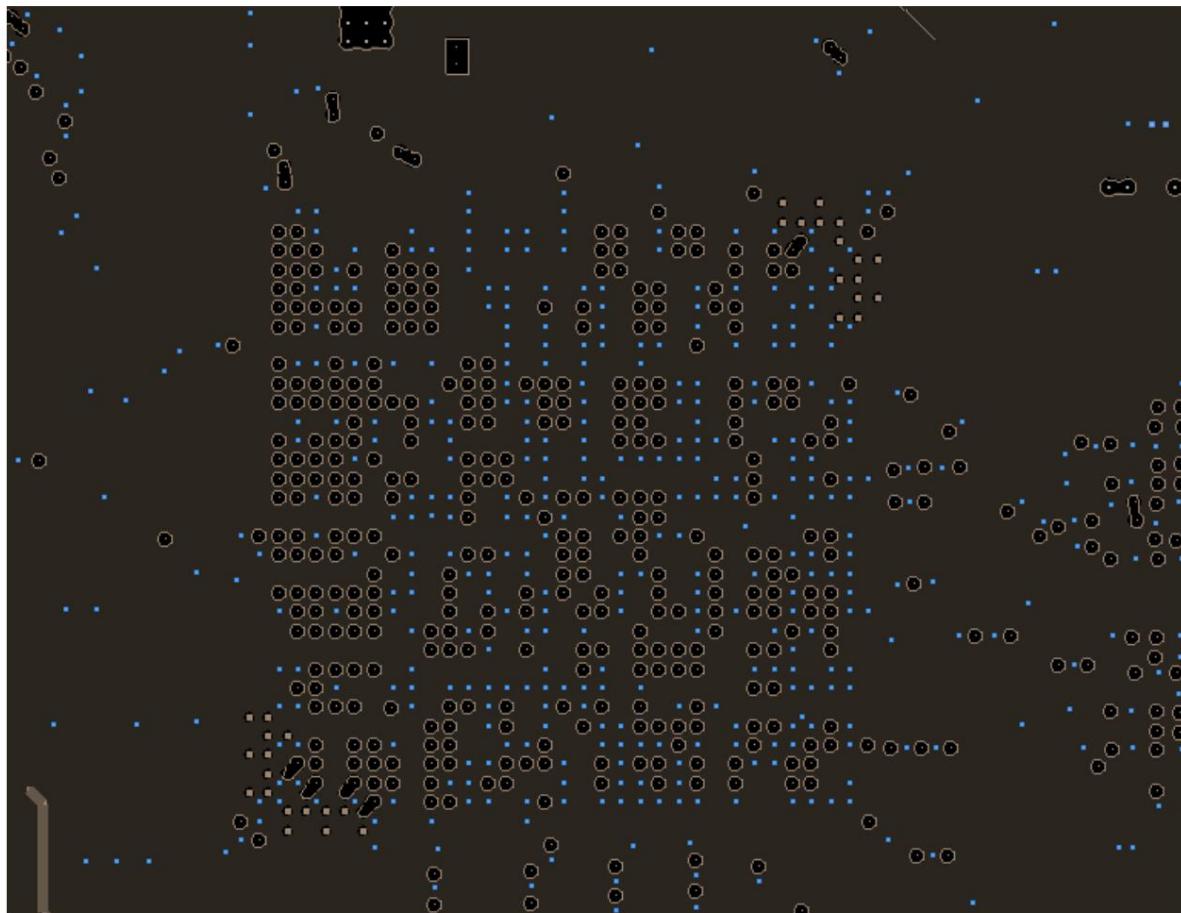


Figure 3-10 RK3588 fan-out diagram 2

As shown in the figure below, the copper coverage of the power layer is regular. The vias are placed in a regular manner to make the various power supplies have as large a copper coverage channel as possible, effectively improving the power supply.

Electricity quality.

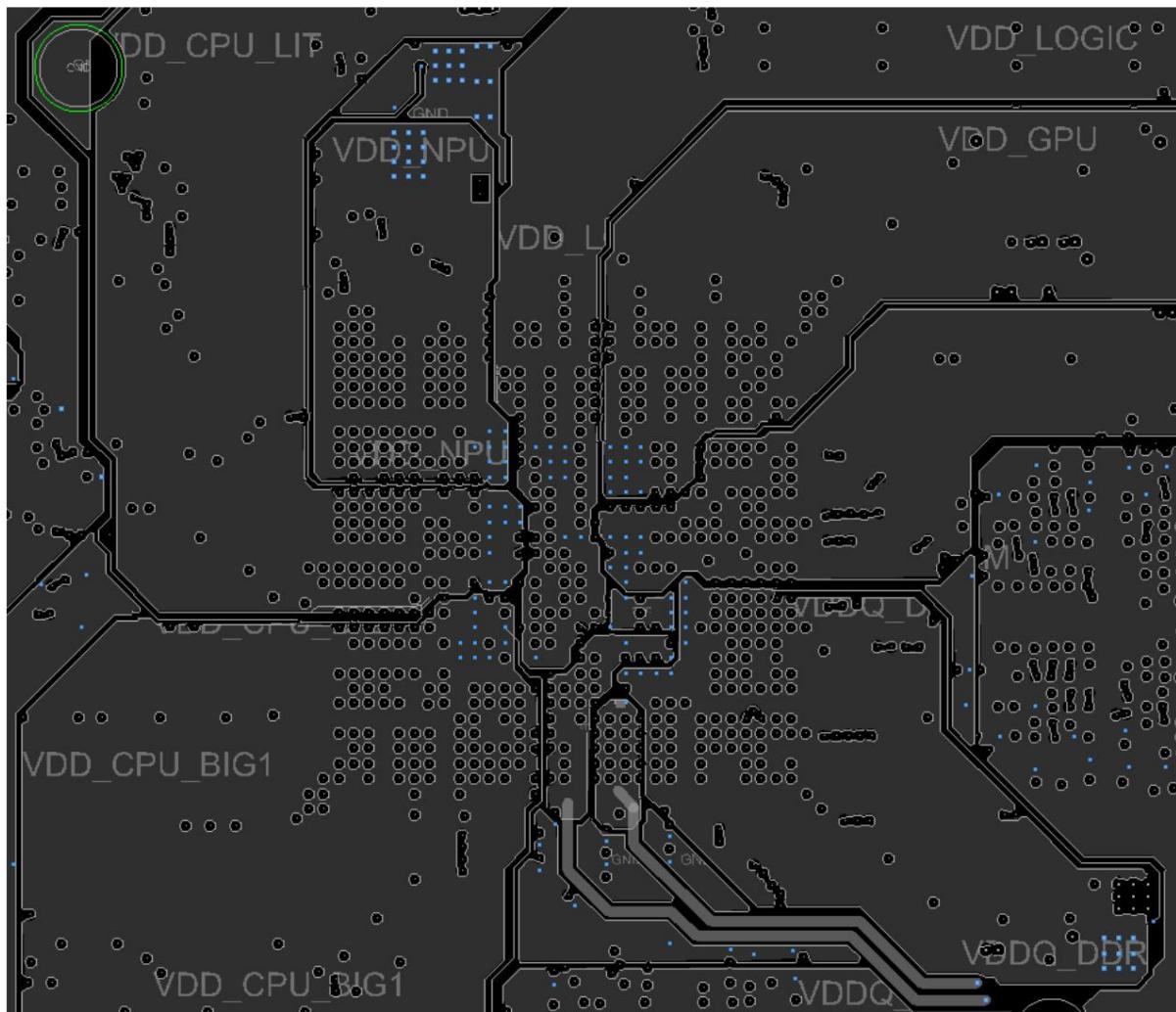


Figure 3-11 RK3588 fan-out diagram 3

As shown in the figure below, the bottom layer routing (the inner layer routing is similar), the layer-changing via is set according to the grid and placed in the middle of the ball.

The fan-out is 3.5mil wide.

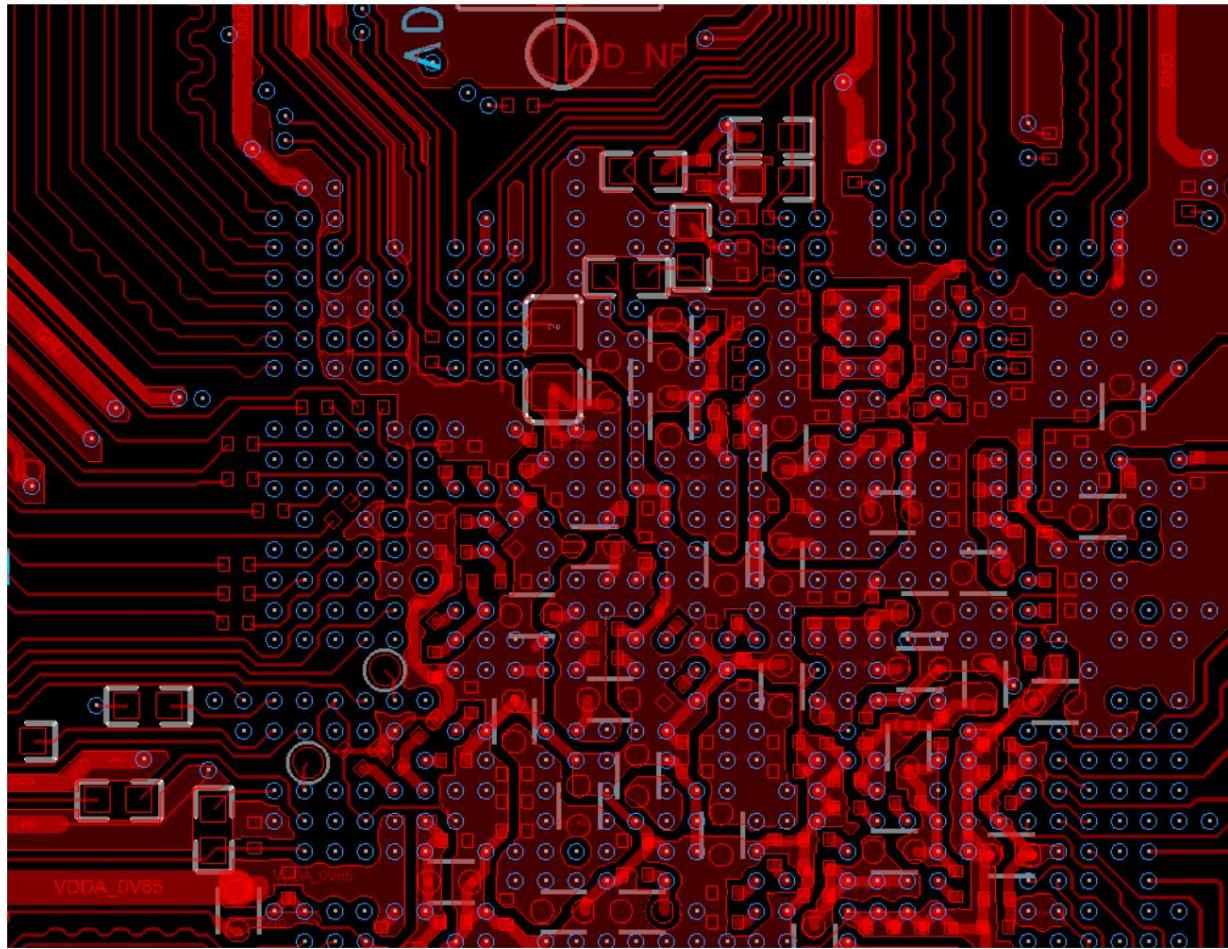


Figure 3-12 RK3588 fan-out diagram 4

3.2 General Wiring Recommendations

(1) The trace length should include vias and packages.

(2) The intra-differential pair delay difference refers to the delay difference between the two traces of the same differential signal pair; while the inter-differential pair delay difference refers to the delay difference between the two traces of different differential signals.

The signal spacing refers to the air spacing.

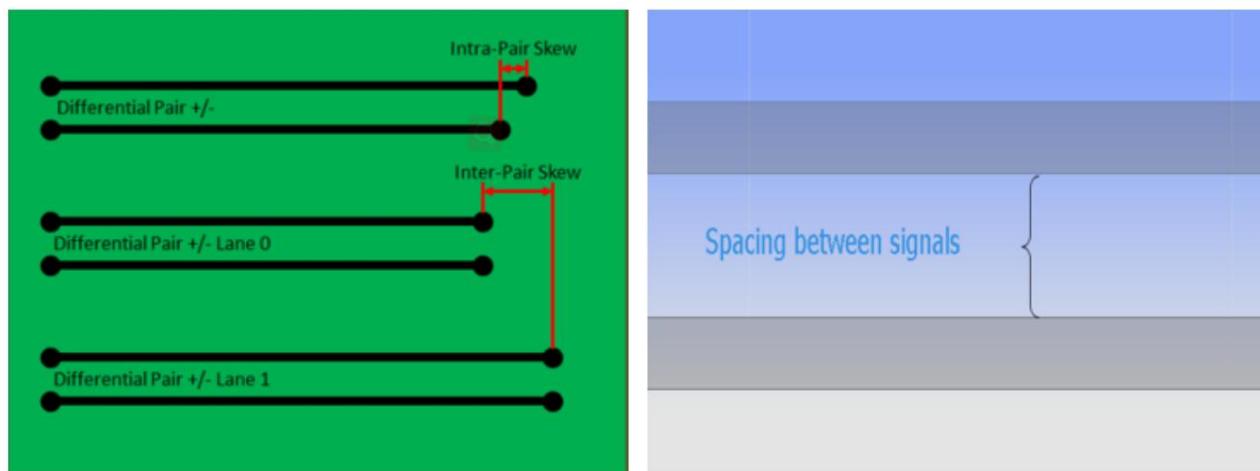


Figure 3-13

(3) The routing should have a complete and continuous reference layer plane.

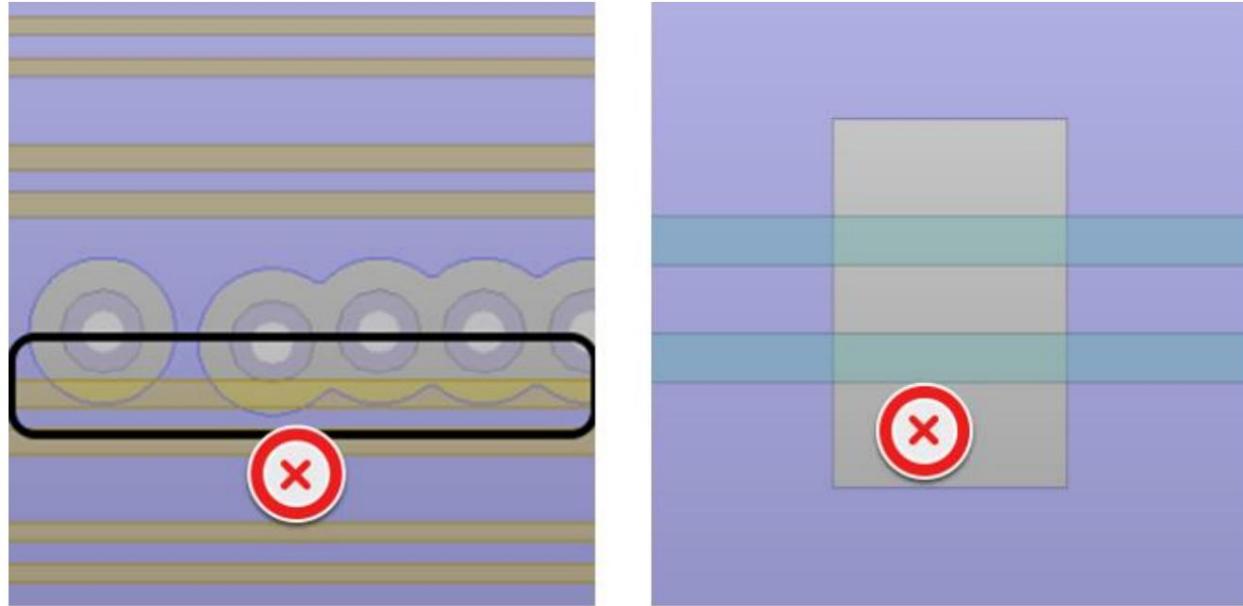


Figure 3-14

(4) Since the solder pads of the surface mount device will cause the impedance to decrease, in order to reduce the impact of the impedance mutation, it is recommended to press the solder pad directly below the surface mount pad.

The common surface mount components include capacitors, ESD, common mode suppression inductors, connectors, etc.

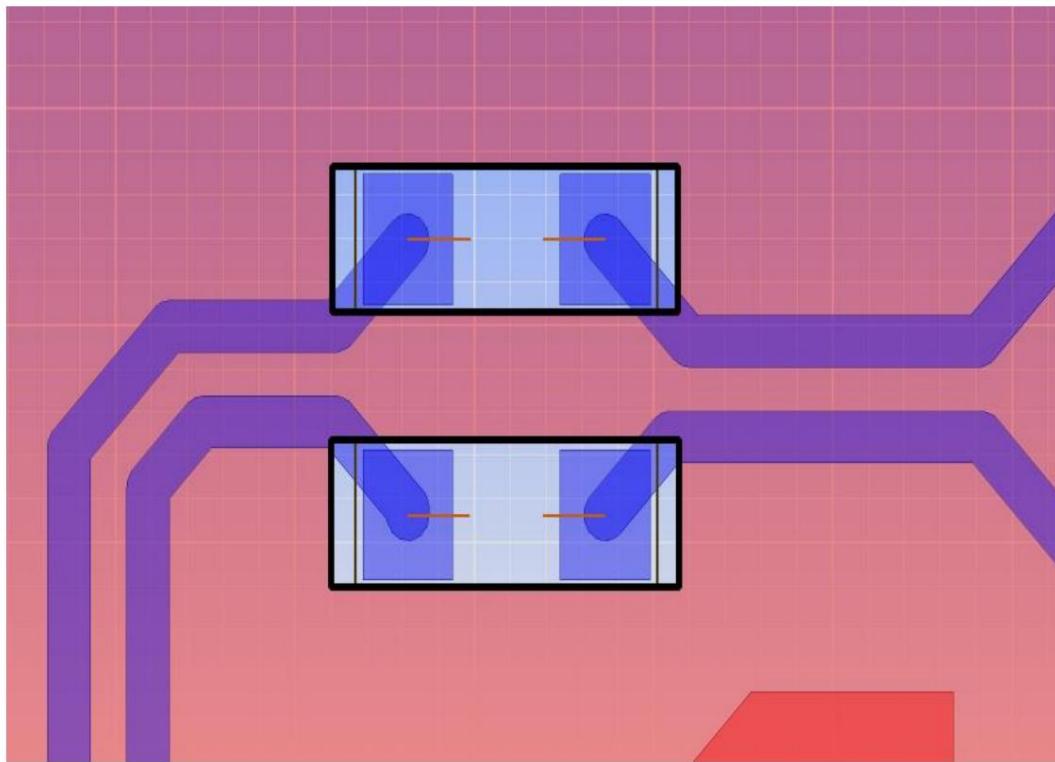


Figure 3-15

(5) It is recommended that the distance between the traces and the ground copper foil on the same layer should be at least 4 times the trace width.

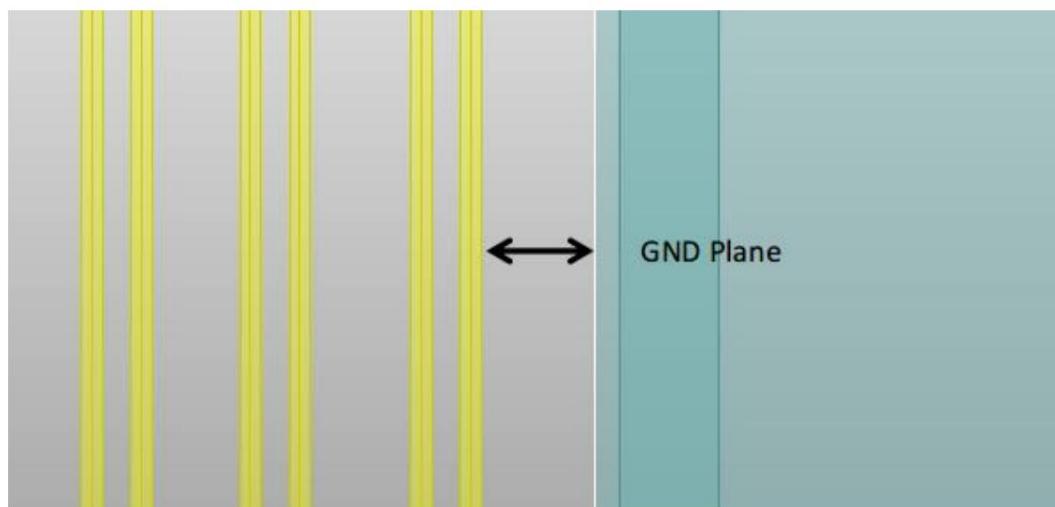


Figure 3-16

(6) Avoid the via stub effect, especially when the stub length exceeds 12mil. It is recommended to evaluate the effect of the via stub on signal integrity through simulation.

The influence of sex.



Figure 3-17

(7) Avoid high-speed signal cross-zone. It is recommended that high-speed signals be at least 40 mils away from the edge of the reference plane.

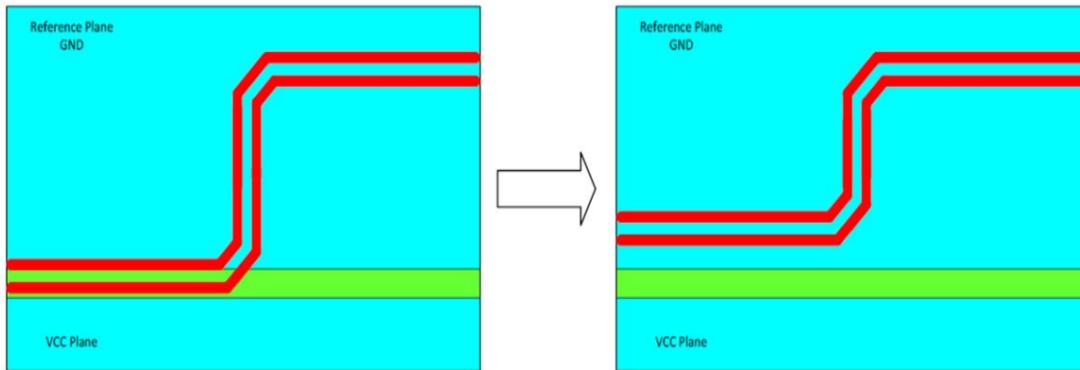


Figure 3-18

(8) It is recommended not to place test points on high-speed signals.

(9) When routing, try to minimize corners. It is recommended to use 135 degrees instead of 90 degrees.

(10) Place the coupling capacitor as close to the connector as possible.

(11) The series resistor should be placed close to the sending device, such as the series resistor on the eMMC clock signal, which is recommended to be placed close to the CPU side.

(within 400 mil).

(12) It is recommended to drill a ground through hole on each ground pad of the IC (such as eMMC particles, FLASH particles, etc.).

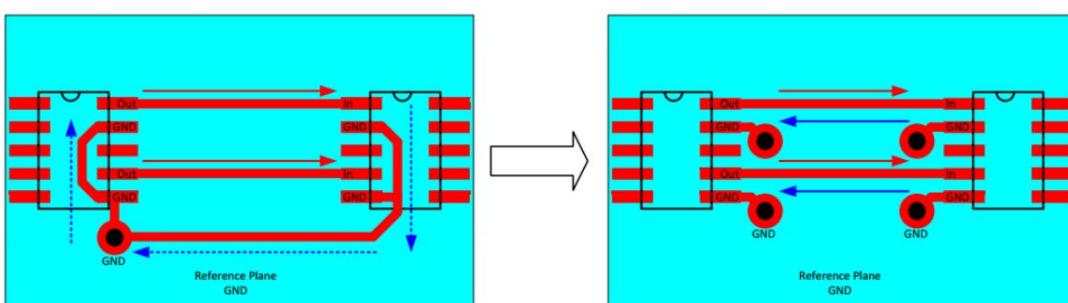


Figure 3-19

(13) Avoid using clock devices (such as crystals, crystal oscillators, clock generators, clock distributors), switching power supplies, magnetic devices, plug-ins, etc.

Peripheral wiring such as vias.

(14) Remove all non-functional pads.

(15) It is recommended that a ground through hole be drilled for each ground pad of the ESD device, and the through hole should be as close to the pad as possible.

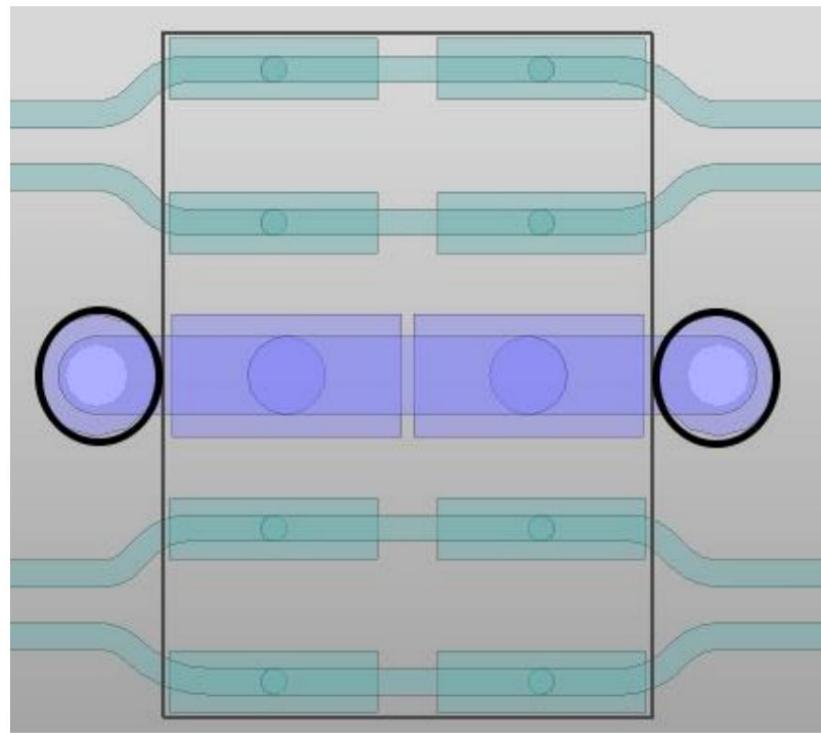
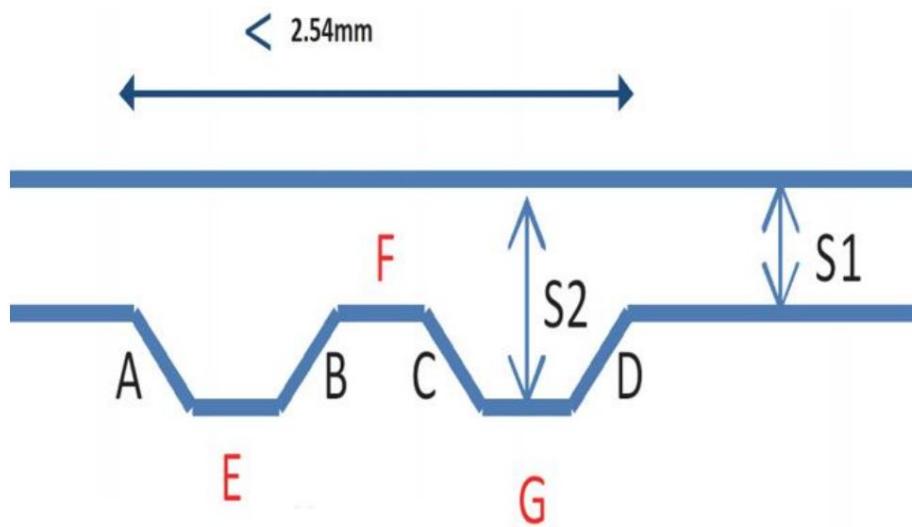


Figure 3-20

(16) Differential signals require equal length within a pair, that is, the delay difference between P and N should be as small as possible. Therefore, when there is a delay between the differential lines P and N,

When there is a delay difference, compensate for it by winding the wires nearby. Pay special attention to the winding dimensions, which should meet the requirements shown in the figure below to reduce the impact of impedance changes.



Recommended dimensions: $A=B=C=D$, $E=F=G=3W$ (W =trace width) and $S2 < 2S1$

Figure 3-21

(17) If there is unequal length (within 300 mils) within the differential line pair, make winding compensation as soon as possible.

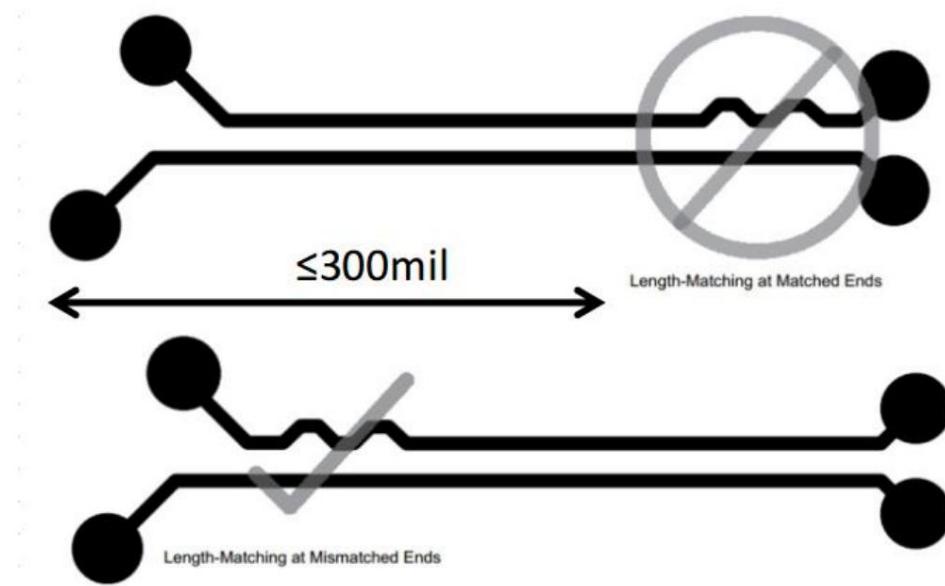


Figure 3-22

(18) When the routing layer is changed and the reference layer before and after the layer change is the ground plane, a companion via needs to be placed next to the signal via to ensure the return current path.

For differential signals, signal vias and return vias should be placed symmetrically; for single-ended signals, it is recommended to place them next to the signal vias.

Place a return via on the side to reduce crosstalk between vias.

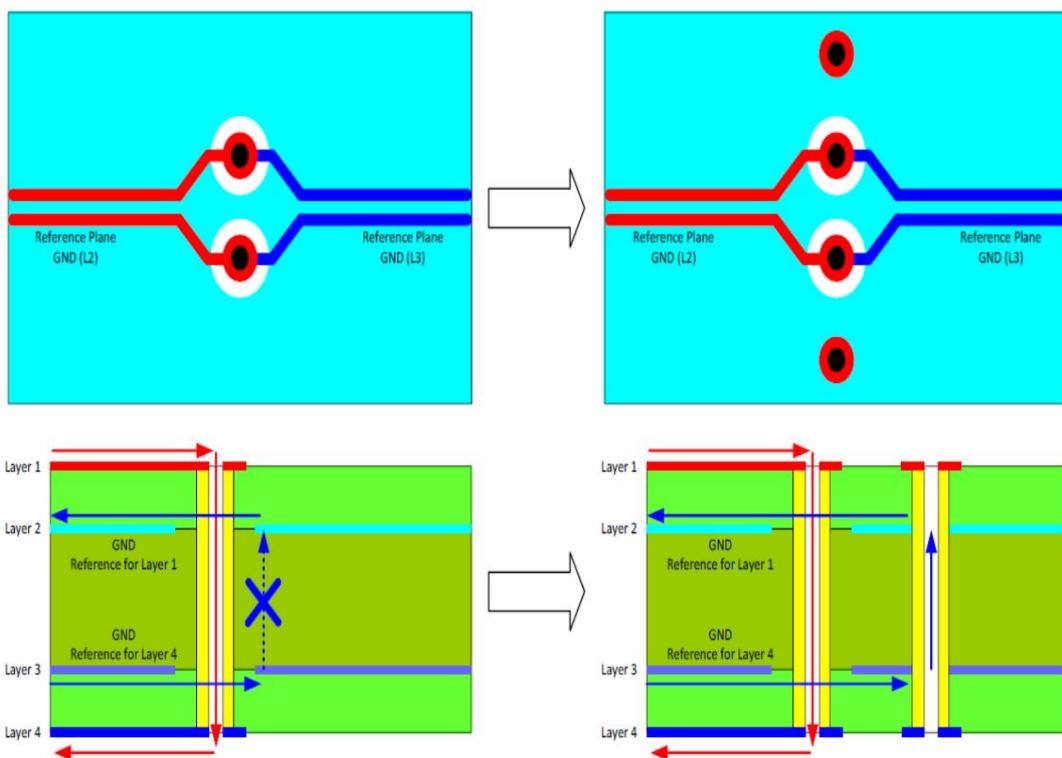


Figure 3-23



Figure 3-24

(19) The differential pair routing should be symmetrical.

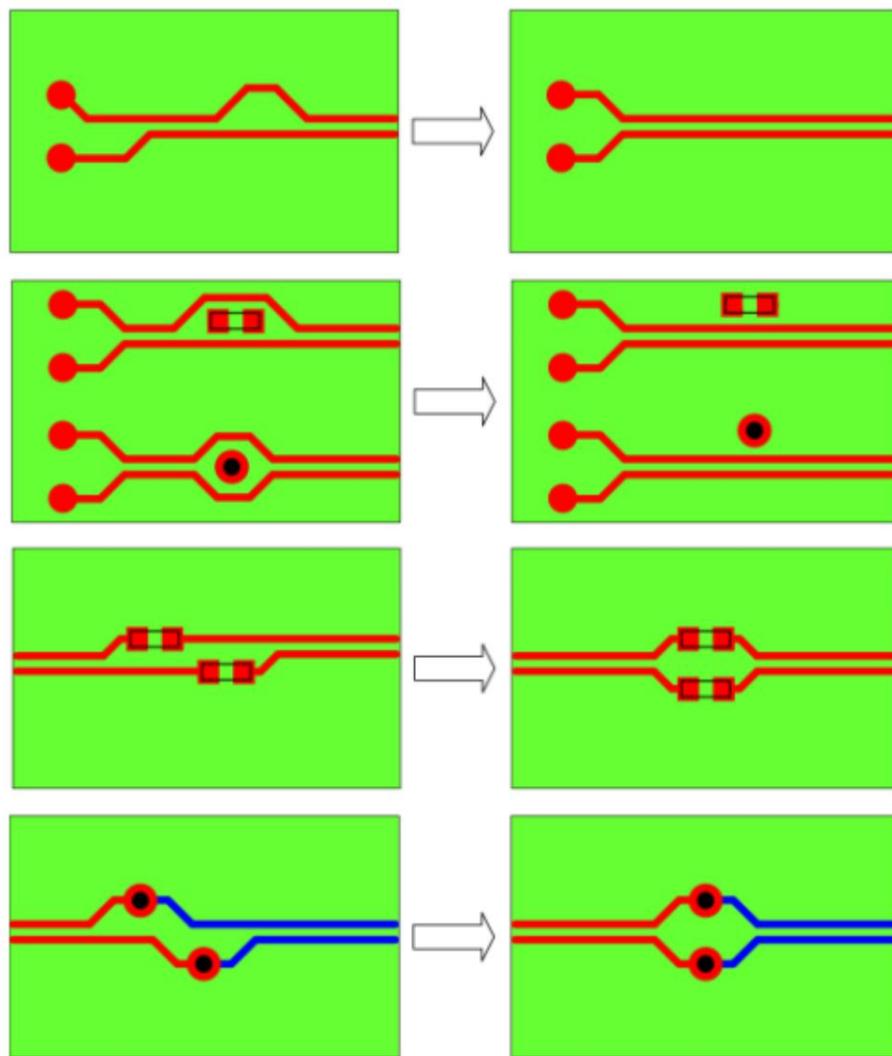


Figure 3-25

(20) It is recommended to drill at least one ground through hole on each ground pad of the high-speed connector, and the through hole should be as close to the pad as possible.

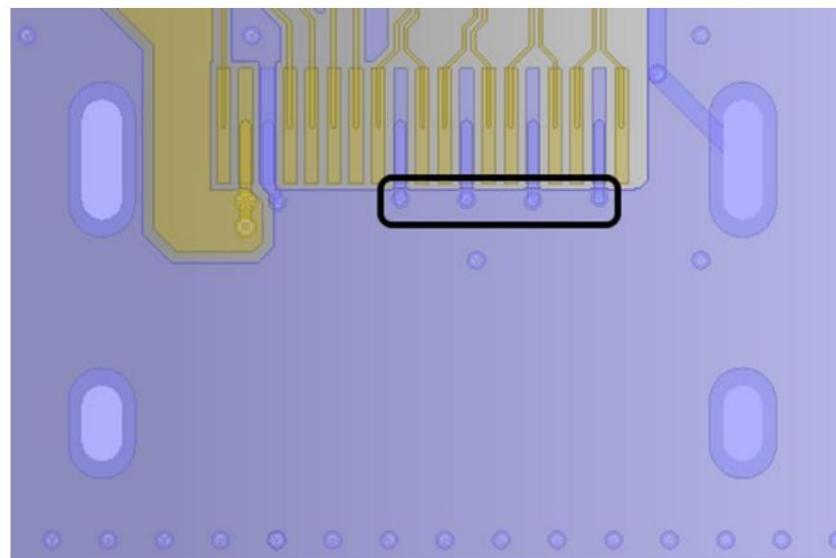


Figure 3-26

(21) When laying copper at the connector position, be careful not to let the ground copper cover exceed the ground pad.

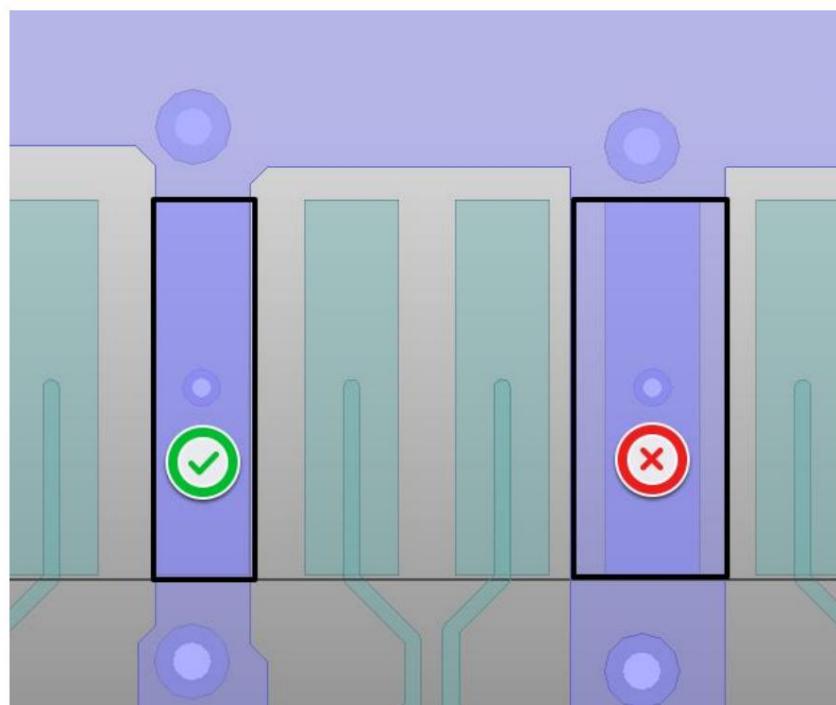


Figure 3-27

(22) The distance between the connector's ground copper and the signal PAD must be at least 3 times the line width.

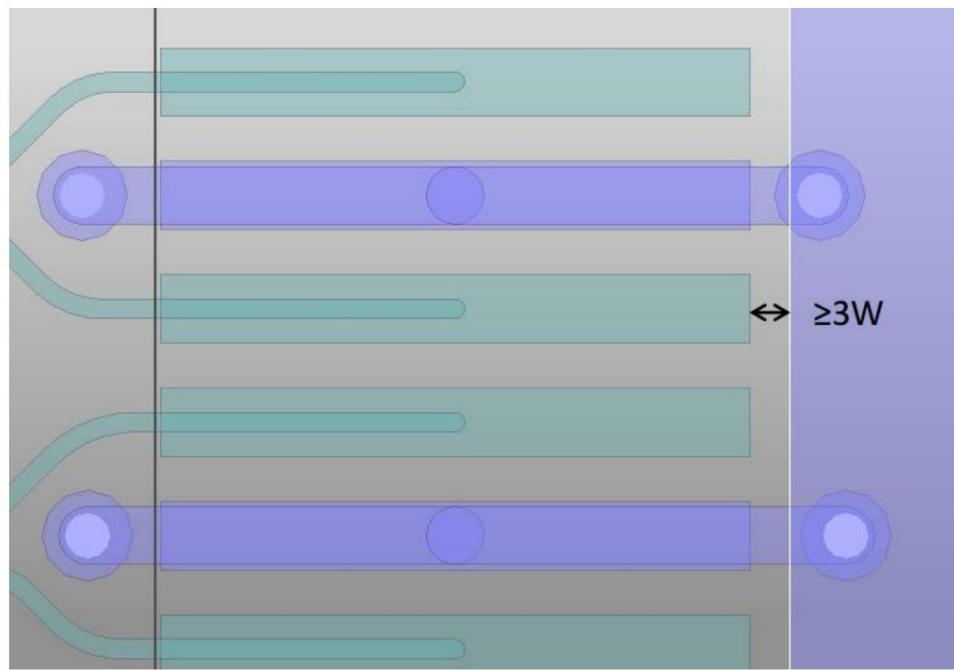


Figure 3-28

(23) Use traces to connect the plane breaks in the BGA area.

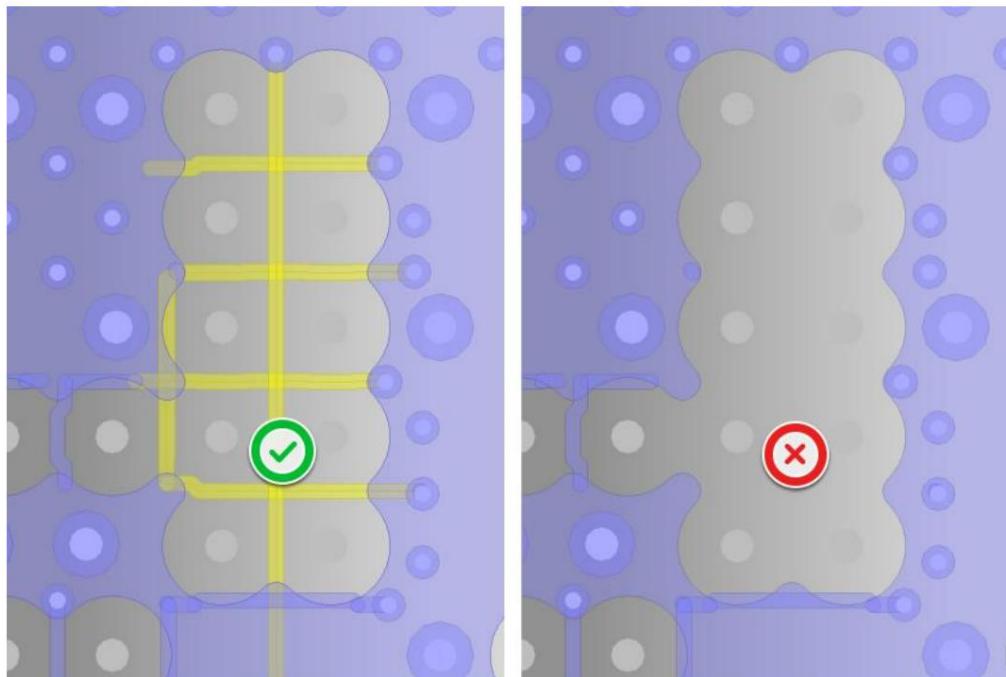


Figure 3-29

(24) The recommended land leasing methods are as follows:

L is the ground via spacing of the ground wire;

D is the distance between the ground wire and the signal wire, and it is recommended to be $\geq 4*W$.

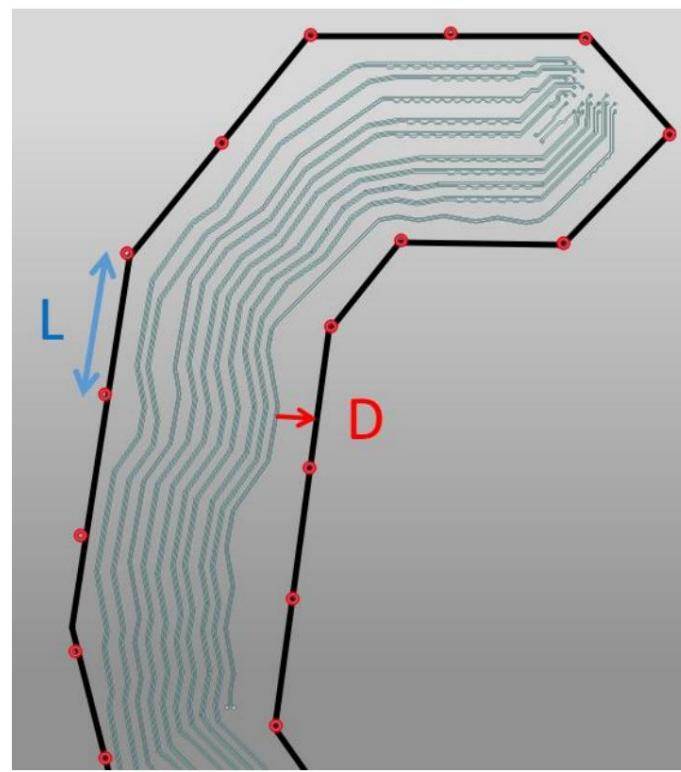


Figure 3-30

(25) Some important high-speed single-ended signals, such as clock signals, reset signals, etc. (such as emmc_clk, emmc_dat strobe,

It is recommended to use ground wires (such as RGMII_CLK). At least one ground via should be drilled every 500 mils.

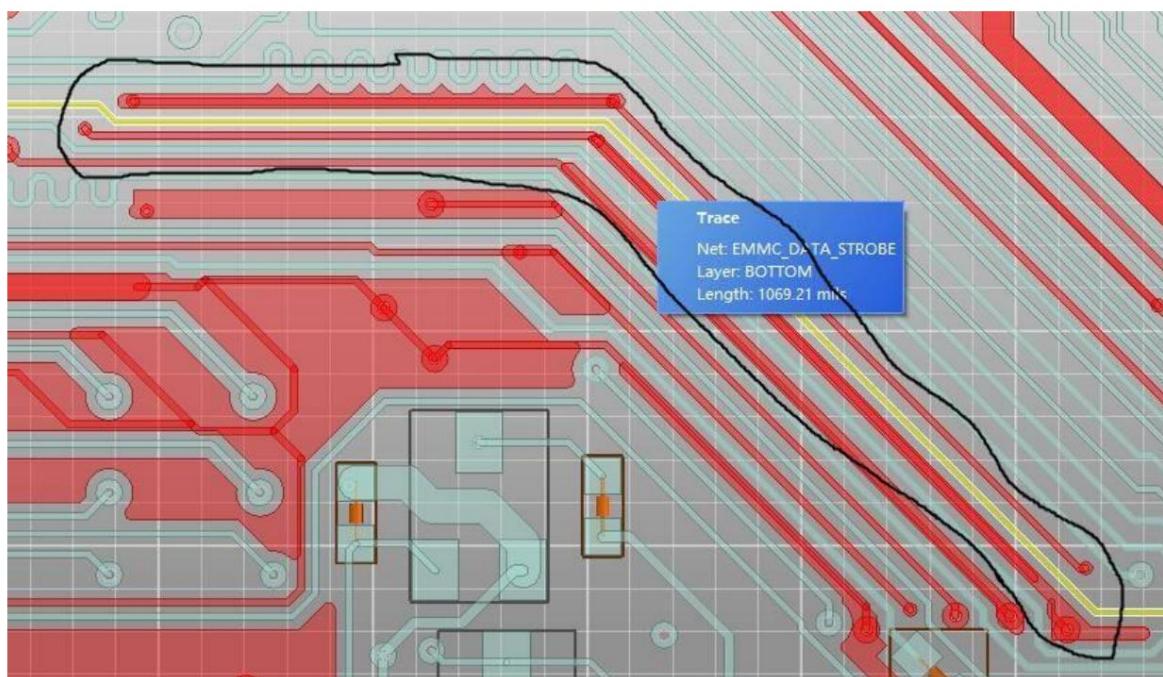


Figure 3-31

(26) It is recommended to use serpentine winding as shown below to reduce the crosstalk caused by winding.

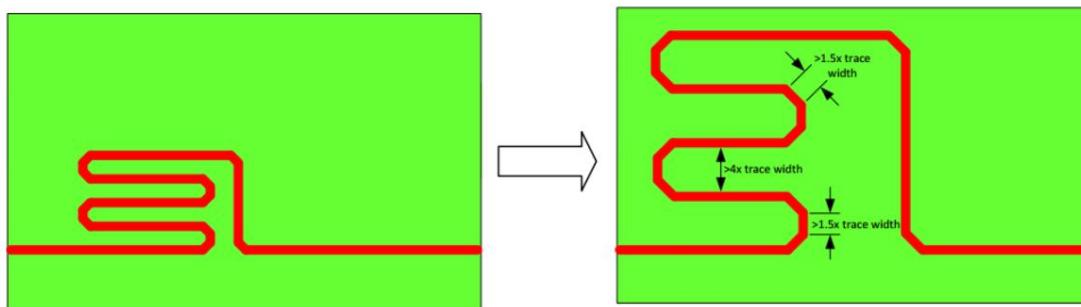


Figure 3-32

(27) Try to reduce the length of the stump as much as possible. It is recommended that the stump length be zero.

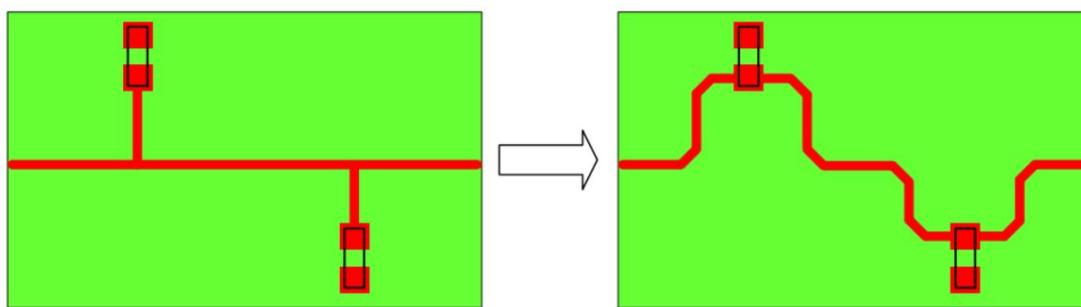


Figure 3-33

(28) When the trace crosses a region, it is recommended to add a stitching capacitor between the two reference planes; when the reference layer is split, it is recommended to add a stitching capacitor between the two reference planes.

Add stitching capacitors at the split to provide a complete return path.

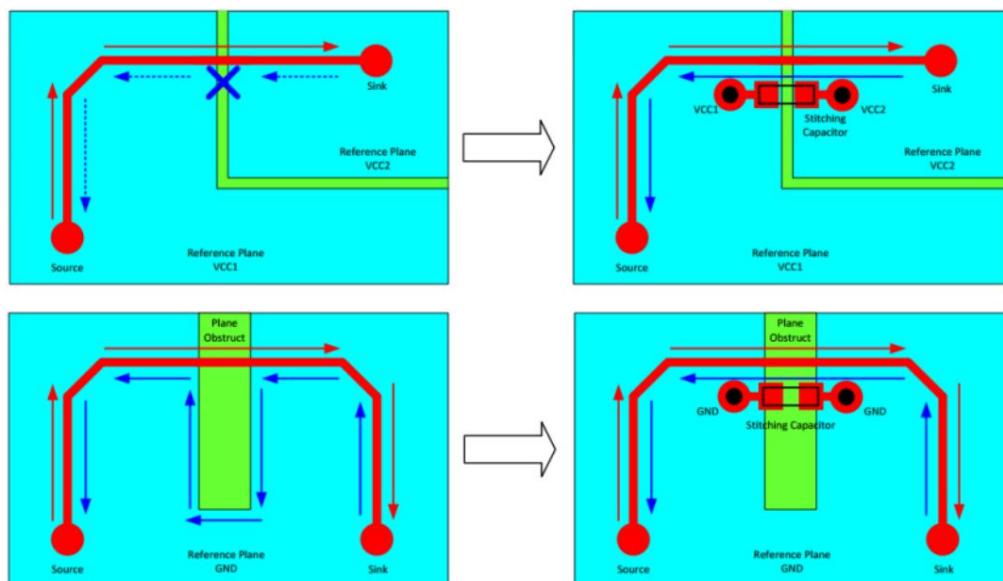


Figure 3-34

(29) It is recommended that in the RK3588 BGA area, there should be one ground via for every 1.3 ground pads, and the ground vias should connect the ground pads and Connect all ground planes together.

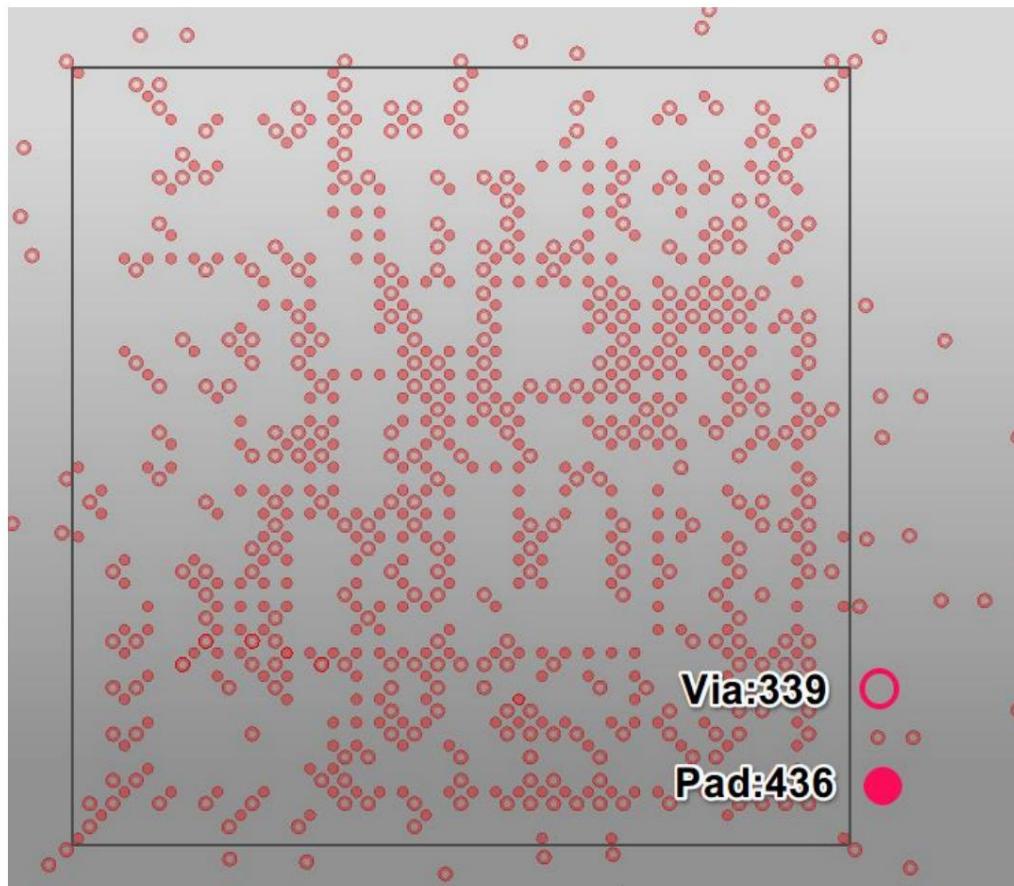


Figure 3-35

3.3 Recommendations for High-Speed Signal Routing at 8GT/s and Above

The signals of the interfaces below RK3588 can operate at 8GT/s and above. Due to the high speed, the PCB design requirements will be more stringent.

Based on the "General Wiring Recommendations" section, you need to follow the requirements of this section for wiring.

Table 3-1 RK3588 8GT/s and above differential signals

interface	High-Speed Differential Signaling
DP1.4@8.1Gbps	TYPEC0_SS RX1P/DP0_TX0P TYPEC0_SS RX1N/DP0_TX0N TYPEC0_SS TX1P/DP0_TX1P TYPEC0_SS TX1N/DP0_TX1N TYPEC0_SS RX2P/DP0_TX2P TYPEC0_SS RX2N/DP0_TX2N TYPEC0_SS TX2P/DP0_TX3P TYPEC0_SS TX2N/DP0_TX3N TYPEC1_SS RX1P/DP1_TX0P TYPEC1_SS RX1N/DP1_TX0N TYPEC1_SS TX1P/DP1_TX1P TYPEC1_SS TX1N/DP1_TX1N TYPEC1_SS RX2P/DP1_TX2P TYPEC1_SS RX2N/DP1_TX2N TYPEC1_SS TX2P/DP1_TX3P TYPEC1_SS TX2N/DP1_TX3N
HDMI2.1@12Gbps	HDMI_TX0_D0P/EDP_TX0_D0P HDMI_TX0_D0N/EDP_TX0_D0N HDMI_TX0_D1P/EDP_TX0_D1P HDMI_TX0_D1N/EDP_TX0_D1N HDMI_TX0_D2P/EDP_TX0_D2P HDMI_TX0_D2N/EDP_TX0_D2N HDMI_TX0_D3P/EDP_TX0_D3P HDMI_TX0_D3N/EDP_TX0_D3N HDMI_TX1_D0P/EDP_TX1_D0P HDMI_TX1_D0N/EDP_TX1_D0N HDMI_TX1_D1P/EDP_TX1_D1P HDMI_TX1_D1N/EDP_TX1_D1N HDMI_TX1_D2P/EDP_TX1_D2P HDMI_TX1_D2N/EDP_TX1_D2N HDMI_TX1_D3P/EDP_TX1_D3P HDMI_TX1_D3N/EDP_TX1_D3N
PCI-E3.0@8Gbps	PCI-E30_PORT0_RX0P PCI-E30_PORT0_RX0N PCI-E30_PORT0_RX1P PCI-E30_PORT0_RX1N PCI-E30_PORT1_RX0P PCI-E30_PORT1_RX0N PCI-E30_PORT1_RX1P PCI-E30_PORT1_RX1N

3.3.1 Digging the reference layer in the BGA pad area

If the working speed of the interface in Table 3-1 is $\geq 8\text{GT/s}$, it is recommended to dig out the L2 reference layer directly below these signals in the RK3588 BGA area.

To reduce the pad capacitance effect. Hollow size $R = 10\text{mil}$.

If the working speed of the interface in Table 3-1 is lower than 8GT/s , for example, the DP interface only works at 5.4GT/s , then there is no need to dig the reference area of the BGA.

Test level.

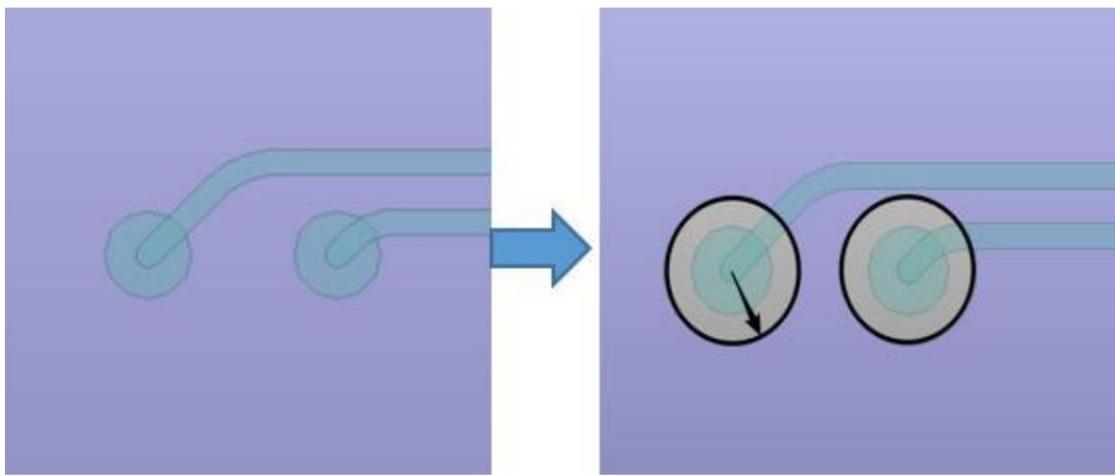


Figure 3-36

3.3.2 Avoiding the glass fiber weaving effect

The glass fiber weave effect means that the PCB substrate is made of glass fiber and epoxy resin filled and pressed together, and the dielectric constants of these two materials are different.

When the D+ line of the differential line is filled with resin and the D- line is filled with glass fiber, the characteristics of the D+ and D- lines will be different.

Due to different impedances, the time delays of the two traces will also be different, resulting in time delay differences within the differential pair and affecting the eye diagram quality.



Figure 3-37

When the interface rate in Table 3-1 reaches 8GT/s and the cable length exceeds 1.5 inches, be careful to handle the fiberglass weaving effect.

One of the ways to avoid the impact of glass fiber weaving effect.

Method 1: Change the routing angle, such as 10°~35°; or rotate the board 10° during PCB processing to ensure that all routing lines do not collide with the fiberglass.

parallel.

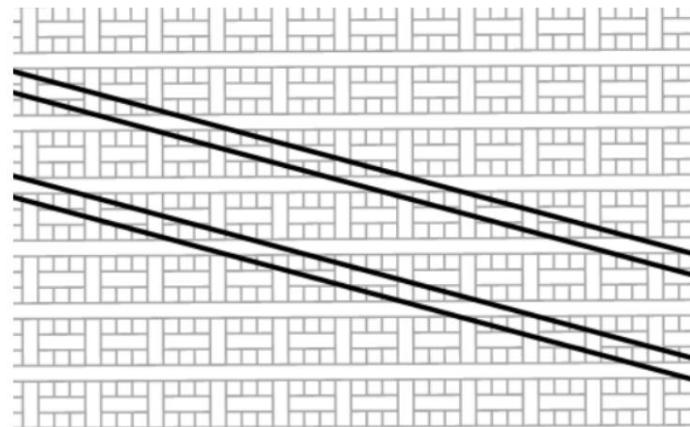


Figure 3-38

Method 2: Use the following routing (zigzag), the W in the figure below must be at least 3 times greater than the glass fiber braid spacing. Recommended values are W=60mil, $\gamma=10^\circ$, L=340mil $\sqrt{2}$

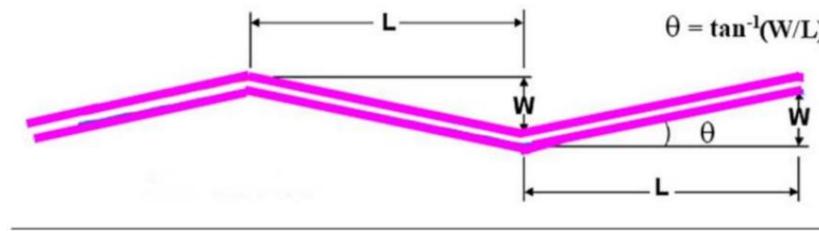


Figure 3-39

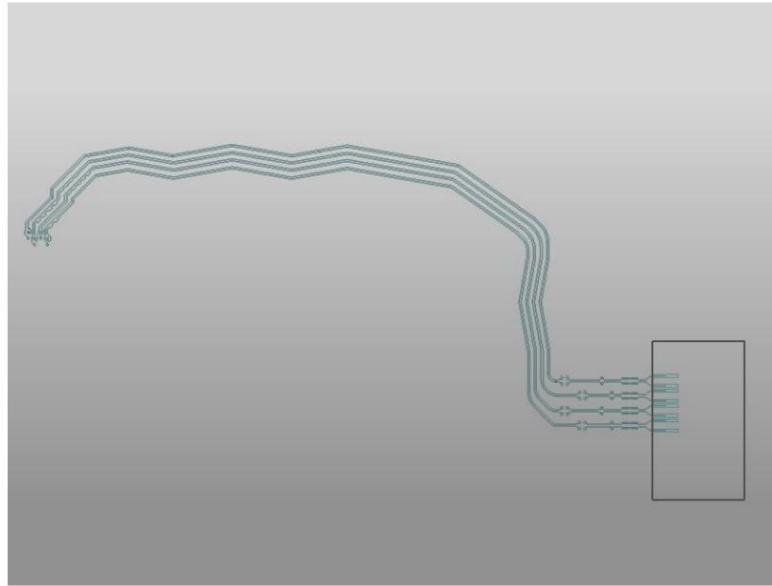


Figure 3-40

3.3.3 Differential Via Recommendations

If the operating rate of the interfaces in Table 3-1 is \geq 8GT/s, it is recommended to optimize the via sizes of the differential pairs of these interfaces based on simulation of the actual stackup.

The following are the reference dimensions of vias based on the EVB first-order HDI stackup:

R_Drill=0.1mm (drilling radius)

R_Pad=0.2mm (via pad radius)

D1: Differential via center spacing

D2: Anti-pad size of the surface layer to the bottom layer

D3: Center distance between signal via and return ground via

Table 3-2 Reference dimensions of differential vias

Way	D1(thousand)	D2(mil)	D3(miles)	Differential via impedance
1	26	18	22~26	100 ohm
2	24	18	22~26	95 ohm
3	22	18	22~26	90 ohm
4	22	15	22~26	85 ohm

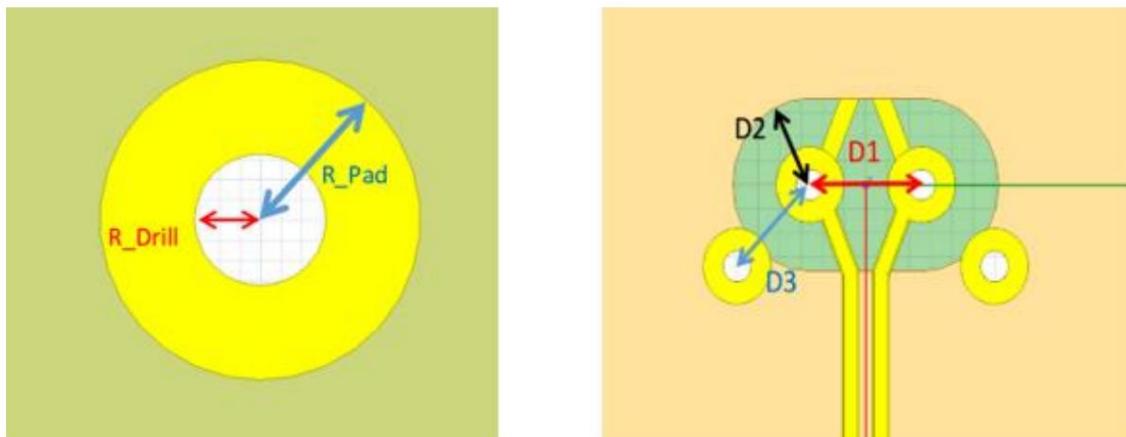


Figure 3-41

3.3.4 Coupling Capacitor Optimization Suggestions

If the operating rate of the interfaces listed in Table 3-1 is $\geq 8\text{GT/s}$, the differential DC capacitors of these interfaces are recommended to be optimized as follows.

Hollow out one or two ground planes according to the interface. If the L2 ground reference layer directly below the capacitor pad is hollowed out, an interlayer reference is required, that is,

The L3 layer should be the ground reference layer; if the L2 and L3 ground reference layers are hollowed out, then the L4 layer should be the ground reference layer.

Determined through simulation, the reference dimensions of the first-order HDI stackup based on EVB are given below.

At the same time, four ground vias are drilled around the coupling capacitor to connect the ground reference layers of layers L2 to L4.

Table 3-3 Coupling capacitor pad hollowing size reference values

interface	Knockout layer	D1	H	L
DP1.4	L2 and L3 layers	25mil	20mil	Same length as pad
HDMI2.1	L2 and L3 layers	25mil	20mil	Same length as pad
PCI-E3.0	L2 layer	25mil	20mil	Same length as pad

D1: Center distance between differential coupling capacitors; L: Hollow length; H: Hollow width.

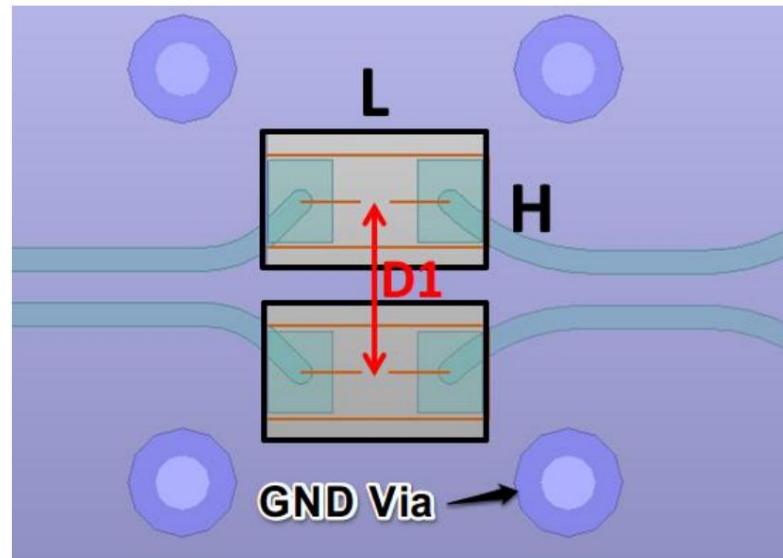


Figure 3-42

3.3.5 ESD Optimization Suggestions

If the operating rate of the interfaces listed in Table 3-1 is $\geq 8\text{GT/s}$, the differential pair ESD devices of these interfaces are recommended to be optimized as follows.

Hollow out the L2 and L3 ground reference layers directly below the ESD pad. The L4 layer is used as the interlayer reference layer and needs to be a ground plane. The hollowing size needs to be combined with the ESD model.

The model is determined by simulation based on the actual stack. The following is the ESD model ESD73034D based on the EVB first-order HDI stack.

Reference size.

At the same time, four ground vias are drilled around each ESD to connect the ground reference layers of L2~L4 layers.

Table 3-4 Reference dimensions for ESD device pad cutouts

interface	Knockout layer	H	IN
DP1.4	L2 and L3 layers	22mil	Same length as pad
HDMI2.1	L2 and L3 layers	22mil	Same length as pad

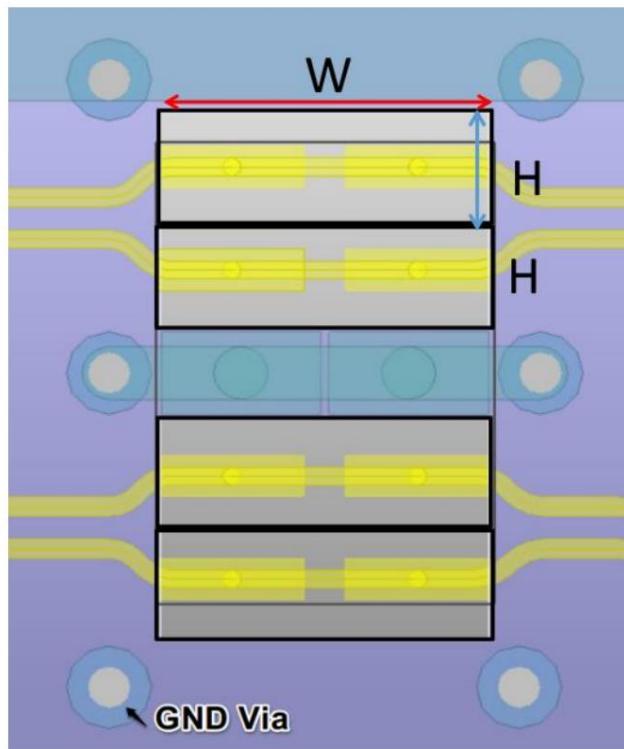


Figure 3-43

3.3.6 Connector Optimization Suggestions

If the working speed of the interface in Table 3-1 is $\geq 8\text{GT/s}$, the connectors of these interfaces must meet the corresponding standard requirements (such as HDMI2.1/DP1.4/PCI-E3.0 protocol standards). Recommended connectors include Molex, Amphenol, and HRS.

Hollow out one or two ground planes according to the interface. If the L2 ground reference layer directly below the connector pad is hollowed out, an interlayer reference is required.

That is, the L3 layer should be used as the ground reference layer; if the ground reference layers of L2 and L3 are hollowed out, then the L4 layer needs to be the ground plane as the interlayer reference layer.

The hollowing size needs to be determined through simulation based on the connector model and actual stacking.

It is recommended to drill two ground holes on each ground pad of the connector, and the ground holes should be as close to the pad as possible.

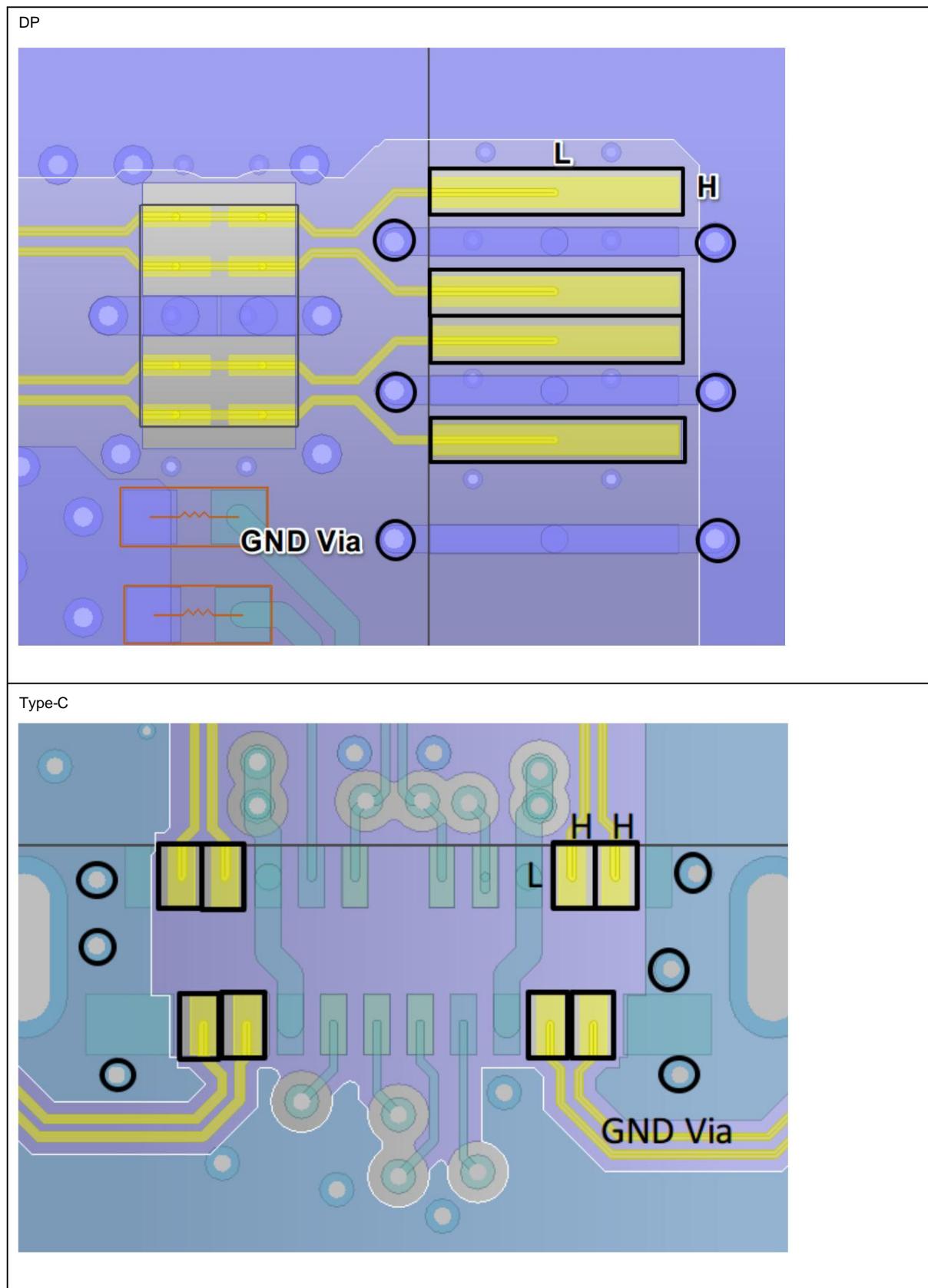
The following gives the reference dimensions of the cutout based on the EVB first-order HDI stackup.

Table 3-5 Connector pad cutout dimensions reference values

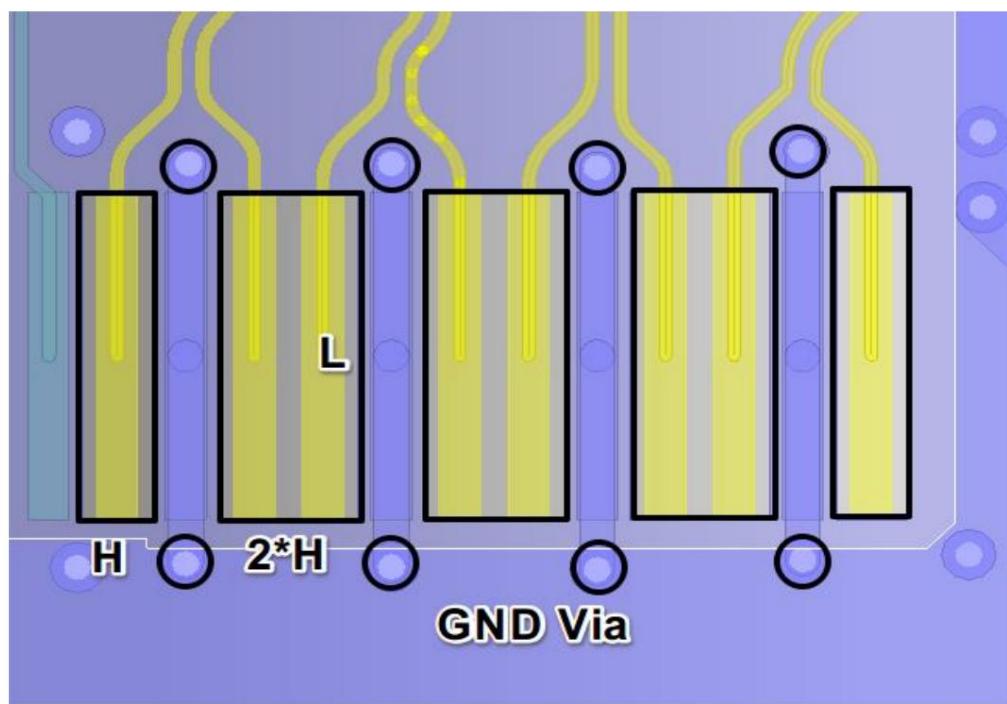
Connectors	model	Knockout layer	H	L
DP	Molex 472720029	L2 and L3 layers	18mil, same length as pad	
Type-C	Molex 1054500101	L2 and L3 layers	20mil, same length as pad	
HDMI2.1	Molex 2086581051	L2 and L3 layers	20mil, same length as pad	
PCI-E3.0	Amphenol 10076266-101TLF	L2	91mil	89mil

Recommended connector wiring method:

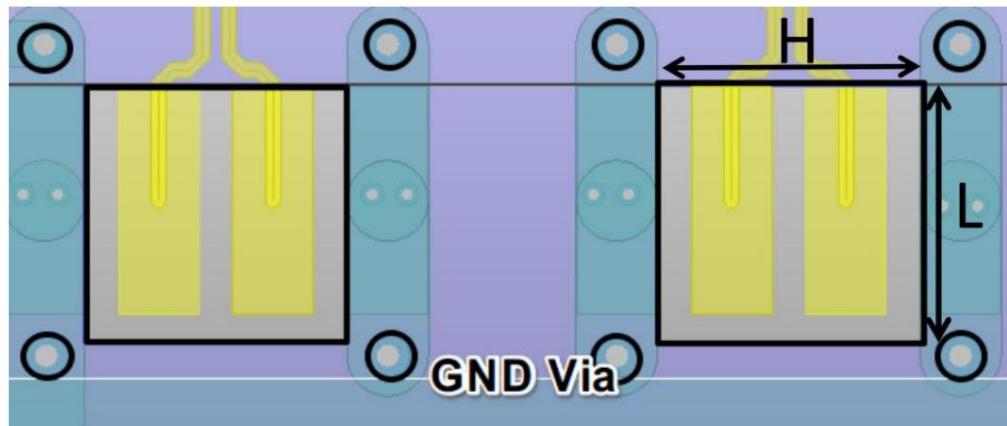
Table 3-6 Recommended connector wiring methods



HDMI2.1



PCI-E3.0



3.4 Interface PCB Design Recommendations

3.4.1 Clock/Reset Circuit PCB Design

In the PCB design of the clock circuit, please note:

ü The crystal circuit layout needs to be given priority. When laying out, it should be placed on the same layer as the chip and as close as possible to avoid drilling holes. The crystal routing

Keep it as short as possible, away from interference sources, and as far away from the edge of the board as possible;

ü The crystal and clock signals need to be grounded throughout. At least one GND via should be added every 200-300mil.

The ground reference surface of the adjacent layer must be intact;

ü When the crystal circuit is placed on a different layer from the chip, the crystal routing and grounding must be done throughout to avoid interference;

ü No traces should be placed along the clock traces Xin and Xout, as well as in the area below the crystal, to prevent noise from coupling into the clock circuit. ü A ground ring can be placed on the top layer below the crystal. This ground ring is connected to the adjacent ground layer through vias to isolate noise. ü The second layer below the crystal maintains a complete ground reference plane, avoiding any trace splitting, which helps isolate noise and maintains the crystal output.

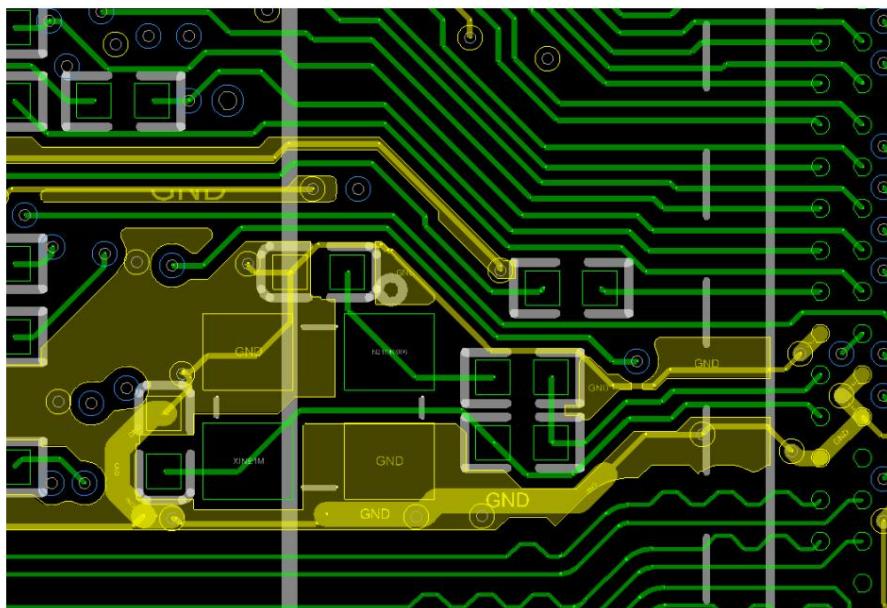


Figure 3-44 RK3588 crystal layout and routing

ü The decoupling capacitors for PLL_DVDD0V75, PLL_AVDD1V8, OSC_1V8, and PMU_0V75 power supplies must be placed between the chip and the

On the back of the pin, when routing, try to make it pass through the capacitor pad first and then to the chip pin.

When designing the PCB for the Reset circuit, please note:

ü During layout, the RESETn reset signal should be kept away from the board edge and metal connectors to prevent abnormalities caused by ESD from causing reset mode.

Block freeze;

ü The RESETn filter capacitor should be placed as close to the chip pin as possible. The signal must pass through the capacitor before entering the chip. Pay attention to the filter capacitor.

The ground pad must have a 0402 ground via. If space permits, it is recommended to have two or more for better grounding.

ü The RESETn signal should be kept away from strong interference signals such as DCDC and RF to prevent interference. If the trace is long, it is recommended to wrap it with ground.

And add at least one GND via every 400mil of the ground wire;

ü The TVS protection diode of the RESETn button should be placed as close to the button as possible. The signal topology is: button-->TVS-->100 ohm-->capacitor (near CPU & PMIC)-->CPU & PMIC. When ESD occurs, the ESD current must first pass through the TVS device attenuation device.

reduce.

3.4.2 PMIC/Power Circuit PCB Design

3.4.2.1 PCB Design of RK806 Power Solution

From the perspective of power quality, the overall layout should be such that RK806 is placed as close to RK3588 as possible (when considering heat dissipation design, it needs to be placed appropriately, not too close).

When placing the components, give priority to BUCK1, BUCK2, BUCK3, and BUCK4 of RK806.

The routing (copper coating) of the power supply with a relatively large output current to the RK3588 is smooth.

Note: ȳ Taking the

vias of 0.5*0.3mm as an example, the recommended via for high-voltage power supply is 0.8A, and the recommended via for low-voltage power supply (below 1V) is 0.5A.

calculate;

ȳ The GND end of the high current buck input and output capacitors must have the same number of vias as the positive end to achieve a better filtering effect.

(Many customers tend to ignore the number of vias on the GND side of the capacitor);

ȳ It is not recommended to use thermal pads and cross connections on the pads and vias of the power supply components. They should be completely covered with copper.

The EPAD ground pad of RK806 should be equipped with enough vias. It is recommended to ensure 5*5 0.5*0.3mm or 6*6 0.4*0.2mm.

Above the vias, reduce the ground impedance and enhance heat conduction; on the board with blind and buried vias, drill some more blind vias to help reduce impedance.

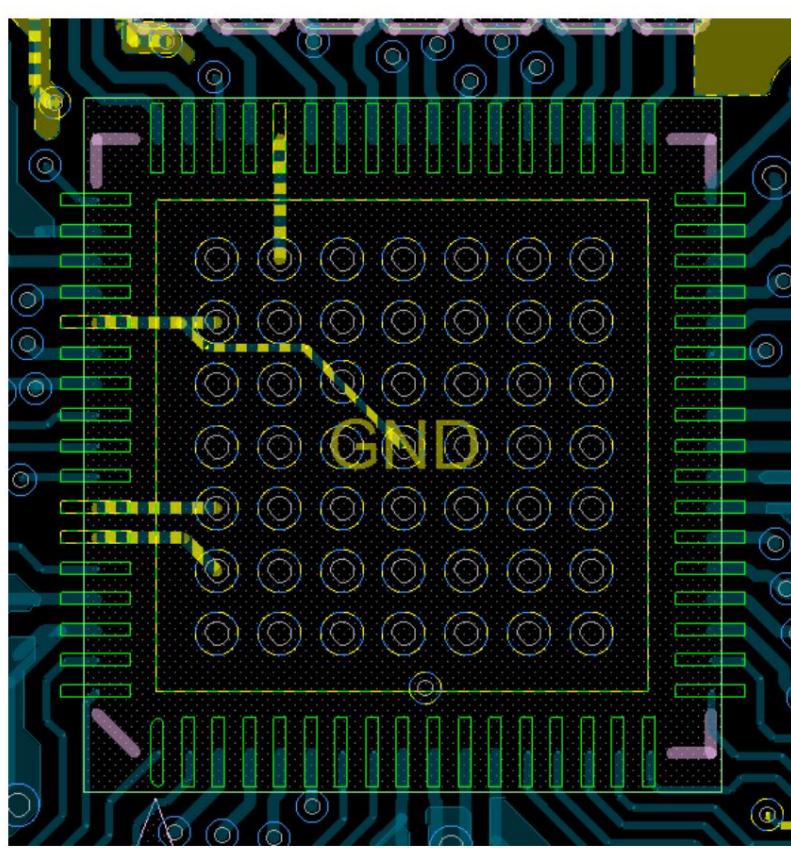


Figure 3-45 RK806 EPAD via distribution

ȳ RK806 BUCK1\3 design requirements:

The input capacitor must be as close to the chip as possible (if the input capacitor is placed on the back of the chip, make sure the GND end of the capacitor is close to the bottom of the chip).

Make the connection loop between the input capacitor and VCC and GND as small as possible. Make sure the SW trace is as short and thick as possible (as far as possible after the chip pin is connected).

It is possible to enlarge the area as early as possible) to improve the overcurrent capacity and power efficiency; For places where vias are required, if VCC1/3 is combined to supply at least

Five 0.5*0.3mm vias are required. If separate, each requires three or more 0.5*0.3mm vias. The GND terminals of the BUKC1 and BUCK3 output capacitors can be shared, but at least 15 or more 0.5*0.3mm vias are required. Smaller vias or blind vias can be used as supplementary holes if space is available. If the BUCK1 output layer is changed, at least 15 or more 0.5*0.3mm vias are required. Similarly, BUCK3 requires at least 12 or more 0.5*0.3mm vias.

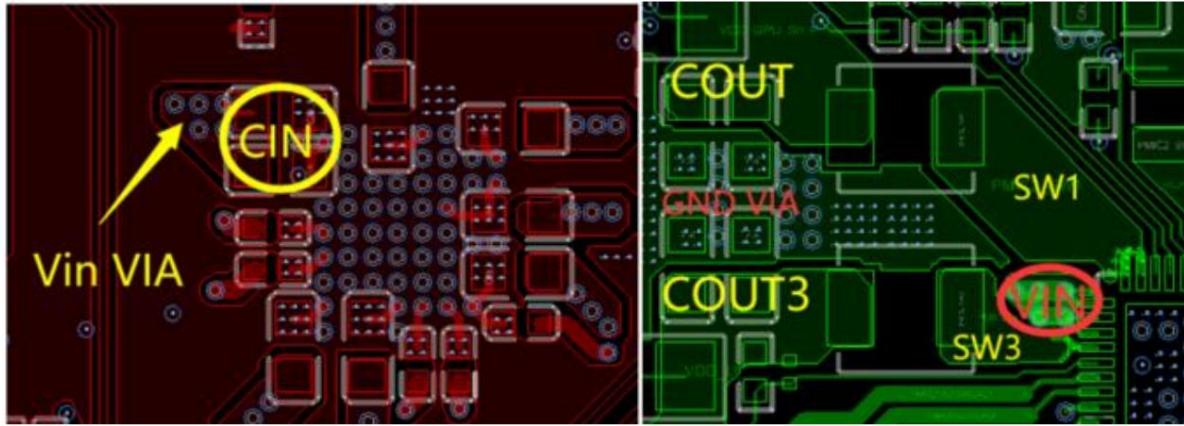


Figure 3-46 RK806 BUCK1/BUCK3 layout and routing

ŷ BUCK2 PCB design requirements for RK806: The input capacitor must

be as close to the chip as possible (if the input capacitor is placed on the back of the chip, the GND end of the capacitor must be close to the bottom of the chip). The connection loop between the input capacitor and VCC and GND should be as small as possible. The SW trace should be as short and thick as possible (as far as possible after the chip pin is connected).

It is possible to make the area larger as early as possible) to improve the overcurrent capacity and power efficiency; For places where vias are required, VCC2 power supply requires at least 3 0.5*0.3mm vias, the GND end of the output capacitor needs at least 12 0.5*0.3mm vias. If there is space, you can drill smaller vias or blind holes.

Hole supplement: If there is a layer change in the output, at least 12 or more 0.5*0.3mm layer change vias are guaranteed.

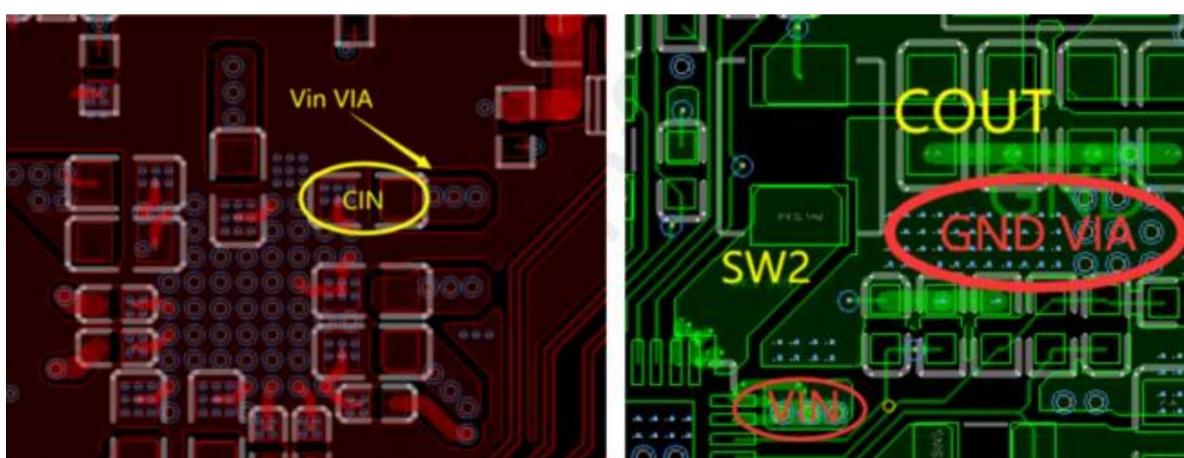


Figure 3-47 RK806 BUCK2 layout and routing

ŷ RK806 BUCK4 PCB design requirements:

The input capacitor must be as close to the chip as possible (if the input capacitor is placed on the back of the chip, make sure the GND end of the capacitor is close to the bottom of the chip).

Make the connection loop between the input capacitor and VCC and GND as small as possible. Make sure the SW trace is as short and thick as possible (as far as possible after the chip pin is connected). (The area may be increased early) to improve the flow capacity and power efficiency. For areas where vias are required, the VCC4 power supply requires at least three 0.5*0.3mm vias, and the GND end of the output capacitor requires at least 12 or more 0.5*0.3mm vias. If there are insufficient vias, blind vias can be used to supplement them.

If there is a layer change in the output, at least 12 or more 0.5*0.3mm layer change vias must be ensured.

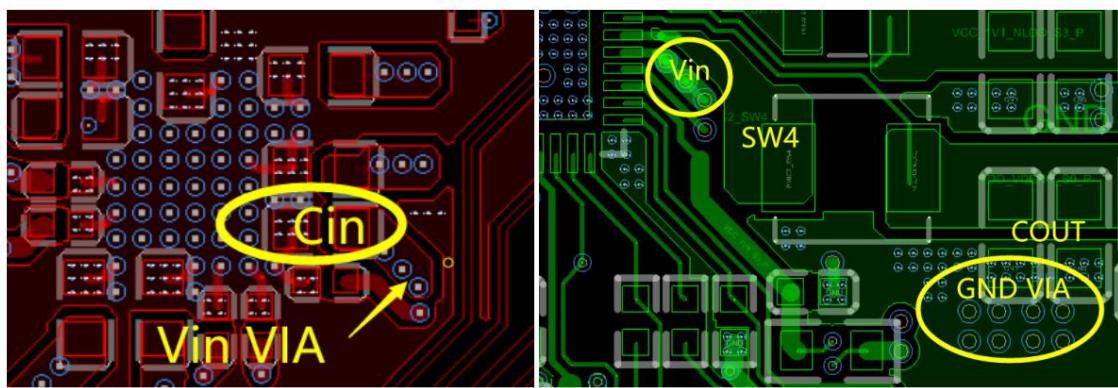


Figure 3-48 RK806 BUCK4 layout and routing

ÿ RK806 2.5A BUCK (BUCK) PCB design requirements: The input capacitor must be as close

to the chip as possible (if the input capacitor is placed on the back of the chip, the GND end of the capacitor must be close to the bottom of the chip). The connection loop between the input capacitor and VCC and GND should be as small as possible. The SW trace should be as short and thick as possible (as far as possible after the chip pin is connected).

(It is possible to enlarge the area as early as possible) to improve the power supply overcurrent capacity and efficiency; For places where vias are required, VCC5/6/7/8/9/10 power supply should be at least Two 0.5*0.3mm vias are required (if the pins are close to VCC5 and VCC7, and VCC6 and VCC10, three 0.5*0.3mm vias are required). The GND end of the output capacitor requires at least five or more 0.5*0.3mm vias. If it is insufficient, blind holes can be used to supplement it. If the output has a layer change, at least five or more 0.5*0.3mm layer change vias are guaranteed.

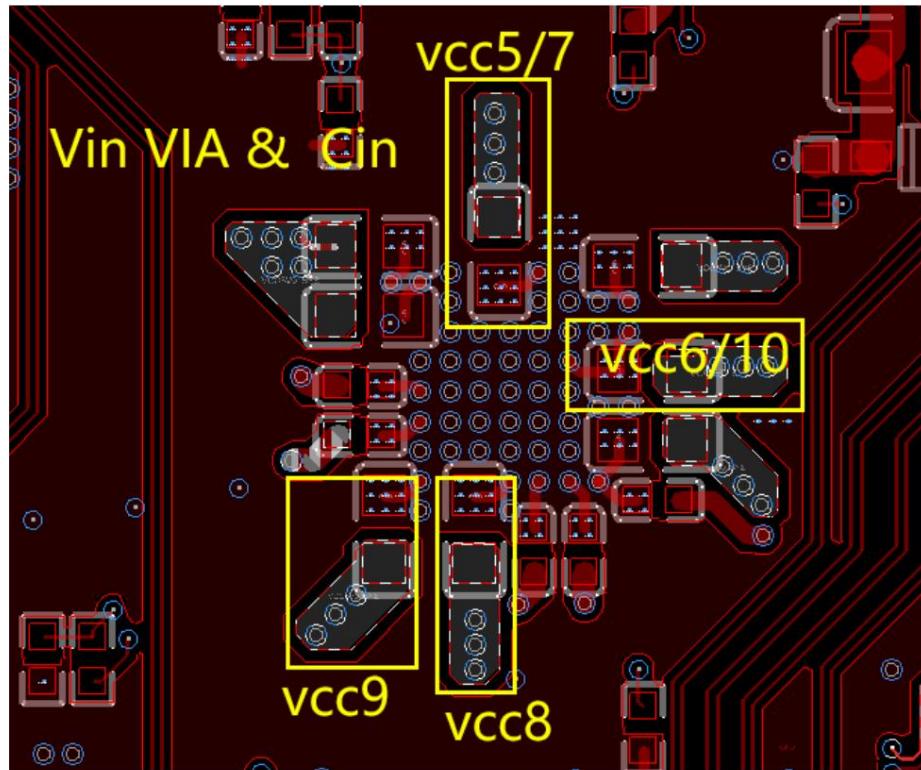


Figure 3-49 RK806 2.5A BUCK VCC input capacitor layout and routing

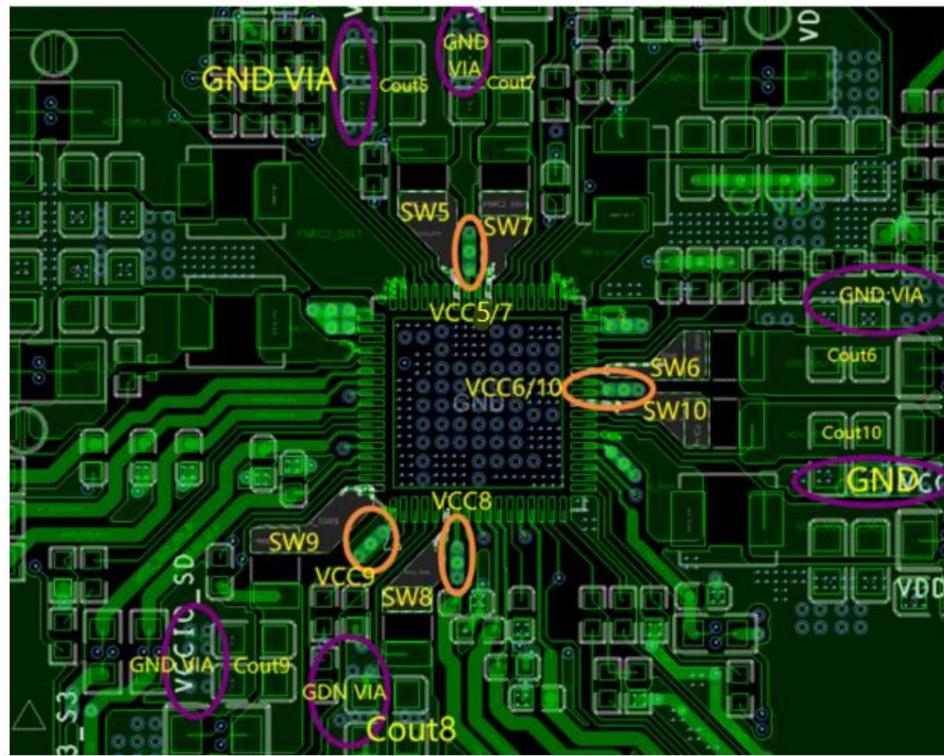


Figure 3-50 RK806 2.5A BUCK layout and routing

ŷ RK806 LDO PCB design requirements:

ŷ The input capacitor must be as close to the chip as possible, and the connection loop between the input capacitor, VCC11/12/13/14 and GND must be as small as possible;

ŷ The output capacitor must be as close to the chip as possible, and the output capacitor must be connected to PLDO1/2/3/4/5/6, NLDO1/2/3/4/5 and GND.

The connection loop should be as small as possible;

ŷ The thick wire is generally designed to be 1mm wide and 1A wide. The LDO with large current output should be designed according to the actual power supply requirements of the backend.

After being led out from the chip, it should be thickened to the required size as soon as possible. Special attention should be paid to the trace length and loss of the low-voltage, high-current NLDO.

To meet the supply voltage and ripple requirements of the target chip.

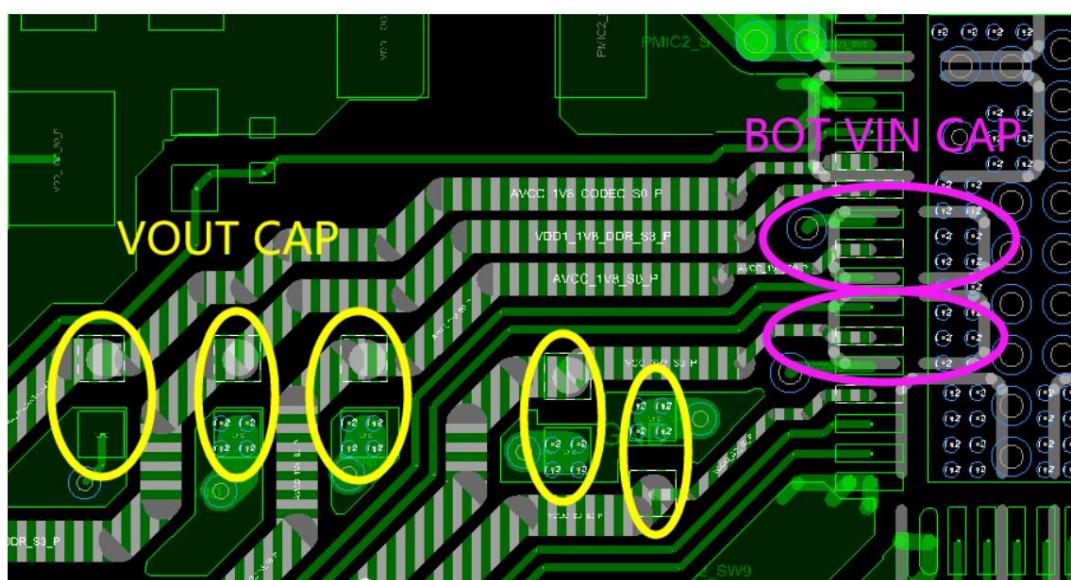


Figure 3-51 RK806 LDO layout and routing example

ÿ The VCCA capacitor of RK806 must be placed close to the pins and away from other interference sources. The ground pad of the capacitor must be well grounded, that is, VCCA

The path between the capacitor ground pad and the RK806 EPAD must be as short as possible and must not be divided by other signals;

ÿ The 100nF capacitor of Pin 67 (RESETB) of RK806 must be close to the RK806 pin to improve the chip's anti-interference ability; ÿ It is recommended that the RK806 pin

part is not covered with copper, and all pins are connected to the outside through routing. The routing line width must not exceed the pin width.

Prevent the solder pad from becoming larger after the board is made and the patch is easily tinned

3.4.2.2 DC-DC PCB Design for Discrete Power Supplies

The input capacitor Cin and output capacitor Cout are placed between Vin pin, Vout pin and GND of DC/DC, and the Vin and Vout pins should be minimized.

The loop area between the GND of the DC/DC can reduce the power ripple amplitude and greatly improve the reliability of the chip, as shown in the following figure:

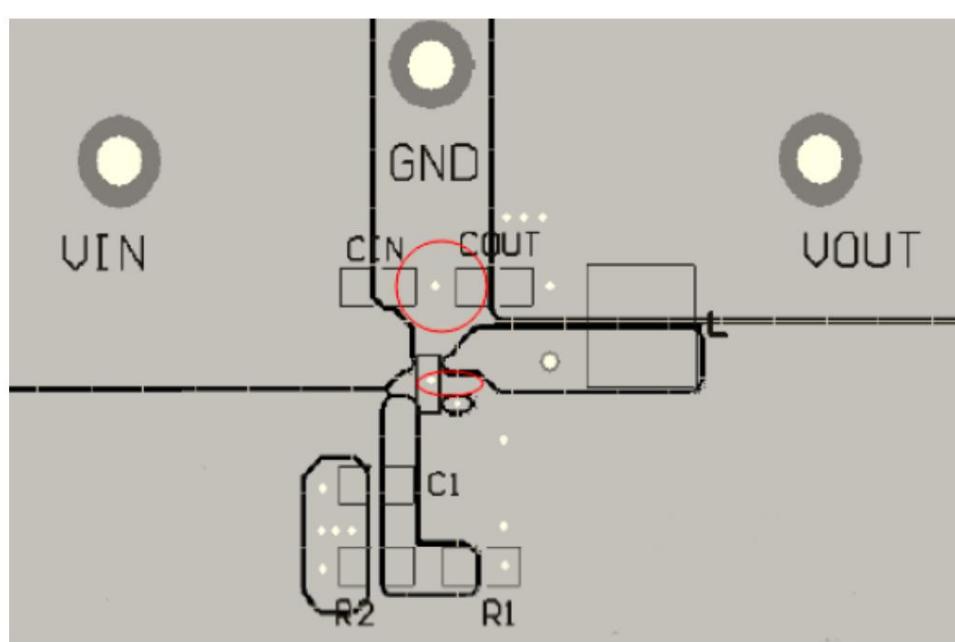


Figure 3-52 Discrete power supply DC/DC layout and routing

For the input capacitor Cin, output capacitor Cout, and DC/DC GND, ensure as many vias as possible. Four or more 0503 vias are recommended. If the Vin and Vout power supplies switch layers, additional vias are recommended. Four or more 0503 vias are recommended (this is related to current flow, as described below). Place the inductor as close to the DC/DC as possible, using thick and short traces. Route the resistor ground at the FB terminal as far away from interference sources as possible.

3.4.2.3 RK860 Power Supply PCB Design

RK860-x is used as an auxiliary power supply for a single RK806-1, usually to power high current CPU, GPU or NPU.

Keep it as close to RK3588 as possible (preferably within 10mm).

The recommended PCB layout for the RK860 is as follows: the input and output capacitors are placed at both ends of the chip and as close to the chip as possible. The capacitors, inductors, and chip are laid out on the same layer. The GND pads of the capacitors and the GND pads of the chip are oriented in the same direction to form a minimum closed loop.

Place the inductor between the output capacitor and the chip, ensuring the SW trace is as short as possible to prevent interference with other modules. The chip's VOUT feedback signal must be taken from the output capacitor (avoid taking the signal from the inductor pad) and kept as close to the SW as possible. Where vias are required, five 0.5*0.3mm vias can be drilled for the VIN pin, and at least 12 0.5*0.3mm vias are required for the buck output. In particular, the GND vias should be placed as close to the chip GND and capacitor pads as possible. If the board uses blind or buried vias, add additional blind vias to the GND pads of the chip and capacitor.

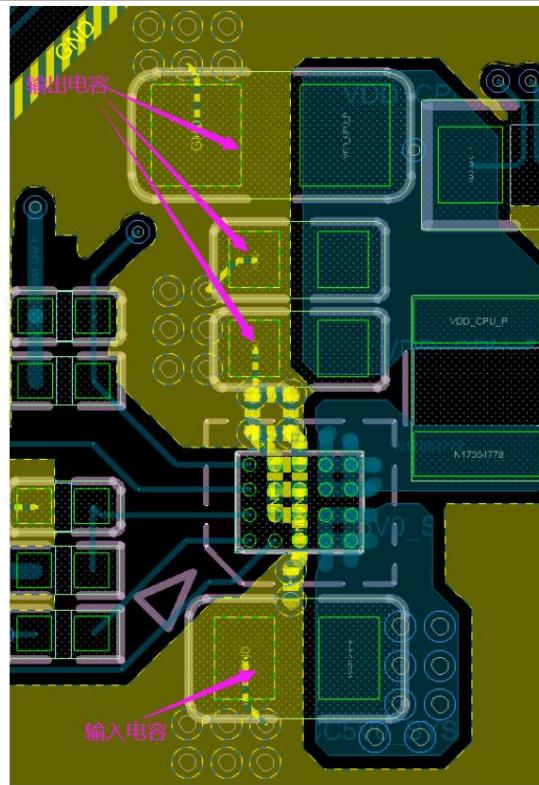


Figure 3-53 VDD_CPU power supply DC/DC layout and routing

3.4.2.4 DC-DC Remote Feedback Design for VDD_LOGIC, VDD_GPU, VDD_NPU, and VDD_CPU Power Supplies

The 100ohm feedback resistor needs to be placed close to the output capacitor. One end of the resistor is connected to the DC-DC output capacitor and the other end is connected to the PMIC.

The VOUT feedback pin is connected to the farthest load in the same power network as the RK3588 power pin. The feedback line width is 4mil.

The feedback line must be routed along with the power copper to avoid interference; the feedback line must be spaced at least 6 mils from other signals, such as VDD_GPU power copper and

Feedback line routing diagram. Other power supply lines are handled similarly.

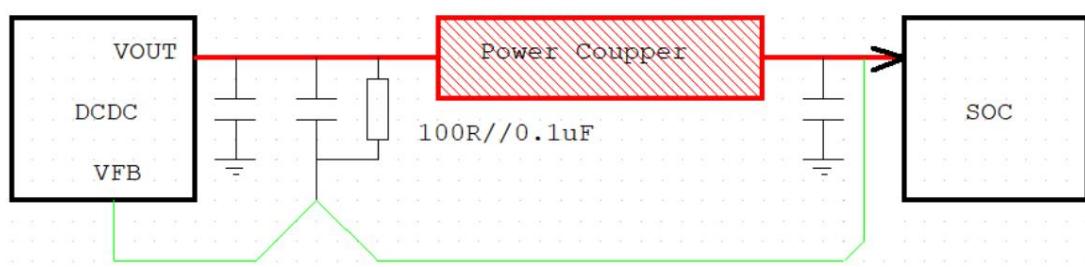
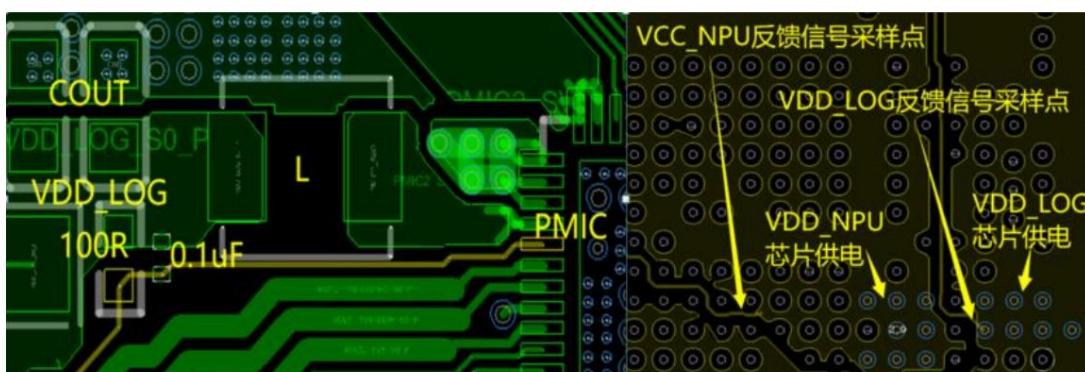


Figure 3-54 DC/DC remote feedback design diagram

3.4.2.5 RK3588 VDD_CPU_BIG0/1 Power Supply PCB Design

The copper width of VDD_CPU_BIG0/1 must meet the current requirements of the chip. The copper connected to the chip power pin is wide enough and the path cannot be too narrow. The vias are too severe to be divided, so the effective line width must be calculated to ensure that there are sufficient paths connected to each power pin of the CPU.

When the VDD_CPU_BIG power supply is switched on the periphery, as many power vias as possible should be drilled (12 or more 0.5*0.3mm vias) to reduce the voltage drop caused by the layer-switching vias. The number of GND vias for the decoupling capacitor should be consistent with the number of its power vias, otherwise the capacitance effect will be greatly reduced.

The power pins of RK3588 chip VDD_CPU_BIG0/1 ensure that there is a corresponding via on each ball edge and the top layer is connected.

"Well" shape, cross connection, recommended trace width is 10mil.

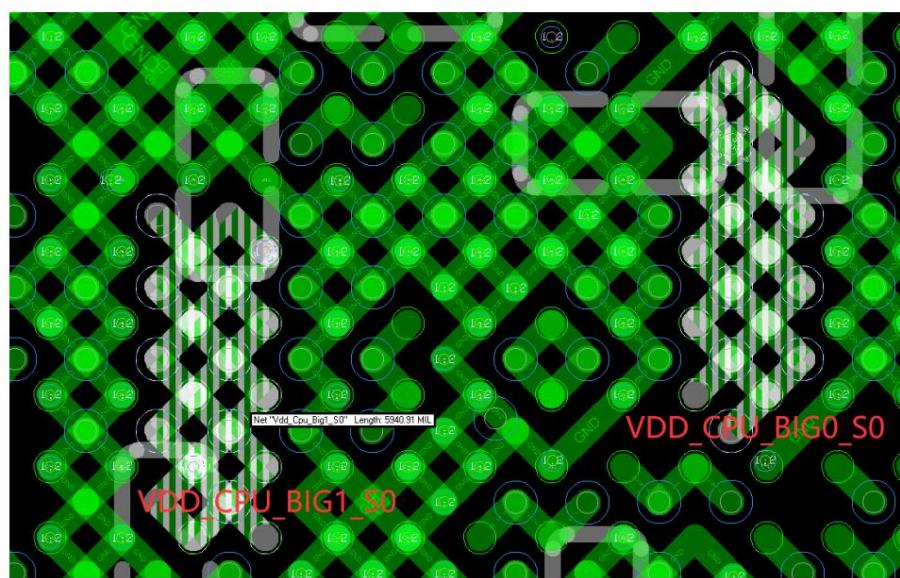


Figure 3-55 RK3588 chip VDD_CPU_BIG0/1 power pin routing and vias

The decoupling capacitor close to the VDD_CPU_BIG power pin of RK3588 on the schematic diagram must be placed on the back of the corresponding power pin.

Place the GND pad as close as possible to the GND Ball in the center of the chip, and the remaining decoupling capacitors as close as possible to RK3588.

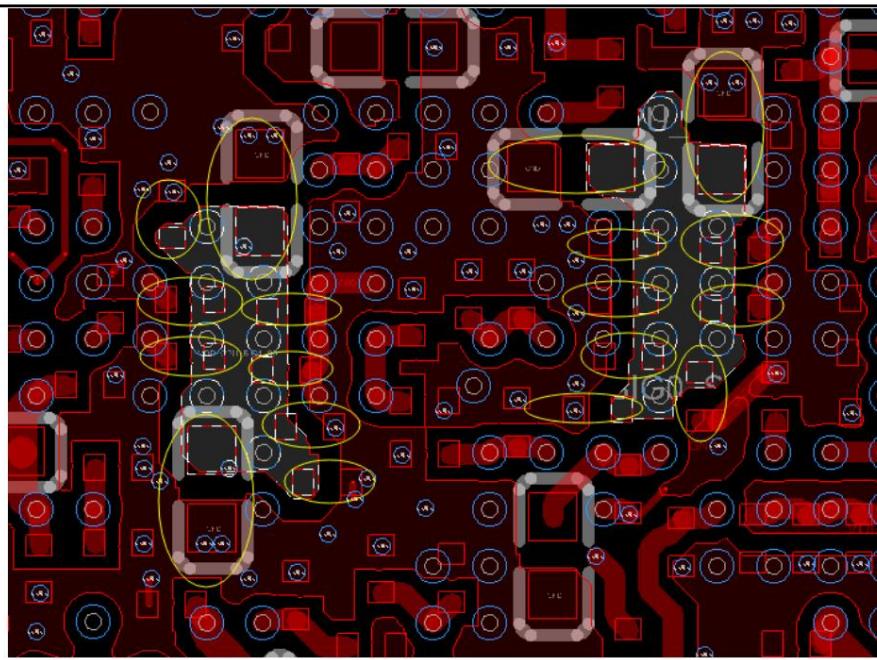


Figure 3-56 Decoupling capacitor placement on the back of the RK3588 chip VDD_CPU0/1 power pin

VDD_CPU_BIG current is relatively large and requires double-layer copper cladding. The total line width of VDD_CPU_BIG power supply in the CPU area must not be less than 300mil.

The width of the peripheral area should not be less than 600mil. Copper cladding should be used as much as possible to reduce the voltage drop caused by the wiring (other signal layer change vias should not be placed arbitrarily).

They must be placed regularly, leaving as much space as possible for power supply, which is also beneficial for the copper coating of the ground layer).

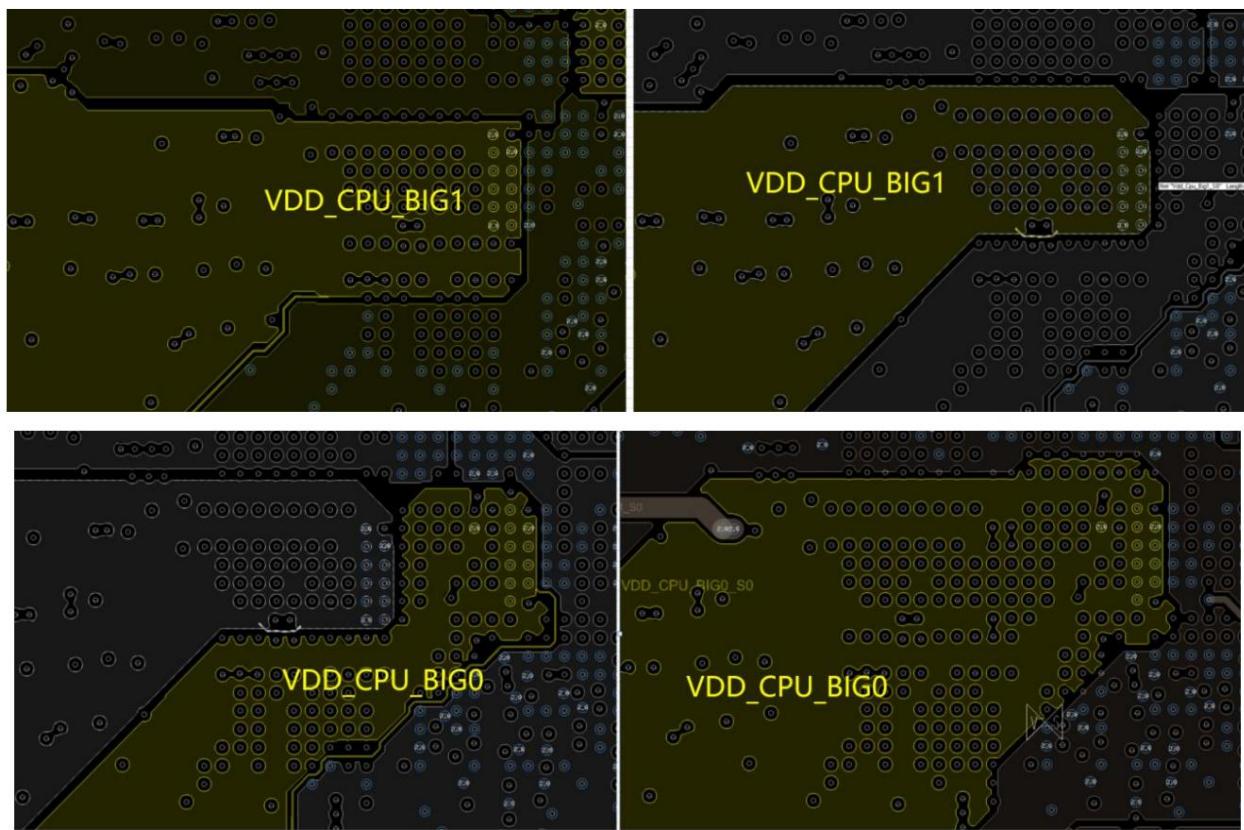


Figure 3-57 RK3588 chip VDD_CPU_BIG0/1 power layer copper coverage

The recommended number of GND vias within the 40mil range (via center to via center spacing) of the BIG0 power via is ≥ 12 .

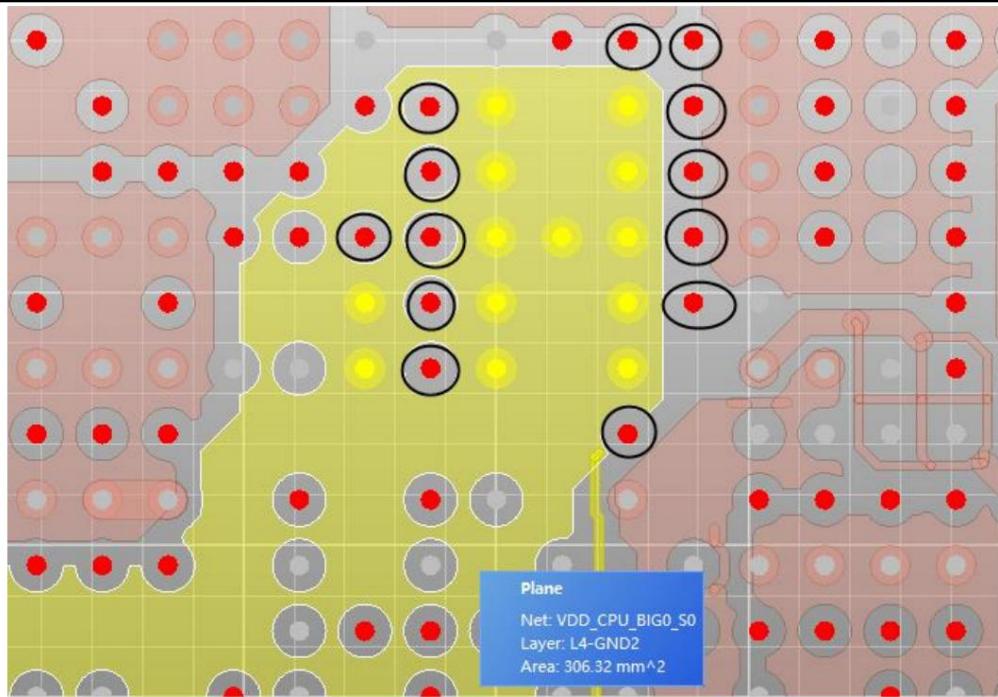


Figure 3-58 BIG0 power ground via placement diagram

The number of GND vias within the 40-mil range (via center to via center spacing) of the BIG1 power via is recommended to be ≥ 12 .

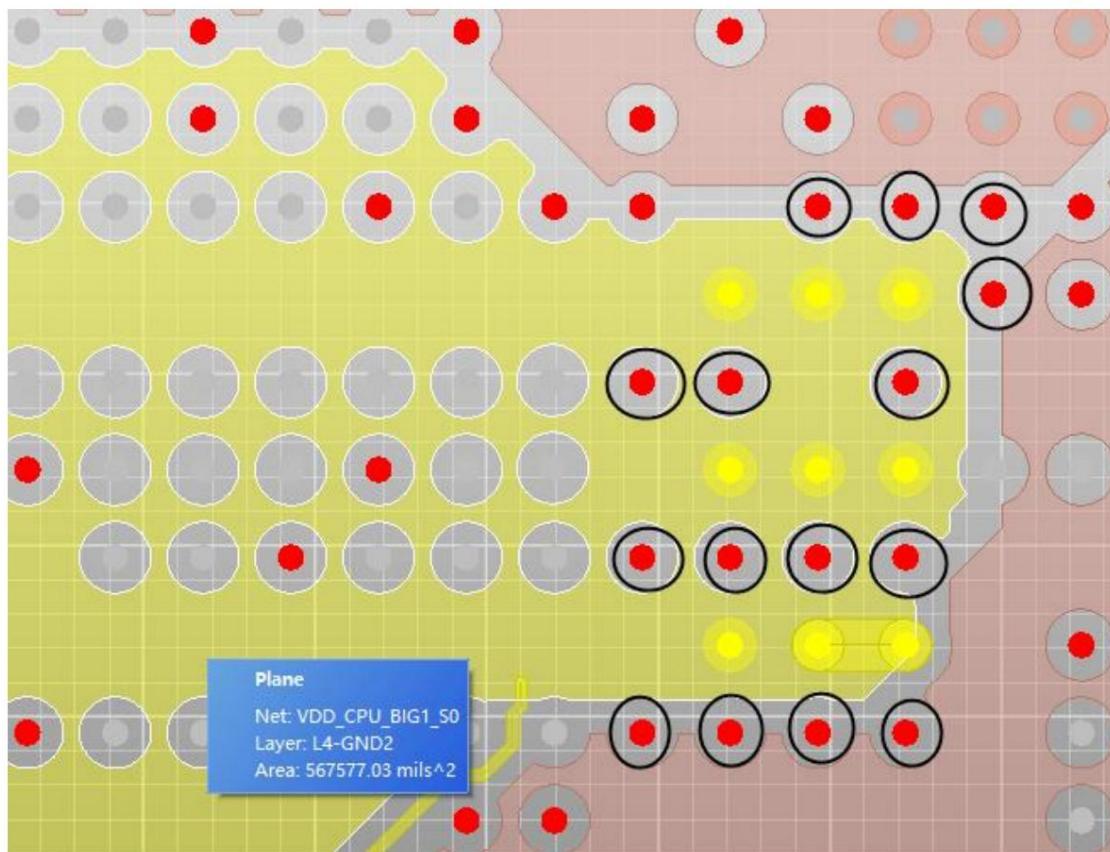


Figure 3-59 BIG1 power ground via placement diagram

3.4.2.6 RK3588 VDD_LOGIC Power Supply PCB Design

The copper width of VDD_LOGIC must meet the current requirements of the chip. The copper connected to the chip power pin is wide enough and the path cannot be crossed.

The hole segmentation is too severe, and the effective line width must be calculated to confirm that the path connected to each power PIN of the CPU is sufficient.

When the VDD_LOGIC power supply is changed on the periphery, it is necessary to make as many power vias as possible (more than 8 vias of 0.5*0.3mm) to reduce

The voltage drop caused by the layer-changing vias; the number of GND vias of the decoupling capacitor should be consistent with its power vias, otherwise the capacitance effect will be greatly reduced.

The power pin of RK3588 chip VDD_LOGIC, each ball needs to correspond to a via, and the top layer should be in a "well" shape, cross

For connection, the recommended trace width is 10 mil.

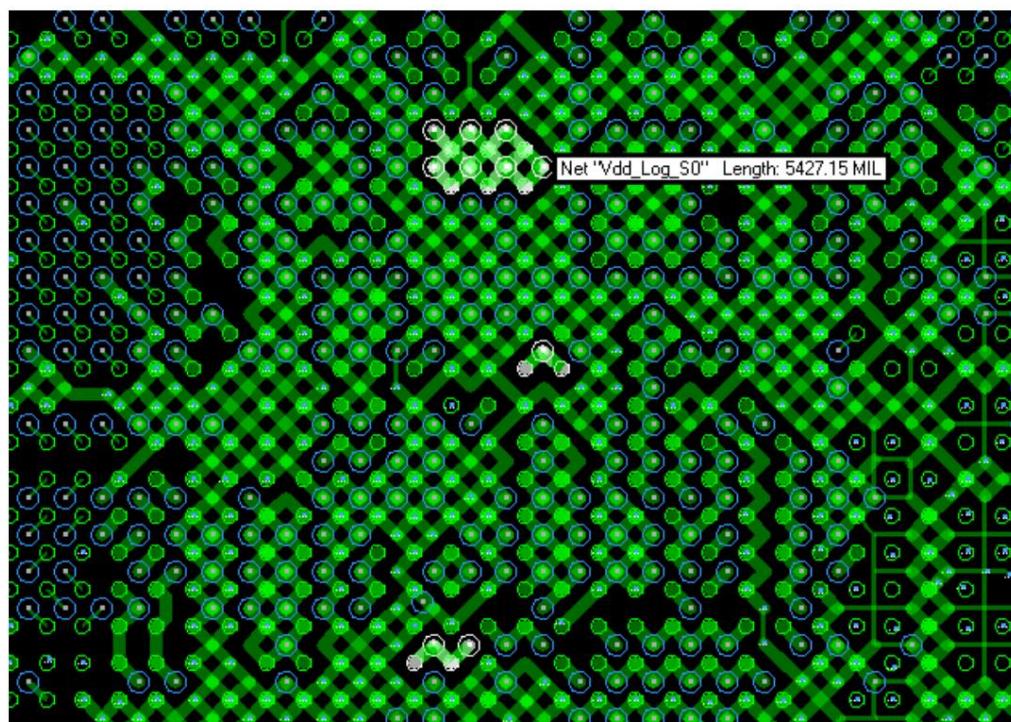


Figure 3-60 RK3588 chip VDD_LOGIC power pin routing and vias

The decoupling capacitor close to the VDD_LOGIC power pin of RK3588 on the schematic diagram must be placed on the back of the corresponding power pin.

Place the GND pad as close as possible to the GND Ball in the center of the chip, and the remaining decoupling capacitors as close as possible to RK3588.

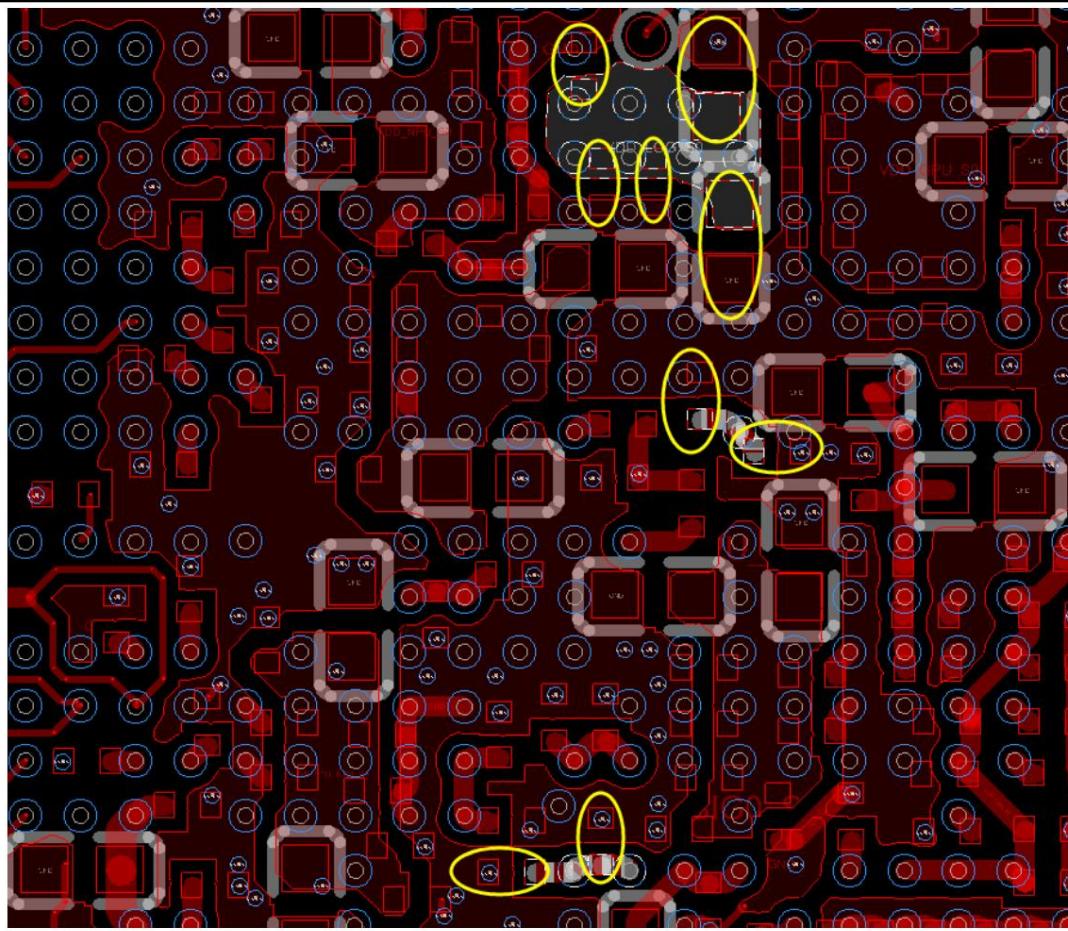


Figure 3-61 Decoupling capacitor placement on the back of the RK3588 chip VDD_LOGIC power pin

The width of VDD_LOGIC power supply in CPU area shall not be less than 120mil, and the width of peripheral area shall not be less than 200mil.

To reduce the voltage drop caused by the wiring (please do not place other signal layer-changing vias randomly, they must be placed regularly, and try to make room for the power supply).

(is conducive to copper coating of the ground layer).

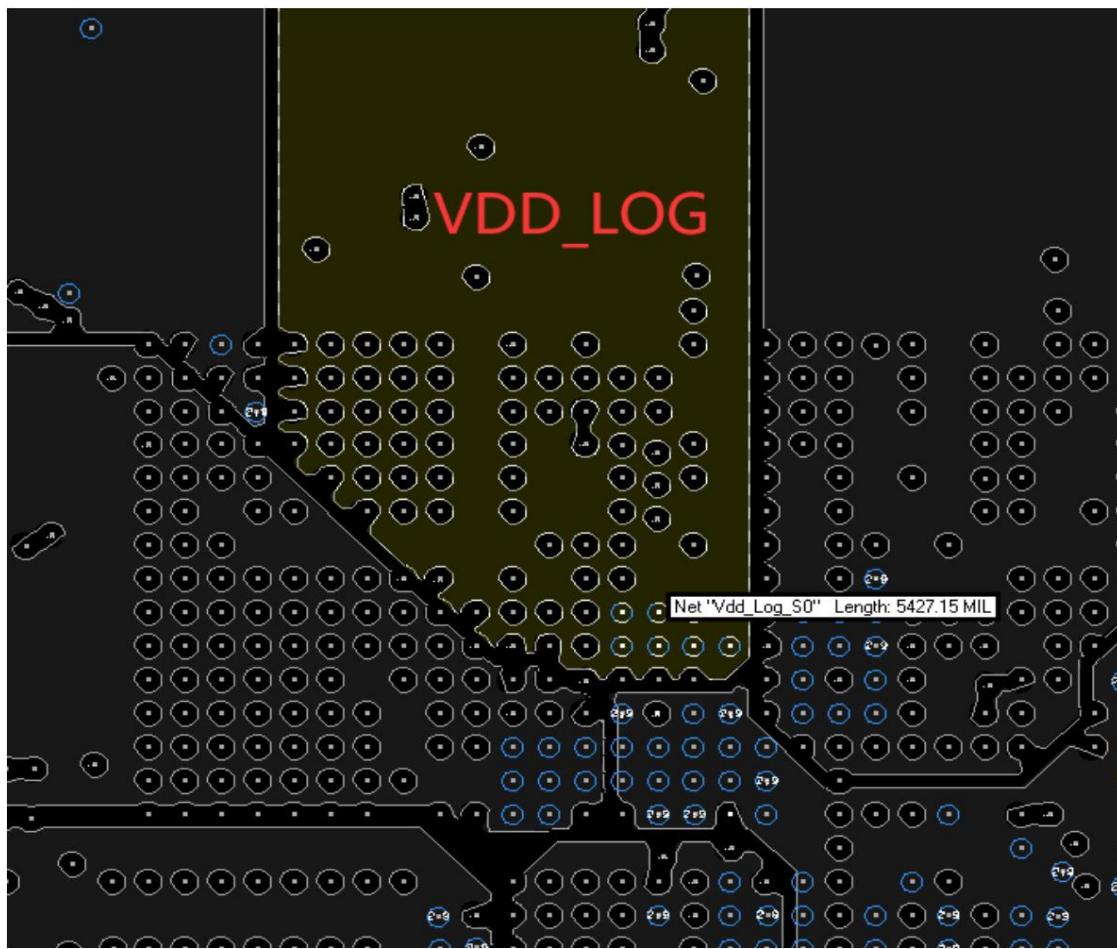


Figure 3-62 RK3588 chip VDD_LOGIC power layer copper coverage

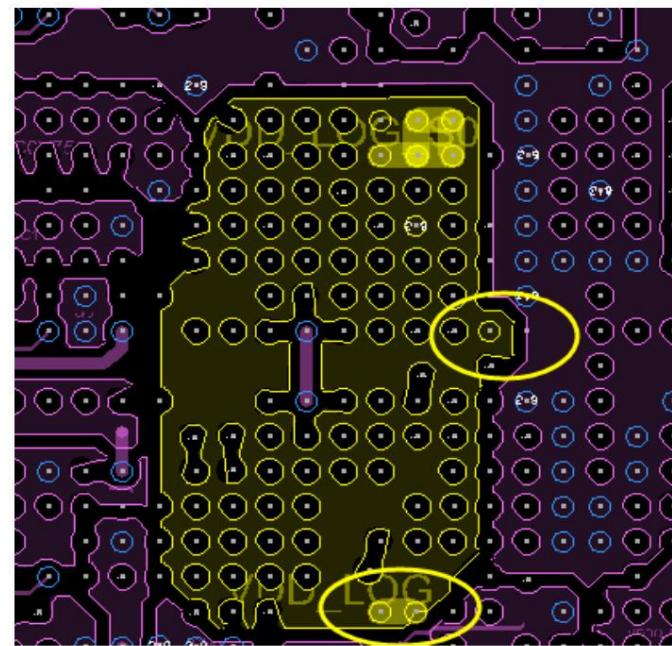


Figure 3-63 RK3588 chip VDD_LOGIC chip low power supply copper replacement situation

The recommended number of GND vias within the 40-mil range of the power vias (via center to via center spacing) is 11.

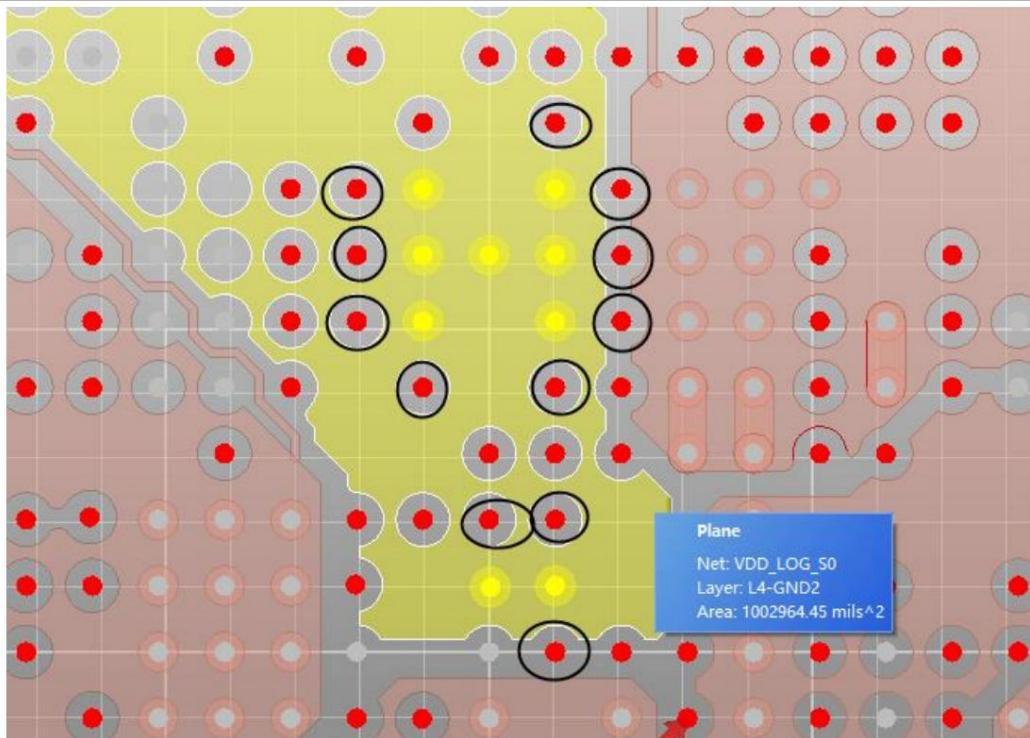


Figure 3-64 LOGIC power ground via placement diagram

3.4.2.7 RK3588 VDD_GPU Power Supply PCB Design

The copper width of VDD_GPU must meet the current requirements of the chip. The copper connected to the chip power pin is wide enough and the path cannot be blocked by vias.

The segmentation is too severe, and the effective line width must be calculated to confirm that the path connected to each power PIN of the CPU is sufficient.

When the power supply of VDD_GPU is changed on the periphery, it is necessary to make as many power vias as possible (more than 10 vias of 0.5*0.3mm) to reduce the switching time.

The voltage drop caused by the layer vias; the number of GND vias of the decoupling capacitor should be consistent with its power vias, otherwise the capacitance effect will be greatly reduced.

The power pin of RK3588 chip VDD_GPU needs to correspond to one via for each ball, and the top layer should be in a "well" shape, with cross connections.

It is recommended that the trace width be 10 mil.

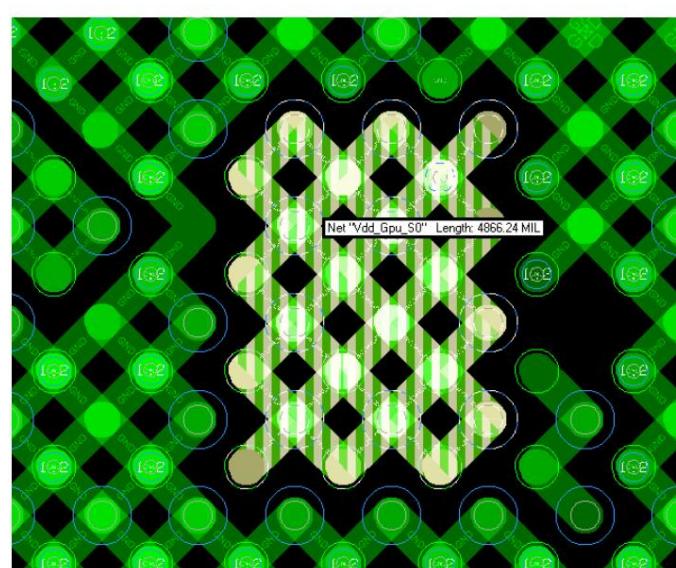


Figure 3-65 RK3588 chip VDD_GPU power pin routing and vias

The decoupling capacitor close to the VDD_GPU power pin of RK3588 on the schematic diagram must be placed on the back of the corresponding power pin, and the GND of the capacitor

Place the pad as close to the GND Ball in the center of the chip as possible, and the remaining decoupling capacitors as close to RK3588 as possible.

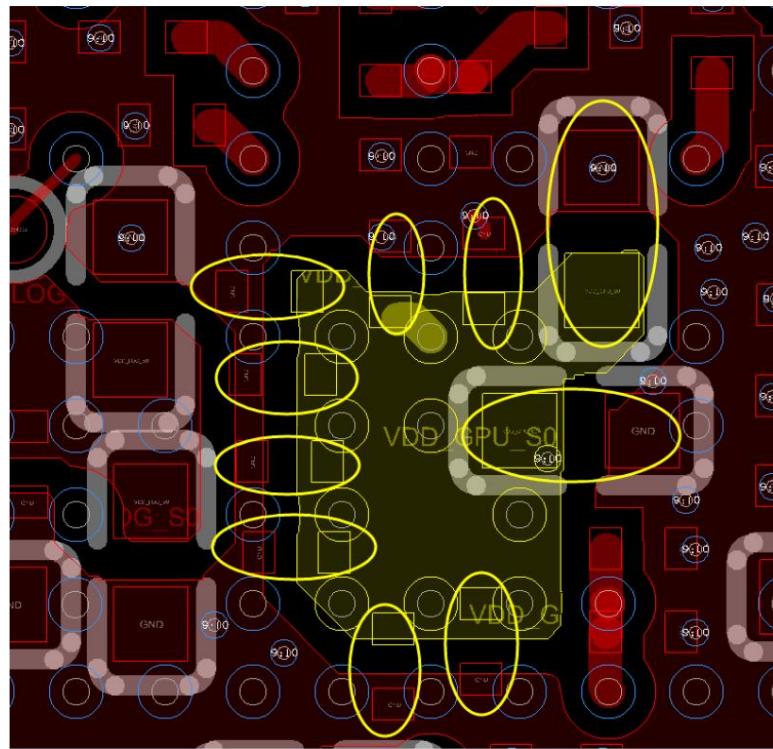


Figure 3-66 Decoupling capacitor placement on the back of the RK3588 chip VDD_GPU power pin

The VDD_GPU power supply line width in the GPU area shall not be less than 300mil, and the width in the peripheral area shall not be less than 500mil, using a two-layer copper cladding method.

Reduce the voltage drop caused by the wiring (please do not place other signal layer vias randomly, they must be placed regularly, and try to make room for power supply, which is also beneficial copper cladding of the ground layer).

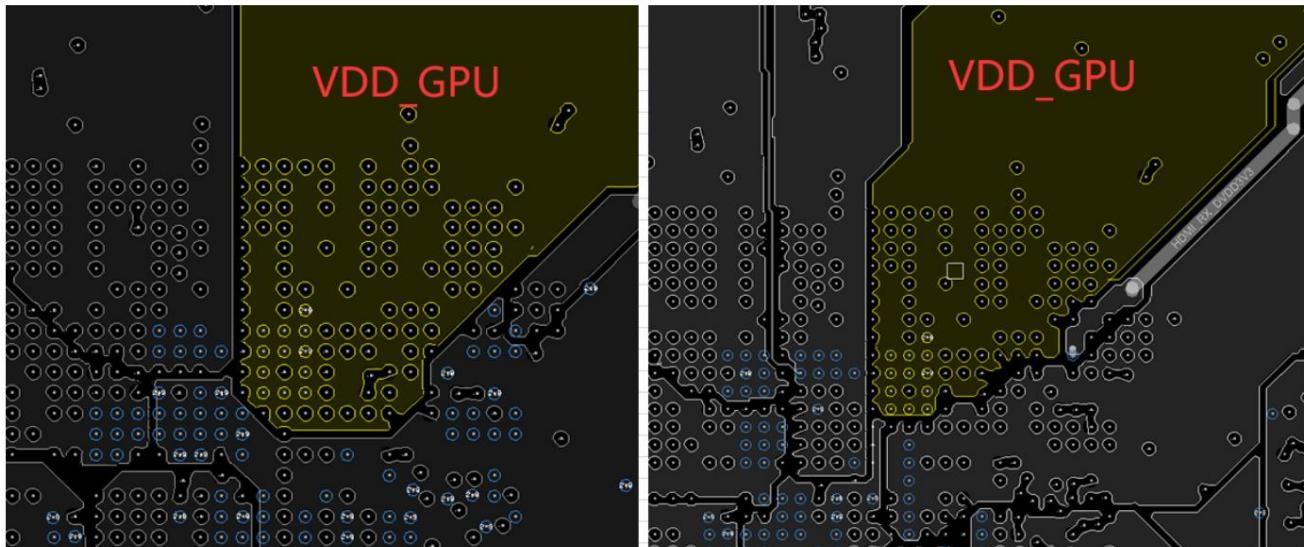


Figure 3-67 RK3588 chip VDD_GPU power layer copper coverage

The recommended number of GND vias within the 40mil range of the power vias (via center to via center spacing) is 14.

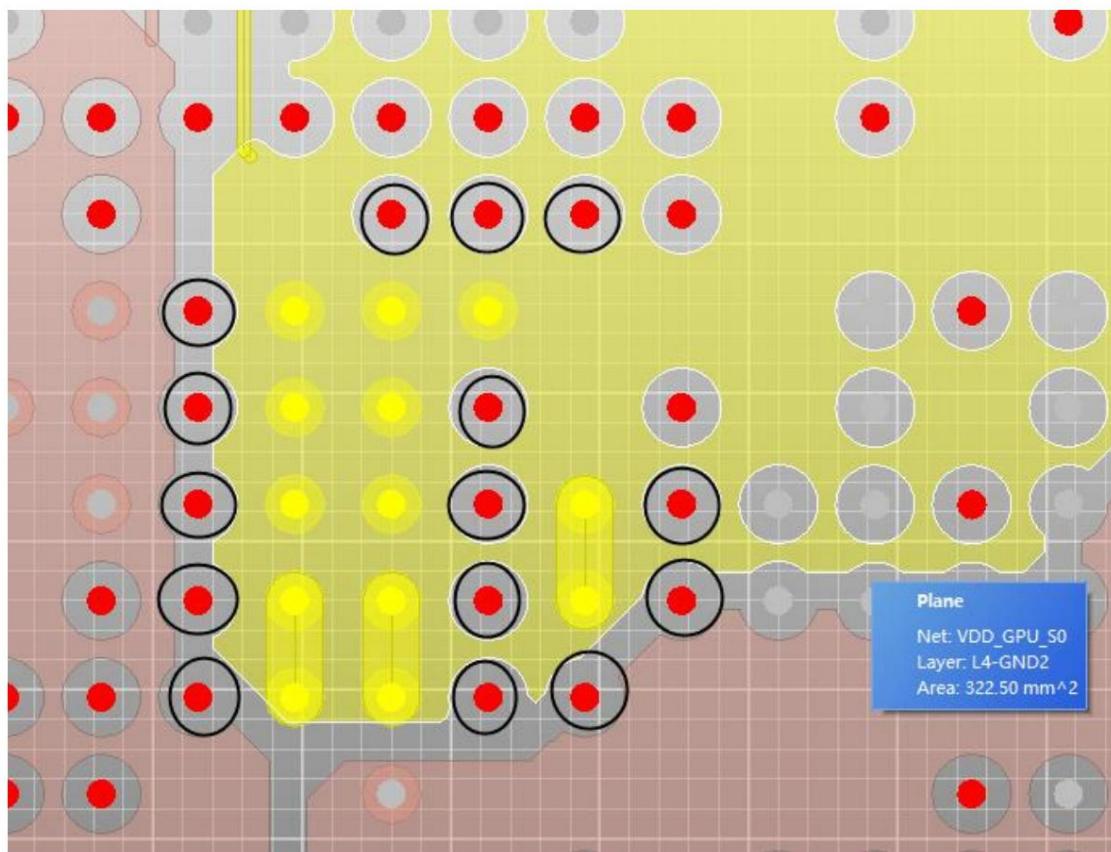


Figure 3-68 GPU power ground via placement diagram

3.4.2.8 RK3588 VDD_NPU Power Supply PCB Design

The copper width of VDD_NPU must meet the current requirements of the chip. The copper connected to the chip power pin is wide enough and the path cannot be blocked by vias.

The segmentation is too severe, and the effective line width must be calculated to confirm that the path connected to each power PIN of the CPU is sufficient.

When the power supply of VDD_NPU is changed on the periphery, it is necessary to make as many power vias as possible (more than 7 vias of 0.5*0.3mm) to reduce the switching time.

The voltage drop caused by the layer vias; the number of GND vias of the decoupling capacitor should be consistent with its power vias, otherwise the capacitance effect will be greatly reduced.

The power pin of RK3588 chip VDD_NPU has a corresponding via near each ball, and the top layer is in a "well" shape, crossing

For connection, the recommended trace width is 10 mil.

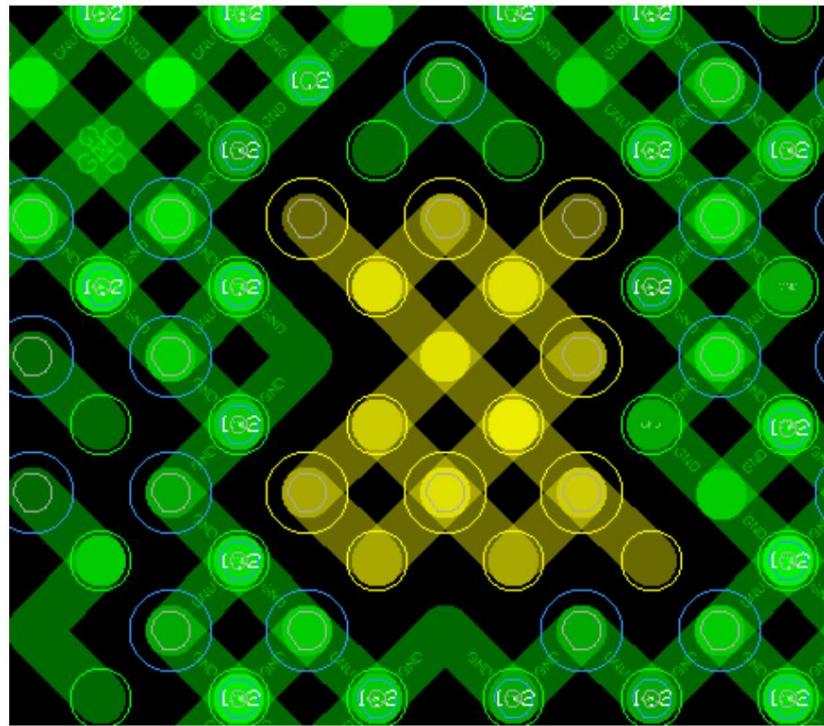


Figure 3-69 RK3588 chip VDD_NPU power pin routing and vias

The decoupling capacitor close to the VDD_NPU power pin of RK3588 on the schematic diagram must be placed on the back of the corresponding power pin, and the GND of the capacitor

Place the pad as close to the GND Ball in the center of the chip as possible, and the remaining decoupling capacitors as close to RK3588 as possible.

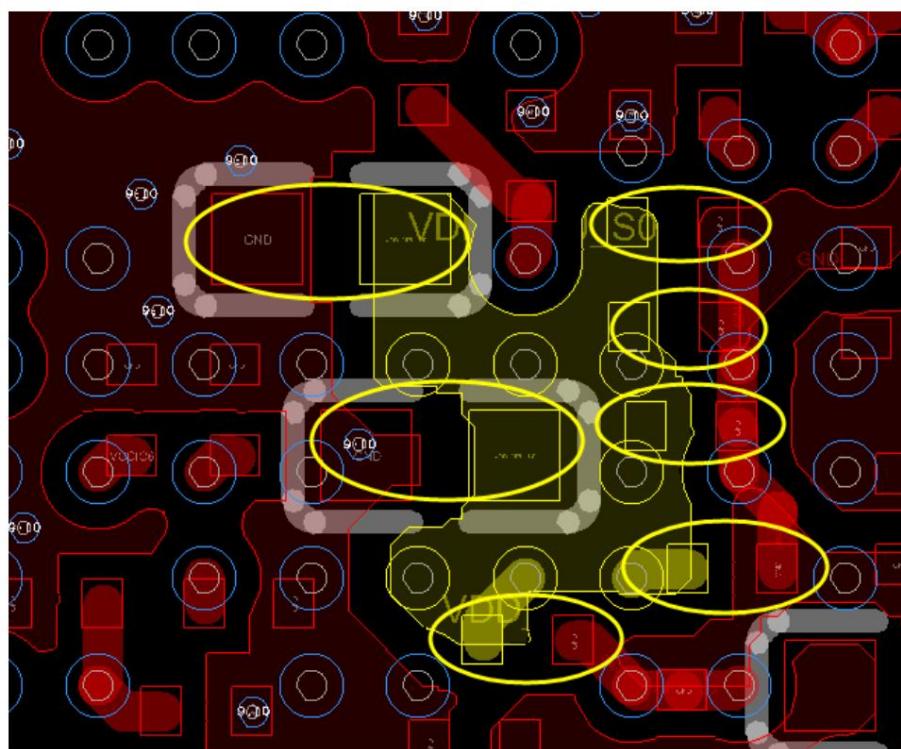


Figure 3-70 Decoupling capacitor placement on the back of the RK3588 chip VDD_NPU power pin

The width of the VDD_NPU power supply line in the NPU area shall not be less than 300mil, and the width of the peripheral area shall not be less than 500mil. Copper cladding should be used as much as possible.

Reduce the voltage drop caused by the wiring (please do not place other signal layer vias randomly, they must be placed regularly, and try to make room for power supply, which is also beneficial

copper cladding of the ground layer).

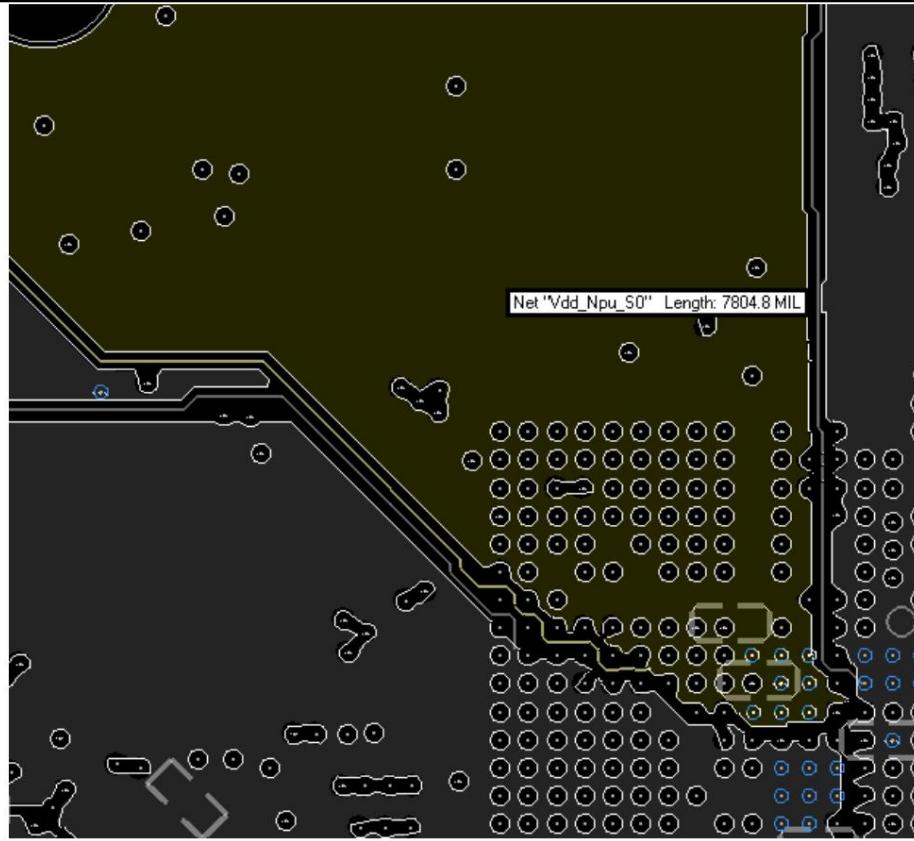


Figure 3-71 RK3588 chip VDD_NPU power layer copper coverage

The recommended number of GND vias within the 40mil range of the power vias (via center to via center spacing) is ≥ 9 .

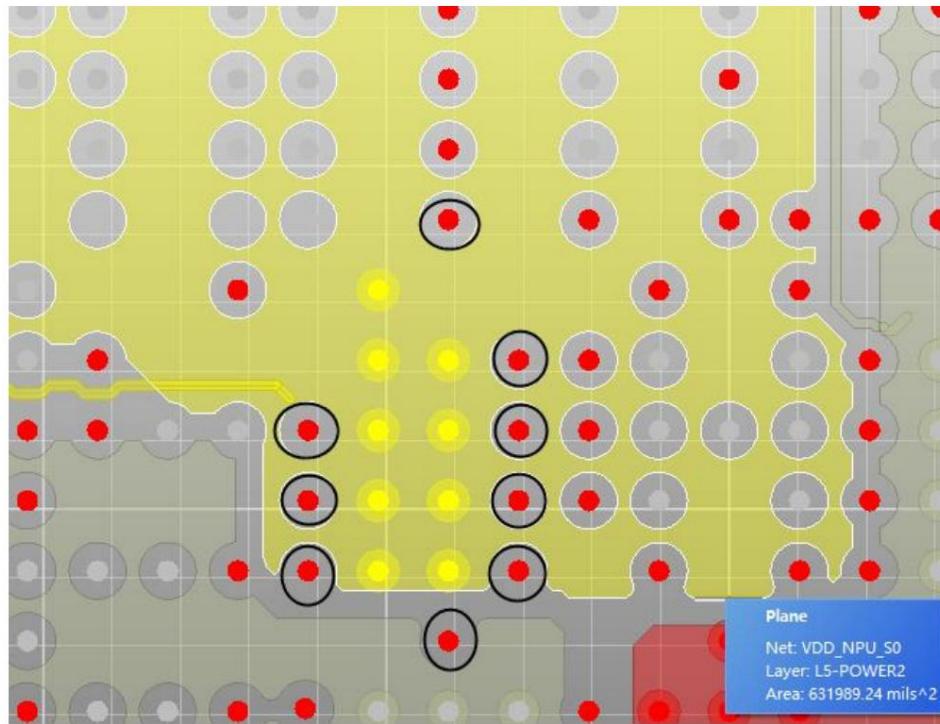


Figure 3-72 NPU power ground via placement diagram

3.4.2.9 RK3588 VDD_CPU_LIT Power Supply PCB Design

The copper width of VDD_CPU_LIT must meet the current requirements of the chip. The copper connected to the chip power pin is wide enough and the path cannot be blocked.

The via segmentation is too severe, and the effective line width must be calculated to ensure that there is enough path to connect to each power pin of the CPU.

When the VDD_CPU_LIT power supply is changed on the periphery, as many power vias as possible (more than 9 0.5*0.3mm vias) should be drilled to reduce the voltage drop caused by the layer change vias; the number of GND vias of the decoupling capacitor should be consistent with its power vias, otherwise the capacitance effect will be greatly reduced.

The power pins of the RK3588 chip VDD_CPU_LIT have a corresponding via near each ball, and the top layer is arranged in a "well" shape.

For cross-connection, the recommended trace width is 10 mil.

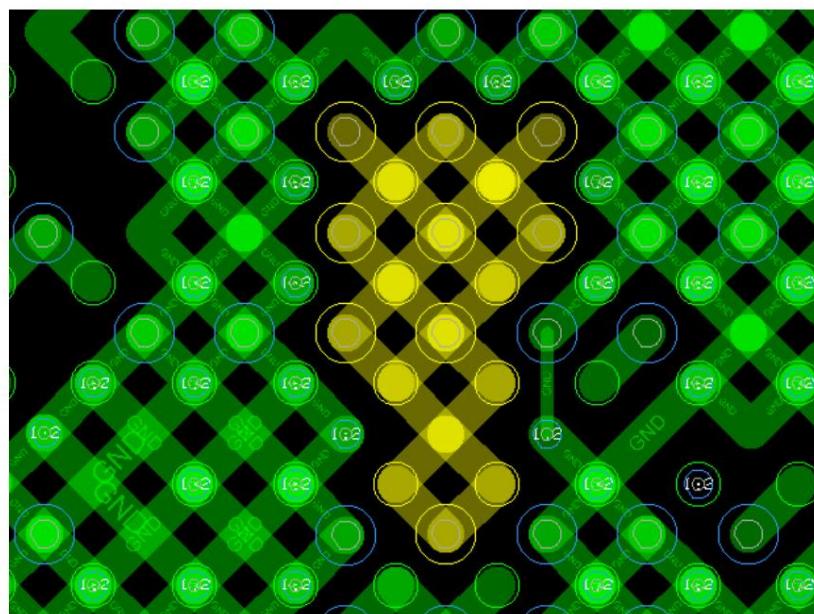


Figure 3-73 RK3588 chip VDD_CPU_LIT power pin routing and vias

The decoupling capacitor close to the VDD_CPU_LIT power pin of RK3588 on the schematic diagram must be placed on the back of the corresponding power pin.

Place the GND pad as close as possible to the GND Ball in the center of the chip, and the remaining decoupling capacitors as close as possible to RK3588.



Figure 3-74 Decoupling capacitor placement on the back of the RK3588 chip VDD_CPU_LIT power pin

The VDD_CPU_LIT power supply line width in the CPU area shall not be less than 120mil, and the width in the peripheral area shall not be less than 300mil. A double-layer power supply is used.

Copper covering method can reduce the voltage drop caused by routing (other signal layer-changing vias should not be placed randomly, they must be placed regularly, and try to make room for power supply, which is also conducive to copper covering of the ground layer).



Figure 3-75 RK3588 chip VDD_CPU_LIT power layer copper coverage

The recommended number of GND vias within the 40mil range of the power vias (via center to via center spacing) is ≥ 9.

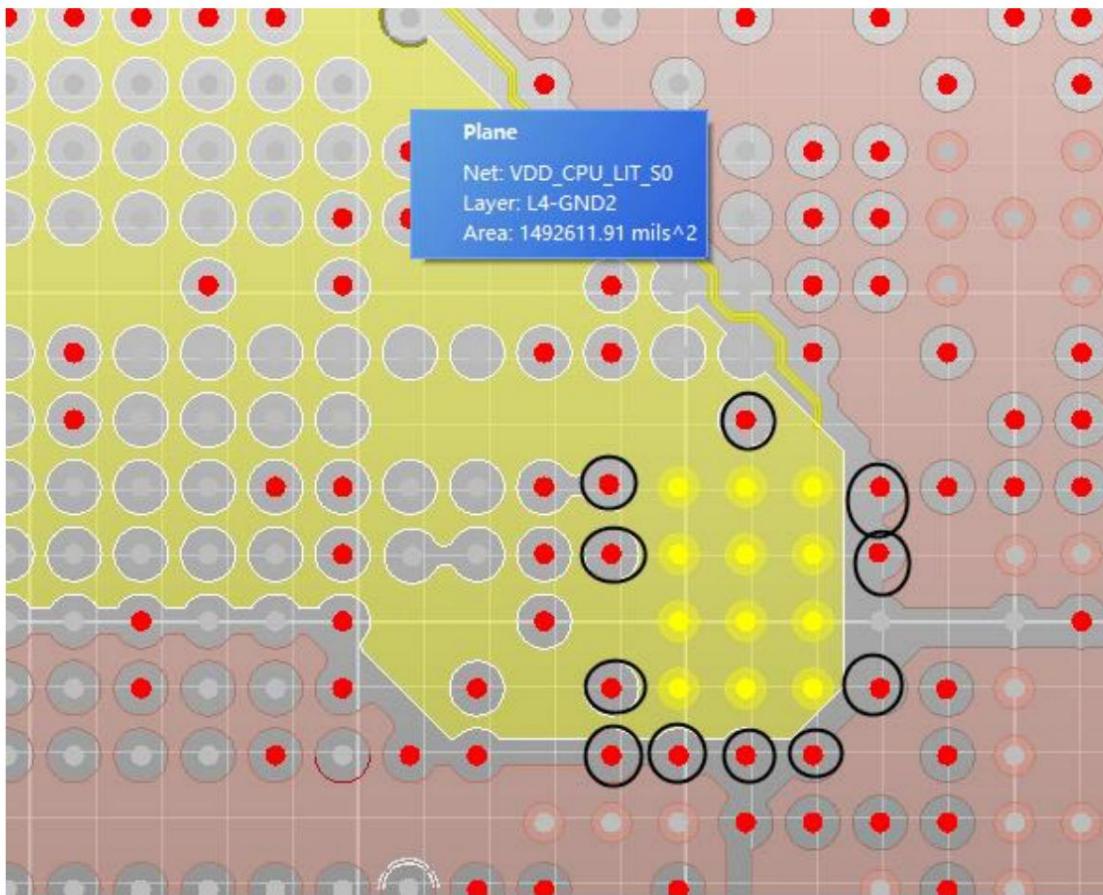


Figure 3-76 LIT power ground via placement diagram

3.4.2.10 RK3588 VDD_VDENC Power Supply PCB Design

The copper width of VDD_VDENC must meet the current requirements of the chip. The copper connected to the chip power pin is wide enough and the path cannot be crossed.

The hole segmentation is too severe, and the effective line width must be calculated to confirm that the path connected to each power PIN of the CPU is sufficient.

When the VDD_VDENC power supply is changed on the periphery, it is necessary to make as many power vias as possible (more than 9 vias of 0.5*0.3mm) to reduce

The voltage drop caused by the layer-changing vias; the number of GND vias of the decoupling capacitor should be consistent with its power vias, otherwise the capacitance effect will be greatly reduced.

The power pins of the RK3588 chip VDD_VDENC have a corresponding via near each ball, and the top layer is arranged in a "well" shape.

For cross-connection, the recommended trace width is 10 mil.

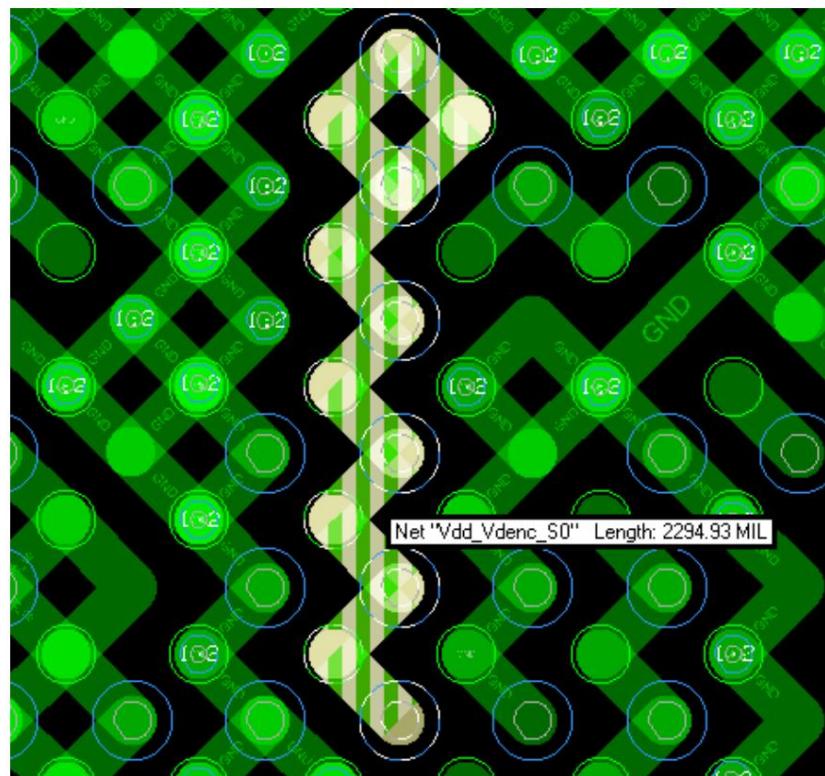


Figure 3-77 RK3588 chip VDD_VDENC power pin routing and vias

The decoupling capacitor close to the VDD_VDENC power pin of RK3588 on the schematic diagram must be placed on the back of the corresponding power pin.

Place the GND pad as close as possible to the GND Ball in the center of the chip, and the remaining decoupling capacitors as close as possible to RK3588.

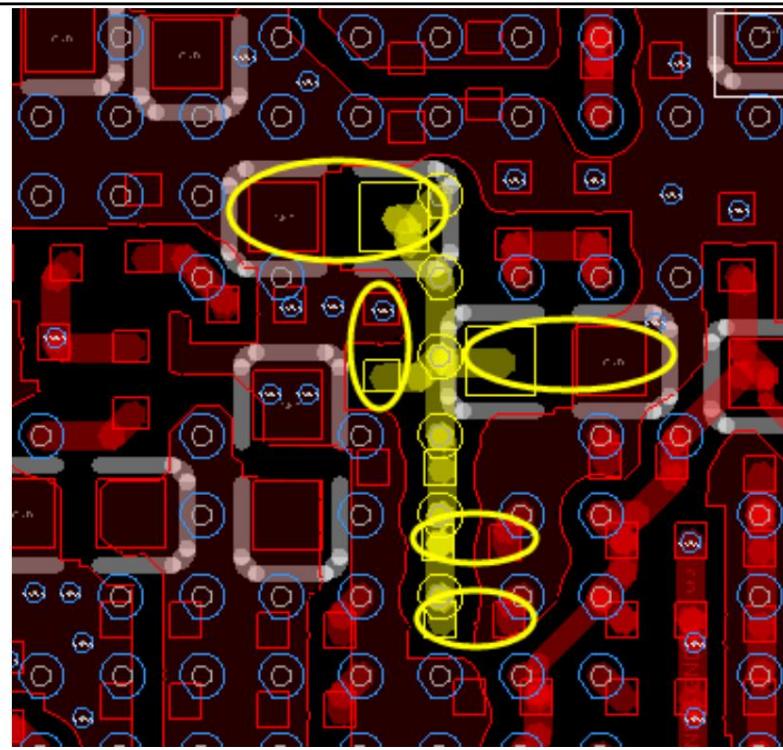


Figure 3-78 Decoupling capacitor placement on the back of the RK3588 chip VDD_VDENC power pin

The width of VDD_VDENC power supply in CPU area shall not be less than 100mil, and the width of peripheral area shall not be less than 300mil. Double-layer power supply cover shall be used.

Copper method, reduce the voltage drop caused by the wiring (other signal layer change vias should not be placed randomly, they must be placed regularly, and try to make room for power supply).

It is also beneficial to the copper coating of the ground layer.



Figure 3-79 RK3588 chip VDD_VDENC power layer copper coverage

The recommended number of GND vias within the 30mil range of the power vias (via center to via center spacing) is 8.

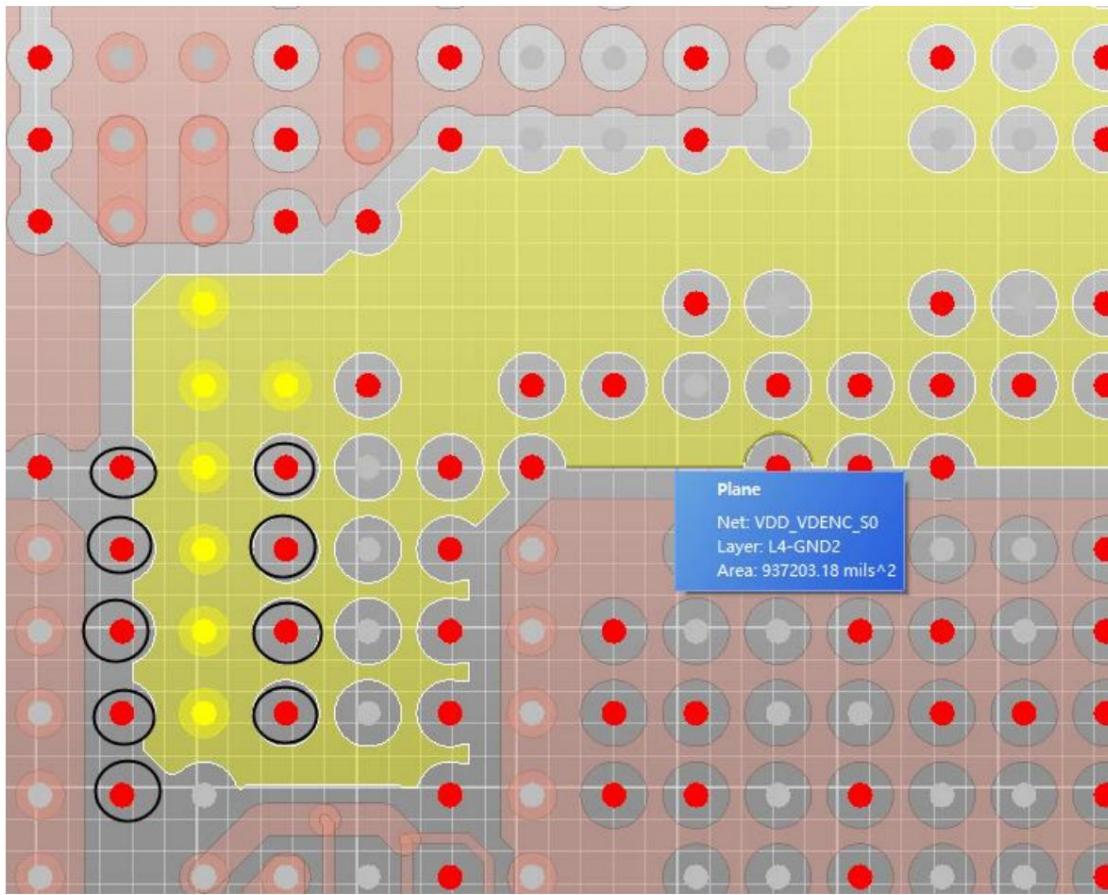


Figure 3-80 VDENC power ground via placement diagram

3.4.2.11 RK3588 VCC_DDR Power Supply PCB Design

The copper width of VCC_DDR must meet the current requirements of the chip. The copper connected to the chip power pin is wide enough and the path cannot be blocked by vias.

The segmentation is too severe, and the effective line width must be calculated to confirm that the path connected to each power PIN of the CPU is sufficient.

When the VCC_DDR power supply is changed on the periphery, it is necessary to make as many power vias as possible (more than 9 vias of 0.5*0.3mm) to reduce the change time.

The voltage drop caused by the layer vias; the number of GND vias of the decoupling capacitor should be consistent with its power vias, otherwise the capacitance effect will be greatly reduced.

The power pins of RK3588 chip VCC_DDR, each ball needs to correspond to a via, and the top layer should be in a "well" shape, cross-connected

It is recommended that the trace width be 10 mil.



Figure 3-81 RK3588 chip VCC_DDR & VDDQ_DDR power pin routing and vias

For LPDDR4x:



Figure 3-82 RK3588 chip LPDDR4x mode VCC_DDR/VCC0V6_DDR power pin routing and vias

The decoupling capacitor close to the VCC_DDR power pin of RK3588 on the schematic diagram must be placed on the back of the corresponding power pin, and the GND of the capacitor

Place the pad as close to the GND Ball in the center of the chip as possible, and the remaining decoupling capacitors as close to RK3588 as possible.

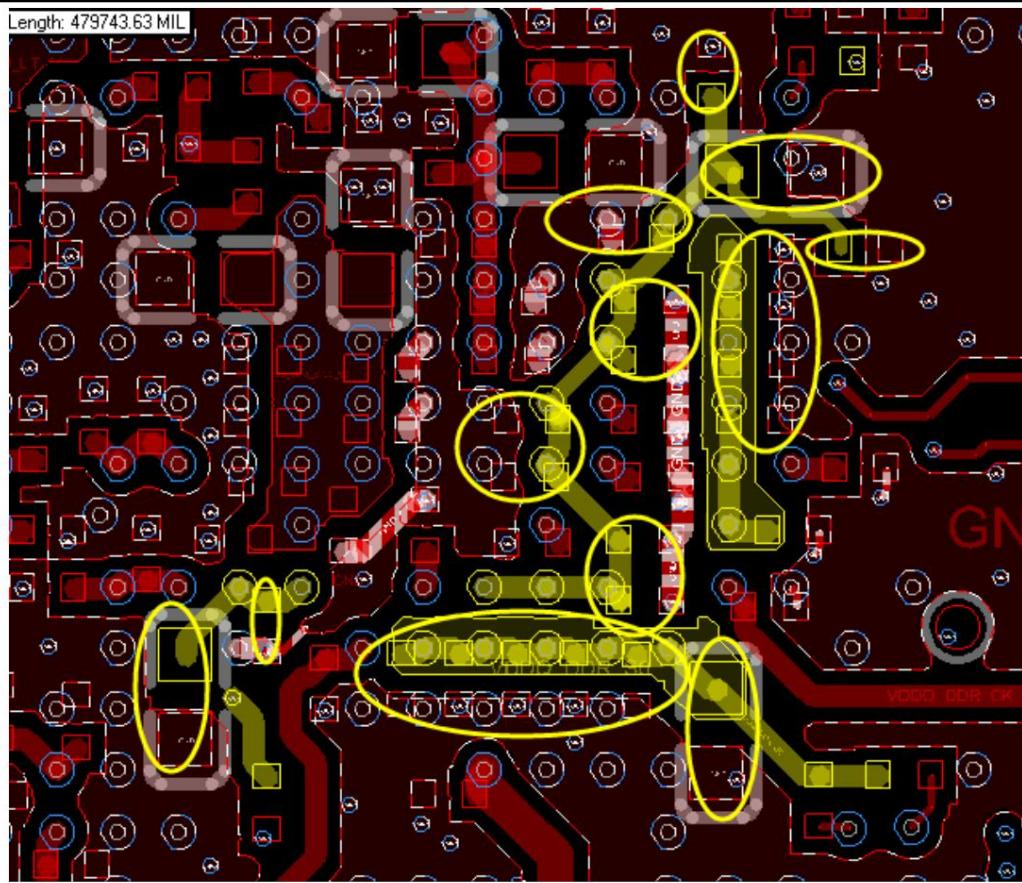


Figure 3-83 Decoupling capacitor placement on the back of the RK3588 chip VCC_DDR & VDDQ_DDR power pins

The VCC_DDR power supply line width in the CPU area shall not be less than 120mil, and the width in the peripheral area shall not be less than 200mil. Copper cladding shall be used as much as possible.

Reduce the voltage drop caused by the wiring (please do not place other signal layer vias randomly, they must be placed regularly, and try to make room for power supply, which is also beneficial

copper cladding of the ground layer).

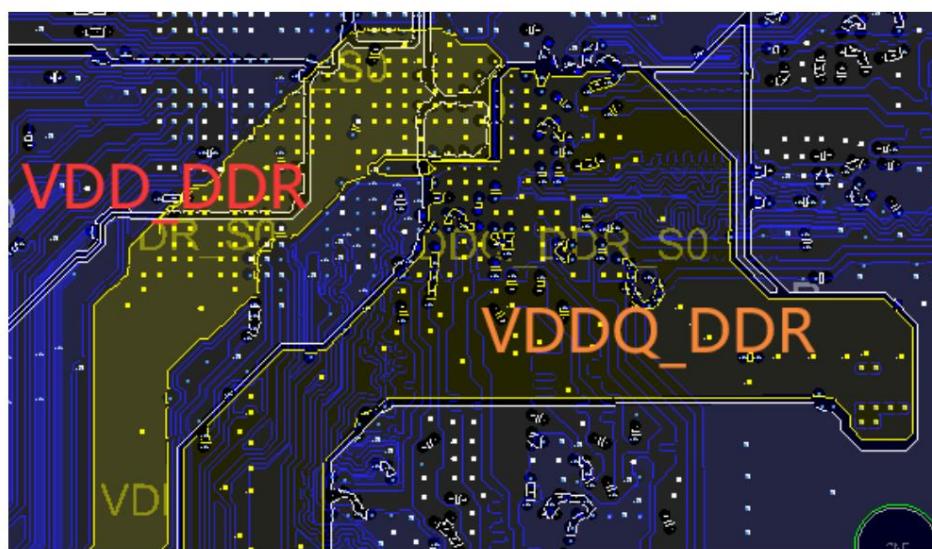


Figure 3-84 RK3588 chip VCC_DDR & VDDQ_DDR power layer copper coverage

3.4.2.12 RK3588 GND pin PCB design

The GND pin of the RK3588 chip should have at least one via for every 1.5 balls, and try to have one via for every ball.

It provides better SI and PI conditions and also helps with heat dissipation.

The adjacent layer of the RK3588 chip must be a complete GND plane to ensure that the main reference ground is close to the CPU ball to ensure power integrity and enhance the heat dissipation of the PCB.

The GND balls of the same network under the RK3588 chip are arranged in a "well" shape on the top layer and cross-connected. The recommended trace width is 10 mil.

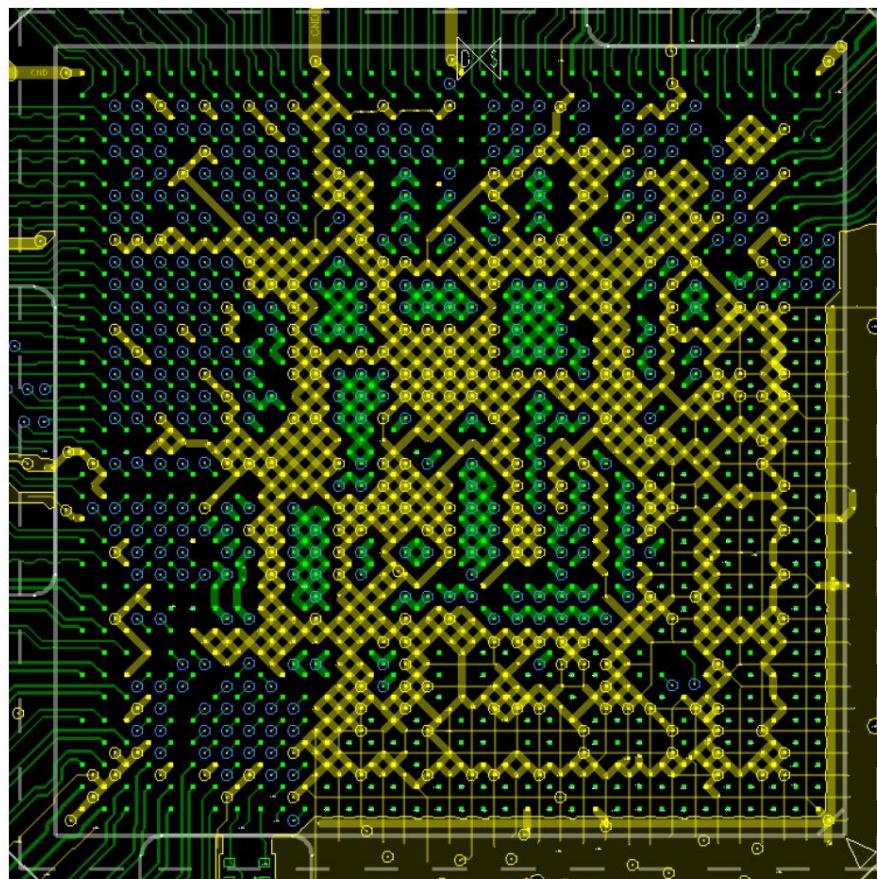


Figure 3-85 RK3588 chip VSS pin routing and vias

During layout, when placing the layer-changing vias for each signal of RK3588, they must be placed in the middle of the ball interval and in a regular pattern. As shown in the figure, the copper covering of the GND layer. The ground in the middle of the RK3588 chip has a large area of copper connected to the copper outside. On the one hand, it is beneficial to power supply and signal integrity, and on the other hand, it is beneficial to chip heat dissipation.

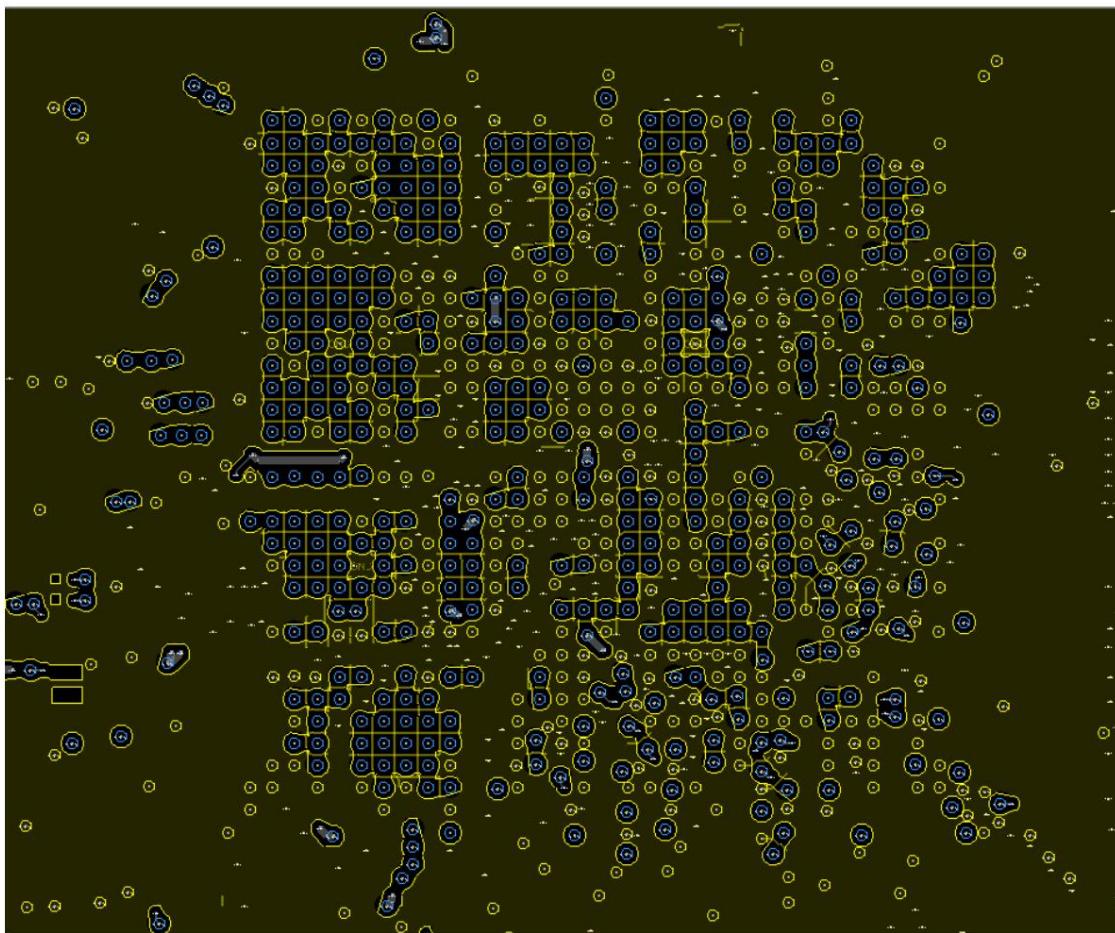


Figure 3-86 RK3588 chip ground layer copper coverage

3.4.2.13 PCB Design of Other Power Supplies for RK3588

The decoupling capacitors of other power supplies of RK3588 must be placed on the back of the chip pins. When routing, try to form a pattern that passes through the capacitor pads first and then to the chip pins.

3.4.3 DRAM Circuit PCB Design

The performance of 10-layer HDI PCB for LPDDR4 and LPDDR4X interfaces is better than that of 8-layer through-hole PCB. It is recommended to give priority to 10-layer HDI PCB.

The LPDDR5 interface template is a 10-layer HDI PCB board.

3.4.3.1 DRAM Circuit PCB Design (10 -Layer HDI PCB)

Since the RK3588 DDR interface rate is j4266bps, PCB design is difficult, so we strongly recommend using the DDR template and corresponding DDR firmware we provide. The DDR template is released after rigorous simulation and test verification. If you design the PCB yourself, please refer to the following

PCB design suggestions: It is strongly recommended to perform simulation optimization before releasing the board.

(1) For CPU pins, the number of corresponding GND vias is recommended to strictly refer to the template design and GND vias cannot be deleted. Example 10 layers

The HDI first-order PCB template and the CPU pin GND via design are shown in the figure below.

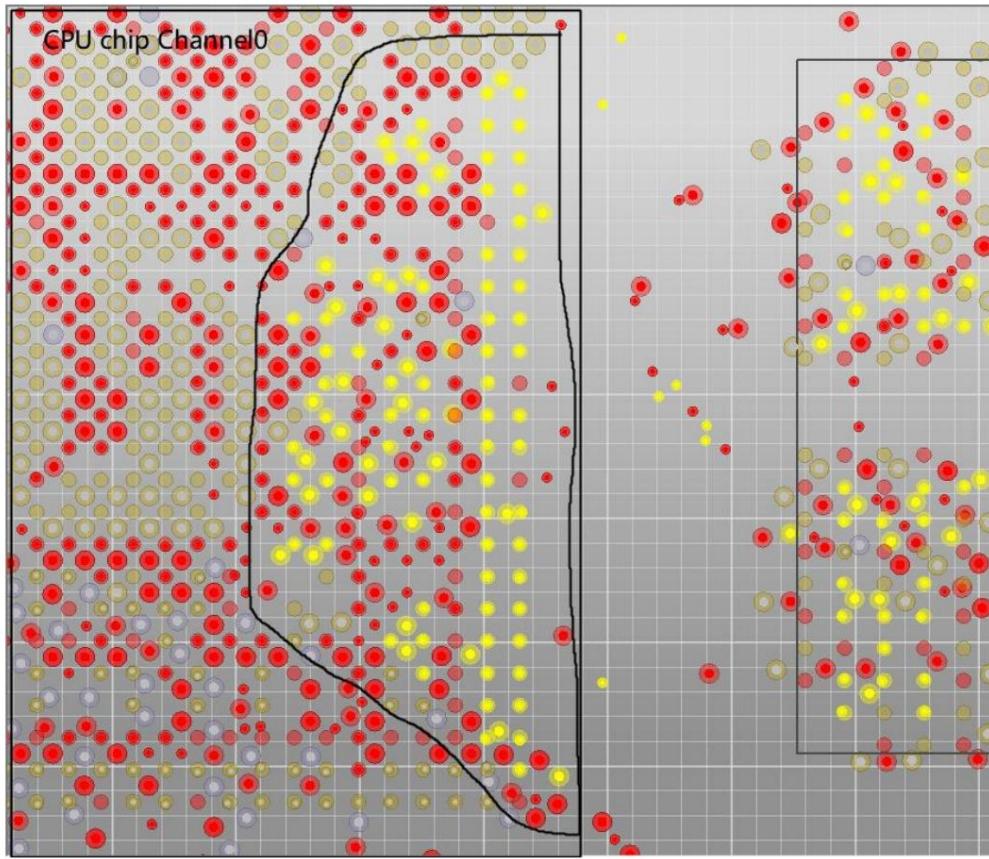


Figure 3-87

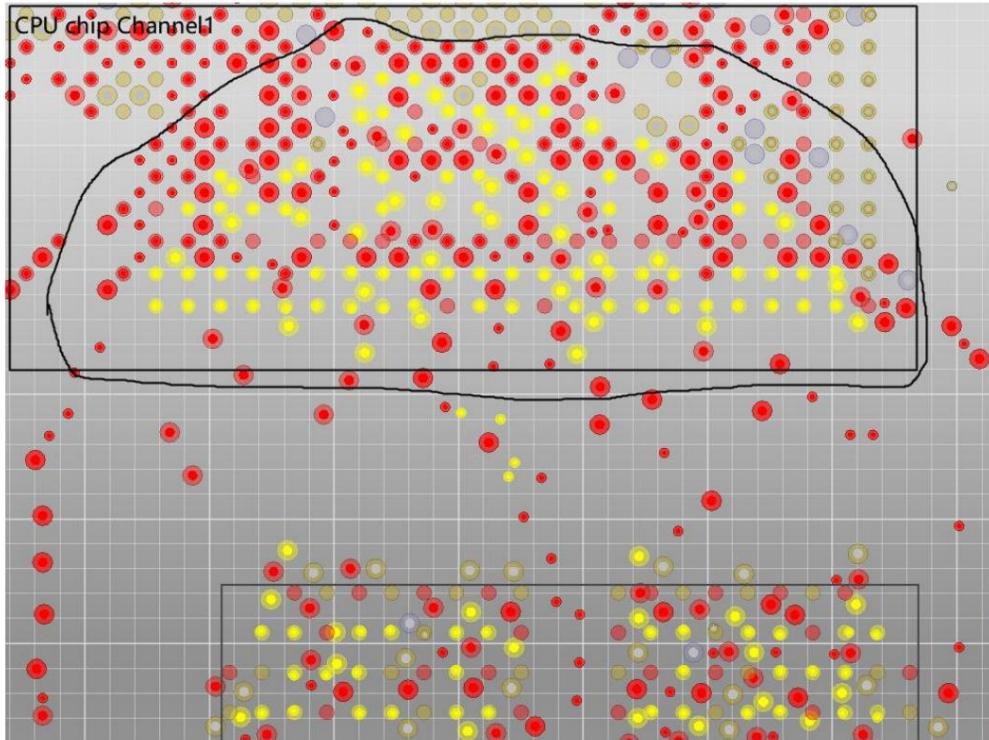


Figure 3-88

(2) Before and after the signal layer is changed, when the reference layer is the GND plane, within the range of 25mil (the center distance between vias) of the signal via GND return vias need to be added to improve the signal return path. GND vias need to connect the GND reference planes before and after the signal layer change. Each signal via must have at least one GND return via. Increasing the number of GND return vias as much as possible can further improve signal quality.

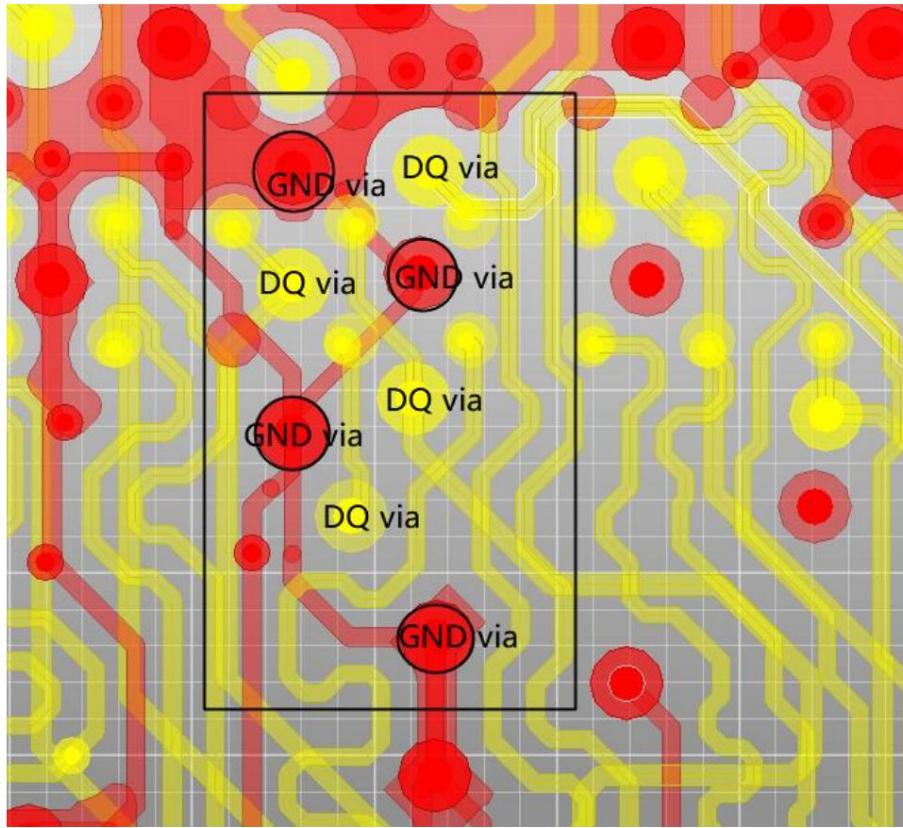


Figure 3-89

(3) The position of GND vias and signal vias will affect the signal quality. It is recommended that GND vias and signal vias be placed crosswise as shown in the figure below.

Although the figure below also shows 4 GND return vias, the situation where 4 signal vias are placed together should be avoided, as the crosstalk of the vias will be the greatest in this case.

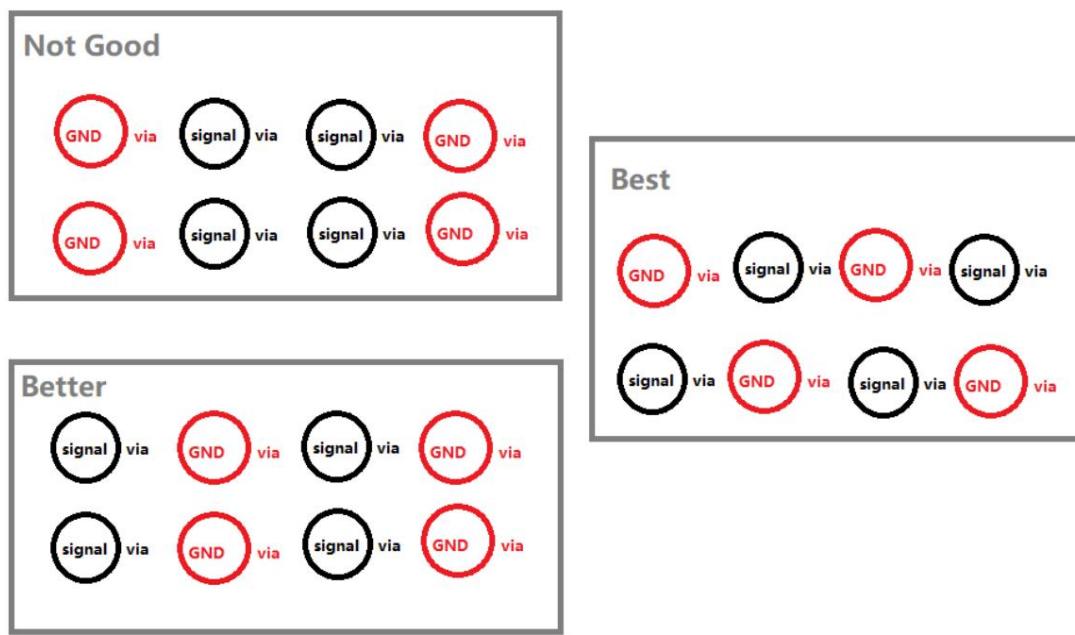


Figure 3-90

(4) DQ and DQS signals need to refer to a complete GND plane. If the GND plane is incomplete, it will have a great impact on the signal quality.

It is recommended that the address and control signals should preferably reference the complete GND plane. If this cannot be met, it is acceptable to route the address and control signals on the inner layer, with one layer referencing the complete GND plane and one layer referencing the power plane.

(5) As shown in the figure below, when the vias cause the signal reference layer to break, you can consider using GND traces to optimize the lower reference layer to improve the signal quality.

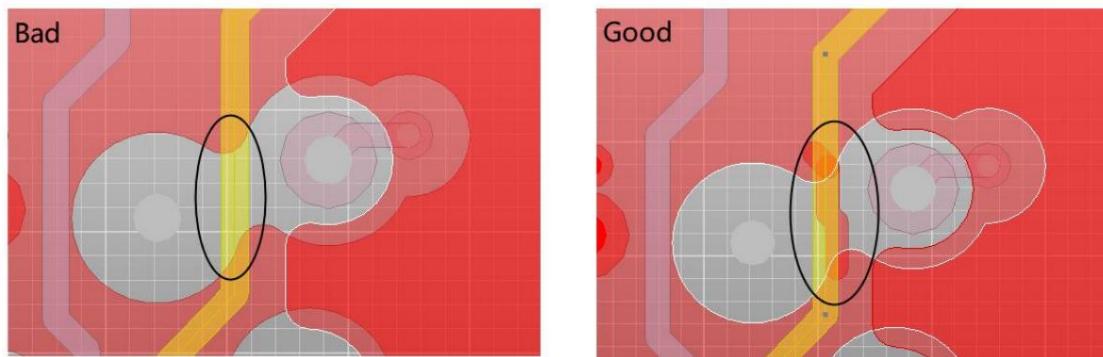


Figure 3-91

(6) The closer the trace is to the edge of the reference layer, the greater the signal impedance will be. The distance between the trace and the edge of the reference layer is recommended to be $\geq 12\text{mil}$.

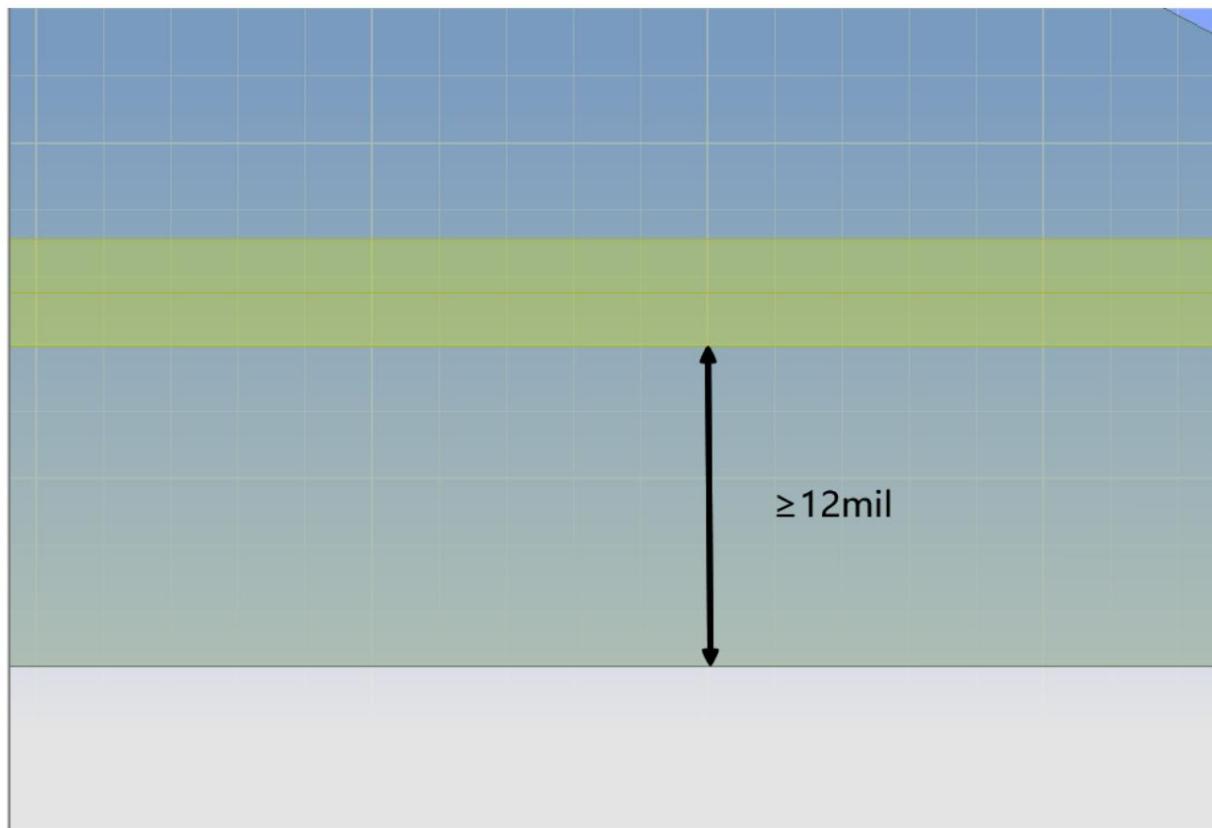


Figure 3-92

(7) The delay of stripline and microstrip line is different. The delay of microstrip differential signal is different from that of single-ended signal.

The delay difference with single-ended signal is small. Refer to Demo PCB design, DQ, DQS, CLK, WCLK signals are routed on the inner layer. CKE signal is recommended to be routed on the surface layer to better meet the target impedance of 50 ohms, and other address lines and control lines are routed on the inner layer.

For inner layer routing, the inner layer signal rate difference is not much, the PCB is designed according to the equal length rule, and the PCB software setting will be relatively simple.

(8) The crosstalk of the winding itself will affect the signal delay. It is recommended that $S \geq 3W$ when the wiring is of equal length.

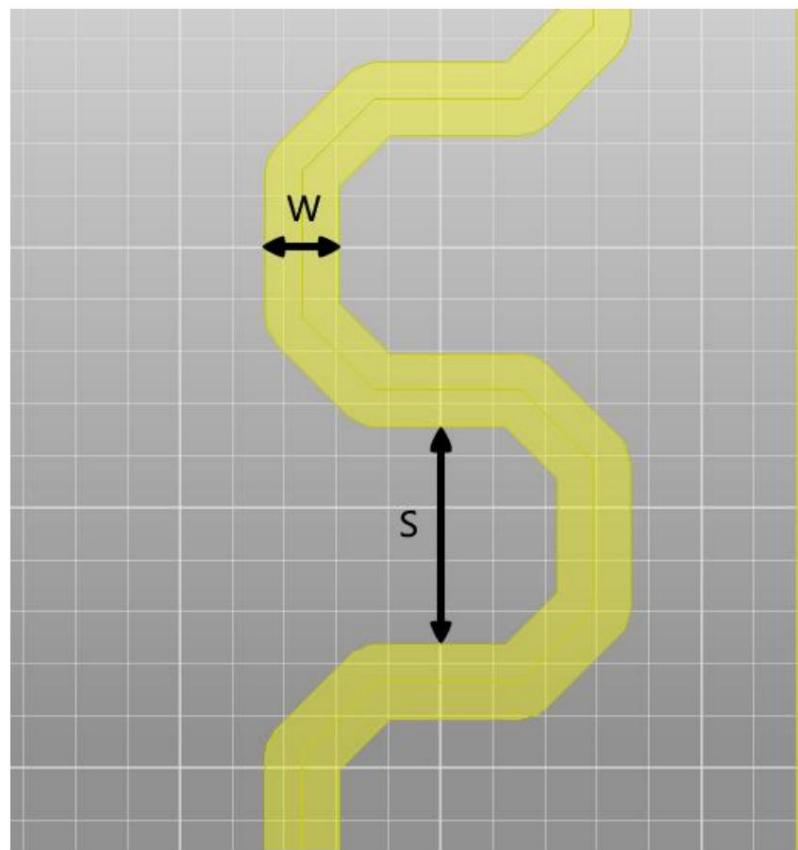


Figure 3-93

(9) When making equal length, the length of the via needs to be considered.

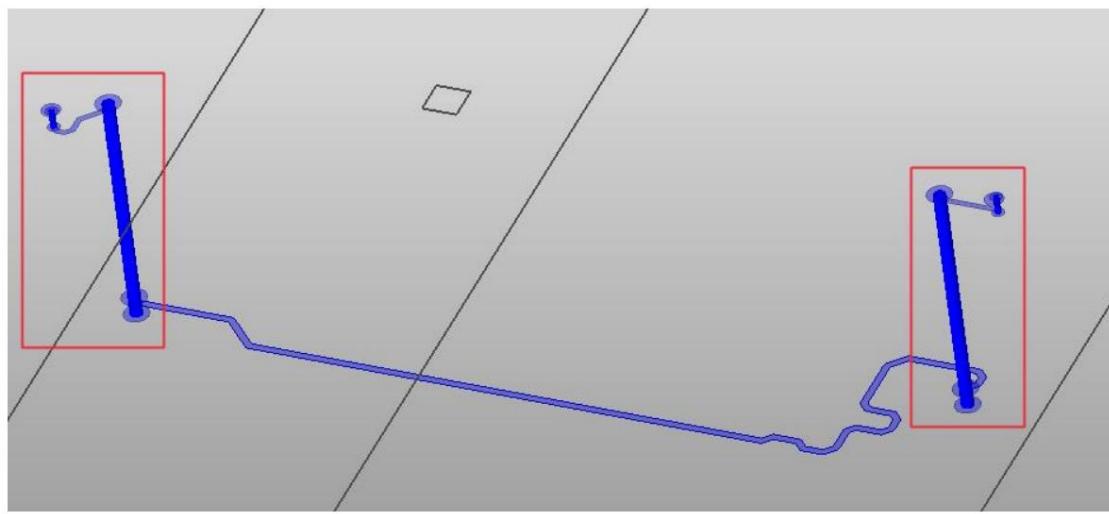


Figure 3-94

(10) In the DDR particle area, one pin corresponds to one GND via, and GND vias should be added as much as possible where there is space.

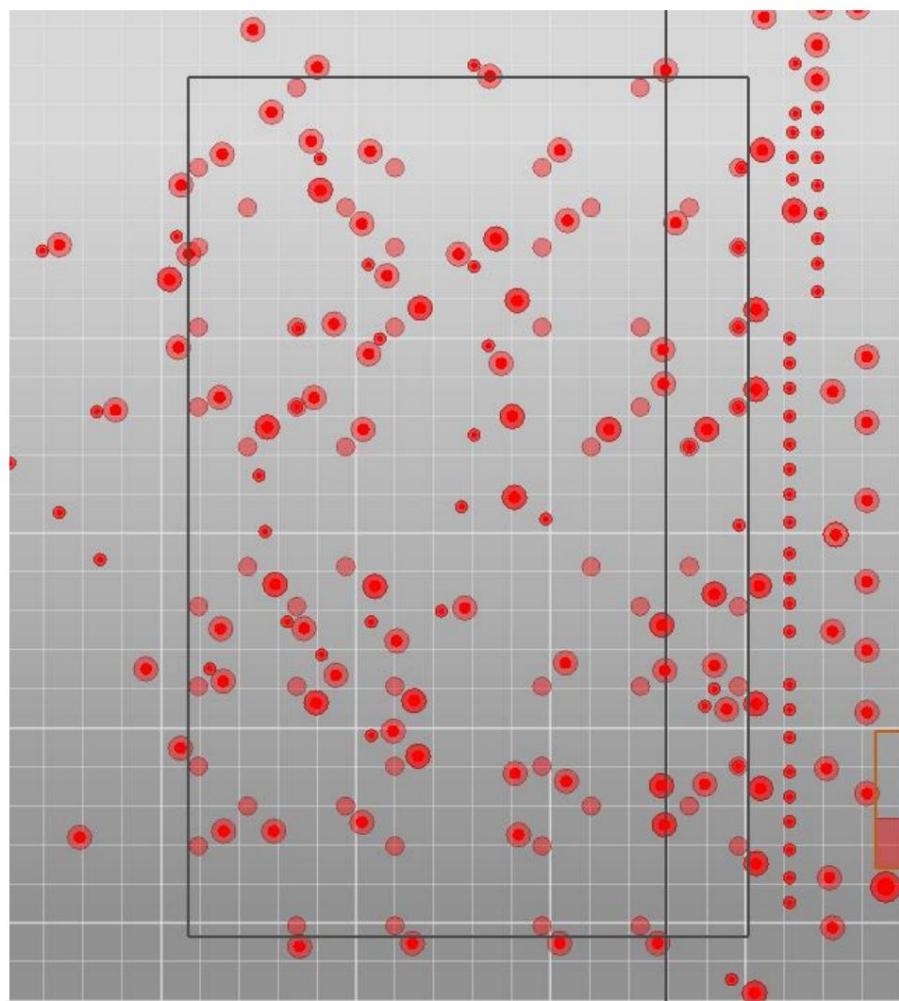


Figure 3-95

(11) Non-functional pads will damage the copper foil and increase the parasitic capacitance of the vias. The non-functional pads of the vias need to be deleted.

(12) The closer the trace is to the via, the worse the reference plane is. The distance between the trace and the via drilling is recommended to be $\geq 8\text{mil}$, and it can be increased where there is space.

spacing.

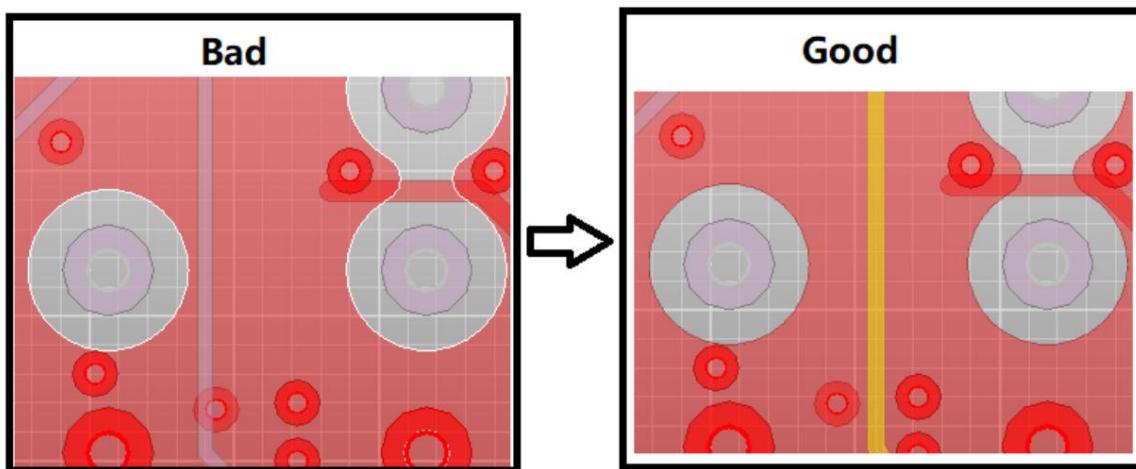


Figure 3-96

(13) Using routing to optimize the cracks in the plane can improve the return path.

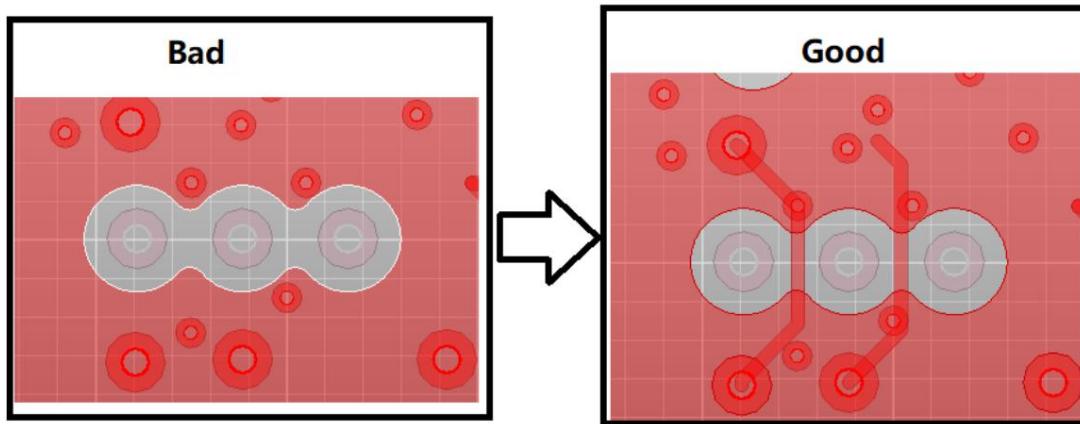


Figure 3-97

(14) DQS, CLK, and WCLK signals need to be grounded. It is recommended to use a GND conductor or copper foil every $\approx 400\text{mil}$.

hole.

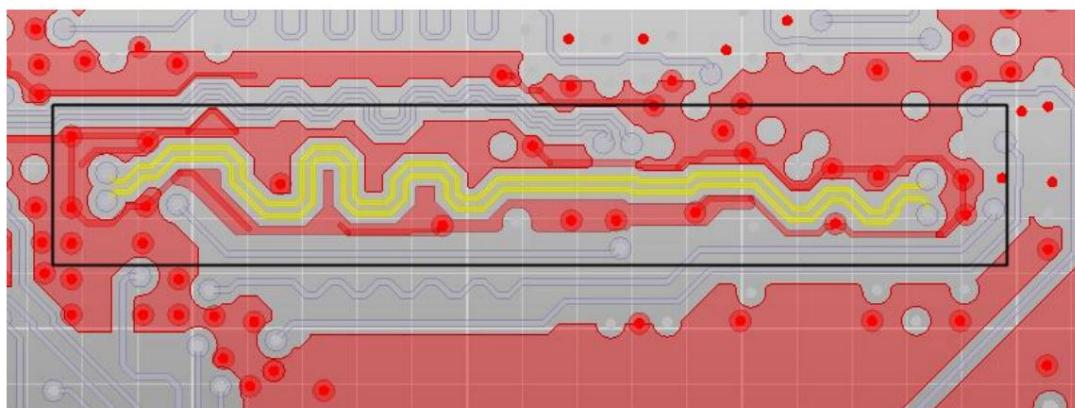


Figure 3-98

(15) For the VDD_DDR_S0 power supply, it is recommended to drill $\approx 0.050\text{3}$ vias when changing the power supply layer in the DCDC area.



Figure 3-99

(16) For the VDDQ_DDR_S0 power supply, it is recommended to drill $\varnothing 0.0503$ vias when changing the power supply layer in the DCDC area.

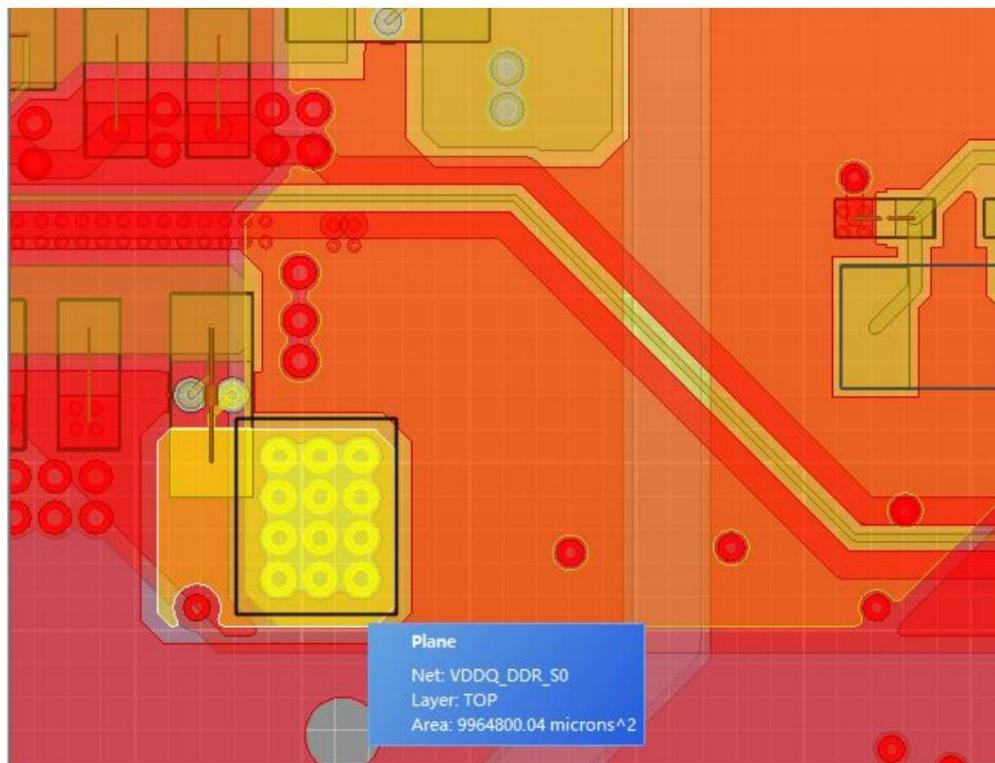


Figure 3-100

(17) For VDD2_DDR_S3 and VDD2H_DDR_S3 power supplies, it is recommended to use $\varnothing 0.0503$

Via. An example is as follows

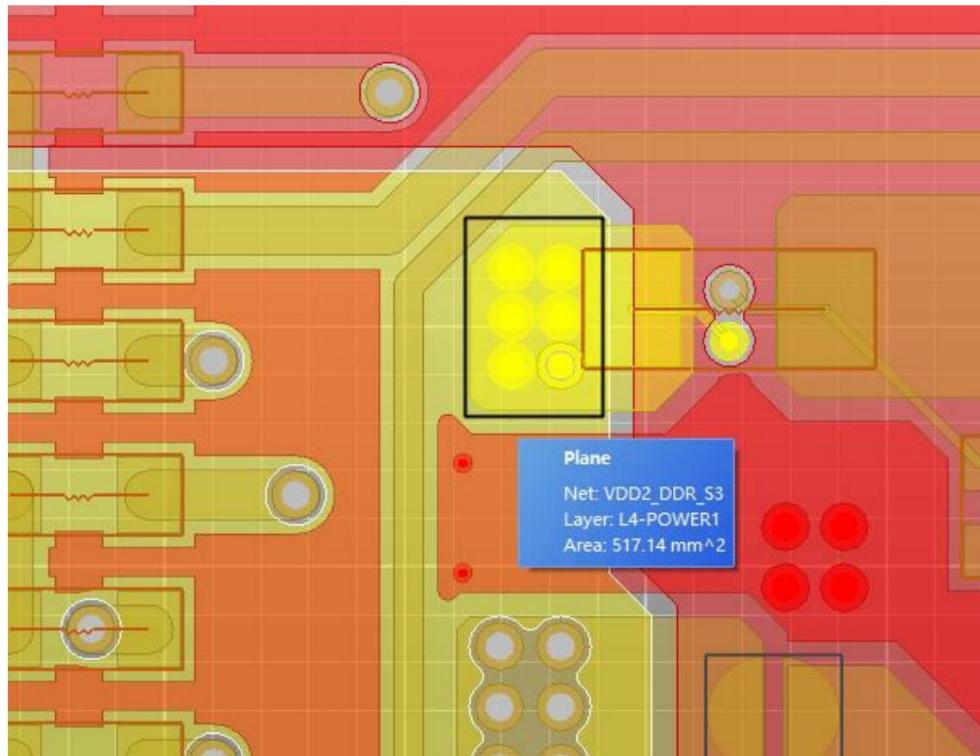


Figure 3-101

(18) For the VDD1_1V8_DDR power supply, it is recommended to drill at least 2 0402 vias when changing the power plane layer.

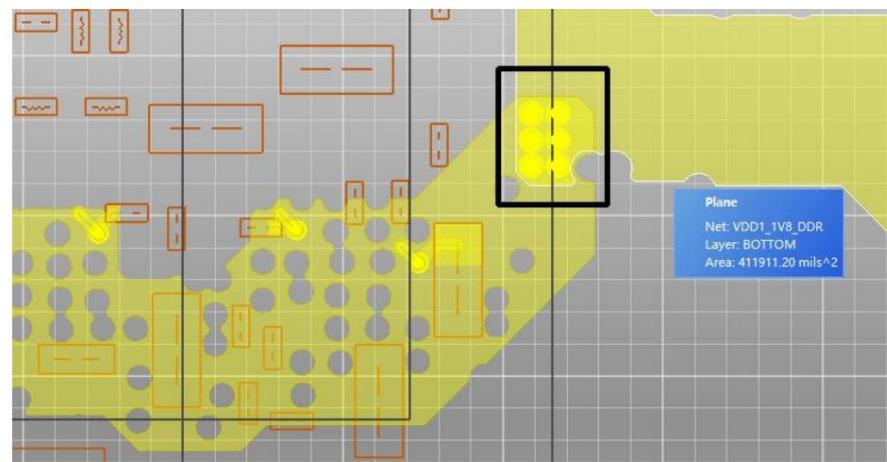


Figure 3-102

(19) It is recommended that at least one via be used for each capacitor pad. For capacitors with 0603 or 0805 packages, two vias are recommended for each pad.

hole.

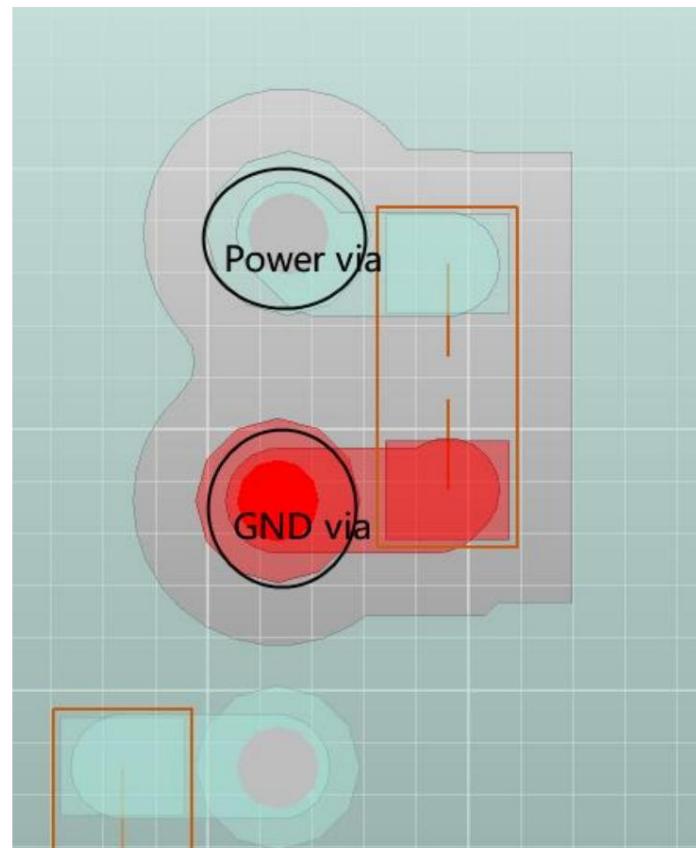


Figure 3-103

(20) Placing vias close to the pins can reduce loop inductance.

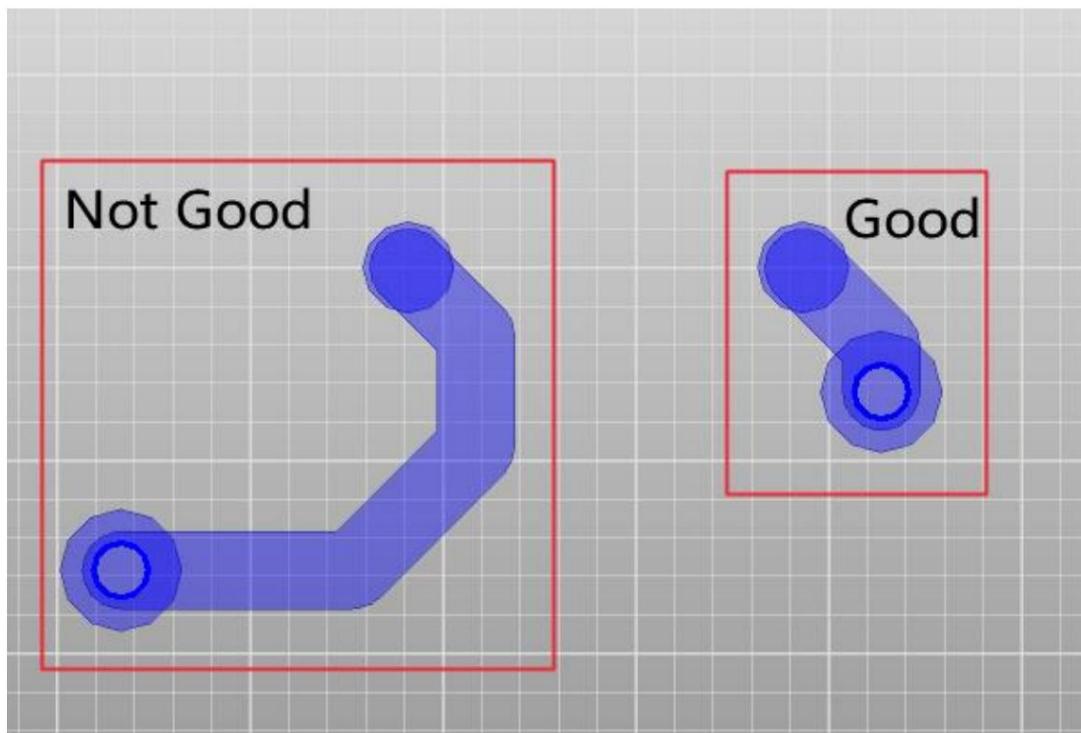


Figure 3-104

(21) The number of power vias corresponding to the CPU's VDDQ_DDR_S0 and VDD_DDR_S0 pins is based on the DDR template.

It is recommended to delete the power vias.

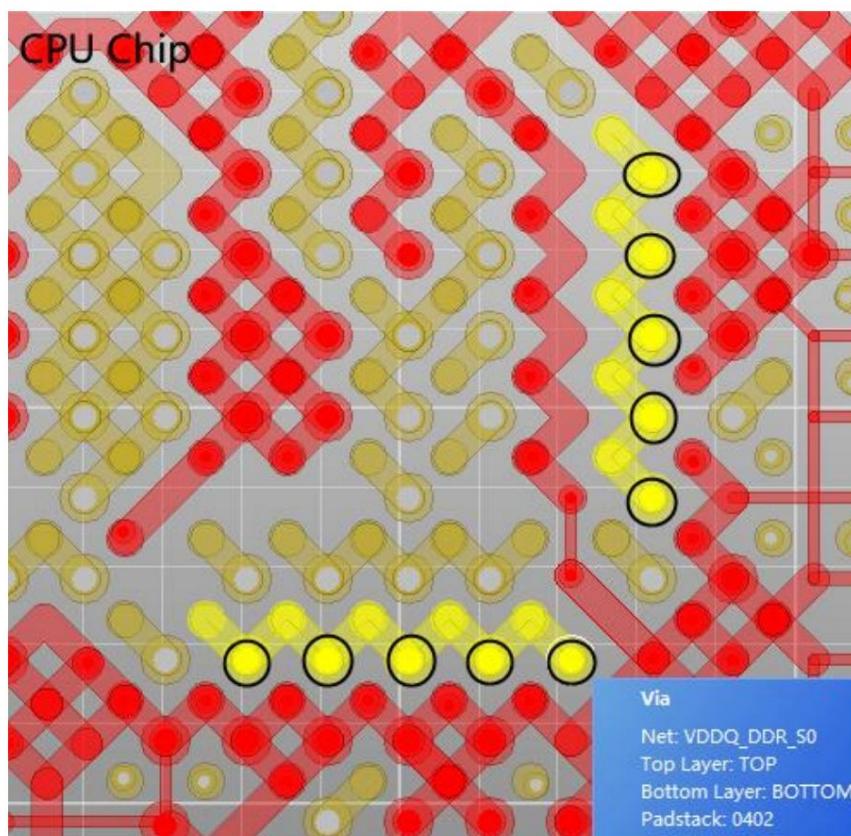


Figure 3-105

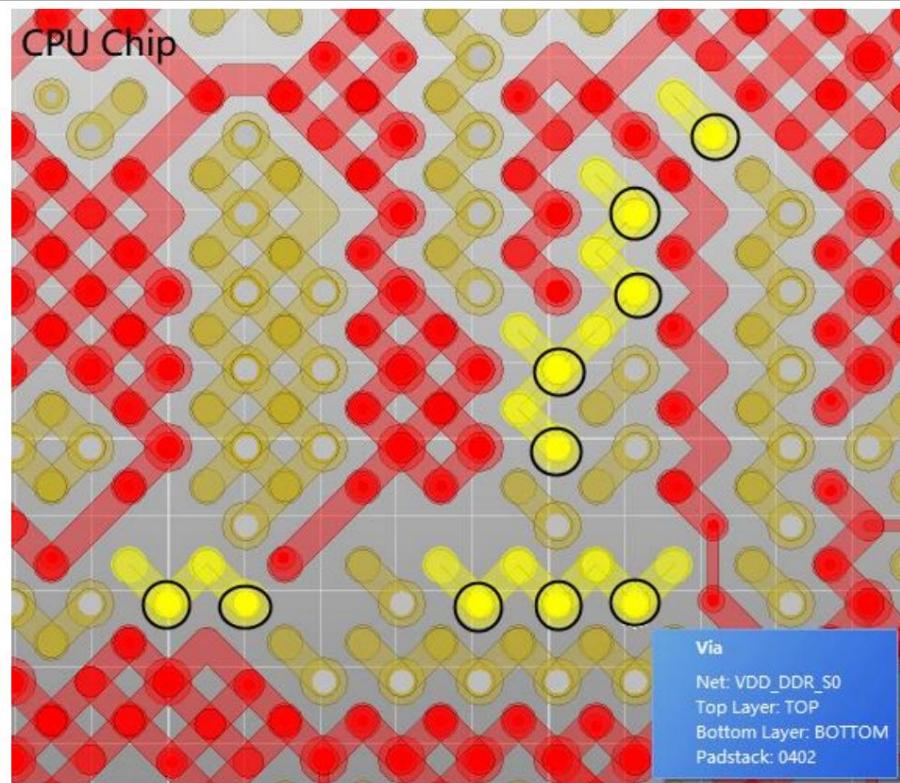


Figure 3-106

(22) DDR chip VDDQ_DDR, VDD2_DDR_S3, VDD1_1V8_DDR power supply, it is recommended to have one pin, corresponding to

An example of a power via is shown below.

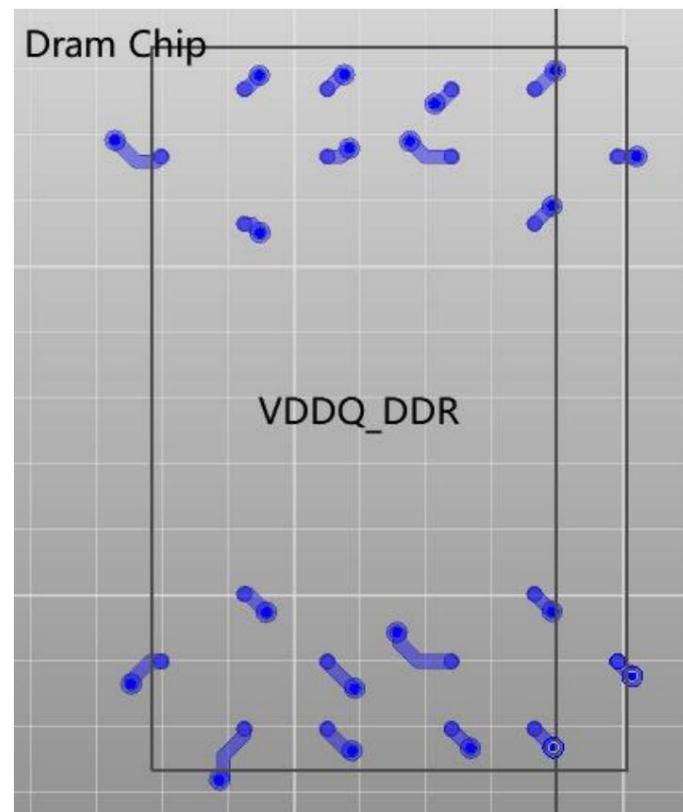


Figure 3-107

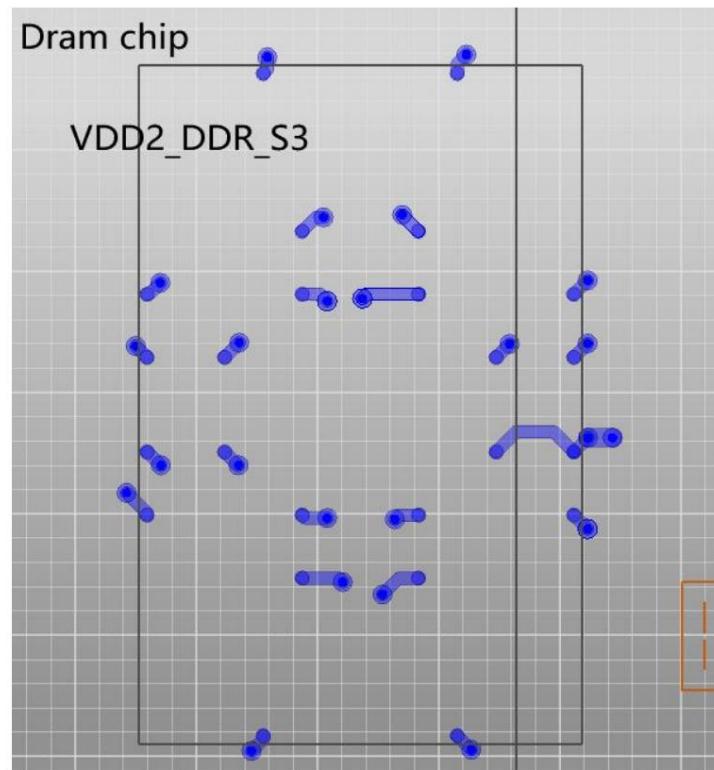


Figure 3-108

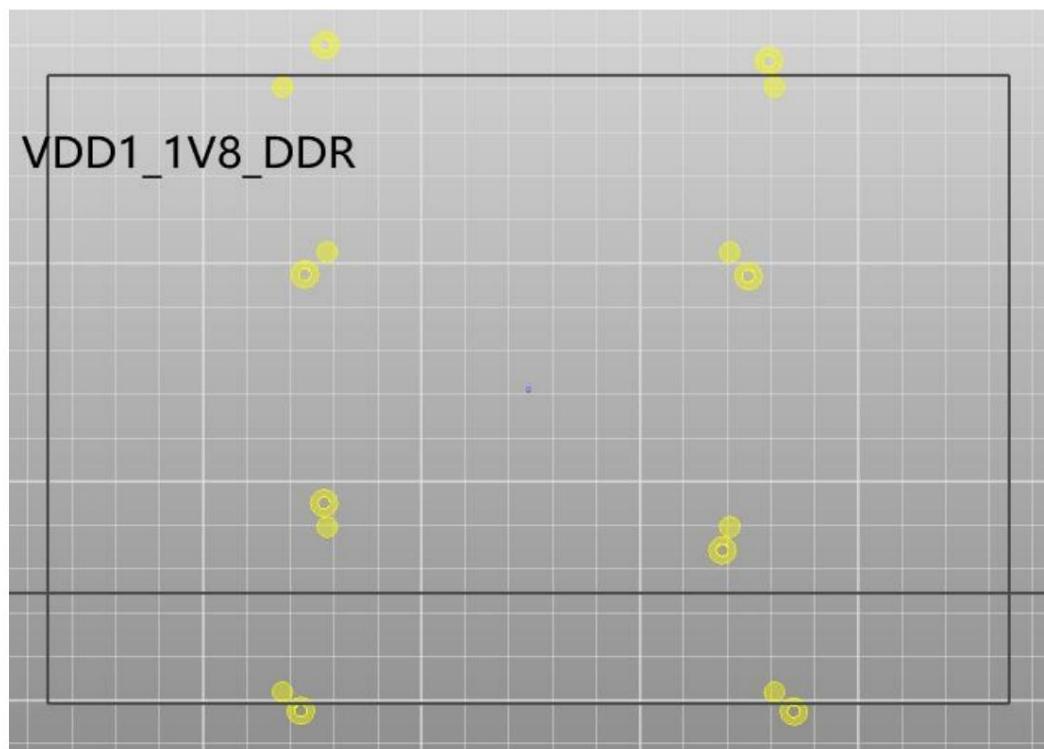


Figure 3-109

(23) DDR chip VDD2H_DDR_S3 power supply, it is recommended that each power pin has ≥ 0.7 power vias.

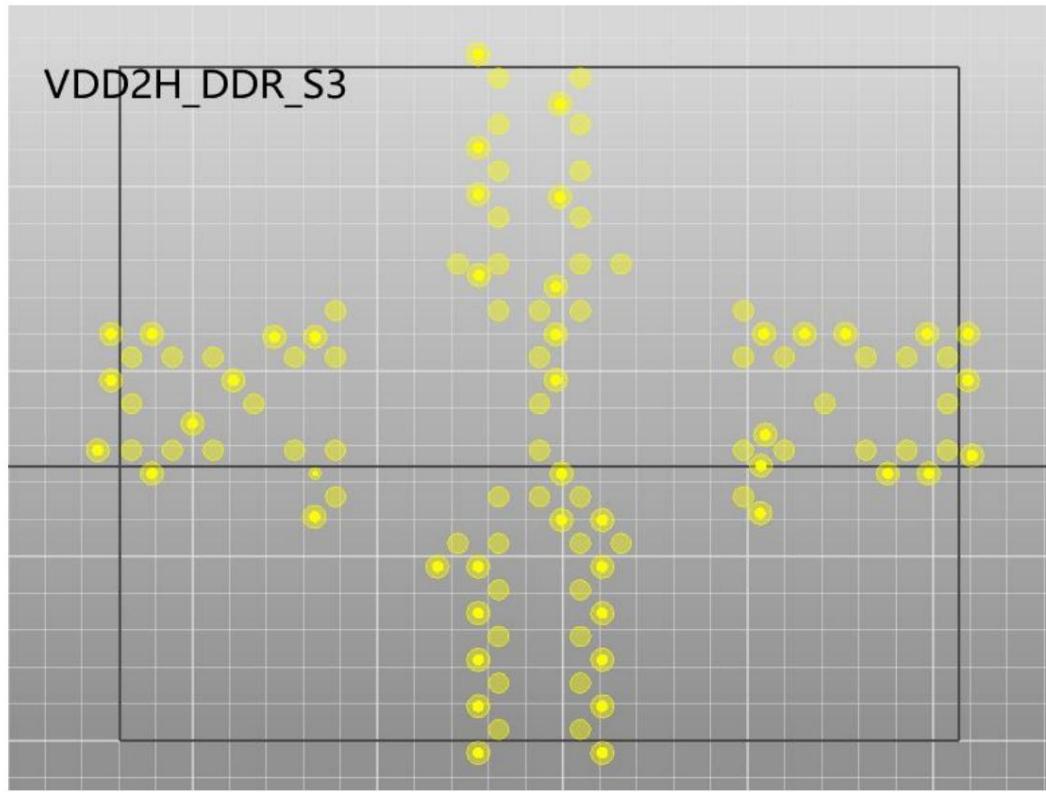


Figure 3-110

(24) When changing the DDR power supply (VDDQ_DDR, VDD2_DDR_S3, VDD_DDR, VDD2H_DDR_S3),

There are enough power vias (≥ 8 0402 vias or ≥ 6 0503 vias), as shown below.



Figure 3-111

(25) Avoid the power layer from being damaged by routing or continuous vias.

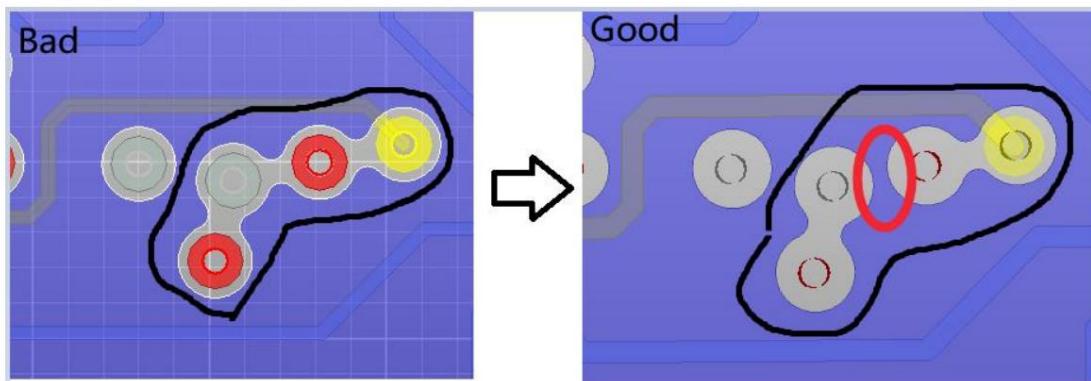


Figure 3-112

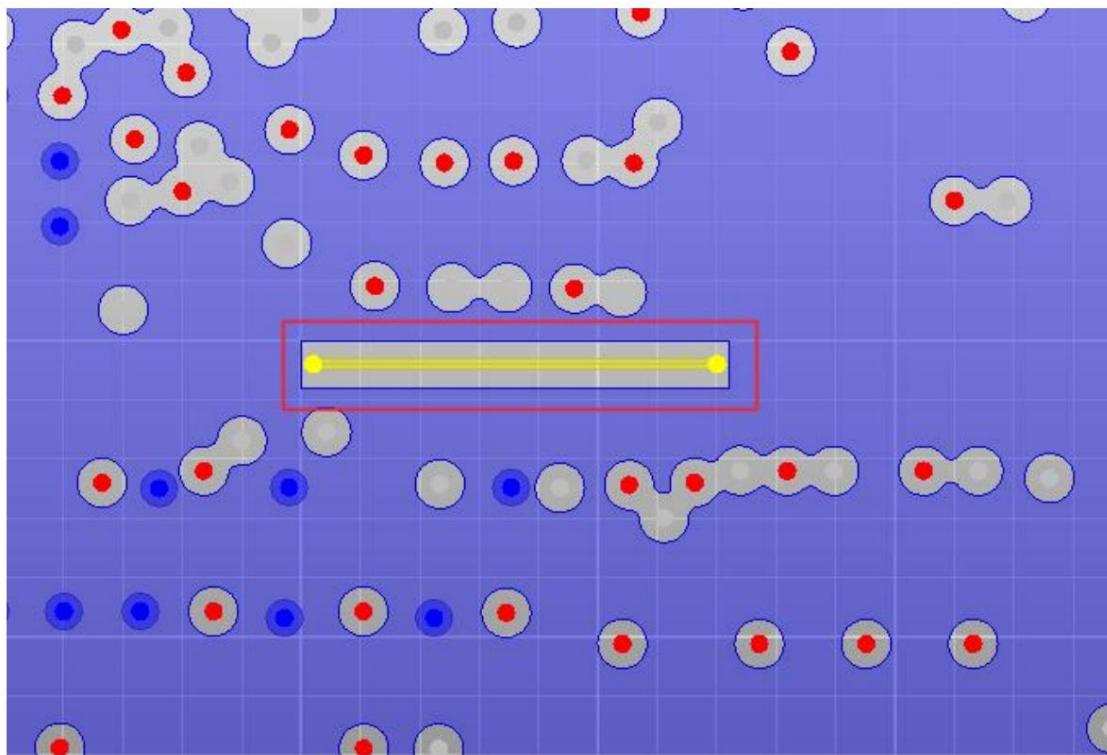


Figure 3-113

(26) The decoupling capacitors of DDR chips should be placed close to the pins to reduce the installation inductance of the capacitors. The number of capacitors recommended is

It is not recommended to remove capacitors in template design. Capacitors of different capacitance values should be placed evenly and dispersed.

(27) The recommended PDN requirements for the CPU area VDD_DDR_S0 power supply are shown in the figure below.

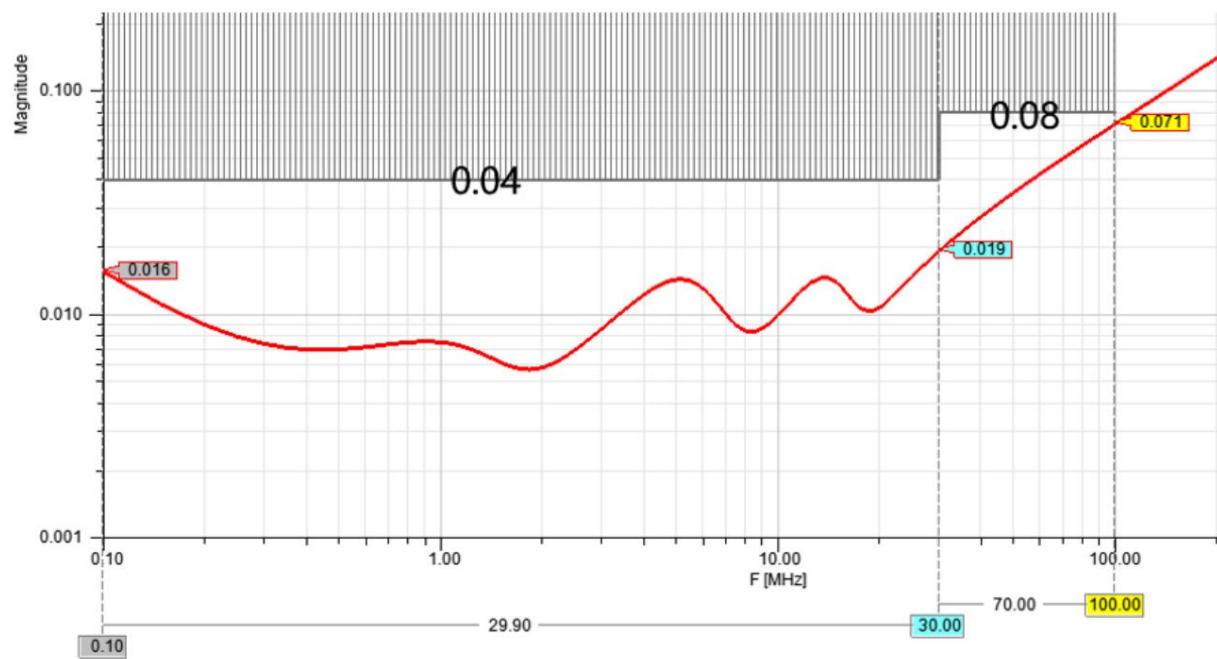


Figure 3-114

(28) The recommended PDN requirements for the CPU region VDDQ_DDR_S0 power supply are shown in the figure below.

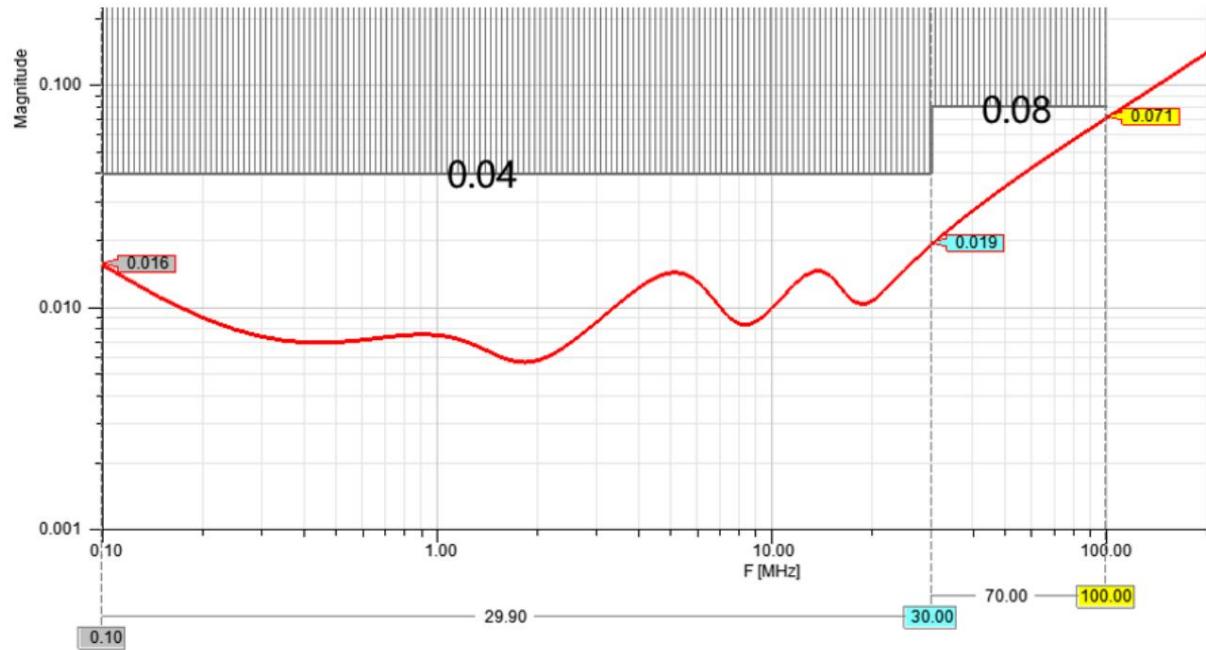


Figure 3-115

(29) The recommended PDN requirements for the VDDQ_DDR power supply in the DDR chip area are as follows.

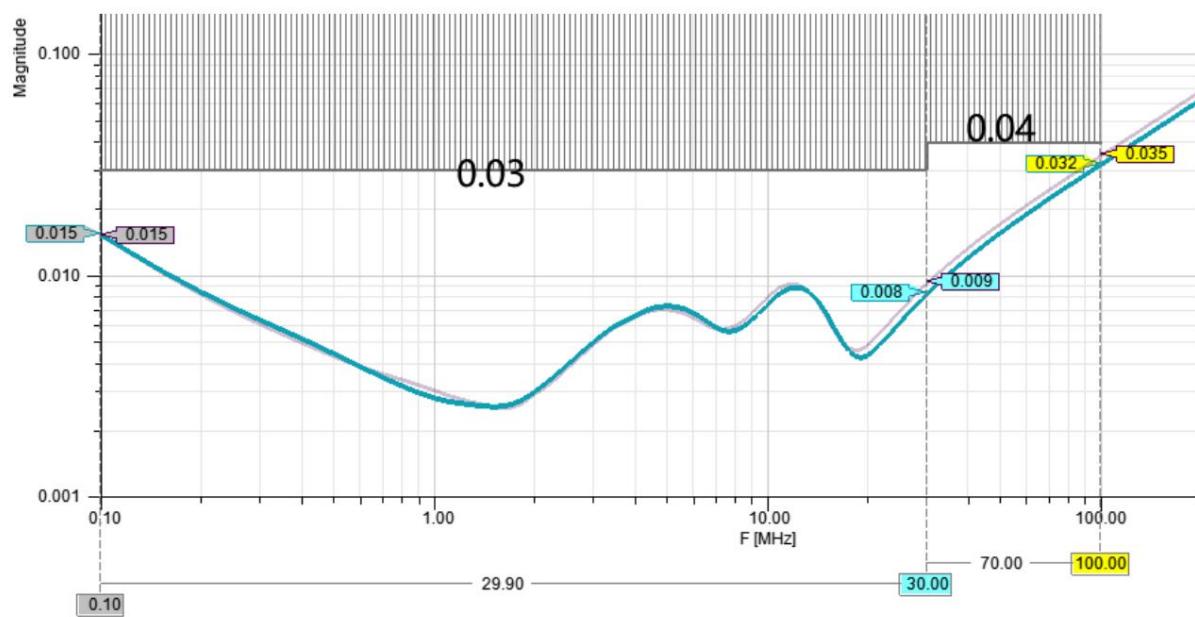


Figure 3-116

(30) The recommended PDN requirements for the VDD2_DDR_S3 power supply in the DDR chip area are as follows.

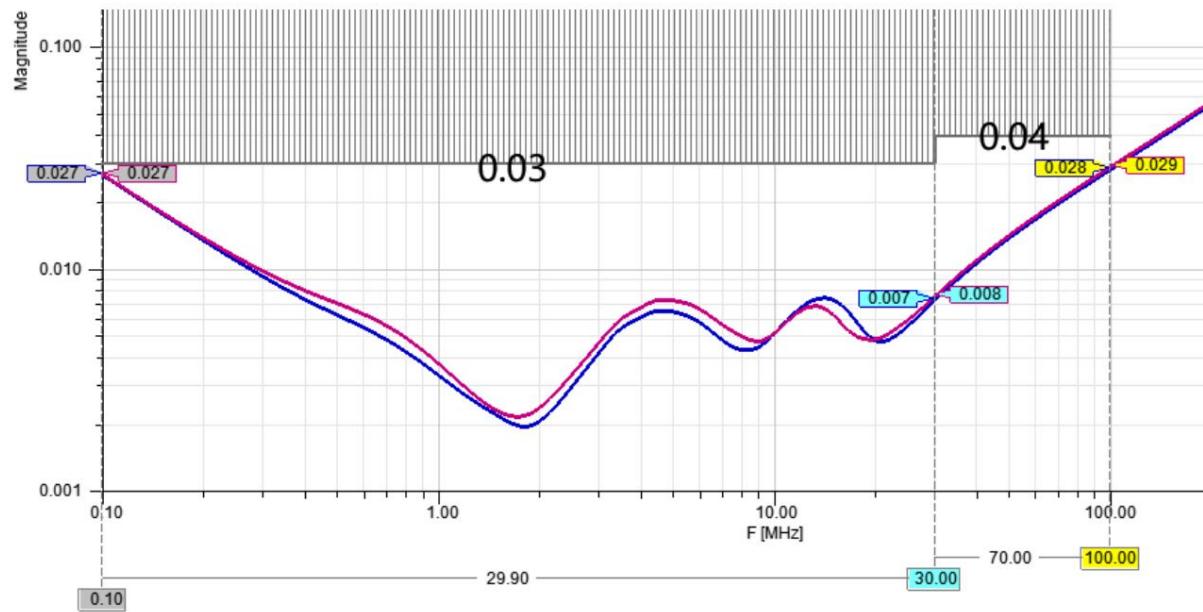


Figure 3-117

(31) The recommended PDN requirements for the VDD2H_DDR_S3 power supply in the DDR chip area are as follows.

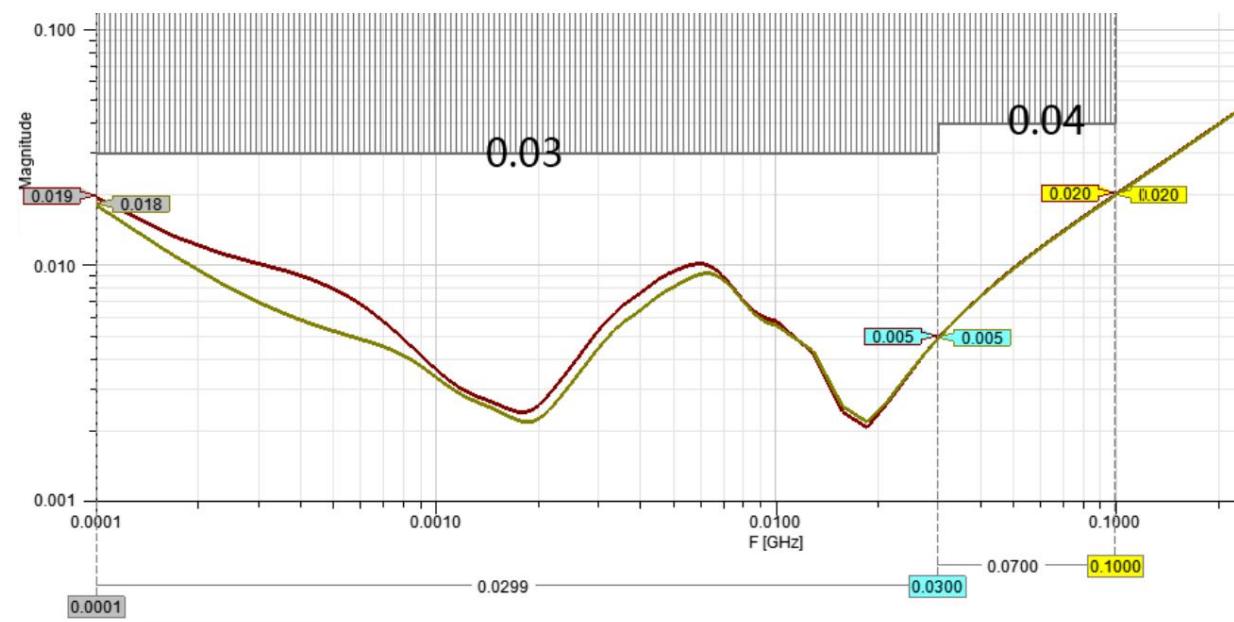


Figure 3-118

3.4.3.1.1 LPDDR5

Due to the 10-layer HDI board, DQ, DM, DQS, WCLK, address, and CLK signals are routed on the inner layer, and the rates of differential and single-ended signals are

The difference is small, so the design rules require equal length, which makes PCB software settings simpler.

Table 3-7 LPDDR5 routing requirements

parameter	Require
DQ, DM single-ended signal impedance	40 Ohm \pm 10%
Single-ended signal impedance of address and control lines	(40~50) Ohm \pm 10%
Differential signal impedance	(80~90) Ohm \pm 10%
The same length between DQ, DQS and WCLK (within the same byte)	\leq 25mil
The same length between DM, DQS, and WCLK (within the same byte)	\leq 25mil
Equal length between address, control lines and CLK	\leq 40mil
DQS_P and DQS_N are of equal length (within the same byte)	\leq 5mil
WCLK_P and WCLK_N are of equal length (within the same byte)	\leq 5mil
Equal length between CLK_P and CLK_N	\leq 5mil
Equal length between DQS, WCLK and CLK	\leq 200mil
The spacing between different bytes (airgap)	\geq 2 times the trace width
The airgap between DQs in the same byte	\geq 2 times the trace width
The airgap between DQ and DQS in the same byte	Recommended \geq 3 times the trace width At least 2 times the trace width
The airgap between DQ and WCLK in the same byte	Recommended \geq 3 times the trace width At least 2 times the trace width
The airgap between address control lines	\geq 2 times the trace width
Spacing between CLK and other signal lines	Recommended \geq 3 times the trace width At least 2 times the trace width

3.4.3.1.2 LPDDR4X

Due to the 10-layer HDI board, DQ, DM, DQS, WCLK, address, and CLK signals are routed on the inner layer, and the rates of differential and single-ended signals are

The difference is small, so the design rules require equal length, which makes PCB software settings simpler.

Table 3-8 LPDDR4X routing requirements

parameter	Require
DQ, DM single-ended signal impedance	40 Ohm ± 10%
Address control line (except CKE signal) single-ended signal impedance	40 Ohm ± 10%
CKE Single-ended signal impedance	50 Ohm ± 10%
Differential signal impedance	(80~90) Ohm ± 10%
The same length between DQ and DQS (within the same byte)	≥ 25mil
Equal length between DM and DQS (within the same byte) Equal length between address, control lines and CLK	≥ 25mil
DQS_P and DQS_N are of equal length (within the same byte)	≥ 5mil
Equal length between CLK_P and CLK_N	≥ 5mil
The airgap between DQS and CLK is the same length, but the airgap between bytes is different. The airgap between DQ and DQ in the same byte is different.	≥ 2 times the trace width
The airgap between DQ and DQS in the same byte	Recommended ≥ 3 times the trace width At least 2 times the trace width
The airgap between address control lines	≥ 2 times the trace width
Spacing between CLK and other signal lines	Recommended ≥ 3 times the trace width At least 2 times the trace width

3.4.3.1.3 LPDDR4

Due to the 10-layer HDI board, DQ, DM, DQS, WCLK, address, and CLK signals are routed on the inner layer, and the rates of differential and single-ended signals are

The difference is small, so the design rules require equal length, which makes PCB software settings simpler.

Table 3-9 LPDDR4 routing requirements

parameter	Require
DQ, DM single-ended signal impedance	40 Ohm ± 10%
Address control line (except CKE signal) single-ended signal impedance	40 Ohm ± 10%
CKE single-ended signal impedance	50 Ohm ± 10%
Differential signal impedance	(80~90) Ohm ± 10%
The same length between DQ and DQS (within the same byte)	≥ 25mil
Equal length between DM and DQS (within the same byte)	≥ 25mil
Equal length between address, control lines and CLK	≥ 40mil
DQS_P and DQS_N are of equal length (within the same byte)	≥ 5mil
Equal length between CLK_P and CLK_N	≥ 5mil
Equal length between DQS and CLK	≥ 250mil
The airgap between different bytes The airgap between DQs in the same byte	≥ 2 times the trace width
The airgap between DQ and DQS in the same byte	Recommended ≥ 3 times the trace width At least 2 times the trace width
The airgap between address control lines	≥ 2 times the trace width
Spacing between CLK and other signal lines	Recommended ≥ 3 times the trace width At least 2 times the trace width

3.4.3.2 DRAM Circuit PCB Design (8- Layer Through-Hole PCB)

Since the RK3588 DDR interface rate is $\geq 4266\text{bps}$, PCB design is difficult, so we strongly recommend using the DDR template and The corresponding DDR firmware. DDR template is released after rigorous simulation and test verification. If you design the PCB yourself, please refer to the following PCB design suggestions: It is strongly recommended to perform simulation optimization before releasing the board. Compared with the 10-layer first-order HDI design, the signal margin of 8-layer through-holes will be reduced. It is recommended to choose 10-layer DDR template first.

(1) CPU pins, corresponding GND vias, it is recommended to strictly refer to the template design, and do not delete GND vias. 8-layer PCB with through holes Template, CPU pin GND via design is as shown below.

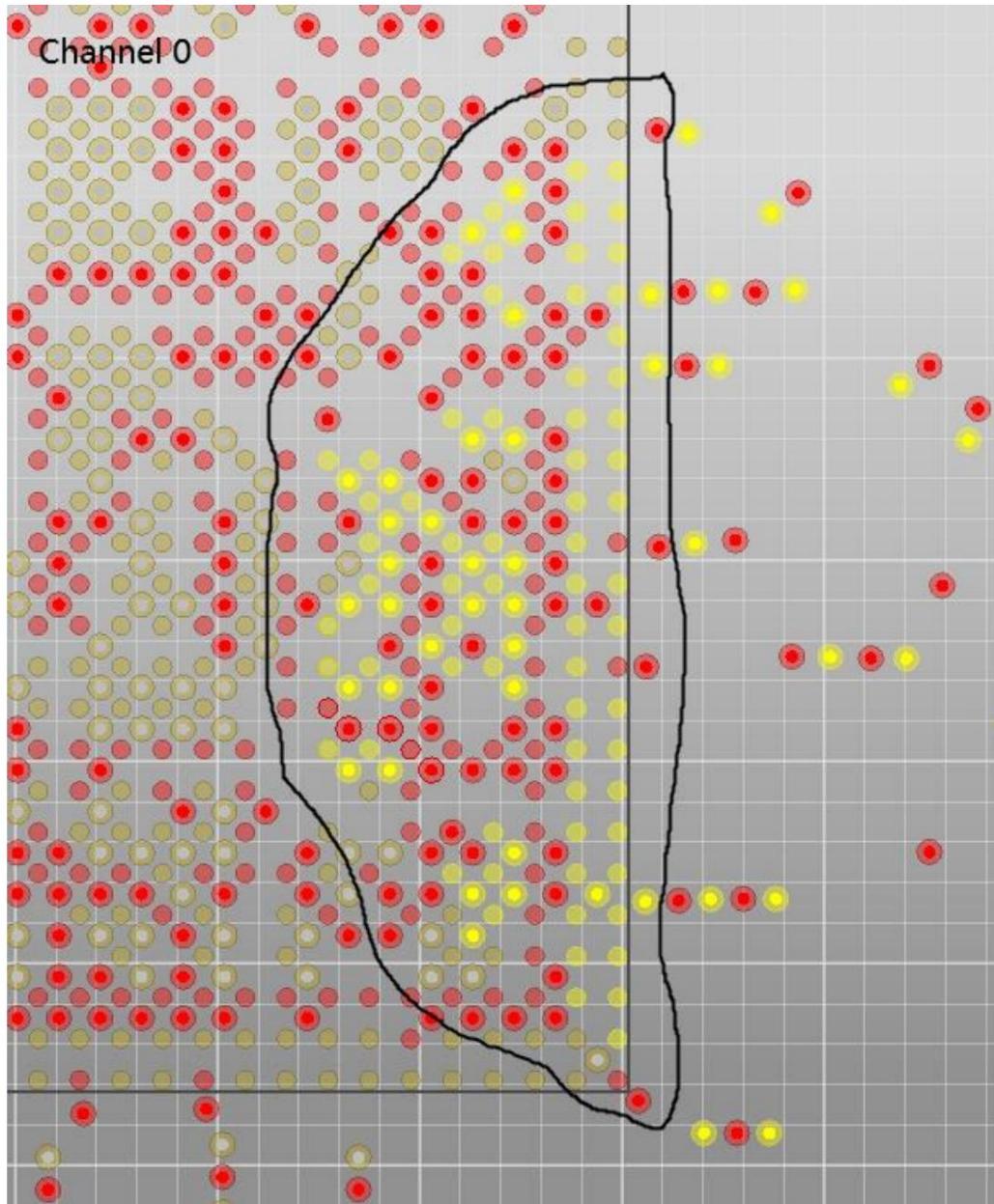


Figure 3-119

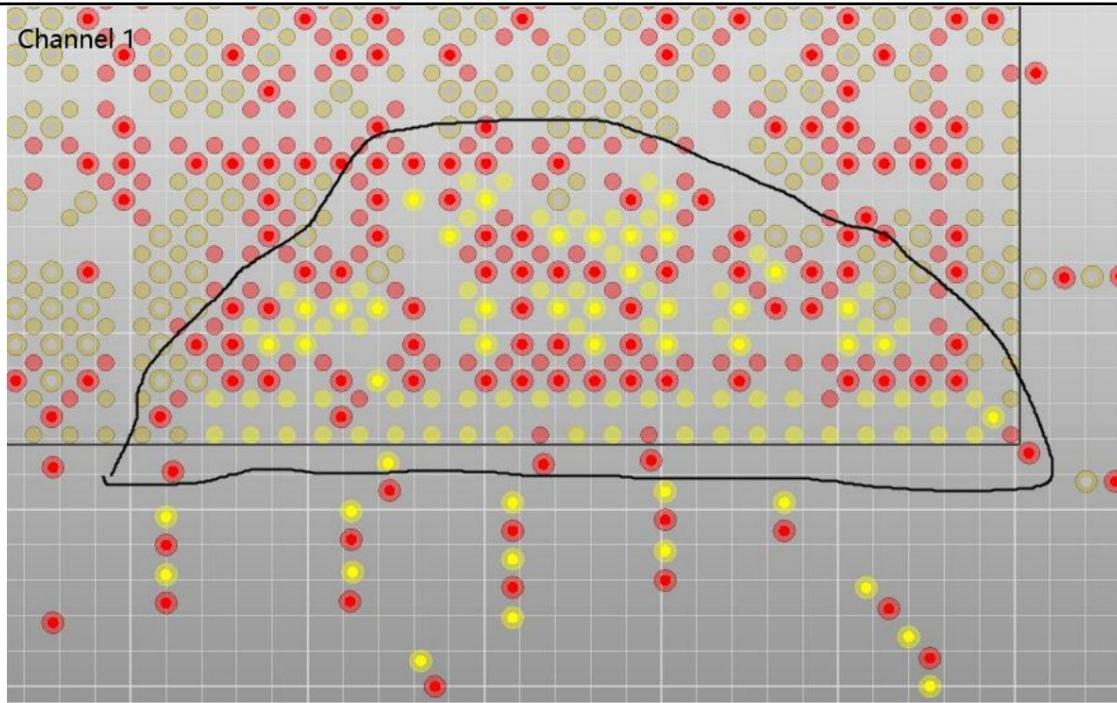


Figure 3-120

(2) Before and after the signal layer is changed, when the reference layer is the GND plane, the signal via hole must be within 25mil (the center distance between via holes).

To add GND return vias to improve the signal return path, the GND vias need to connect the GND reference planes before and after the signal layer changes.

For every signal via, there must be at least one GND return via. Increasing the number of GND return vias as much as possible can further improve signal quality.

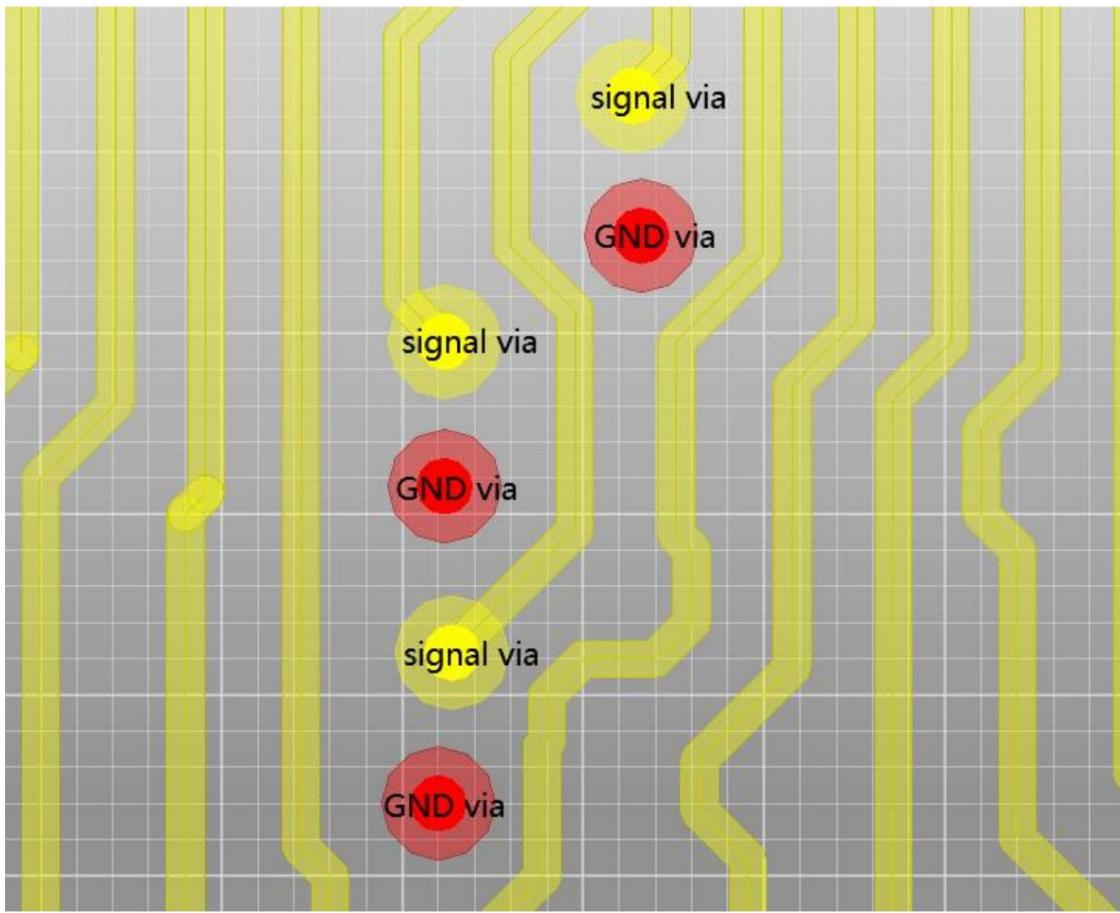


Figure 3-121

(3) The position of GND vias and signal vias will affect the signal quality. It is recommended that GND vias and signal vias be placed crosswise as shown in the figure below.

Although the figure also shows 4 GND return vias, the situation where 4 signal vias are placed together should be avoided. In this case, the crosstalk of the vias is the largest.

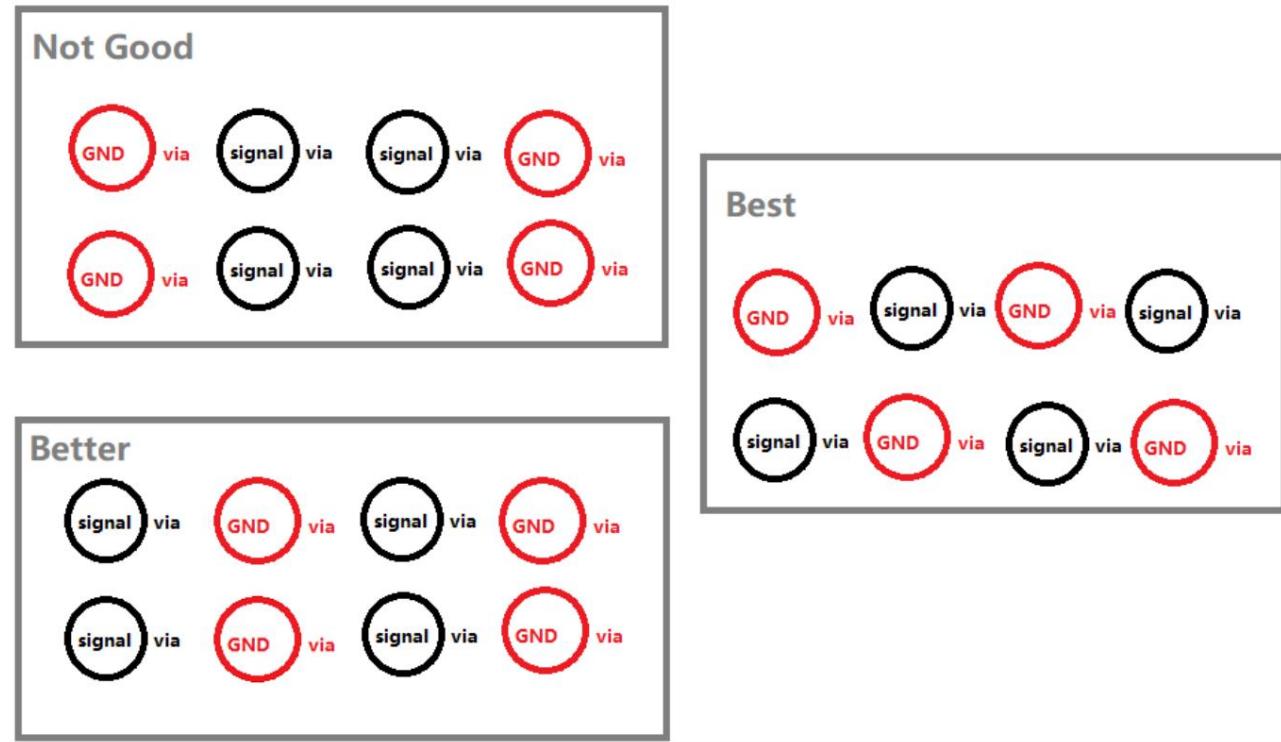


Figure 3-122

(4) For 8-layer boards, it is recommended that DDR signals be routed on the first, sixth, and eighth layers. DQ, DQS, address and control signals, and CLK signals are all routed on the first, sixth, and eighth layers.

Refer to the complete GND plane. If the GND plane is incomplete, it will have a great impact on the signal quality.

(5) As shown in the figure below, when the vias cause the signal reference layer to break, you can consider using GND traces to optimize the lower reference layer to improve signal quality.

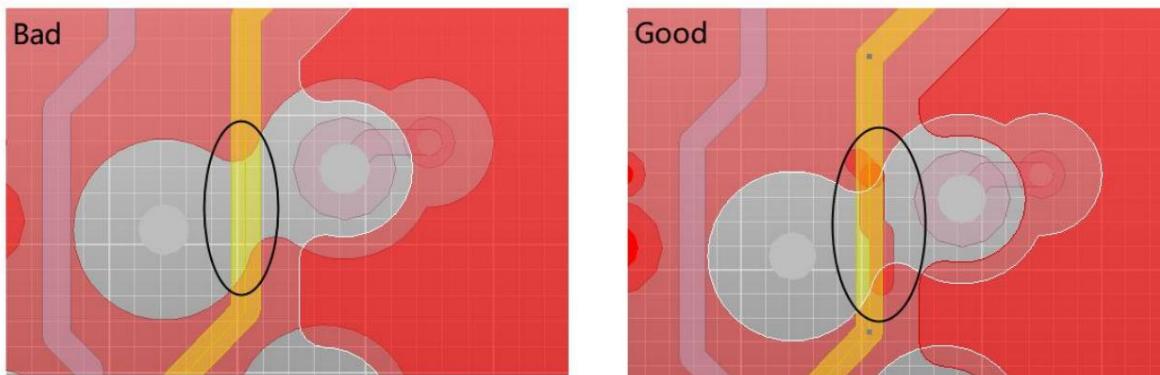


Figure 3-123

(6) The closer the trace is to the edge of the reference layer, the greater the signal impedance will be. The distance between the trace and the edge of the reference layer should be at least $\geq 12\text{mil}$.

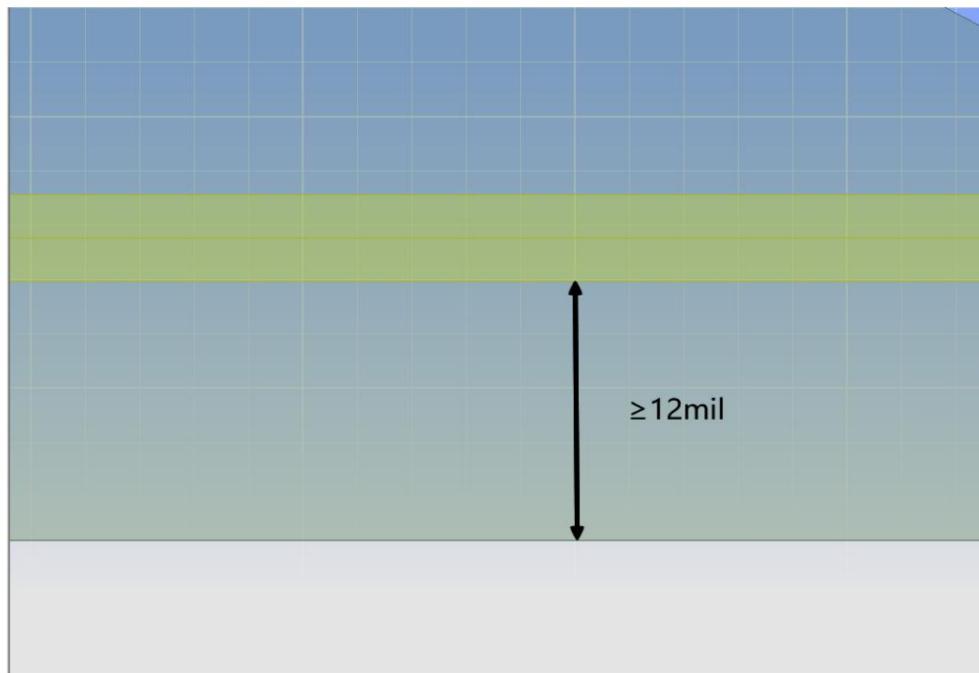


Figure 3-124

(7) The crosstalk of the winding itself will affect the signal delay. It is recommended that $S \geq 3W$ when the wiring is of equal length.

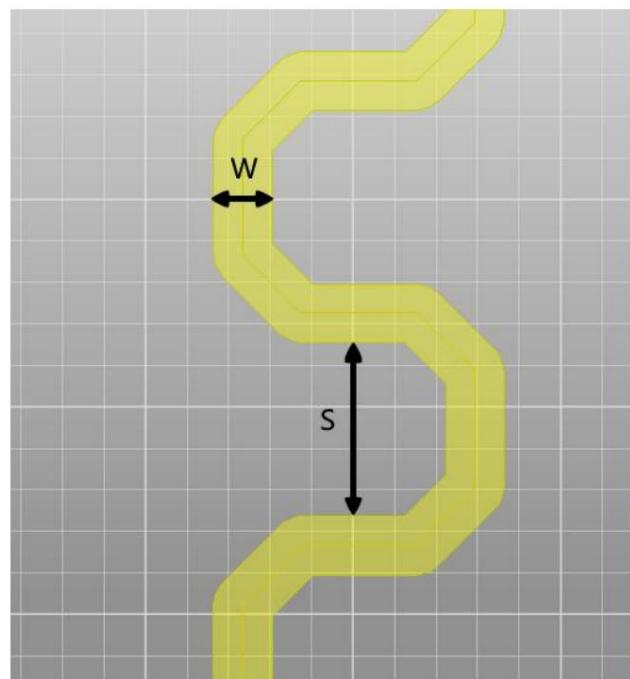


Figure 3-125

(8) When making equal length, the delay of the via needs to be considered.

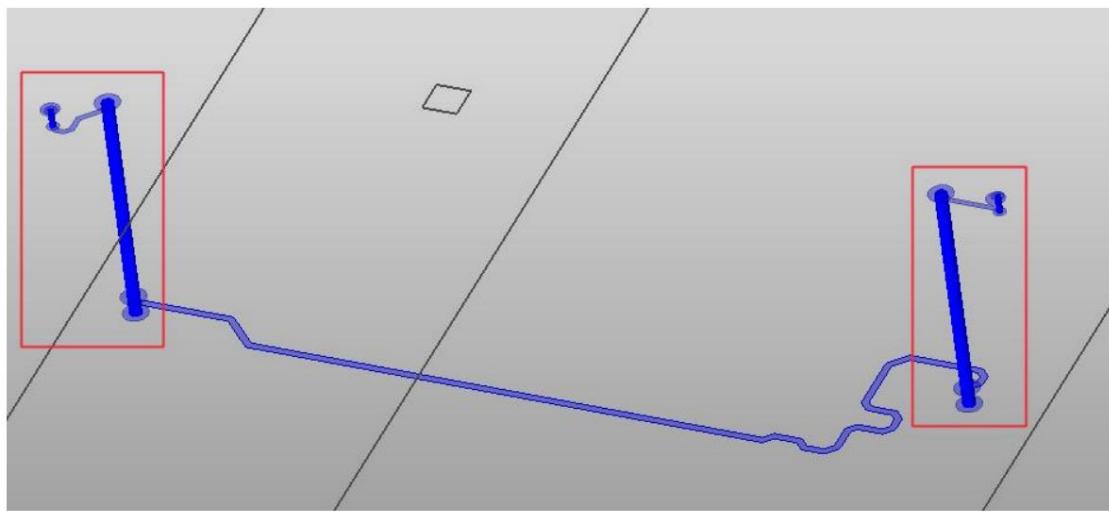


Figure 3-126

(9) In the DDR particle area, one pin corresponds to one GND via, and GND vias should be added as much as possible where there is space.

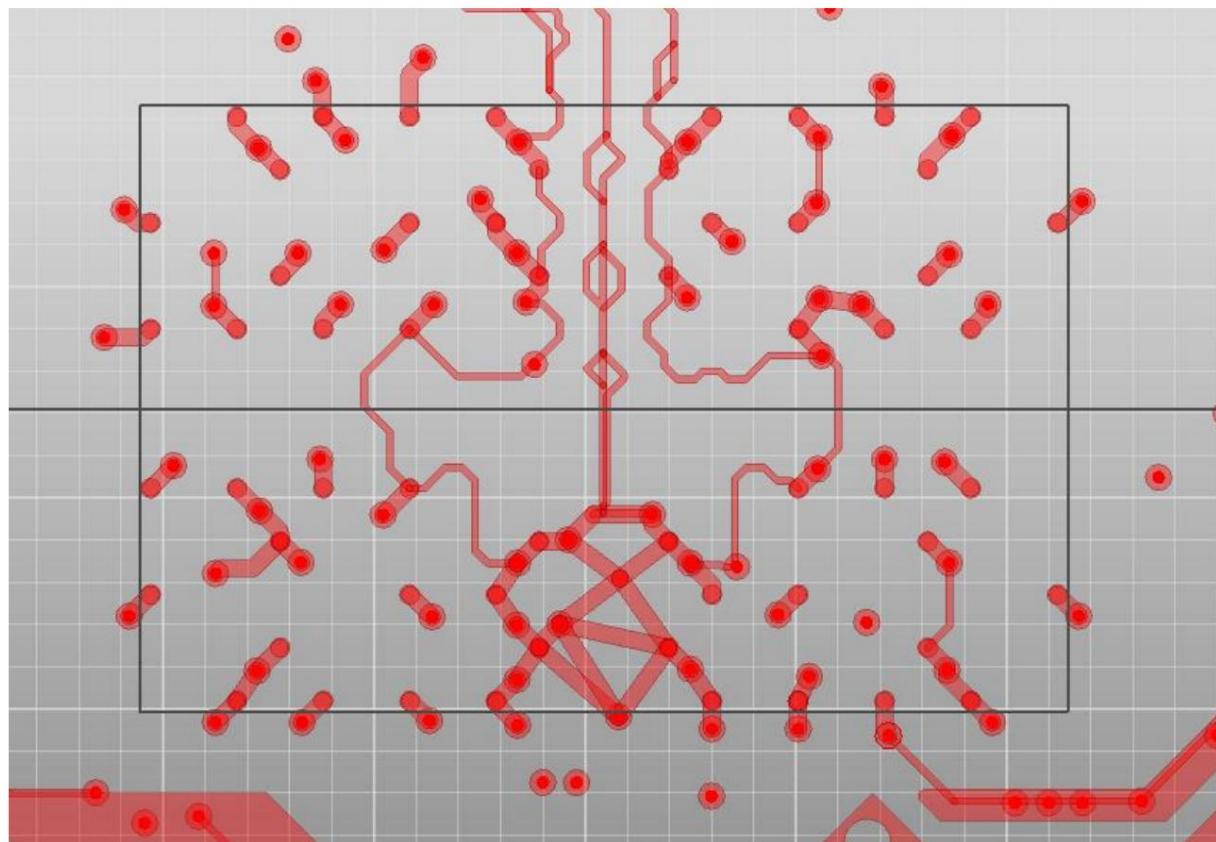


Figure 3-127

(10) Non-functional pads will damage the copper foil and increase the parasitic capacitance of the vias. The non-functional pads of the vias need to be deleted.

(11) The closer the trace is to the via, the worse the reference plane is. The distance between the trace and the via drilling is recommended to be $\geq 8\text{mil}$. If there is space, increase the distance.

distance.

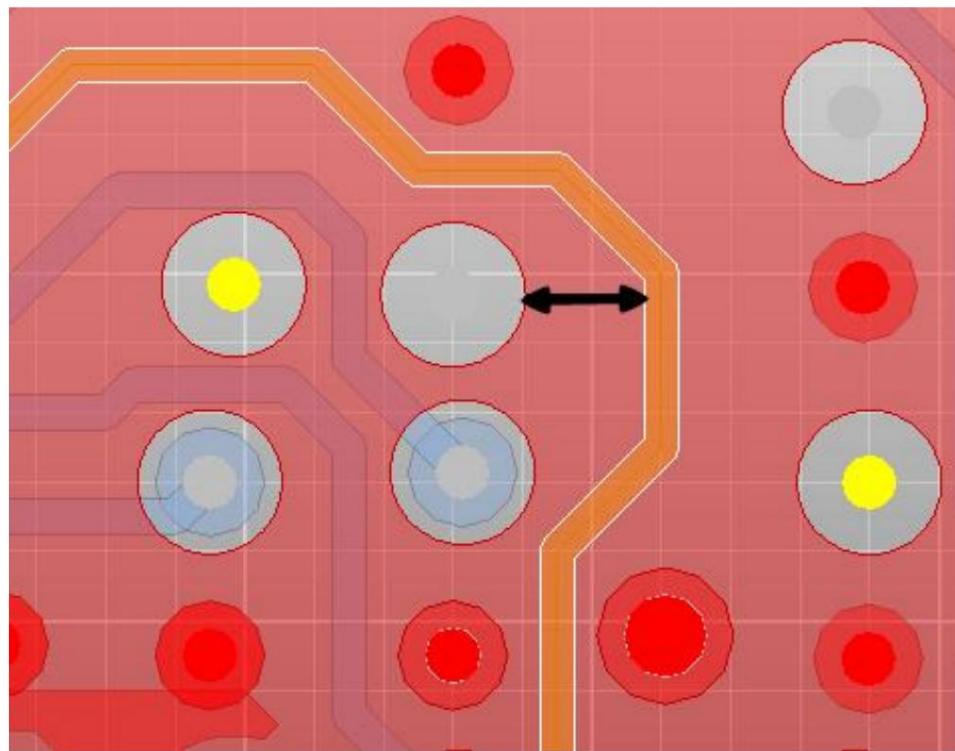


Figure 3-128

(12) Adjusting the via position and optimizing the cracks in the plane can improve the return path.

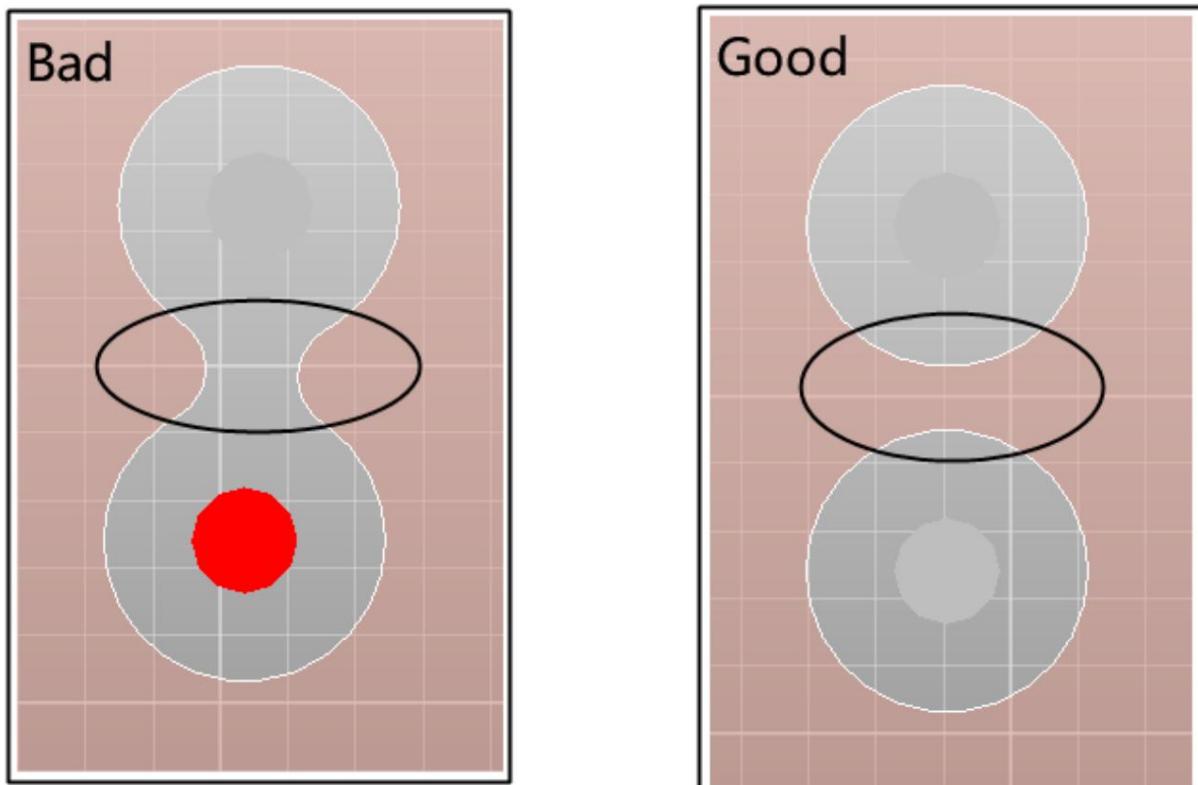


Figure 3-129

(13) DQS, CLK, and WCLK signals need to be grounded. It is recommended to drill a GND via every $\bar{y}400\text{mil}$ for the ground wire or copper foil.

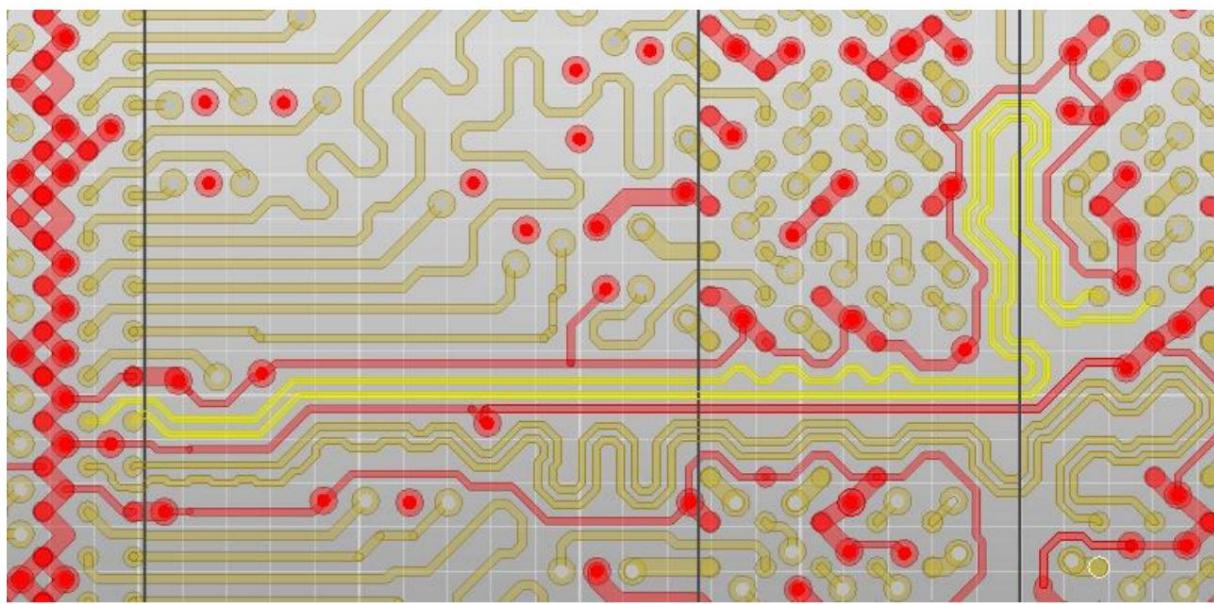


Figure 3-130

(14) For the VDD_DDR power supply, it is recommended to drill $\bar{y}6\ 0503$ vias when changing the power supply layer in the DCDC area.

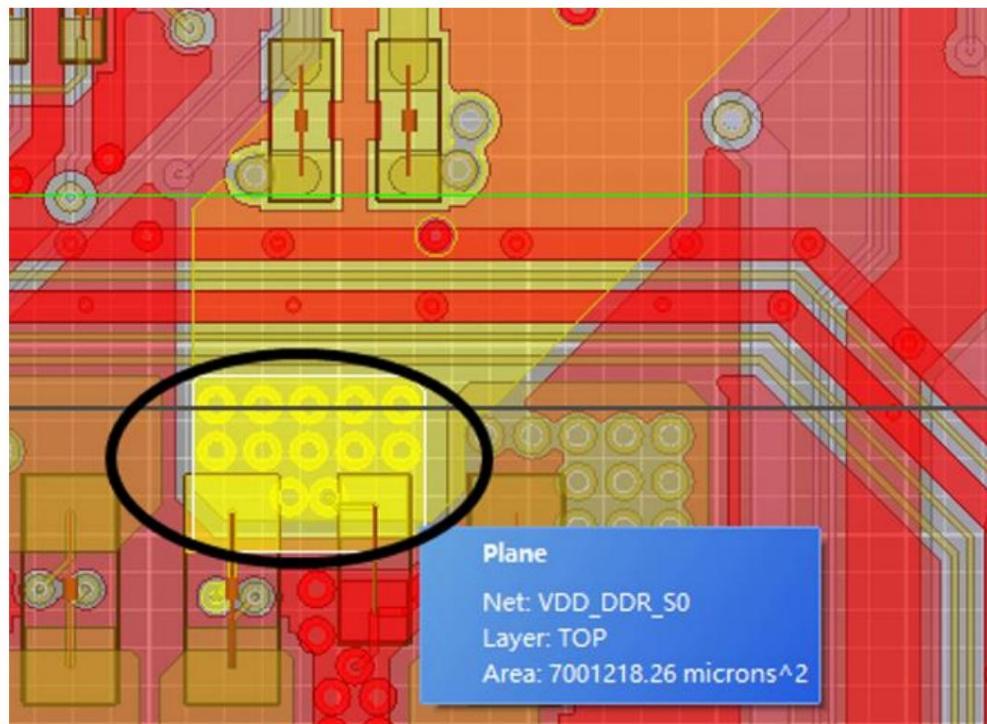


Figure 3-131

(15) For the VDDQ_DDR power supply, it is recommended to drill Ø6 0503 vias when changing the power supply layer in the DCDC area.

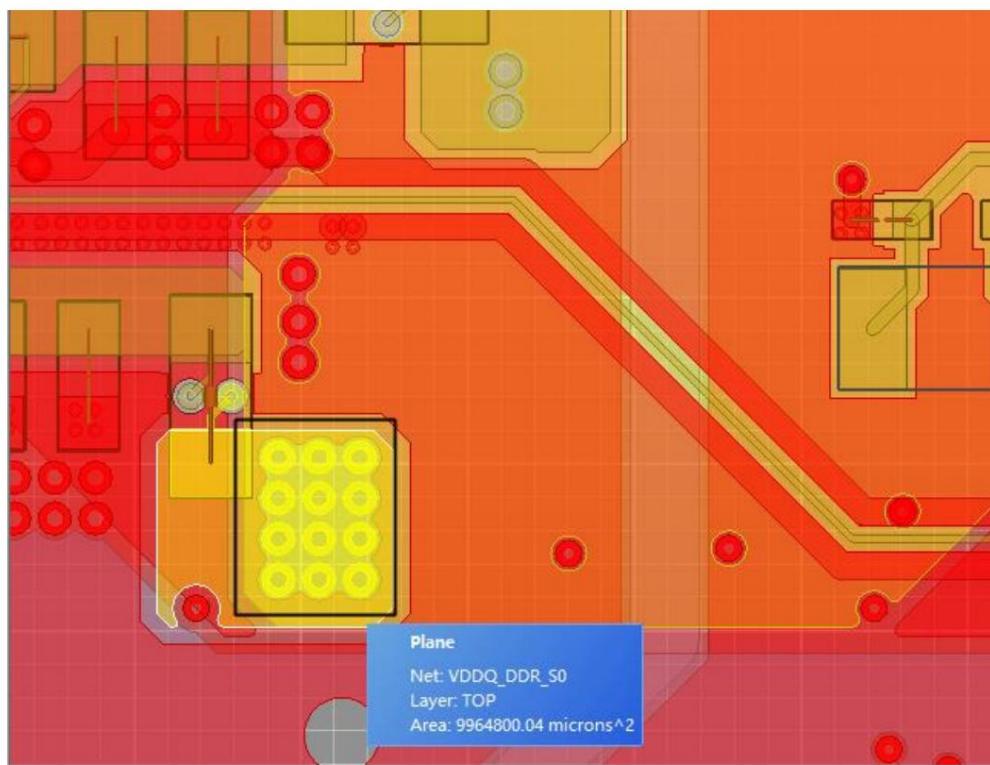


Figure 3-132

(16) For the VDD2_DDR power supply, it is recommended to drill Ø6 0503 vias when changing the power supply layer in the DCDC area.

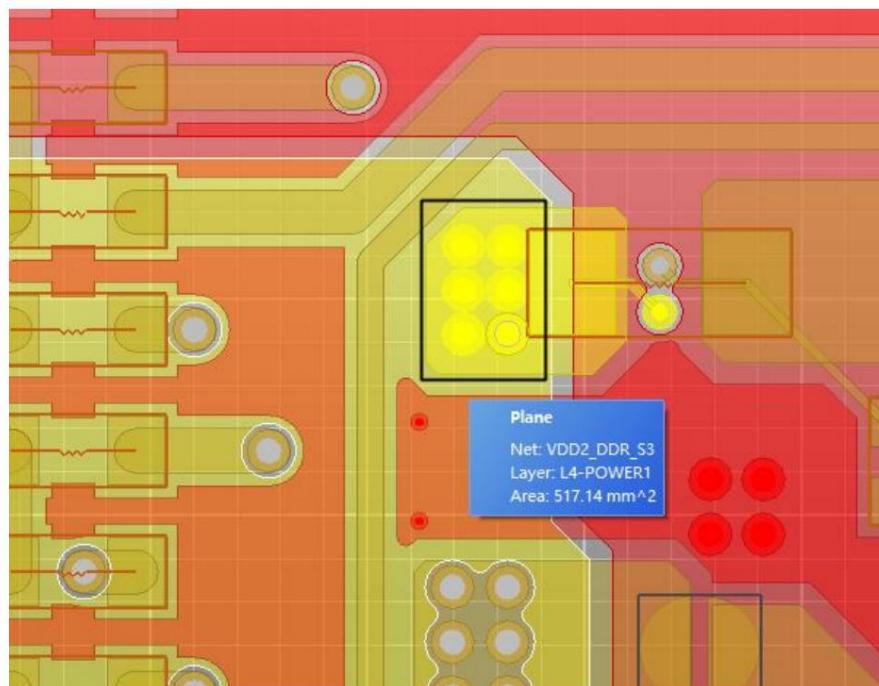


Figure 3-133

(17) For the VDD1_1V8_DDR power supply, it is recommended to drill at least 2 0402 vias when changing the power plane layer.

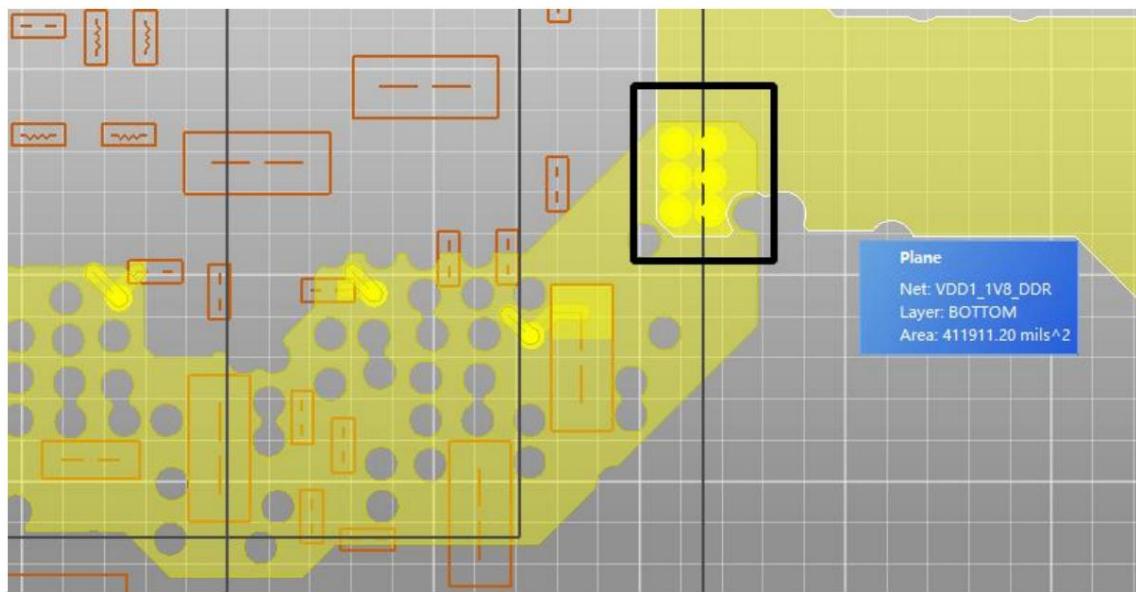


Figure 3-134

(18) It is recommended that at least one via be placed on each capacitor pad. For capacitors with 0603 or 0805 packages, two vias are recommended for each pad.

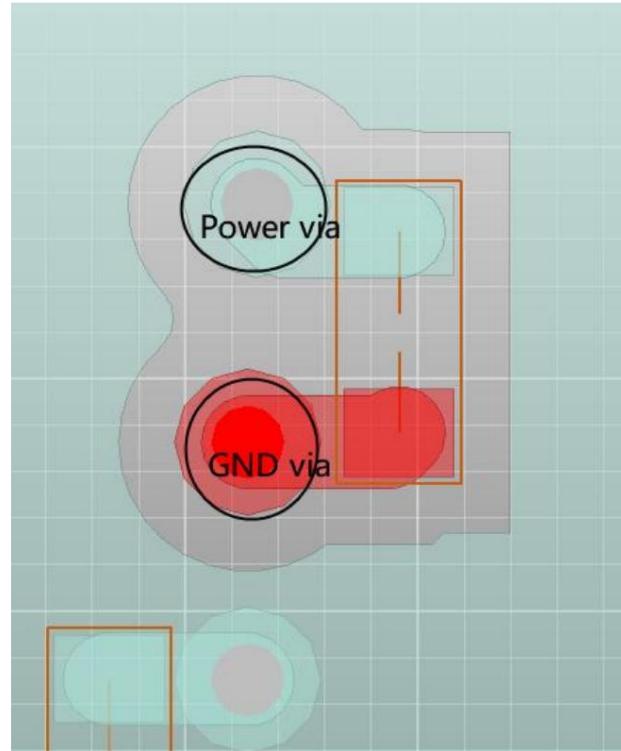


Figure 3-135

(19) Placing vias close to the pins can reduce loop inductance.

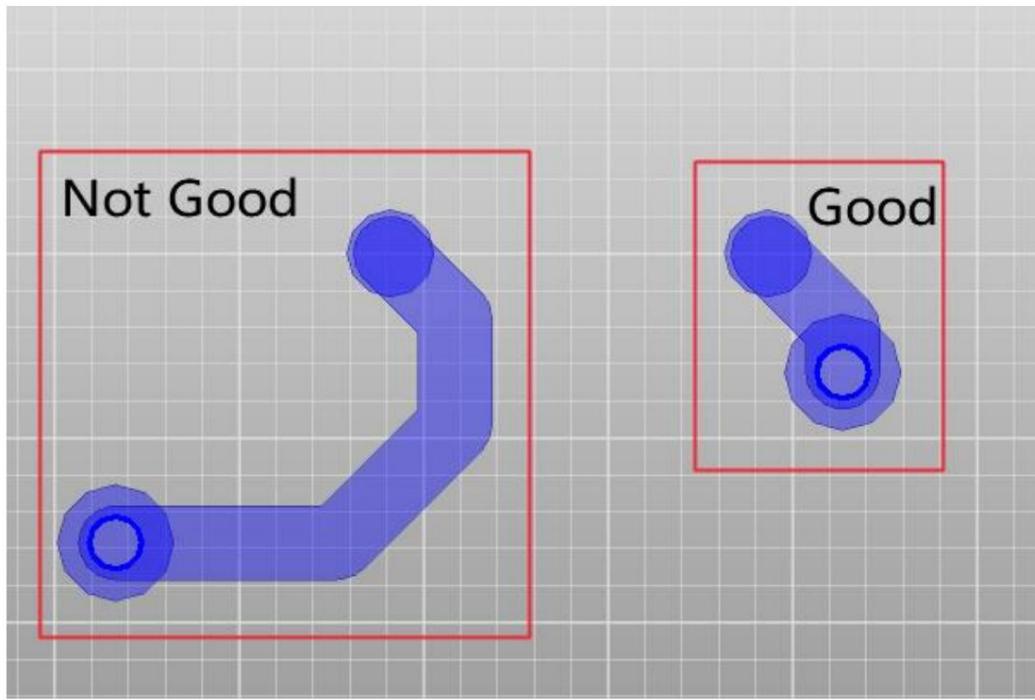


Figure 3-136

(20) The number of power vias corresponding to the CPU's VDDQ_DDR and VDD_DDR pins, refer to the DDR template, it is not recommended to delete the power Via.

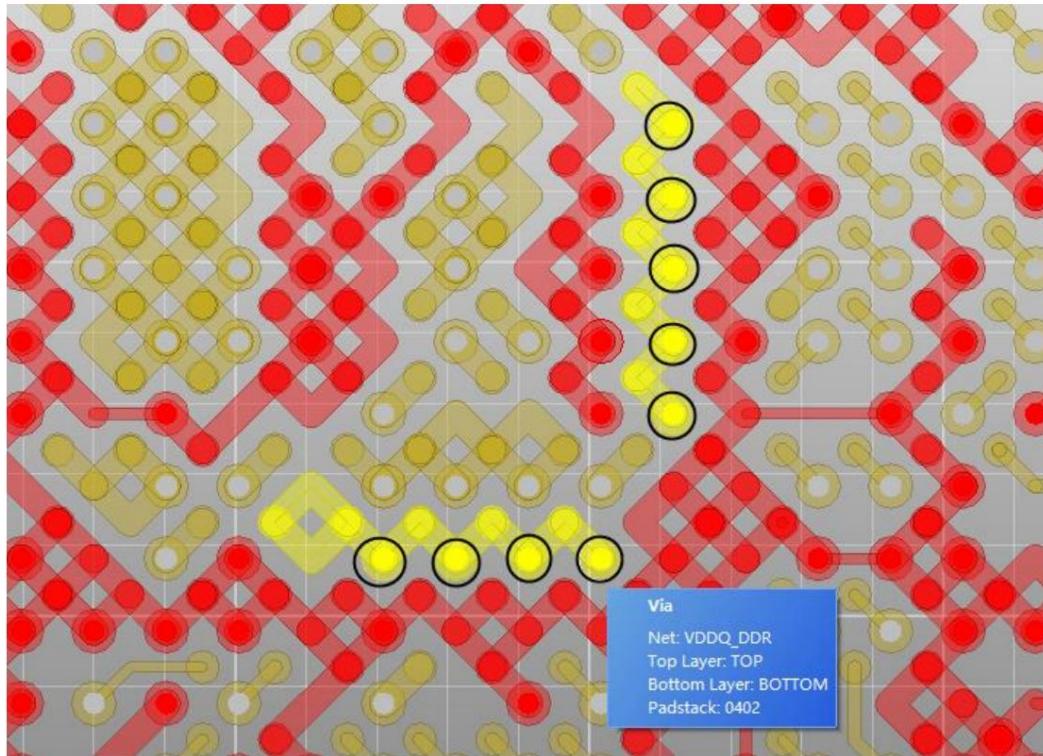


Figure 3-137

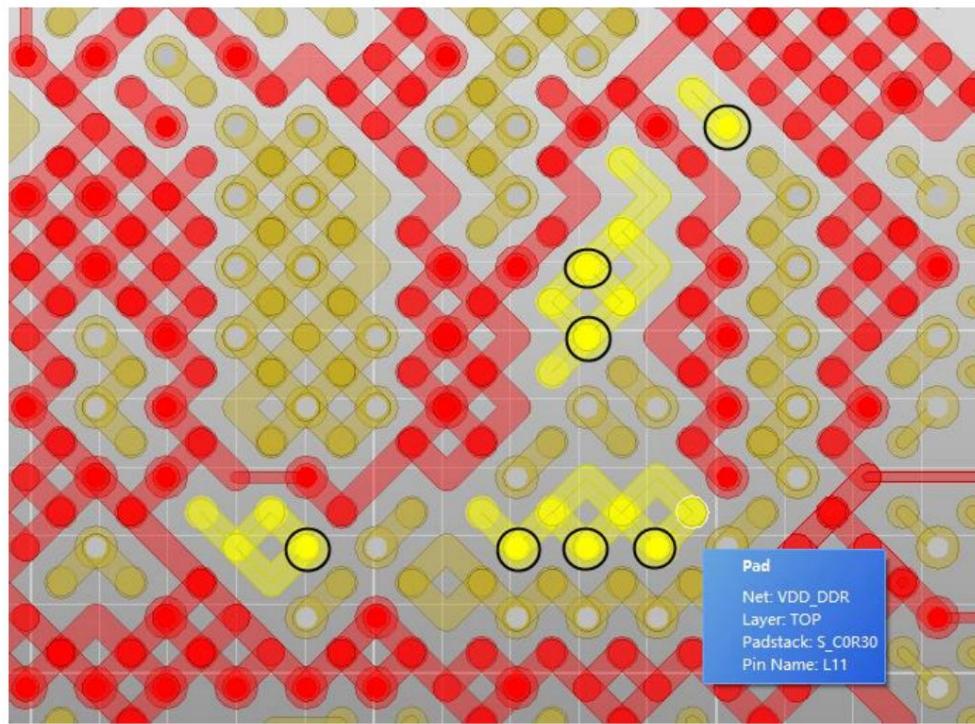


Figure 3-138

(21) For the VDDQ_DRAM, VDD2_DDR, and VDD1_1V8_DDR power supplies of DDR chips, it is recommended that one pin corresponds to one power supply. Source vias, for example.

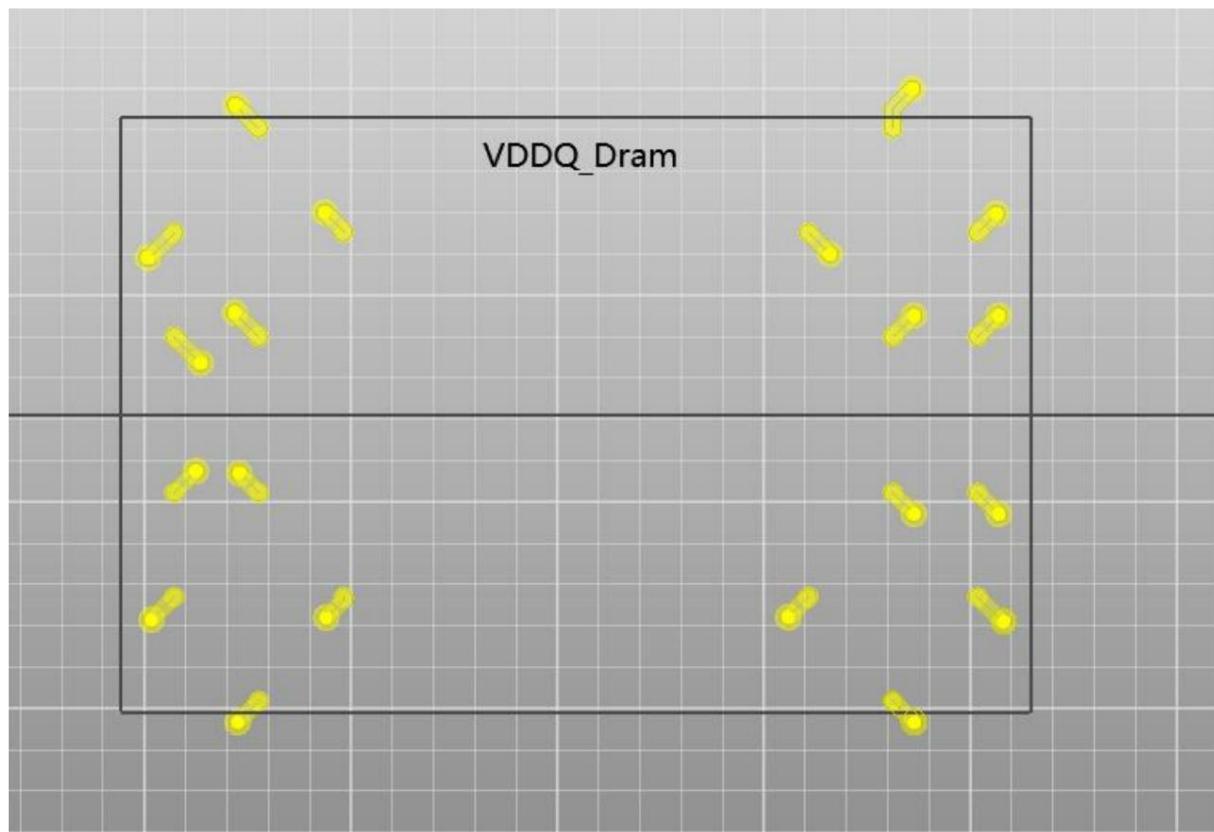


Figure 3-139

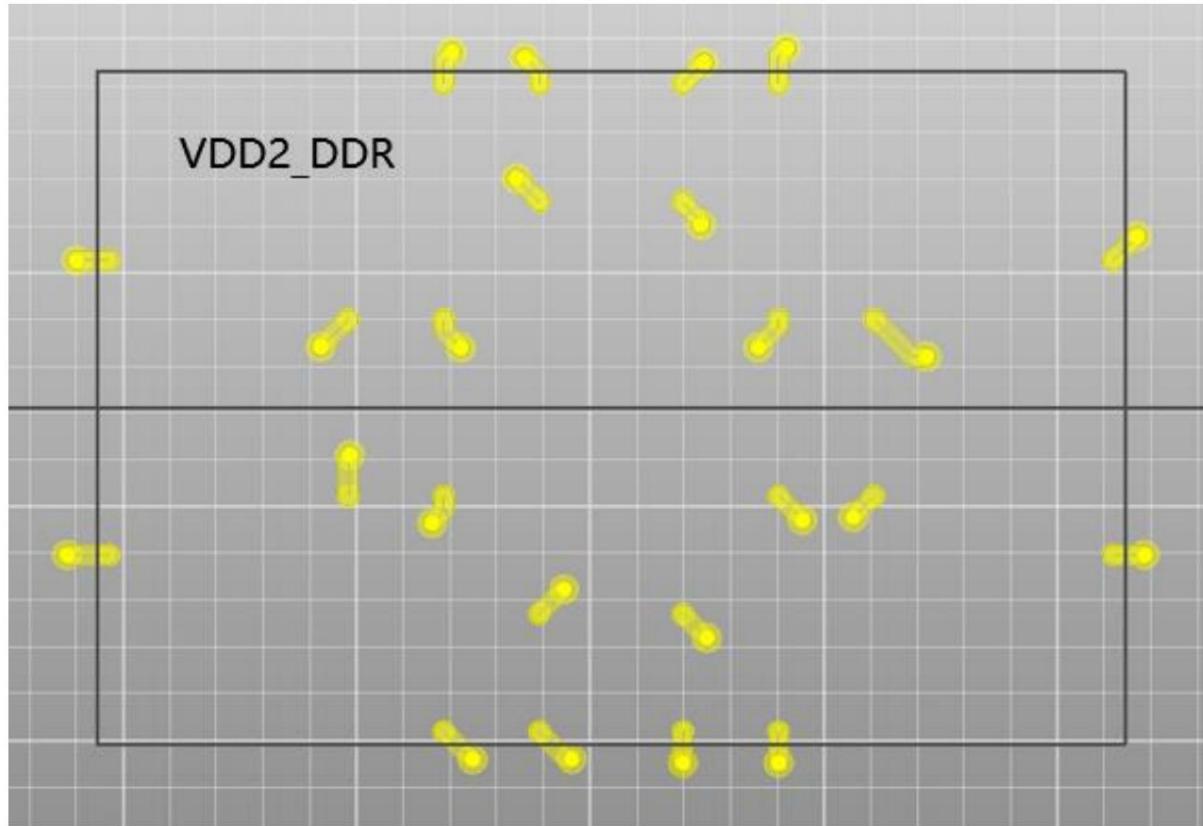


Figure 3-140

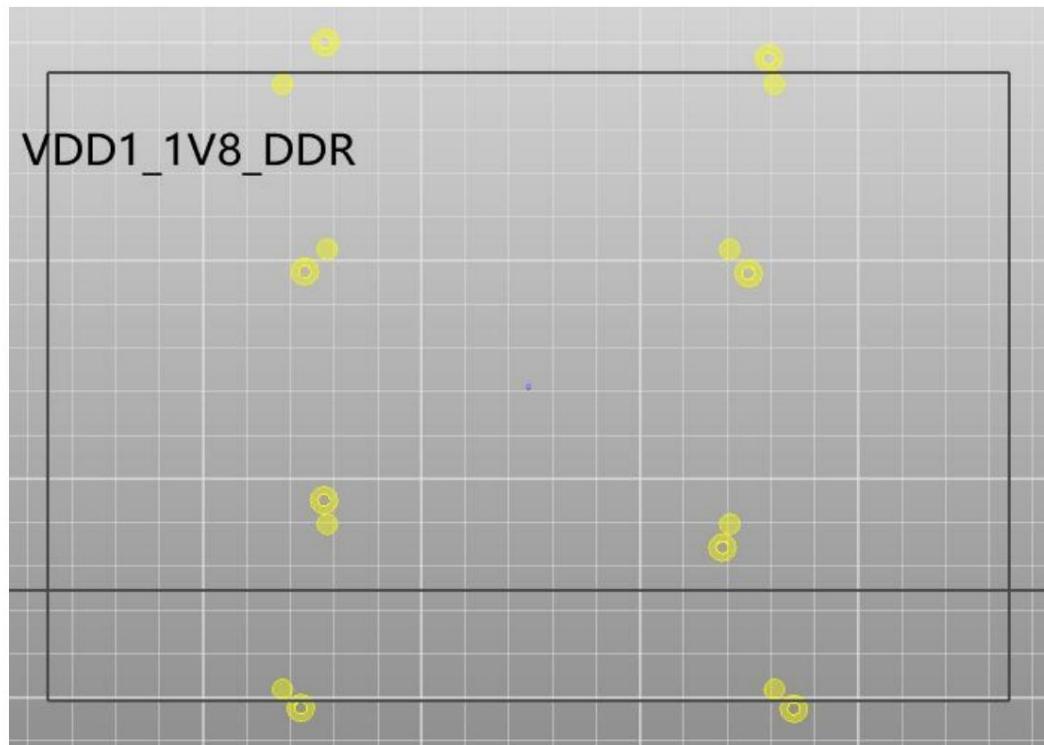


Figure 3-141

(22) When the DDR power supply (VDD_DDR, VDDQ_DDR, VDD2_DDR, VDDQ_DRAM) is switched, sufficient power is required.

The number of source vias (8 0402 vias or 6 0503 vias) is shown below.

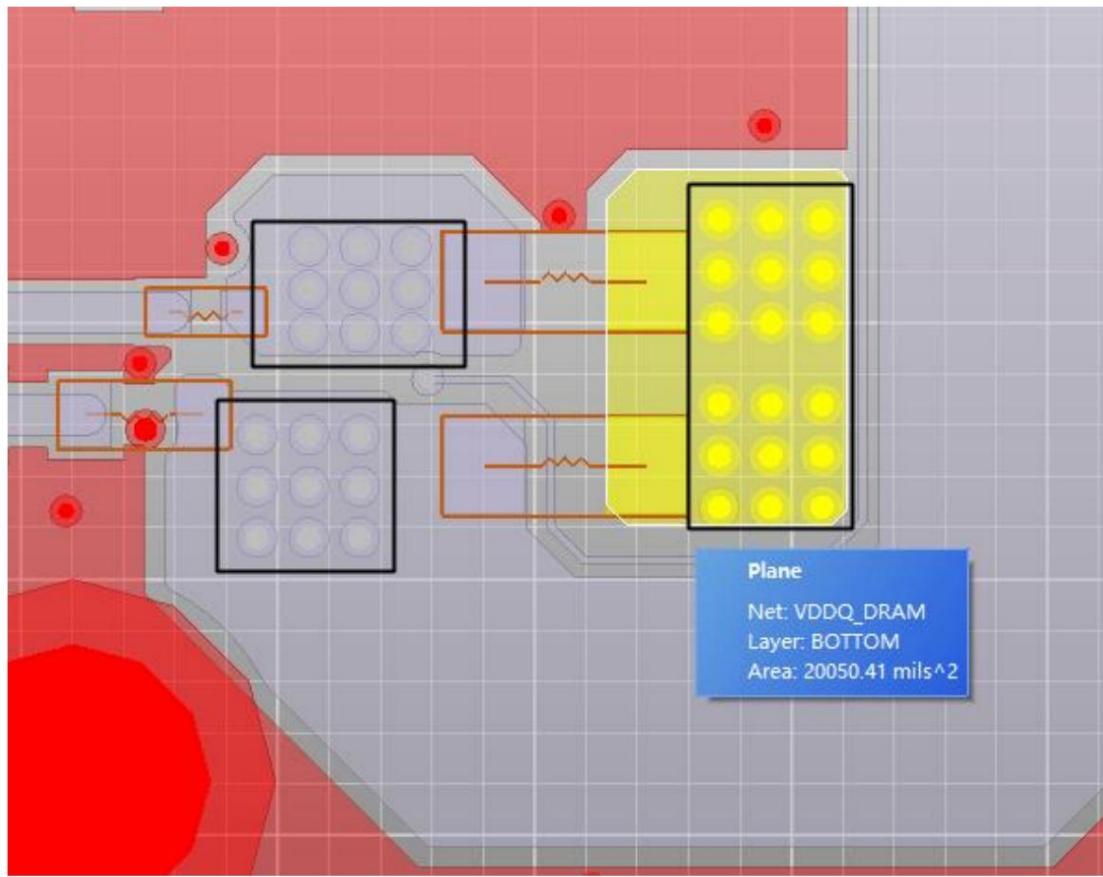


Figure 3-142

(23) Avoid the power layer from being damaged by routing or continuous vias.

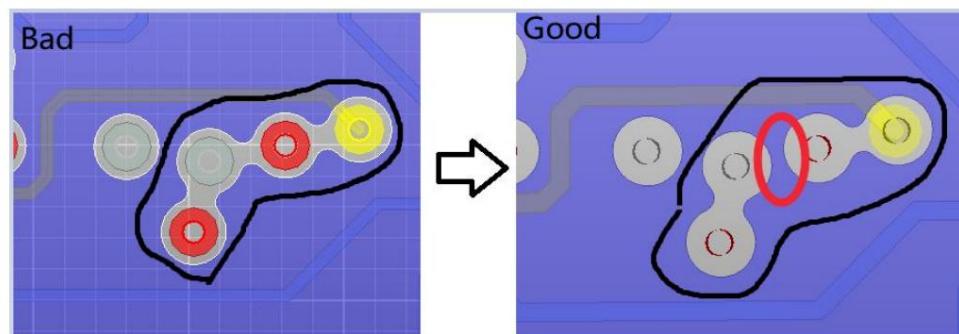


Figure 3-143

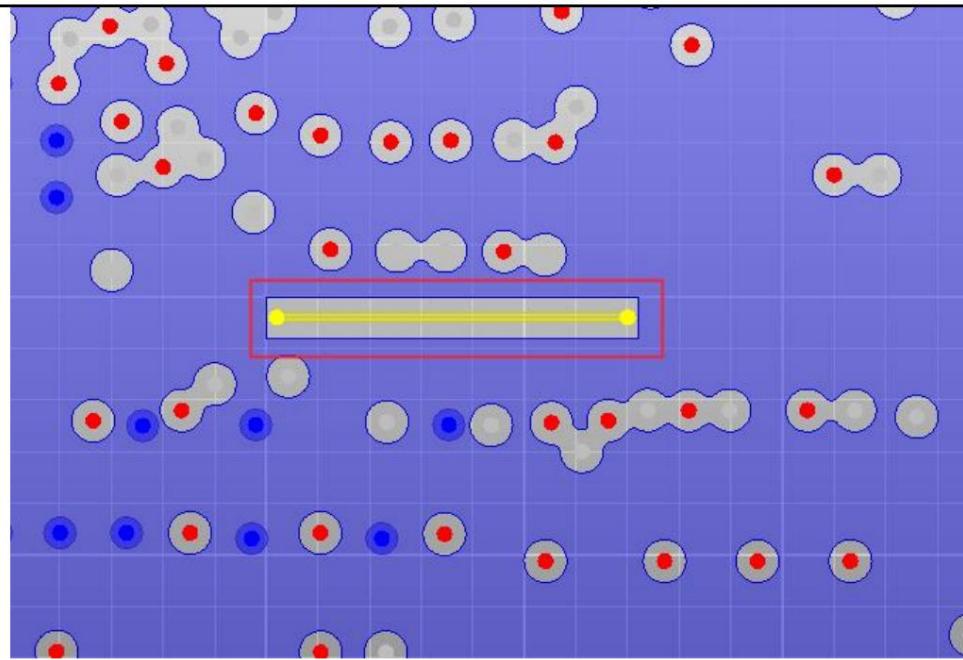


Figure 3-144

(24) The decoupling capacitors of DDR chips should be placed close to the pins to reduce the installation inductance of the capacitors. The number of capacitors is recommended to refer to the template.

It is not recommended to remove capacitors. Capacitors of different values should be placed evenly and dispersed.

(25) The recommended PDN requirements for the CPU area VDD_DDR power supply are shown in the figure below.

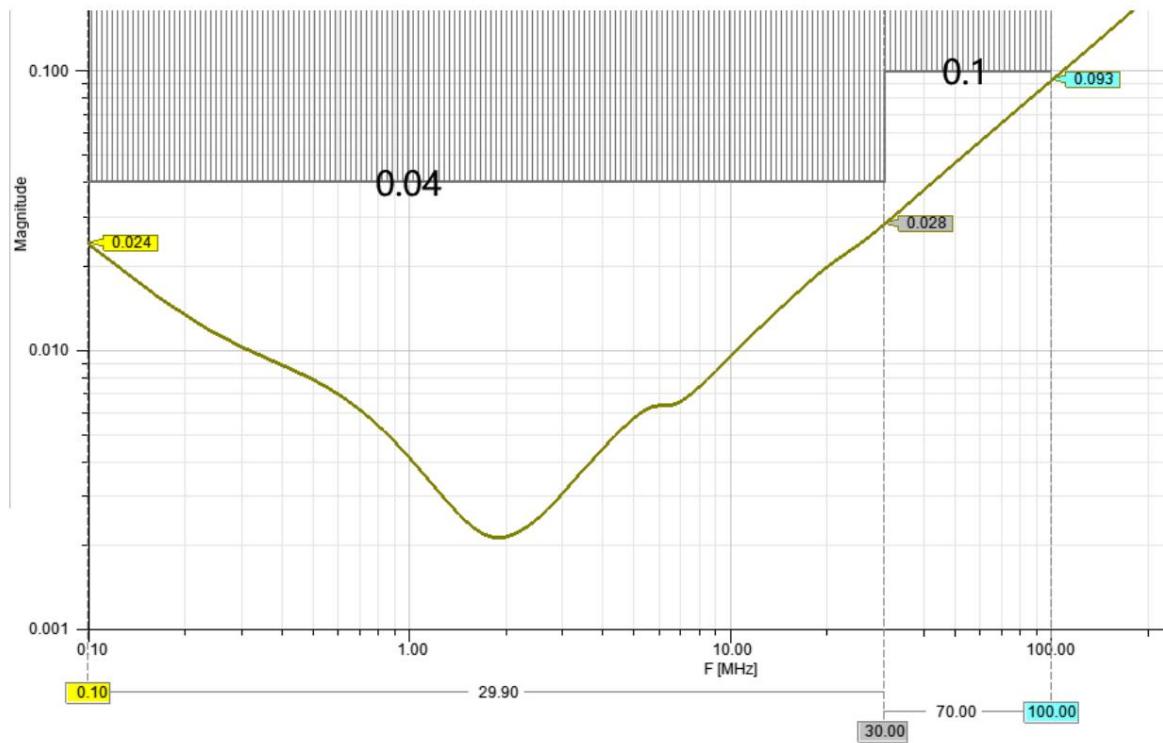


Figure 3-145

(26) The recommended PDN requirements for the CPU area VDDQ_DDR power supply are shown in the figure below.

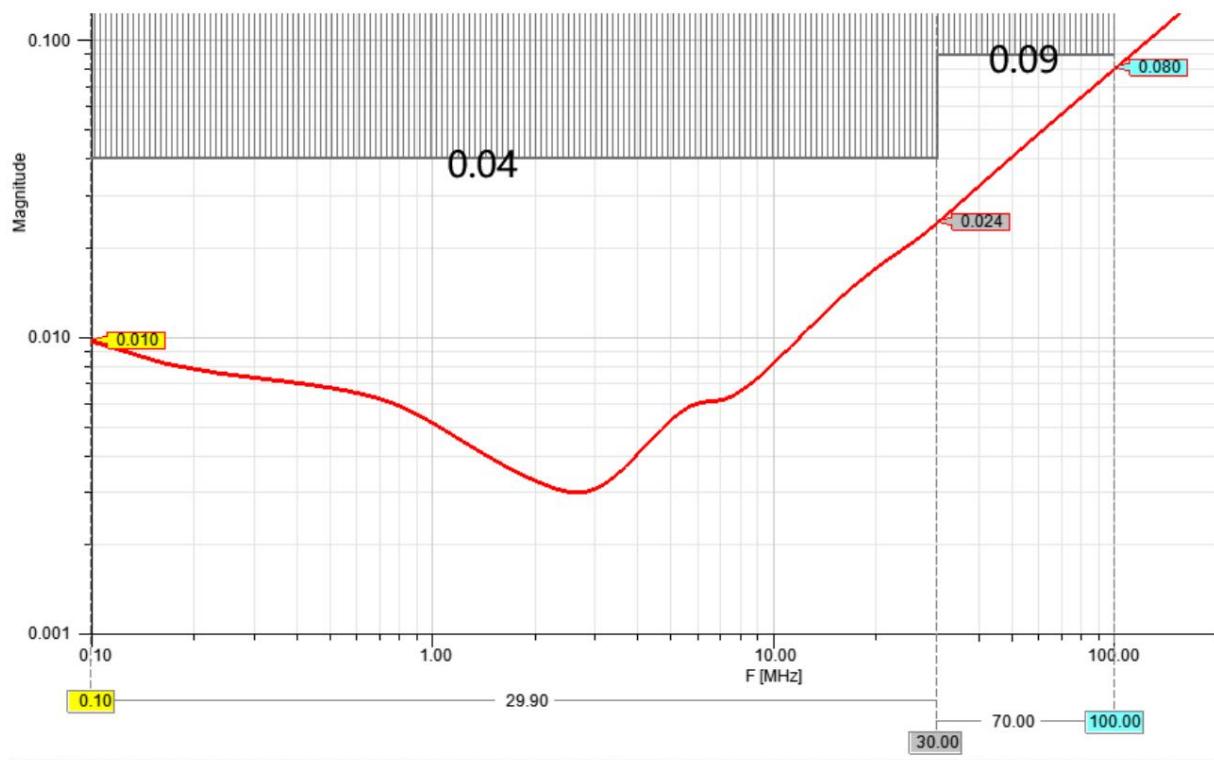


Figure 3-146

(27) The recommended PDN requirements for the VDDQ_DRAM power supply in the DDR chip area are shown in the figure below.

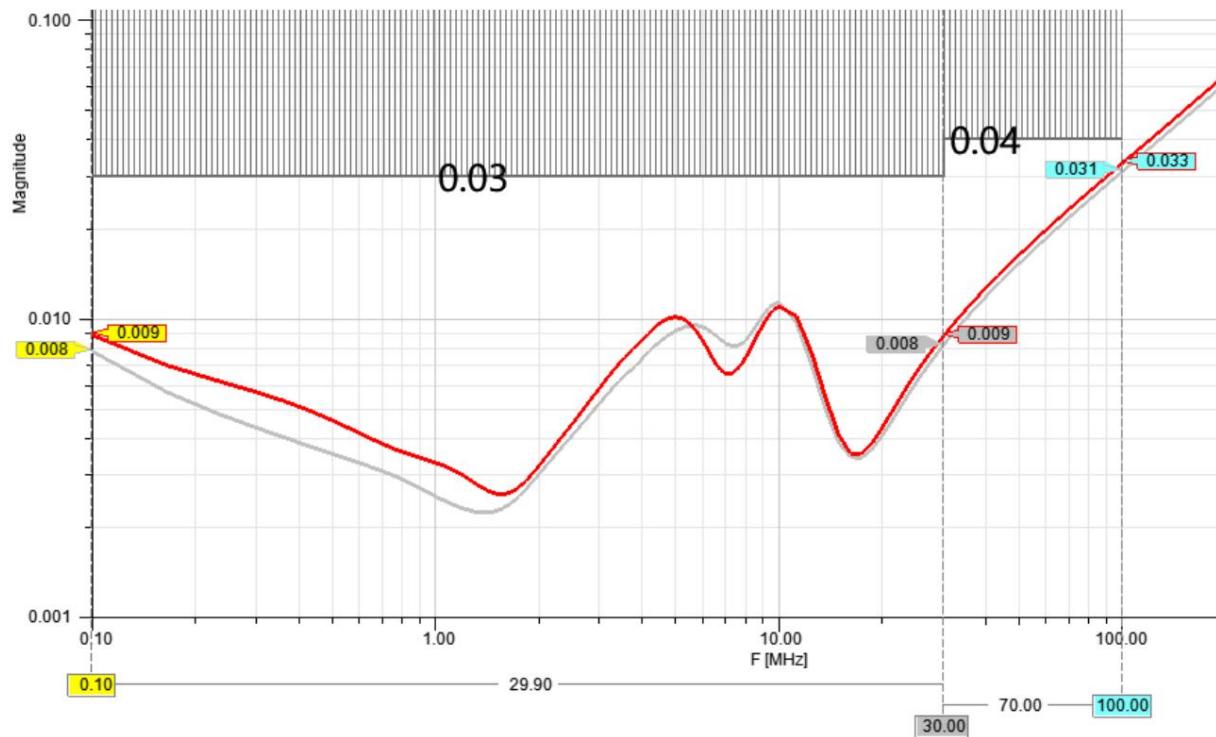


Figure 3-147

(28) The recommended PDN requirements for the VDD2_DDR power supply in the DDR chip area are shown in the figure below.

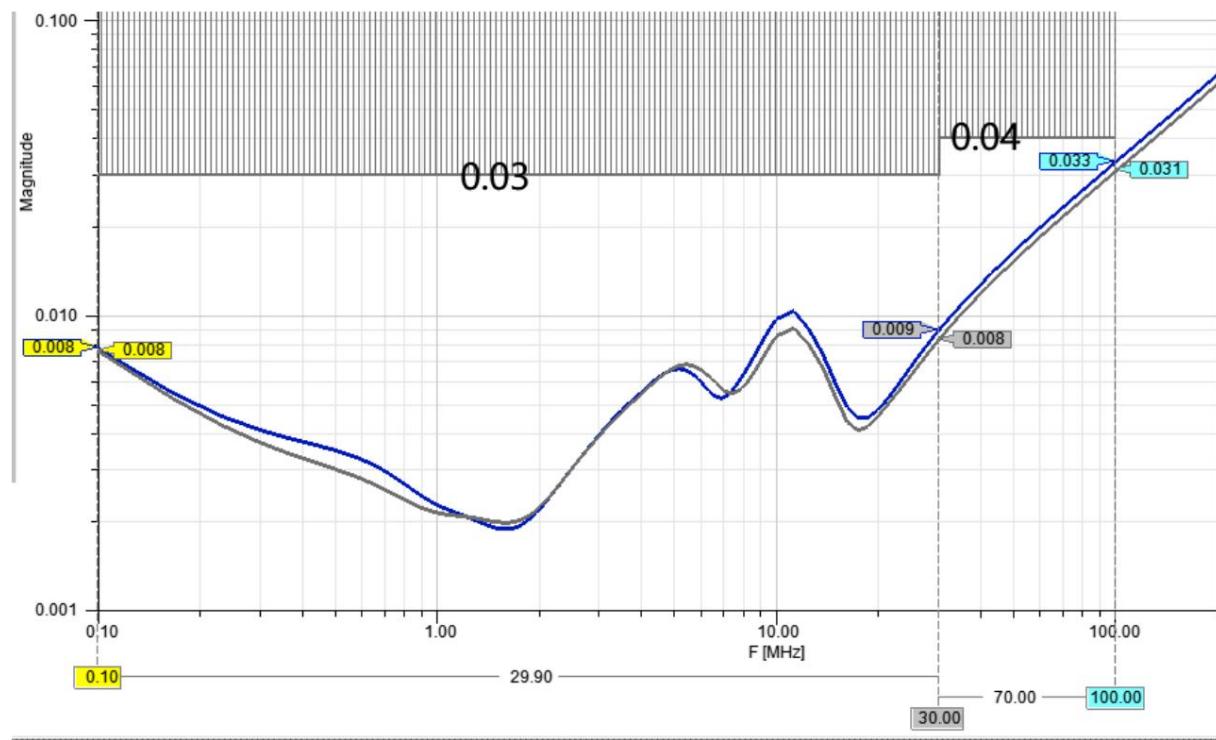


Figure 3-148

3.4.3.2.1 LPDDR4X

Since there are traces on both the surface and inner layers of an 8-layer board, whether it is a single-ended signal or a differential signal, the speed of the surface traces and the inner traces is different.

There is a difference in the speed of single-ended and differential signals for surface routing. There is a small difference in the speed of single-ended and differential signals for inner layer routing.

There are differences in routing speeds. In order to reduce the impact of rate differences on signal margins, design rules need to be based on equal delay requirements.

To set the stackup parameters according to the actual stackup of the board, take the package delay and via delay into consideration. For details, refer to the "Equal Delay Setting Guide" document.

Table 3-10 LPDDR4X routing requirements

parameter	Require
DQ, DM single-ended signal impedance	40 Ohm ± 10%
Address control line (except CKE signal) single-ended signal impedance	40 Ohm ± 10%
CKE single-ended signal impedance	50 Ohm ± 10%
Differential signal impedance	(80~90) Ohm ± 10%
The same length between DQ and DQS (within the same Byte)	≥ 16ps
Equal length between DM and DQS (within the same Byte)	≥ 16ps
Equal length between address, control lines and CLK	≥ 16ps
DQS_P and DQS_N are of equal length (within the same byte)	≥ 1ps
Equal length between CLK_P and CLK_N	≥ 1ps
Equal length between DQS and CLK	≥ 40ps
The spacing between different bytes (airgap)	≥ 2 times the trace width
The airgap between DQs in the same byte	≥ 2 times the trace width
The airgap between DQ and DQS in the same byte	Recommended ≥ 3 times the trace width At least 2 times the trace width
The airgap between address control lines	≥ 2 times the trace width
Spacing between CLK and other signal lines	Recommended ≥ 3 times the trace width At least 2 times the trace width

3.4.3.2.2 LPDDR4

Since there are traces on both the surface and inner layers of an 8-layer board, whether it is a single-ended signal or a differential signal, the speed of the surface traces and the inner traces is different.

There is a difference in the speed of single-ended and differential signals for surface routing. There is a small difference in the speed of single-ended and differential signals for inner layer routing.

There are differences in routing speeds. In order to reduce the impact of rate differences on signal margins, design rules need to be based on equal delay requirements.

To set the stackup parameters according to the actual stackup of the board, take the package delay and via delay into consideration. For details, refer to the "Equal Delay Setting Guide" document.

Table 3-11 LPDDR4 routing requirements

parameter	Require
DQ, DM single-ended signal impedance	40 Ohm ± 10%
Address control line (except CKE signal) single-ended signal impedance	40 Ohm ± 10%
CKE Single-ended signal impedance	50 Ohm ± 10%
Differential signal impedance	(80~90) Ohm ± 10%
The same length between DQ and DQS (within the same Byte)	≥ 16ps
Equal length between DM and DQS (within the same byte) Equal length between address, control lines and CLK	≥ 16ps
DQS_P and DQS_N are of equal length (within the same byte)	≥ 1ps
Equal length between CLK_P and CLK_N	≥ 1ps
The airgap between DQS and CLK is the same length, but the airgap between bytes is different. The airgap between DQ and DQ in the same byte is different.	≥ 2 times the trace width ≥ 2 times the trace width
The airgap between DQ and DQS in the same byte	Recommended ≥ 3 times the trace width At least 2 times the trace width
The airgap between address control lines	≥ 2 times the trace width
Spacing between CLK and other signal lines	Recommended ≥ 3 times the trace width At least 2 times the trace width

3.4.4 DP1.4

Table 3-12 Wiring Requirements - DP1.4

parameter	Require
Trace impedance	Differential 100ohm ±10% (only used as DP interface, no multiplexing) Differential 95OHM±10% (USB3.0/DP1.4 multiplexing)
Delay difference within a differential pair	<6mil
Equal length requirement between differential pairs	<1000mil
Trace length	<6 inches
Spacing between differential pairs	It is recommended to be greater than or equal to 6 times the DP line width
Distance between DP and other signals	It is recommended to be greater than or equal to 6 times the DP line width
The number of vias allowed for each signal	No more than 2 are recommended
Capacitance requirements	100nF is recommended (75nF ~ 200nF including error)
ESD	I/O to ground capacitance does not exceed 0.2pF

It is recommended to add ground holes at the following locations in the BGA area and to perform ground wrapping according to the 24th suggestion in Section 3.2.

The spacing is less than 300mil.

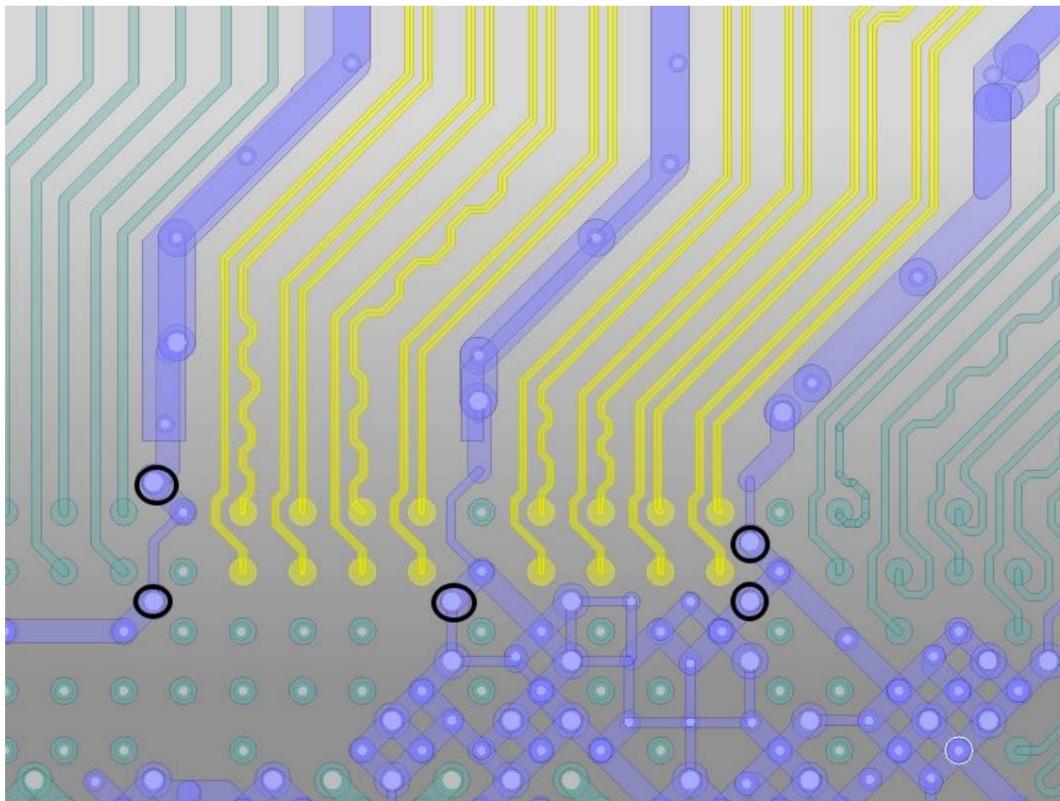


Figure 3-149

3.4.5 PCIe2.0

Table 3-13 Cabling Requirements - PCIE 2.0

parameter	Require
Trace impedance	Differential 85ohm ±10%
Maximum delay difference within a differential pair	<6mil
Equal length requirement between differential pairs	<6inches
Trace length	<6inches
Capacitance requirements	100nF ±20%, 0201 package is recommended
Spacing between differential pairs	It is recommended to be greater than or equal to 4 times the PCI-E line width
Maximum delay difference within the differential pair	<12mil
(REFCLK) Trace impedance (REFCLK)	Differential 100ohm±10%
The distance between PCI-E and other signals	It is recommended to have a width greater than or equal to 5 times the PCI-E line width, and at least 4 times the PCI-E line width.
The number of vias allowed for each signal	No more than 2 are recommended

3.4.6 PCIe3.0

Table 3-14 Wiring Requirements - PECL 3.0

parameter	Require
Trace impedance	Differential 85ohm±10%
Maximum delay difference within a differential pair	<6mil
Equal length requirement between differential pairs	<6inches
Trace length	<6 inches
Capacitance requirements	220nF ±20%, 0201 package is recommended
Spacing between differential pairs	It is recommended to be greater than or equal to 5 times the PCI-E line width
Maximum delay difference within the reference clock (REFCLK) differential pair	<12mil
Reference clock (REFCLK) trace impedance	Differential 100ohm±10%
The distance between PCI-E and other signals	It is recommended to be greater than or equal to 5 times the PCI-E line width
The number of vias allowed for each signal	No more than 2 are recommended

It is recommended to add ground vias at the following locations in the BGA area, and it is recommended to use ground for differential signals, with the ground via spacing of the ground line less than 300 mils.

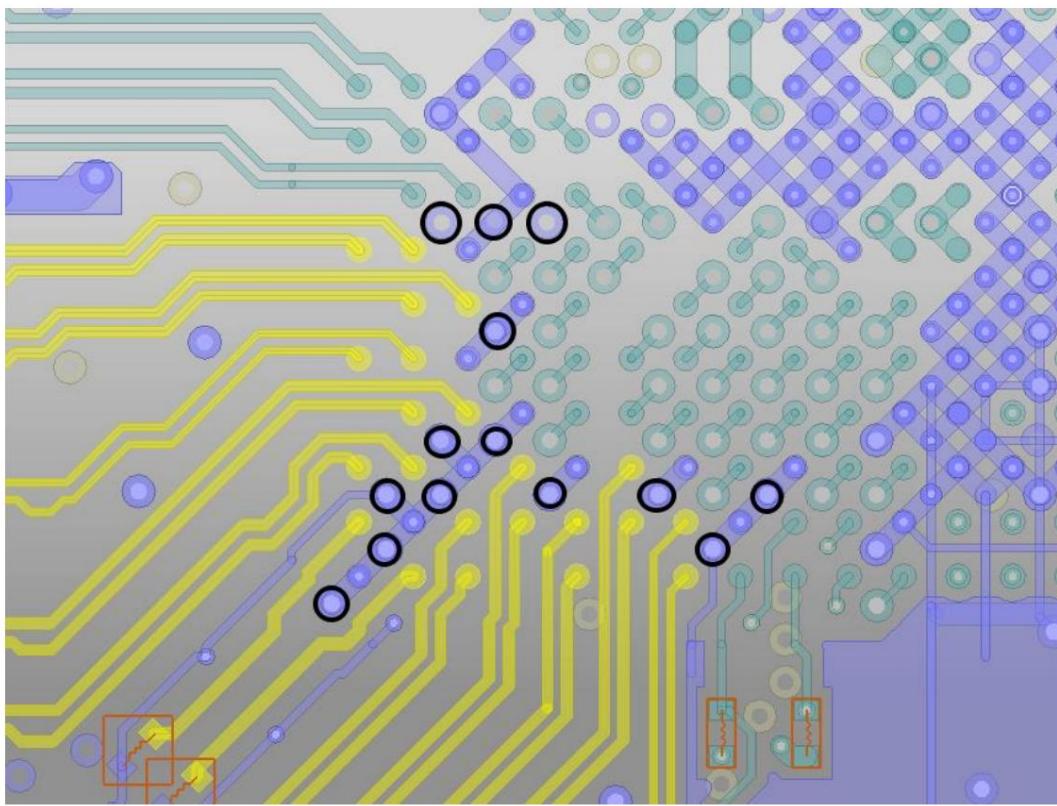


Figure 3-150

3.4.7 HDMI 2.0

Table 3-15 Cabling Requirements - HDMI 2.0.

parameter	Require
Trace impedance	Differential 100ohm ±10%
Maximum delay difference within a differential pair	<6mil
Clock and data length requirements	<480mil
Trace length	<6 inches
Spacing between differential pairs	It is recommended to be greater than or equal to 5 times the HDMI cable width
HDMI and other signal distances	It is recommended to be greater than or equal to 5 times the HDMI cable width
The number of vias allowed for each signal	No more than 2 are recommended

3.4.8 HDMI 2.1

Table 3-16 Cabling Requirements - HDMI 2.1.

parameter	Require
Trace impedance	Differential 100ohm ±10%
Maximum delay difference within a differential pair	<6mil
Equal length requirement between differential pairs	<480mil
Trace length	<4 inches

parameter	Require
Capacitance requirements	220nF ±20%, 0201 package is recommended
Spacing between differential pairs	It is recommended to be greater than or equal to 7 times the HDMI cable width
HDMI and other signal distances	It is recommended to be greater than or equal to 7 times the HDMI cable width
The number of vias allowed for each signal	It is recommended not to add vias
ESD	I/O ground capacitance does not exceed 0.2pF

(1) It is recommended to add ground holes at the following locations in the BGA area and to perform ground wrapping according to the 24th suggestion in Section 3.2.

The hole spacing is less than 150mil.

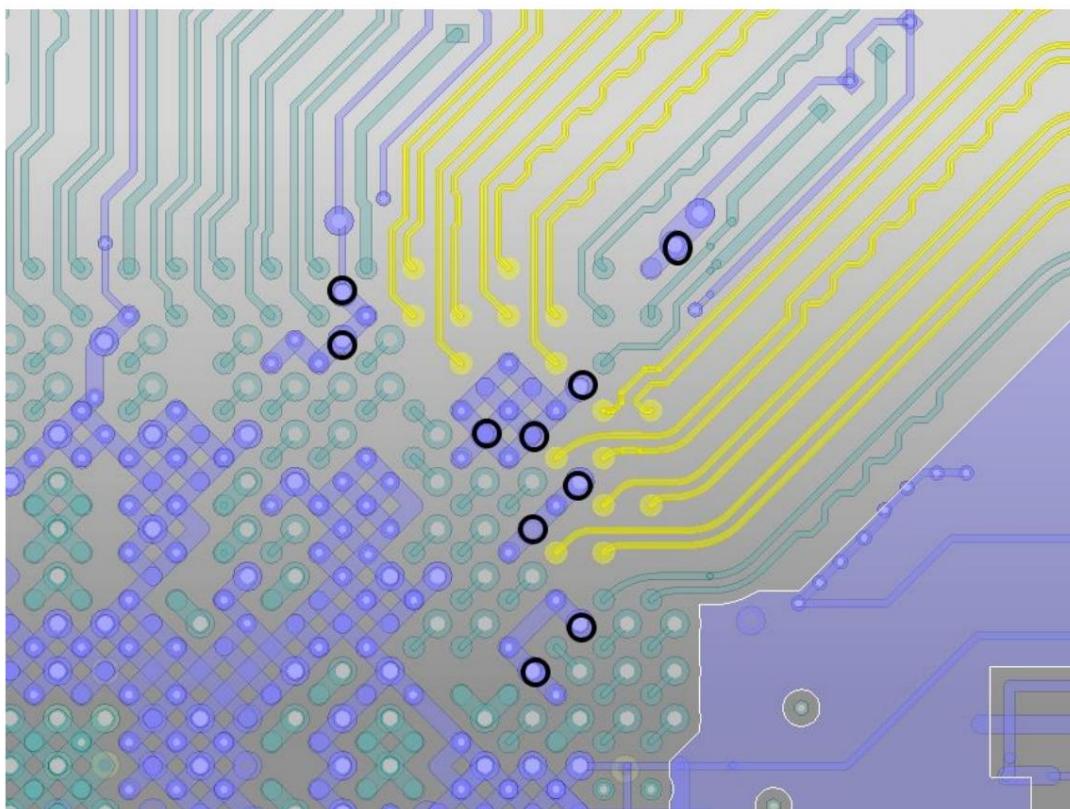


Figure 3-151

(2) Note that the wiring between the DC blocking capacitor and the resistor must be routed according to differential signal routing.

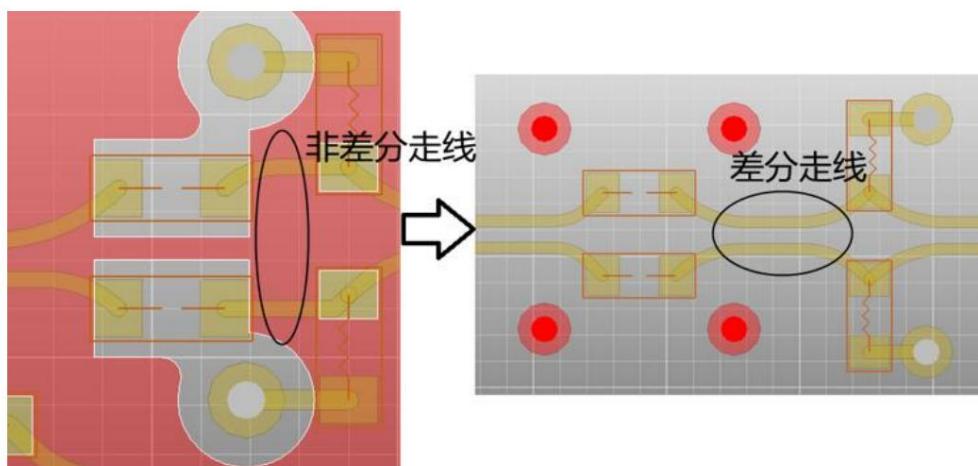


Figure 3-152

(3) The 600 ohm resistor is used as a reference for the interlayer, and the GND copper foil of the same size as the resistor pad is dug out from the adjacent layer. At the same time, differential routing and

There are stubs between the resistor pads.

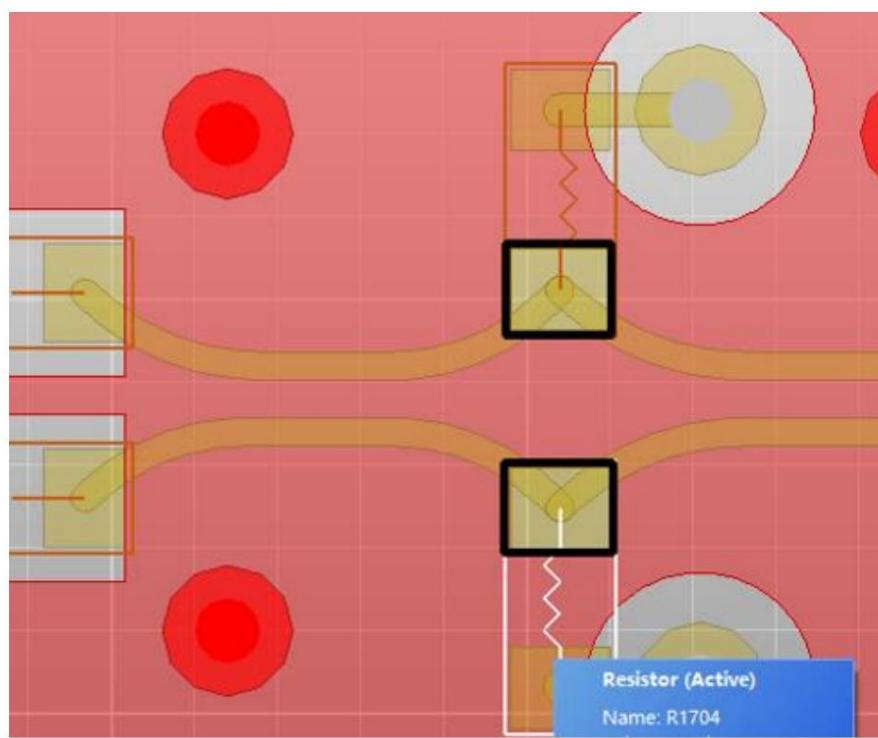


Figure 3-153

3.4.9 SATA 3.0

Table 3-17 Cabling Requirements - SATA 3.0

parameter	Require
Trace impedance	Differential 90ohm ±10%
Maximum delay difference within a differential pair	<6mil
Trace length	<6 inches
Capacitance requirements	10nF ±20%, 0201 package is recommended
Spacing between differential pairs	It is recommended to be greater than or equal to 4 times the SATA line width
SATA and other signal spacing	It is recommended to be greater than or equal to 4 times the SATA line width
The number of vias allowed for each signal	No more than 2 are recommended

3.4.10 USB 2.0

Table 3-18 Cabling Requirements - USB 2.0

parameter	Require
Trace impedance	Differential 90ohm ±10%
Maximum delay difference within a differential pair	<20mil



Trace length	<6 inches
The number of vias allowed for each signal	It is recommended that no more than 4 and no more than 6

3.4.11 USB 3.0

Table 3-19 Cabling Requirements - USB 3.0

parameter	Require
Trace impedance	Differential 90ohm ±10%
Maximum delay difference within a differential pair	<6mil
Trace length	<6 inches
Capacitance requirements	100nF ±20%, 0201 package is recommended
Spacing between differential pairs	It is recommended to be greater than or equal to 4 times the USB cable width
Distance between USB and other signals	It is recommended to be greater than or equal to 4 times the USB cable width
The number of vias allowed for each signal	No more than 2 are recommended

3.4.12 MIPI-D/C PHY

Table 3-20 Cabling Requirements - MIPI-DPHY

parameter	Require
Trace impedance	Differential 100ohm ±10%
Maximum delay difference within a differential pair	<6mil
The length between clock and data is equal	<12mil
Trace length	<6 inches
The number of vias allowed for each signal	No more than 4 are recommended
Spacing between differential pairs	It is recommended to be greater than or equal to 4 times the MIPI line width, and at least 3 times the MIPI line width
MIPI and other signal spacing	It is recommended to be greater than or equal to 4 times the MIPI line width, and at least 3 times the MIPI line width

Table 3-21 Cabling Requirements - MIPI-CPHY

parameter	Require
Trace impedance	Single-ended 50ohm±10%
The maximum delay difference within a group (TRIO_A, TRIO_B, and TRIO_C) and	< 6mil
the equal length requirement between groups (TRIO0, TRIO1, and TRIO2)	<100mil
Trace length	<5 inches
The number of vias allowed for each signal	No more than 2 are recommended
Pair spacing	It is recommended to be greater than or equal to 4 times the MIPI line width
MIPI and other signal spacing	It is recommended to be greater than or equal to 4 times the MIPI line width

It is recommended to add ground vias at the following locations in the BGA area.

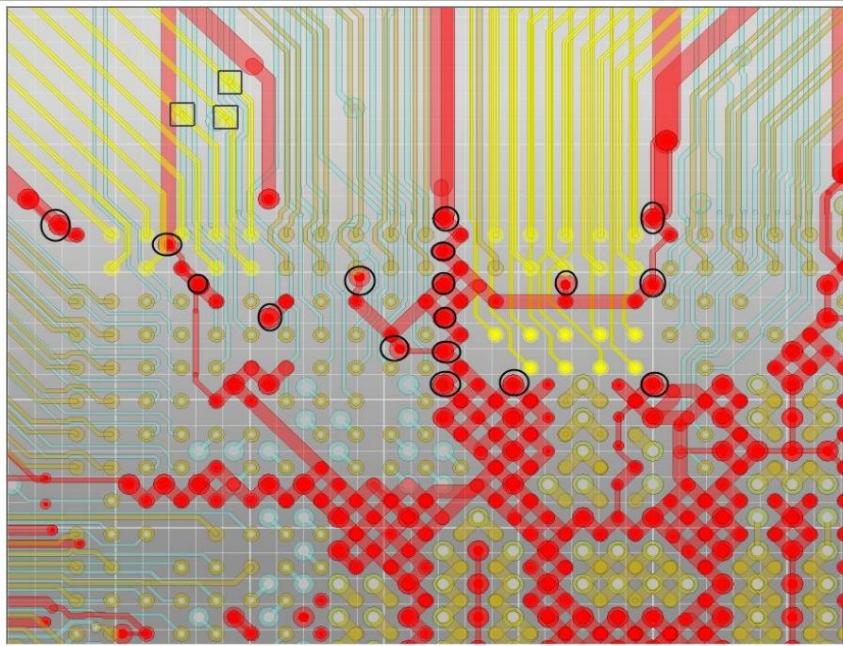


Figure 3-154

3.4.13 eDP

Table 3-22 Cabling Requirements - eDP

parameter	Require
Trace impedance	Differential $85\text{ohm}\pm10\%$
Maximum delay difference within a differential pair	<6mil
Trace length	<6 inches
Spacing between differential pairs	It is recommended to be greater than or equal to 4 times the EDP line width
Capacitance requirements	$100\text{nF}\pm20\%$, 0201 package is recommended
The distance between EDP and other signals	It is recommended to be greater than or equal to 4 times the EDP line width
The number of vias allowed for each signal	No more than 2 are recommended

3.4.14 EMMC

Table 3-23 Wiring requirements - EMMC

parameter	Require
Trace impedance	Single-ended $50\text{ohm}\pm10\%$
The length between clock and data is equal	<120mil
Trace length	<3.5 inches
Distance between eMMC signal lines	At least 2 times the eMMC line width
Distance between eMMC and other signals	It is recommended to use 3 times the line width, at least 2 times the eMMC line width
The number of vias allowed for each signal	No more than 2 are recommended

Before and after the EMMC signal layer is changed, the reference layer is recommended to be the ground plane, within 30mil of the signal via (the center distance between vias).

It is recommended to add ground return vias to improve the signal return path. The ground vias need to connect the reference planes before and after the signal layer change.

3.4.15 SDMMC

Table 3-24 Cabling Requirements - SDMMC

parameter	Require
Trace impedance	Single-ended 50ohm ±10%
The length between clock and data is equal	<120mil
Trace length	<4 inches
Spacing between SDMMC signal lines	At least 2 times the SDMMC line width

3.4.16 SDIO

Table 3-25 Cabling Requirements - SDIO

parameter	Require
Trace impedance	Single-ended 50ohm ±10%
The length between clock and data is equal	<120mil
Trace length	<4 inches
Spacing between SDIO signal lines	At least 2 times the SDIO line width

3.4.17 FSPI

Table 3-26 Cabling Requirements - FSPI

parameter	Require
Trace impedance	Single-ended 50ohm ±10%
Clock and data are equal in length	<200mil
Trace length	<4 inches
Spacing between SFC signal lines	At least 2 times the SFC line width

3.4.18 BT1120

Table 3-27 Wiring Requirements - BT1120

parameter	Require
Trace impedance	Single-ended 50ohm ±10%
Clock and data are equal in length	<180mil
Trace length	<5 inches
Spacing between BT1120 signal lines	Recommended $\sqrt{2}$ times BT1120 line width

3.4.19 RGMII

Table 3-28 Wiring Requirements - RGMII

parameter	Require
Trace impedance	Single-ended 50ohm ±10%
(TXD(0-3), TXEN) to TXCLK equal length	<120mil
(RXD(0-3), RXDV) to RXCLK equal length	<120mil
Trace length	<5 inches
Spacing between RGMII signal lines	Recommended 2 times RGMII line width
RGMII and other signal spacing	It is recommended to use 3 times the RGMII line width, at least 2 times the RGMII line width

3.4.20 Audio Interface Circuit PCB Design

For the digital audio interface of the RK3588 platform, you need to follow the Rockchip_RK3588_High_Speed_PCB_Design_Guide_EN.

The remaining routing requirements are as follows:

ÿ It is recommended to connect a 22ohm resistor in series to all CLK signals and place them close to RK3588 to improve signal quality;

ÿ All CLK signal lines must not be close together to avoid crosstalk; they need to be independently wrapped with ground, and the spacing between the wrapped lines must be within 300mil.

There are ground vias;

ÿ The decoupling capacitors of each IO power domain of the chip must be placed on the back of the corresponding power pins; for single-sided mounting, the decoupling capacitors closest to the chip should be placed on the back of the corresponding power pins.

Place close together;

ÿ For an I2S interface connected to multiple devices, the related CLKs should be connected according to the daisy chain routing topology;

ÿ For a PDM interface connected to multiple devices, the related CLKs should be connected in a daisy chain topology;

In the case of margin, both CLKs in a group of PDM interfaces can be used to optimize routing branches.

ÿ It is recommended to use ground for the entire SPDIF signal. Ground vias must be provided within 300mil intervals between ground traces.

For peripheral audio signal routing requirements, please refer to the design guide of the corresponding device. If there is no emphasis, please refer to the following instructions:

ÿ The SPKP/SPKN signal coupling traces of the speaker are routed and wrapped with ground as a whole. The trace width is calculated based on the peak current output and is minimized.

Short traces to control line resistance;

If there are ferrite beads, LC filters, or other components placed near the speaker's power amplifier output, it is recommended to place them close to the amplifier output to optimize EMI.

The left and right audio channel outputs of the headphone should be independently grounded to avoid crosstalk and optimize isolation. The recommended trace width is greater than 10 mils.

ÿ When the microphone is connected single-ended, the MIC signal is routed separately and grounded separately;

ÿ When connecting the microphone differentially, especially in most pseudo-differential cases, the traces must be routed according to the differential method and the entire group must be grounded;

ÿ The recommended line width for microphone signals is 8 mil or more;

ÿ All audio signals should be routed away from high-speed signal lines such as LCD and DRAM. It is forbidden to route them on adjacent layers of high-speed signal lines.

The adjacent layer must be a ground plane, and drilling holes near high-speed signal lines to change layers is prohibited;

ÿ All audio signal lines should be routed away from inductive areas, RF signals and devices;

ÿ For the TVS protection diodes of the headphone jack and microphone, place them as close to the connector as possible. The signal topology is: headphone jack/microphone

ÿTVSÿIC; when ESD occurs, the ESD current will first pass through the TVS device to attenuate; do not place

If there are residual piles, it is recommended to increase the ground vias of the TVS ground pin as much as possible, and ensure at least two 0.4mm*0.2mm vias to enhance the static discharge.

Release ability.

3.4.21 WIFI/BT PCB Design

When laying out the overall layout, the WIFI module should be placed appropriately, away from DDR, HDMI, USB, LCD circuits and speakers that are prone to interference.

Module or connector:

The TOP layer below the module is not allowed to be routed. The reference plane must be a complete ground plane. The SDIO/PCIe/UART/PCM signal lines are built

It is recommended to bypass the module projection area and connect to the module pins;

The crystal circuit layout needs to be given priority. It should be placed on the same layer as the chip and as close as possible to avoid drilling holes.

As short as possible, away from interference sources, and as close to the antenna area as possible;

The crystal and clock signals need to be grounded throughout. At least one GND via should be added every 100mil of the ground line.

Verify that the ground reference surface of the adjacent layer is intact;

When the crystal circuit is placed on a different layer from the chip, the crystal routing and grounding must be done throughout to avoid interference;

32.768k is routed separately and grounded, and at least one GND via is added every 400mil of the ground line;

For SDIO WIFI, the SDIO signal PCB design requirements are as follows: Section 3.2.5;

For PCIe WIFI, the PCIe signal PCB design requirements are as follows: Sections 3.2.7 and 3.2.8;

When laying out the module's inductor, ensure that the trace exits the inductor, passes through the capacitor, and then enters the module's power pin.

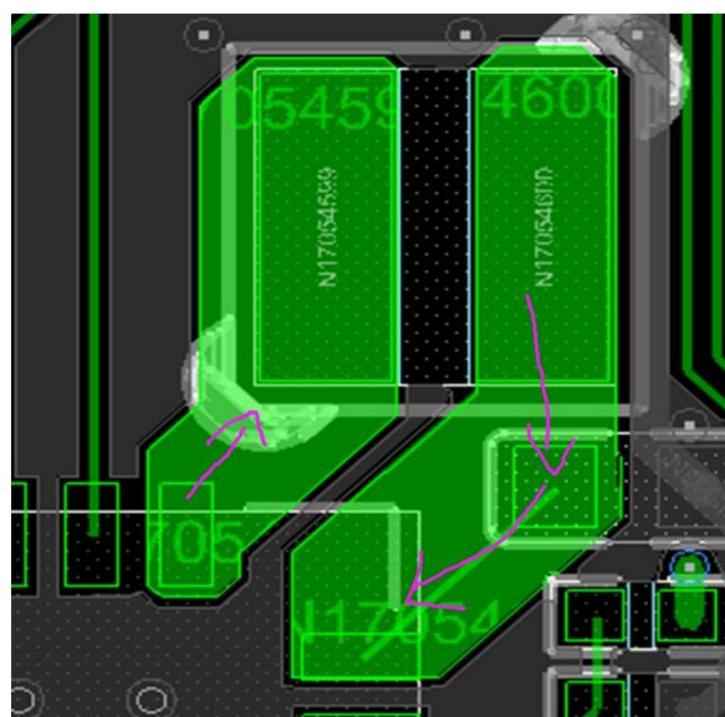


Figure 3-155 Schematic diagram of the inductor and capacitor wiring of the Wi-Fi module

The module's power decoupling capacitor must be close to the module's power pin;

The module's VBAT pin trace width must be greater than 40 mils;

The longer the antenna wiring is, the greater the energy loss is. Therefore, when designing, the antenna path should be as short as possible without branches and should not be changed as much as possible.

layer;

The antenna matching circuit must be close to the antenna base, the antenna line is 50 ohms, and the reference ground is guaranteed to be complete. The impedance should not change suddenly.

There are other signal lines or power supplies; the accompanying ground of the routing needs to be connected to the main ground reference plane using a ground wall;

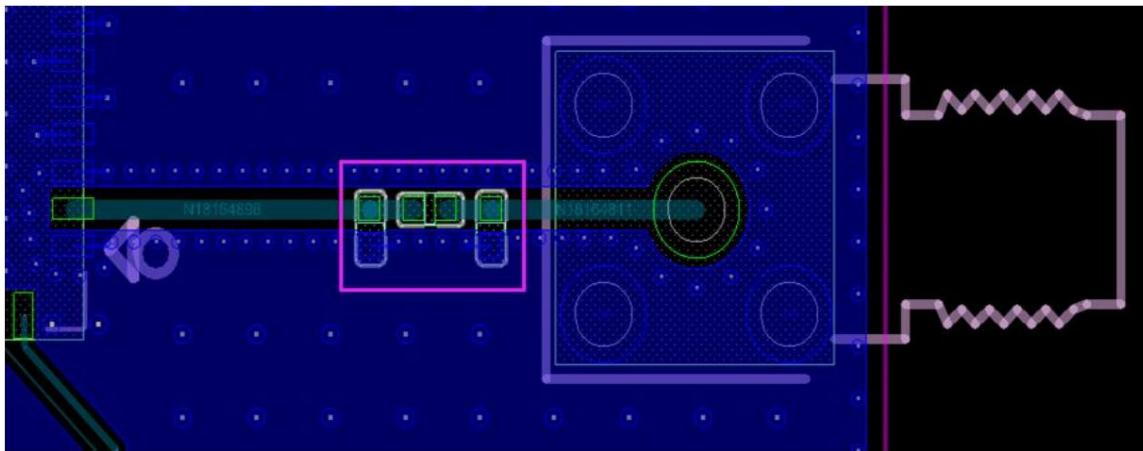


Figure 3-156 Wi-Fi module antenna wiring diagram

ŷ No other signal lines or power supplies are allowed on all layers below the module's antenna and antenna routing area; ŷ If it is a 2X2 MIMO antenna

interface, the direction of the line between the two antenna ports needs to take into account the positions of the two antennas.

The locations need to be as far away as possible to avoid interference, and consider placing them vertically to avoid interference with each other.

3.4.22 VGA OUT PCB Design

ŷ During the overall layout, the VGA seat should be placed as close to the conversion chip as possible, and the VGA analog signal traces should be shortened as much as

possible; ŷ The decoupling capacitors of the conversion chip power supply should be placed as close as possible to the power pins of the conversion

chip; ŷ The width of the VGA_R/G/B traces should be as thick as possible, and it is recommended to be more

than 12mil; ŷ The length difference between VGA_R/G/B should not exceed 200mil; ŷ The VGA_R/

G/B 75ohm resistor must be placed close to the chip; ŷ The VGA_R/G/B filter circuit must be

placed close to the VGA seat; ŷ The VGA_R/G/B signals require separate grounding throughout, and the

ground traces must have ground vias within 300mil intervals; ŷ The adjacent layer of the VGA_R/G/B signals must be a ground plane, not a power plane; ŷ VGA_R/G/B signals should

be kept away from high-speed signal lines such as LCD and DRAM, and it is prohibited to route them on the layers adjacent

to high-speed signal lines; it is prohibited to route them on the layers adjacent to high-speed signal lines; it is prohibited to route them on the layers adjacent to high-speed signal lines.

Drill holes and change layers near high-speed signal lines; do not route through inductive areas; stay away from RF signals and devices;

ŷ The RC filter of VGA_HSYNC/VSYNC must be placed close to the VGA socket, and the wiring must not exceed 6 inches; ŷ All signal TVS tubes of the VGA socket should be

placed as close to the connector as possible. The signal topology is: VGA socket-->TVS-->chip pins;

When ESD occurs, the ESD current must first be attenuated by the TVS device. Avoid stubs on the TVS device traces. It is recommended to increase the number of ground vias for the

TVS ground pin, ensuring at least two 0.4*0.2mm vias, to enhance electrostatic discharge capabilities.

3.4.23 LCD Screen and Touch Screen PCB Design

ŷ The FB-terminal current-limiting resistor of the LED backlight IC should be placed close to the screen base instead of the DC-DC. ŷ In the

backlight boost circuit, pay attention to the placement of capacitors and the power supply routing to ensure that the power supply charge and discharge loop is

minimized. ŷ If there are reserved test points on the screen and touch screen connector, they should be close to the connector, and the stubs on the routing should be as short as possible.

3.4.24 Camera PCB Design

ŷ When the camera uses a connector: When the MIPI differential signal passes through the connector, the GND pin must be used between adjacent differential signal pairs.

row isolation;

ÿ For signals such as CIF/MIPI, if board-to-board connection is achieved through a connector, it is recommended to connect a resistor of a certain value in series with all signals.

(between 2.2ohm and 10ohm, subject to the ability to meet SI test requirements), and reserve TVS components;

If the camera connector has a reserved test point, it should be close to the connector and the stub on the trace should be as short as possible.

ÿ The decoupling capacitors of the AVDD/DOVDD/DVDD power supply connectors need to be placed as close to the Camera connector as possible;

ÿ When laying out the camera, it needs to be kept away from high-power radiating devices, such as GSM antennas.

For MIPI CSI RX signal PCB design requirements, see Section 3.2.9.

4 Thermal design recommendations

Good thermal design is particularly important for improving RK3588 product performance, system stability, and product safety.

4.1 Thermal simulation results

For the RK3588 FCBGA1088_23x23mm_Pitch 0.65mm package, a 10-layer PCB based on EVB was constructed using finite element method. Finite Element Modeling (FEM) can produce a simulation report of thermal resistance. This report is based on the JEDEC JESD51-2 standard. Given that the system design and environment during application may differ from the JEDEC JESD51-2 standard, an analysis needs to be made based on the application conditions.



Notice

Thermal resistance is a reference value when the PCB does not have a heat sink. The specific temperature is related to the design, size, thickness, material and other physical factors of the single board.

4.1.1 Summary of Results

The thermal resistance simulation results are shown in the following table:

Table 4-1 RK3588 thermal resistance simulation report results

Package (EHS-FCBGA)	(°C / W)	(°C / W)	(°C / W)
JEDEC PCB	8.7	3.5	0.12

Note: The data is simulated and for reference only. Please refer to the actual test.

4.1.2 PCB Description

The PCB structure used for thermal resistance simulation is as follows:

Table 4-2 PCB structure for RK3588 thermal resistance simulation

JEDEC PCB	PCB Dimension L x W	101 x 114mm
	PCB Thickness	1.6mm
	Number of Cu Layer	10-layers

4.1.3 Explanation of terms

The terms in this chapter are explained as follows:

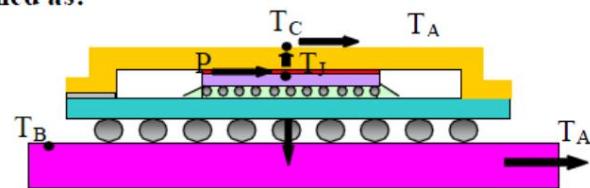
- T_J The maximum junction temperature
- T_A The ambient or environment temperature
- T_C The maximum compound surface temperature
- T_B The maximum surface temperature of PCB bottom

\dot{P} Total input power

The thermal parameter can be define as following

1. Junction to ambient thermal resistance, θ_{JA} , defined as:

$$\theta_{JA} = \frac{T_J - T_A}{P} ; \quad (1)$$



Thermal Dissipation of EHS-FCBGA

Figure 4-1 Definition of $\dot{\theta}_{JA}$

2. Junction to case thermal resistance, θ_{JC} , defined as:

$$\theta_{JC} = \frac{T_J - T_C}{P} ; \quad (2)$$

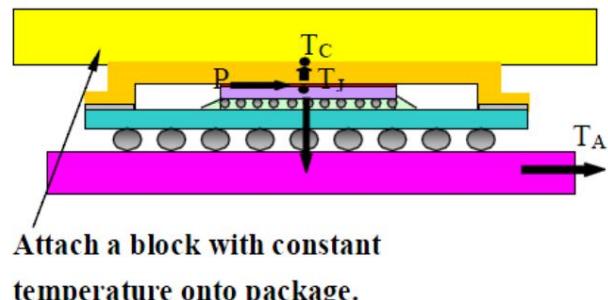


Figure 4-2 Definition of $\dot{\theta}_{JC}$

3. Junction to board thermal resistance, θ_{JB} , defined as:

$$\theta_{JB} = \frac{T_J - T_B}{P} ; \quad (3)$$

Attach a block with constant temperature

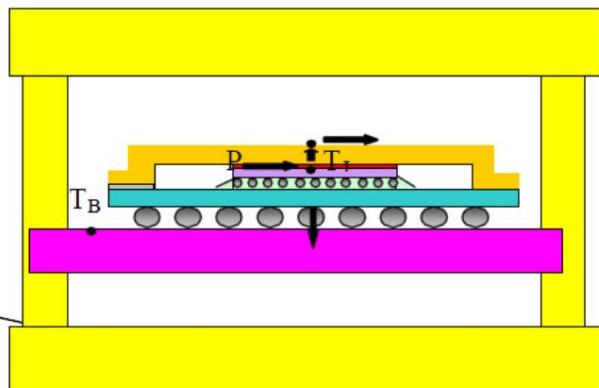


Figure 4-3 Definition of $\dot{\theta}_{JB}$

4.2 Chip Internal Thermal Control Method

4.2.1 Temperature control strategy

In the Linux kernel, a temperature control framework, Linux Generic Thermal System Drivers, is defined, which can control the temperature through different strategies.

There are three commonly used strategies to control the temperature of the system:

Power allocator: The temperature control strategy introduces PID (proportional-integral-derivative) control to dynamically allocate power to each cooling device based on the current temperature. When the temperature is low, the available power is large, which means the operating frequency is high. As the temperature rises, the available power gradually decreases, and the operating frequency also gradually decreases, thus achieving temperature-based frequency limit.

Step wise: Cooling devices reduce their frequencies step by step based on the current temperature. ¦ Fair

share: Cooling devices with more frequency levels are prioritized for frequency reduction. ¦ Userspace: No frequency limit.

The RK3588 chip has a T-sensor inside to detect the on-chip temperature, and uses the Power_allocator strategy by default.

4.2.2 Temperature control configuration

The RK3588 SDK can provide temperature control strategies for CPU and GPU respectively. For specific configuration, please refer to

Rockchip_Developer_Guide_Thermal_CN.pdf

This document is incomplete and will be provided upon completion.

4.3 Circuit Thermal Design Reference

4.3.1 Circuit Schematic Thermal Design Reference

Under the premise of ensuring stability, improve overall power efficiency, such as using less LDO with high voltage difference, reducing the power supply itself in the power conversion process.

Heat generated during the process;

According to the actual product, try not to power on the modules that are not used by the chip or let the software do the power down process; ¦ Select

materials with high thermal conductivity, and re-estimate the required heat sink size according to the "Heat Sink Size Calculation" according to the product definition, usage environment and other conditions.

The size of the radiator to be used, it is recommended to use a larger radiator as possible.

4.3.2 PCB Thermal Design Reference

Among RK3588 products, the RK3588 chip generates the most heat, and all heat dissipation treatments focus on the chip. In addition to the RK3588, other major heat-generating

components include: PMIC, charging IC and its inductor, backlight IC and its inductor. ¦ Reasonable structural design can ensure a heat exchange path between the internal part

of the device and the outside air; ¦ In the overall layout, high-power or heat-generating components are evenly distributed to avoid

local overheating. It is recommended that RK3588 and RK806 be appropriately

Place them neither too close nor too far apart. A distance of 20mm-50mm is recommended. Try not to place them on the edge of the board, as this will affect heat dissipation.

It is recommended to use more than 8 layers of board, try to increase the copper content of the board, it is recommended to use 1oz copper thickness, try to use multiple layers as ground plane, and other layers as

In addition to meeting the needs of power and signal routing, the ground plane should be laid as much as possible to use a large area of copper foil to dissipate heat;

¦ RK3588 VDD_LOGIC, VDD_GPU, VDD_NPU, VDD_CPU, VCC_DDR, VDD_LIT current

It is relatively large, and the routing or copper coating must meet the current carrying capacity, otherwise the temperature rise may increase;

ÿ For chips with EPAD, the EPAD should be filled with as many vias as possible, the adjacent layer must be a ground plane, and the copper foil on the back should be as complete as possible.

It is recommended to use bare copper on the back to facilitate heat dissipation.

ÿ The GND pins of the RK3588 chip are arranged in a "well" shape on the top layer and cross-connected. The recommended trace width is 10 mil to facilitate chip heat dissipation.

ÿ For the GND pin of the RK3588 chip, it is recommended to ensure that each ball has a corresponding ground via, at least every 1.5 balls

Corresponding to a via, a heat conduction path is increased, and the adjacent layer must be a ground plane, which is conducive to chip heat dissipation;

ÿ For the decoupling capacitor ground pad on the back of the RK3588 chip, it is recommended to use full copper cladding instead of using flower holes for connection. Try to keep the ground copper intact.

To improve heat dissipation;

ÿ In open areas, without damaging the power layer, try to increase ground vias and increase heat conduction paths to improve heat dissipation.

5. ESD/EMI Protection Design

5.1 Overview

This chapter provides suggestions for ESD/EMI protection design in RK3588 product design to help customers better improve the product's anti-static,

Anti-electromagnetic interference level.

5.2 Explanation of terms

The terms in this chapter are explained as follows:

ÿ ESD (Electro-Static Discharge): Electrostatic discharge; ÿ EMI (Electromagnetic Interference):

Electromagnetic interference, including conducted interference and radiated interference.

5.3 ESD Protection

ÿ Isolate the mold and retract the connector as far as possible into the shell, so that the distance for static electricity to be discharged to the internal circuit is longer.

The quantity becomes weaker, and the test standard changes from contact discharge conditions to air discharge, etc.

ÿ Protect and isolate sensitive components during PCB layout;

ÿ When laying out, try to place the RK3588 chip and core components in the middle of the PCB. If they cannot be placed in the middle of the PCB, ensure that the shielding cover is away from the

The distance from the edge of the board should be at least 2mm, and the shielding cover should be reliably grounded;

ÿ The PCB should be laid out according to the functional modules and signal flow. Each sensitive part should be independent of each other. It is best to isolate the parts that are prone to interference.

isolation;

ÿ ESD devices should be placed properly, generally at the source, that is, at the interface or where static electricity is released; ÿ Component layout should be away from the edge of the board and at a certain

distance from the connector;

ÿ The PCB surface must have a good GND circuit, and each connector must have a good GND connection circuit on the surface.

The shield should be connected to the surface ground as much as possible, and more ground holes should be drilled at the welding point of the shield. To achieve this, each connection socket is required to be grounded.

Do not run traces on the surface, and do not run traces that cut through the surface copper over a large area.

ÿ Avoid routing traces along the edges of the surface board and drill

more ground vias; ÿ When necessary, isolate the signal from the ground; ÿ Expose

more copper to enhance electrostatic discharge, or to facilitate remedial measures such as adding foam; ÿ If board-to-board connections are achieved via

connectors, it is recommended that all signals be connected in series with resistors of a certain resistance (between 2.2ohm and 10ohm, depending on whether they meet SI testing requirements) and that TVS

devices be reserved to improve anti-static surge capabilities;

ÿ The 100nF capacitor of the RK3588 nPOR pin must be placed close to the pin, and the ground pad of the capacitor must have a 0402 ground via, empty

It is recommended to install more than two cables for better grounding.

ÿ The distance between key signals such as Reset, clock, interrupt and other sensitive signals and the board edge should not be less than 5mm; ÿ If other

peripheral chips have Reset pins, it is recommended to add a 100nF capacitor close to the pin, and the ground pad of the capacitor must have a

0402 ground vias. If space allows, it is recommended to drill more than two for better grounding.

ÿ When the whole machine is designed as a floating device, it is recommended that each interface not be designed

with separate grounding; ÿ When the machine casing is metal, the power supply has three holes, and the metal casing must be well connected to the ground;

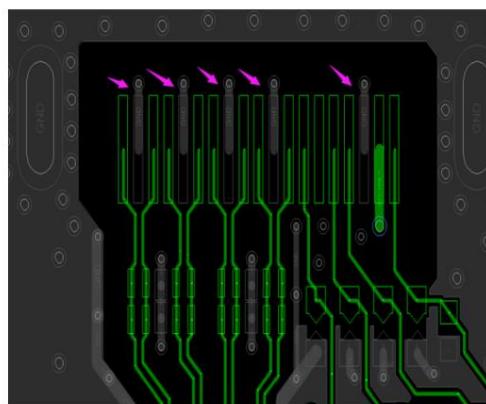
ÿ Reserve space for the shielding cover. The shielding cover should be connected to the surface ground as much as possible, and more ground holes should be drilled at the shielding cover welding point.

This requires that the wiring of each connector should not be on the surface, and there should not be any wiring that cuts off the surface copper foil on a large scale;

ÿ Isolate from the PCB so that static electricity can only be released in certain areas, such as the individual vias of the ground pins of the socket and the connection with the inner layer.

Keep out the surface PCB, and keep the surface copper and pins as far away as possible, that is, keep sensitive signals away from areas prone to static discharge.

(surface copper), etc., as shown in the figure, isolate the distance between HDMI signal and GND on the surface.



5.4 EMI Protection

Electromagnetic interference consists of three elements: interference source, coupling channel, and sensitive equipment. Since we cannot address sensitive equipment, addressing EMI requires addressing the interference source and coupling channel. The best way to resolve EMI is to eliminate the interference source. If this is not possible, find ways to cut off the coupling channel or avoid the antenna effect.

ÿ It is generally difficult to completely eliminate interference sources on a PCB. However, methods such as filtering, grounding, balancing, impedance control, and improving signal quality (such as termination) can be used to address them. These methods are generally combined, but good grounding is the most basic requirement.

ÿ Commonly used materials for EMI include shielding covers, special filters, resistors, capacitors, inductors, magnetic beads, common mode inductors/magnetic rings, and absorbing materials.

Materials, spread spectrum devices, etc.

ÿ Filter selection principle: If the load (receiver) is high impedance (general single-ended signal interfaces are high impedance, such as SDIO,

If the load (receiver) is low impedance (e.g., RBG, CIF), capacitive filtering components should be added to the line. If the load (receiver) is low impedance (e.g., a power supply output interface), inductive filtering components should be added in series. The use of filtering components must not exceed the SI tolerance. Common-mode inductors are commonly used for differential interfaces to suppress EMI.

ÿ The shielding measures on the PCB must be well grounded, otherwise it may cause radiation leakage or the shielding measures to form an antenna effect, and the connector Shielding must comply with relevant technical standards;

ÿ RK3588 can be used in different modules. The degree of spread spectrum should be determined according to the signal requirements of the relevant parts.

RK3588 Spread Spectrum Description;

ÿ The RC circuits between DDR3_CLKP/N, DDR4_CLKP/N, and LPDDR3_CLKP/N must not be deleted to improve EMI. ÿ It is recommended to retain all matching resistors in series with the clocks to provide matching impedance and improve signal quality. ÿ At the DC power input, a power common-mode inductor or EMI filter can be reserved if conditions permit. ÿ Common-mode inductors or filtering circuits should be added to interfaces such as USB, HDMI, VGA, and screen connectors. ÿ When adding a heat sink, be aware that the heat sink may also couple EMI energy and generate radiation. When selecting a heat sink, in addition to meeting thermal design requirements, EMI testing requirements should also be met. Grounding conditions must be reserved for the heat sink. When grounding is required, the heat sink should be grounded. The number of grounding points and how to select them are unclear here, and the first version of the hardware needs to be rectified based on actual conditions during actual laboratory testing.

ÿ EMI and ESD have highly consistent requirements for layout. Most of the aforementioned ESD layout requirements are applicable to EMI.

Protection. In addition, the following requirements are

added: ÿ Ensure signal integrity as much as possible;

ÿ Differential lines should be of equal length and tightly coupled to ensure the symmetry of differential signals to minimize misalignment of differential signals and clocks.

Avoid conversion into common-mode signals that cause EMI problems;

ÿ Components with metal shells such as plug-in devices should avoid coupling interference signals and radiation. Also avoid interference signals from the devices.

The signal is coupled from the housing to other signal lines;

ÿ All clock matching resistors are close to the CPU end (source end), and the traces between the CPU pins and the resistors must be controlled within 400mil.

Within;

ÿ If the PCB has more than 4 layers, it is recommended that all clock signals be routed on the inner layers as much as possible;

ÿ To prevent power radiation, the power layer copper must be retracted, with one H (the dielectric thickness between the power supply and the ground) as the unit. It is recommended

Retracted 20H.

6. Welding process

6.1 Overview

The RK3588 chip is a ROHS certified product, which means it is a lead-free product. This chapter specifies the basic temperature settings for each time period when the client uses the RK3588 chip SMT. It mainly introduces the process control when the client uses the RK3588 chip reflow soldering: mainly lead-free process And mixed process.

6.2 Explanation of terms

The terms in this chapter are explained as follows:

- ÿ Lead-free: lead-free process;
- ÿ Pb-free: lead-free process, all components (mainboard, all ICs, resistors and capacitors, etc.) are lead-free components, and use lead-free solder paste
- Pure lead-free process;
- ÿ Reflow profile: reflow soldering; ÿ Restriction of Hazardous Substances (ROHS): restrictions on the use of certain hazardous substances in electrical and electronic equipment make;
- ÿ Surface Mount Technology (SMT): Surface mount technology; ÿ Sn-Pb: Tin-lead mixed process, which refers to the mixed soldering process using lead solder paste and both lead-free BGA and lead IC.

6.3 Reflow Oven Requirements

6.3.1 Solder paste composition requirements

The ratio of solder alloy to flux is 90%:10% by weight; the volume ratio is 50%:50%. The solder paste should be stored at 2~10°C and should be kept at room temperature before use.

Return to the temperature for 3 to 4 hours and keep a record of the time.

The solder paste needs to be stirred before brushing the board, manually for 3 to 5 minutes or mechanically for 3 minutes, and it will be in a natural vertical flow after stirring.

6.3.2 SMT Curve

Since the RK3588 chip is made of environmentally friendly materials, it is recommended to use Pb-Free process. The reflow curve below is only JEDEC J-STD-020D
The process requirements are recommended values, and the client needs to adjust them according to actual production conditions.

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak		
Temperature min (T_{smin})	100 °C	150 °C
Temperature max (T_{smax})	150 °C	200 °C
Time (T_{smin} to T_{smax}) (t_s)	60-120 seconds	60-120 seconds
Average ramp-up rate (T_{smax} to T_p)	3 °C/second max.	3 °C/second max.
Liquidous temperature (T_L)	183 °C	217 °C
Time at liquidous (t_L)	60-150 seconds	60-150 seconds
Peak package body temperature (T_p)*	See classification temp in Table 4.1	See classification temp in Table 4.2
Time (t_p)** within 5 °C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

* Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and a user maximum.
** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.

Figure 6-1 Reflow curve classification

Package Thickness	Volume mm ³ <350	Volume mm ³ 350 - 2000	Volume mm ³ >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm - 2.5 mm	260 °C	250 °C	245 °C
>2.5 mm	250 °C	245 °C	245 °C

Figure 6-2 Heat resistance standards for lead-free process device packages

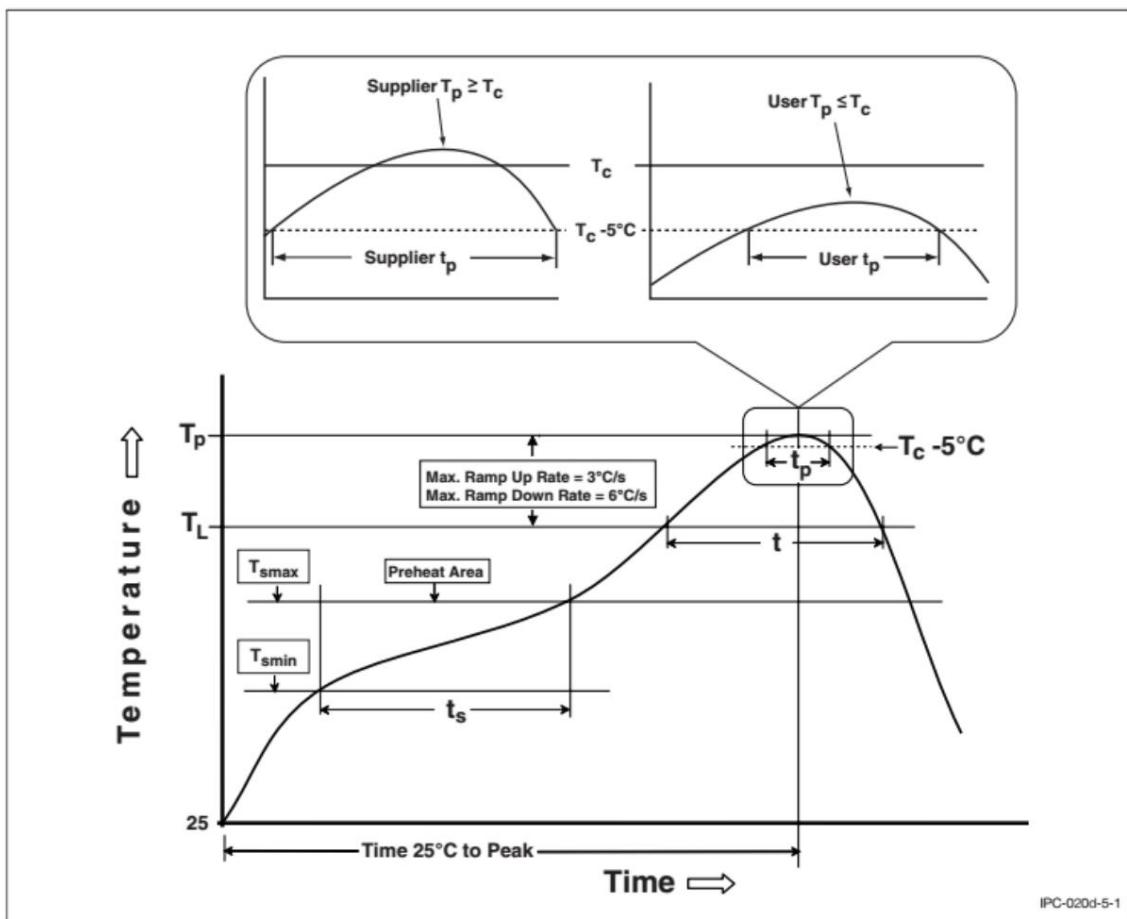


Figure 6-3 Lead-free reflow soldering process curve

6.3.3 SMT Recommended Curve

The SMT curve recommended by our company is shown in Figure 6-4:

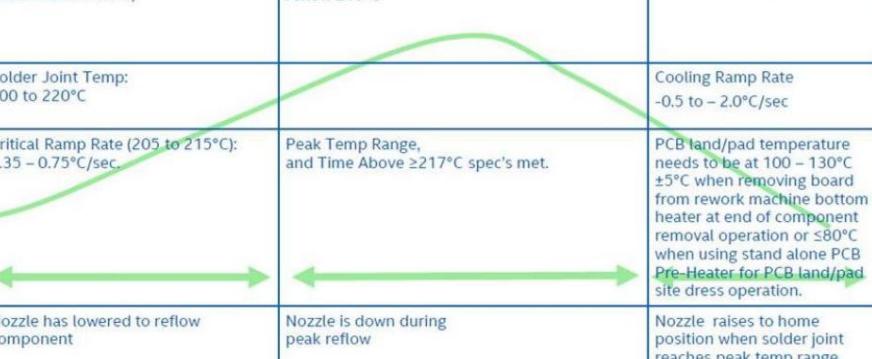
Step 1 Board Preheat	Step 2 Soak Time	Step 3 Peak Reflow & Time Above 220 °C	Step 4 Cool Down
Start with solder joint temp $\leq 40^{\circ}\text{C}$	After nozzle is lowered prior to peak reflow (Soak Time: Paste dependant; consult paste manufacturer)	Solder Joint Temp 230 – 250°C Above $\geq 217^{\circ}\text{C}$ 60 – 90 sec Max delta-t of solder joint temperature at peak reflow $\leq 10^{\circ}\text{C}$	Substrate MAX Temperature $\leq 260^{\circ}\text{C}$ Die Peak Temperature $\leq 300^{\circ}\text{C}$
Rising Ramp Rate 0.5 – 2.5° C/ Sec.	Solder Joint Temp: 200 to 220°C		Cooling Ramp Rate -0.5 to – 2.0° C/sec
Board Preheat Solder Joint Temp: 125 – 150°C	Critical Ramp Rate (205 to 215°C): 0.35 – 0.75°C/sec.	Peak Temp Range, and Time Above $\geq 217^{\circ}\text{C}$ spec's met.	PCB land/pad temperature needs to be at 100 – 130°C $\pm 5^{\circ}\text{C}$ when removing board from rework machine bottom heater at end of component removal operation or $\leq 80^{\circ}\text{C}$ when using stand alone PCB Pre-Heater for PCB land/pad site dress operation.
Preheat with bottom heater, before nozzle is lowered	Nozzle has lowered to reflow component	Nozzle is down during peak reflow	Nozzle raises to home position when solder joint reaches peak temp range

Figure 6-4 Recommended curve parameters for lead-free reflow soldering process

7 Packaging and storage conditions

7.1 Overview

The storage and use specifications of RK3588 are specified to ensure the safe and correct use of the product.

7.2 Explanation of terms

The terms in this chapter are explained as follows:

ÿ Desiccant: A material used to absorb moisture; ÿ Floor life: The maximum time a product is allowed to be exposed to the environment, from the time it is unpacked from the moisture-proof packaging to before reflow soldering; ÿ Humidity Indicator Card (HIC): Humidity Indicator Card; ÿ Moisture Sensitivity Level (MSL): Moisture Sensitivity Level; ÿ Moisture Barrier Bag (MBB): Moisture Barrier Bag; ÿ Rebake: Rebake; ÿ Solder Reflow: reflow soldering; ÿ Shell Life: storage period; ÿ Storage environment: Storage environment.

7.3 Moisture-proof packaging

The dry vacuum packaging materials of the product are as follows:

ÿ Desiccant;
ÿ Six-point humidity card;
ÿ Moisture-barrier bag, aluminum foil, silver opaque, with moisture-sensitive level logo.



Figure 7-1 Chip drying and vacuum packaging

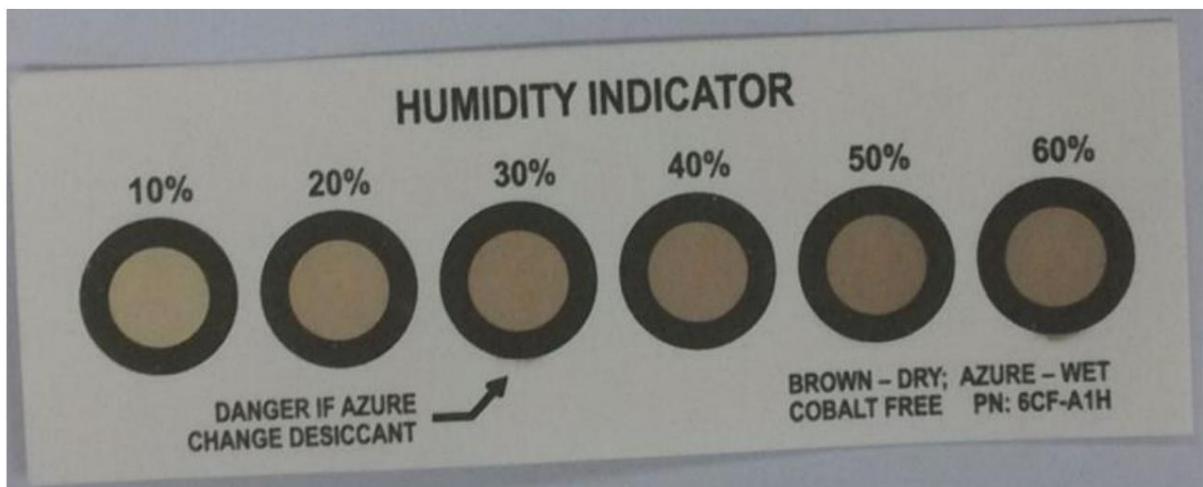


Figure 7-2 Six-point humidity card

7.4 Product Storage

7.4.1 Storage environment

The product is stored in vacuum packaging at a temperature of $\leq 40^{\circ}\text{C}$ and relative humidity of $\leq 90\%$, and the shelf life can reach 12 months.

7.4.2 Exposure time

Under environmental conditions of $\leq 30^{\circ}\text{C}$ and humidity 60%, please refer to the following Table 7-1.

The RK3588 chip has an MSL level of 3 and is very sensitive to humidity. If it is not used immediately after unpacking and is not baked after being left for a long time,

If the chip is not mounted, there is a high probability that the chip will fail.

Table 7-1 Exposure Time Reference Table (MSL)

MSL Level	Exposure time	
	Factory environmental conditions: 30 °C / 60 %RH	
1	Unlimited at 300 / 85 RH	
2	1 year	
2a	4 weeks	
3	168 hours	
4	72 hours	
5	48 hours	
5a	24 hours	
6	Mandatory bake before use and must be reflowed within the time limit specified on the label.	

7.5 Use of Moisture-sensitive Products

After the RK3588 chip packaging is opened, the following conditions must be met before the chip is reflowed:

Continuous or cumulative exposure time is within 168 hours, and the factory environment is 30/60% RH;

Stored in an environment with a RH lower than 10%;

In the following cases, the chip must be baked to remove internal moisture to avoid delamination or popcorn problems during reflow:

When the humidity indicator card is at 23±5, the point >10% has changed color. (Please refer to the humidity indicator card for color changes);

Failure to meet the requirements of 2a or 2b.

Please refer to the following table 7-2 for the chip re-bake time:

Table 7-2 RK3588 Re-bake Reference Table

Package Body	MSL	High Temp Bake @125±10/-0		Medium Temp Bake @90±8/-0		Low Temp Bake @40±5/-0	
		Exceeding Floor Life by > 72h	Exceeding Floor Life by 72h	Exceeding Floor Life by > 72h	Exceeding Floor Life by 72h	Exceeding Floor Life by > 72h	Exceeding Floor Life by 72h
Thickness ≥1.4mm	3	9 hours	7 hours	33 hours	23 hours	13 days	9 days



Notice

The table shows the minimum baking time required after moisture exposure. Low temperature baking is preferred for re-baking.

