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LAB-2

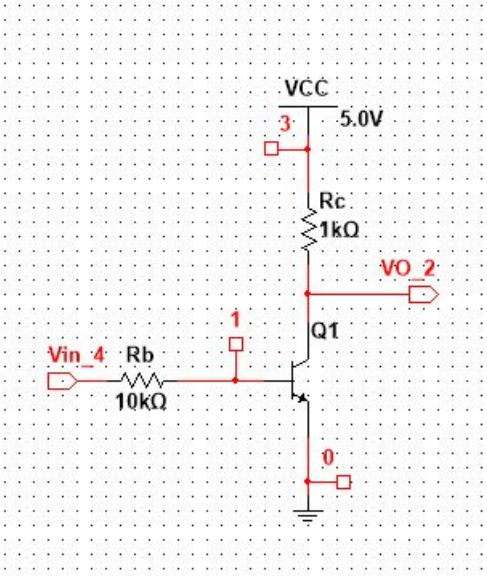
AIM: Implement RTL inverter using NPN BJT having BF=50, Rb= 10k, Rc= 1k, Vcc= 5V. Verify its functionality. Perform static and transient analysis and plot the VTC characteristics and transient response.
Calculate the theoretical and practical fanout and compare them.

Assignment 1: Repeat the above for TTL inverter logic.

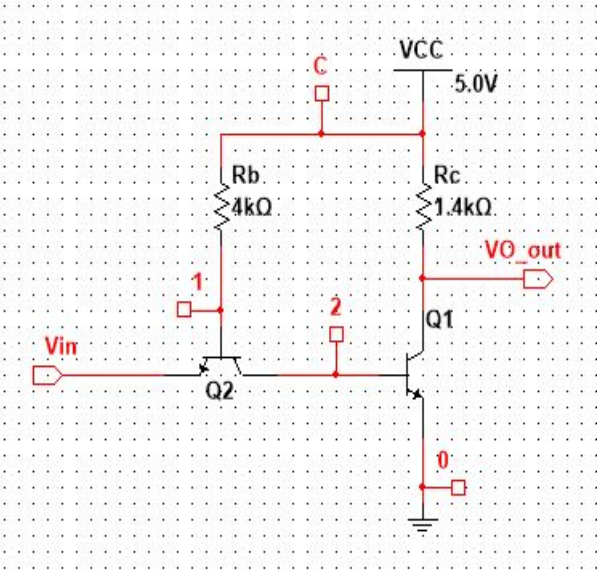
Theory:

This is an inverter implemented with the resistor- transistor logic, the earliest form of logic implemented by transistors. When the input is high (VCC), current flows from the base to the emitter. The transistor wants the collector-emitter current to be ☐ times the base current, but it can't, because the collector is connected to the same voltage through a larger resistor. So, the transistor is in saturation mode; it gets the collector voltage down to the saturation voltage. When the input is low (at ground), no current flows through the base, so the transistor is off, and the collector stays at VCC.

Circuit diagram:



RTL inverter using npn BJT

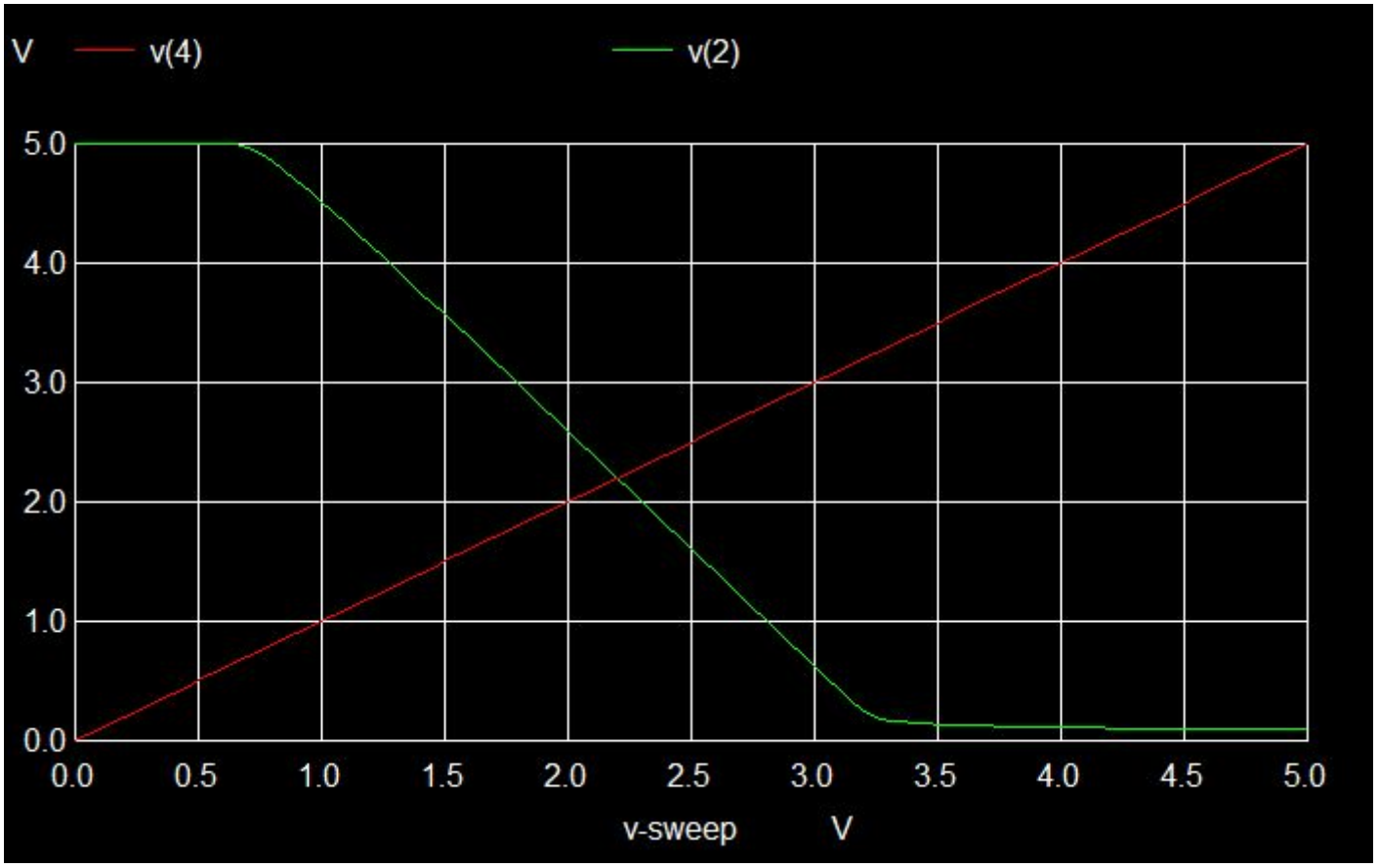


TTL inverter using npn BJT

RTL Inverter static analysis

```
*rtl inverter static analysis*
.model q1 npn BF=20
q11 2 1 0 q1
rc 2 3 1k
rb 4 1 10k
```

```
vcc 3 0 5
vin 4 0 5

.dc vin 0 5 0.05
.control
run
plot v(2) v(4)
.endc
.end
```



Calculation:

Vth= 2.2V

VOH= 5V

VOL= 140 mV

VIH=3.3V

VIL=0.8V

NMH= VOH-VIH= 1.7V

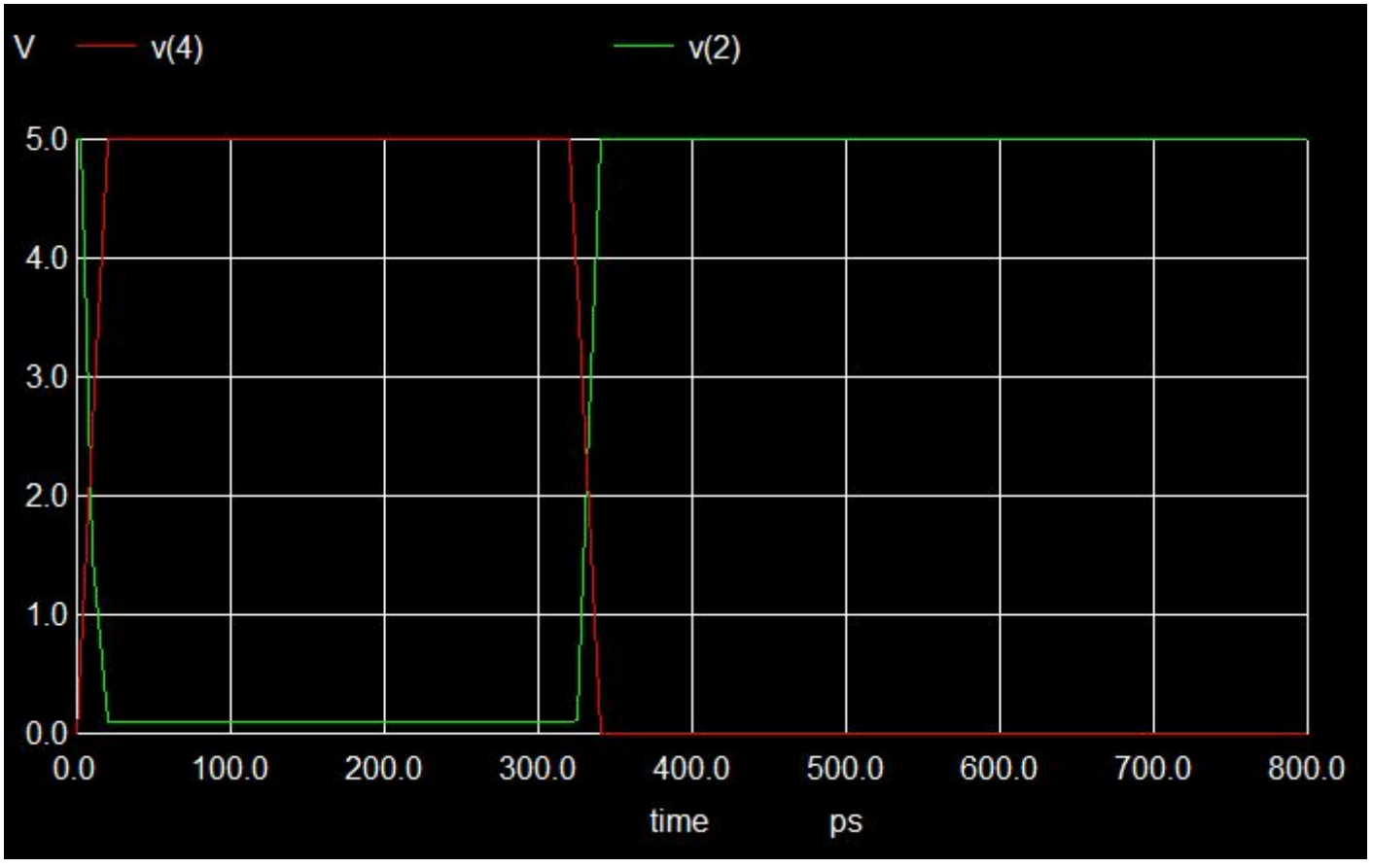
NML= VOL-VIL= 0.66V

Noise Margin= max (NMH, NML)= 1.7V

RTL Inverter transient analysis

Code:

```
*rtl inverter transient analysis*
.model q1 npn BF=20
q11 2 1 0 q1
rc 2 3 1k
rb 4 1 10k
vcc 3 0 5
vin 4 0 pulse(0 5 0ps 0ps 0ps 300ps 1000ps)
.tran 20ps 800ps
.control
run
plot v(2) v(4)
.endc
.end
```



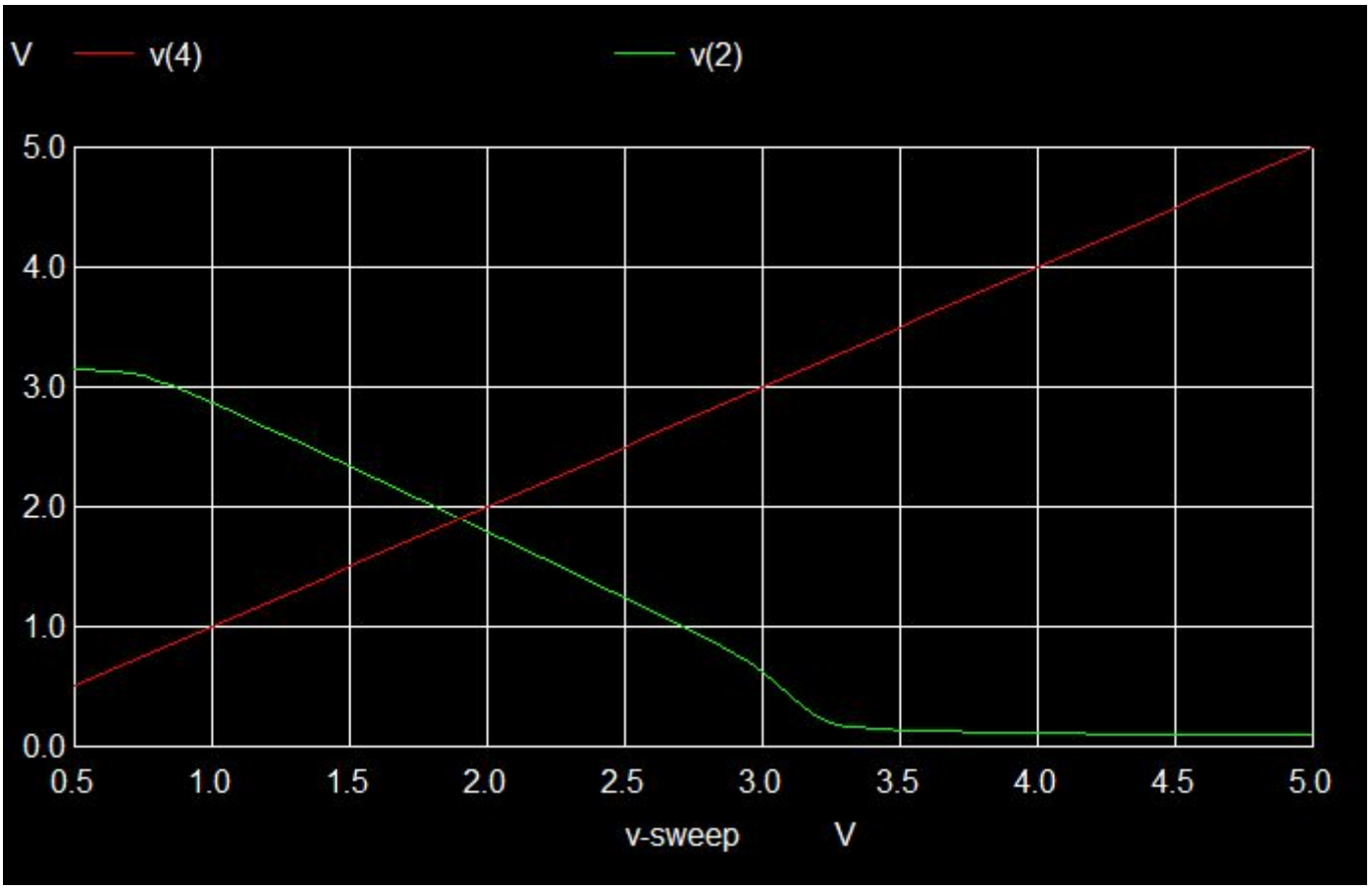
Calculation:

Tphl=1.8 ps
Tplh= 2ps
Tp= (Tphl+ Tplh)/2= 1.9ps

RTL Inverter Fan-out

Code:

```
.model q1 npn BF=20
q11 2 1 0 q1
rc 2 3 1k
rb 4 1 10k
vcc 3 0 5
vin 4 0 5

.subckt rtl out in c 0
q2 out y 0 q1
rb1 in y 10k
rc1 c out 1k
.ends rtl

x1 3 2 0 out1 rtl
x2 3 2 0 out2 rtl
x3 3 2 0 out3 rtl
x4 3 2 0 out4 rtl
x5 3 2 0 out5 rtl
x6 3 2 0 out6 rtl
x7 3 2 0 out7 rtl
x8 3 2 0 out8 rtl

.dc vin 0.5 5 0.05
.control
run
plot v(2) v(4)
.endc
.end
```



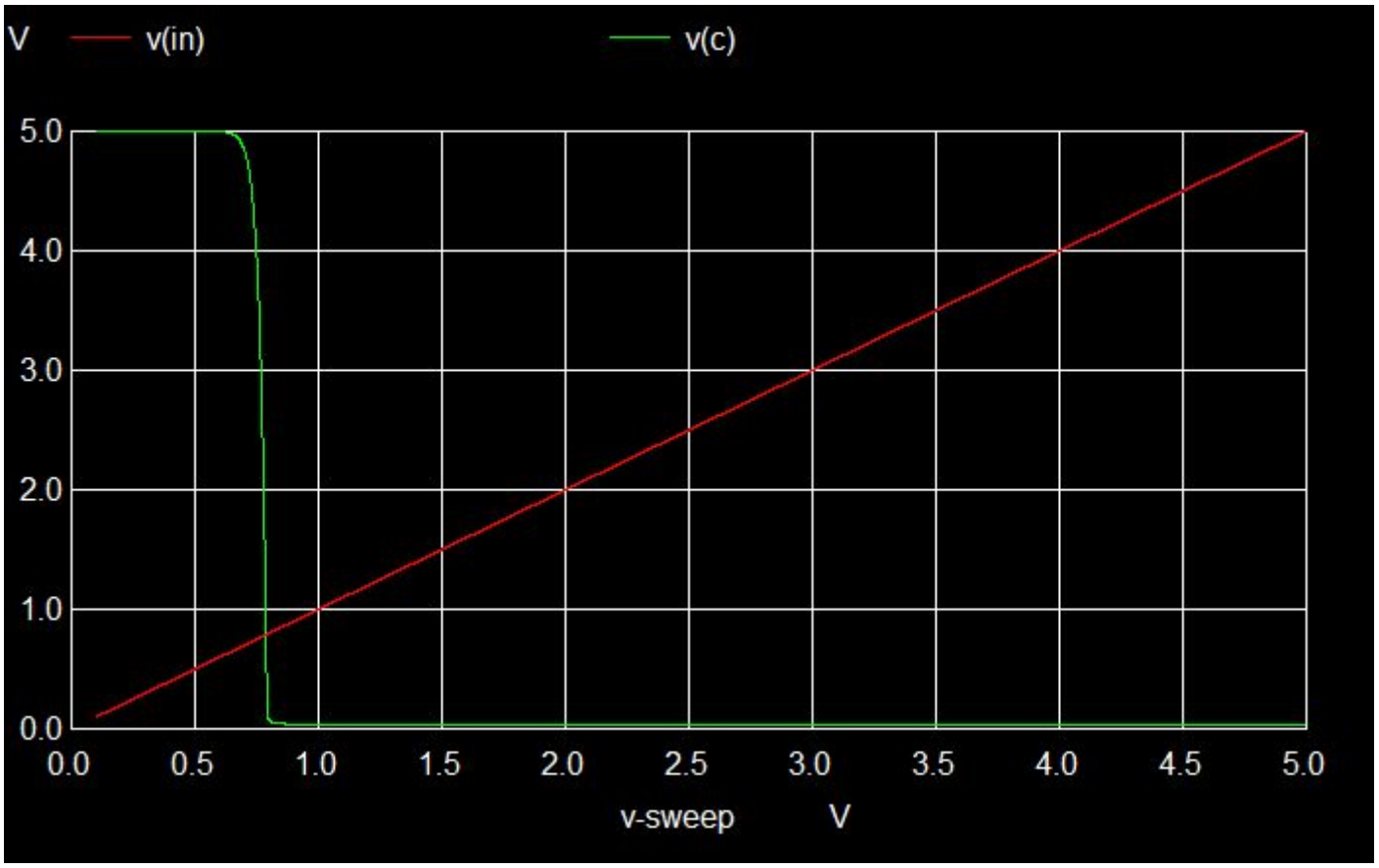
Calculations:
At 8th sub-circuit, VOH = VIH
Therefore, fanout= 8.

Assignment 1:

TTL inverter static analysis

Code:

```
**ttl inverter static***
.model q1 npn BF=20
q10 c 3 0 q1
q11 3 2 in q1
rc 1 c 1.4k
rb 1 2 4k
vcc 1 0 5

vin in 0 5
.dc vin 0.1 5 0.001
.control
run
plot v(c) v(in)
.endc
.end
```



Calculations:

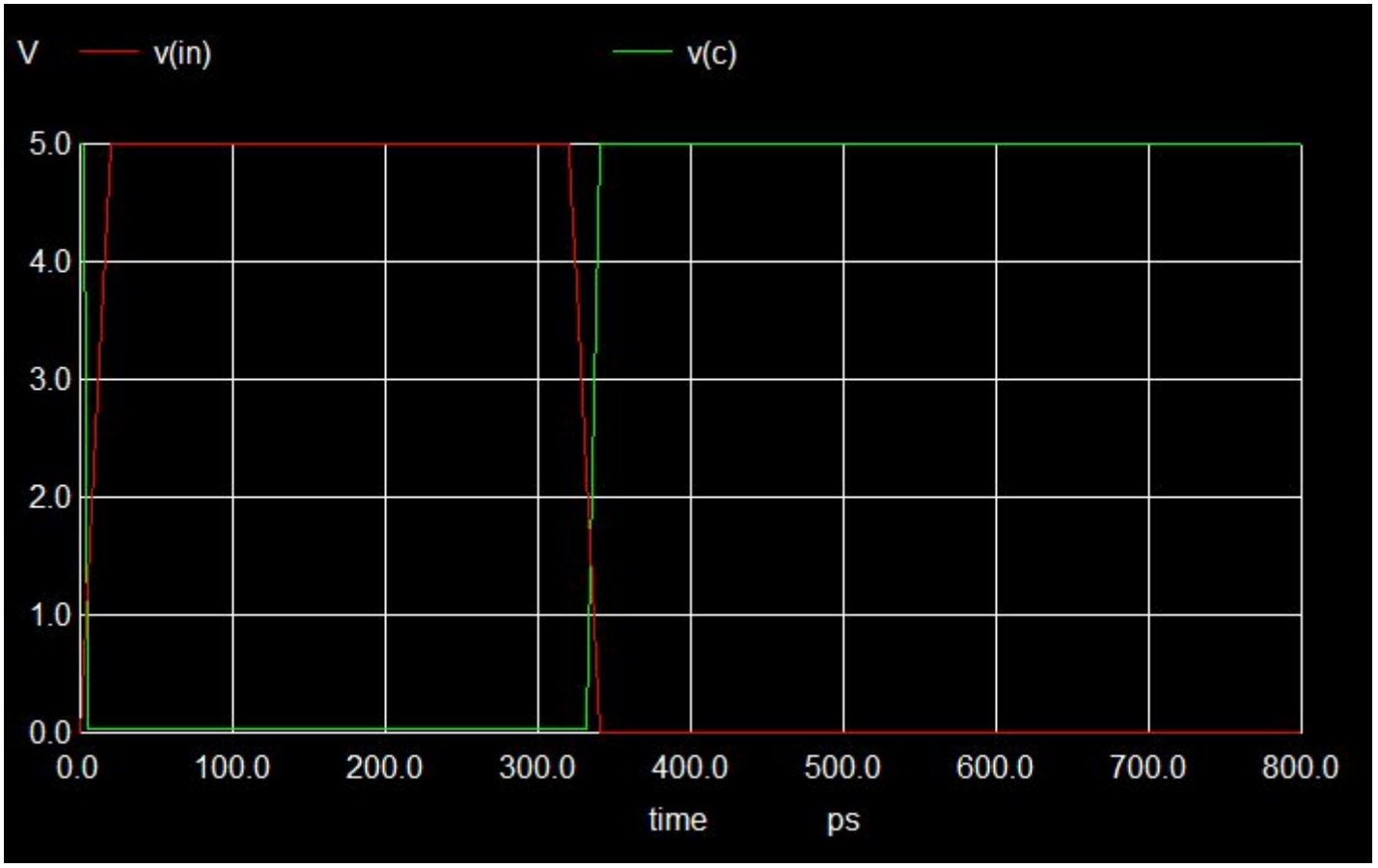
VOH= 5V
VOL=60mV
VIH= 790 mV
VIL= 720mV
NMH= VOH-VIH= 4.21V
NML= VIH-VIL= 660 mV
Noise Margin = max(NMH,NML)= 4.21V

TTL Inverter transient analysis

Code:

```
**ttl inverter transient***

.model q1 npn BF=20
q10 c 3 0 q1
q11 3 2 in q1
rc 1 c 1.4k
rb 1 2 4k
vcc 1 0 5

vin in 0 pulse(0 5 0ps 0ps 0ps 300ps 1000ps)
.tran 20ps 800ps
.control
run
```

```
plot v(c) v(in)
.endc
.end
```



Calculation:

Tphl= 7ps

Tplh=7.5ps

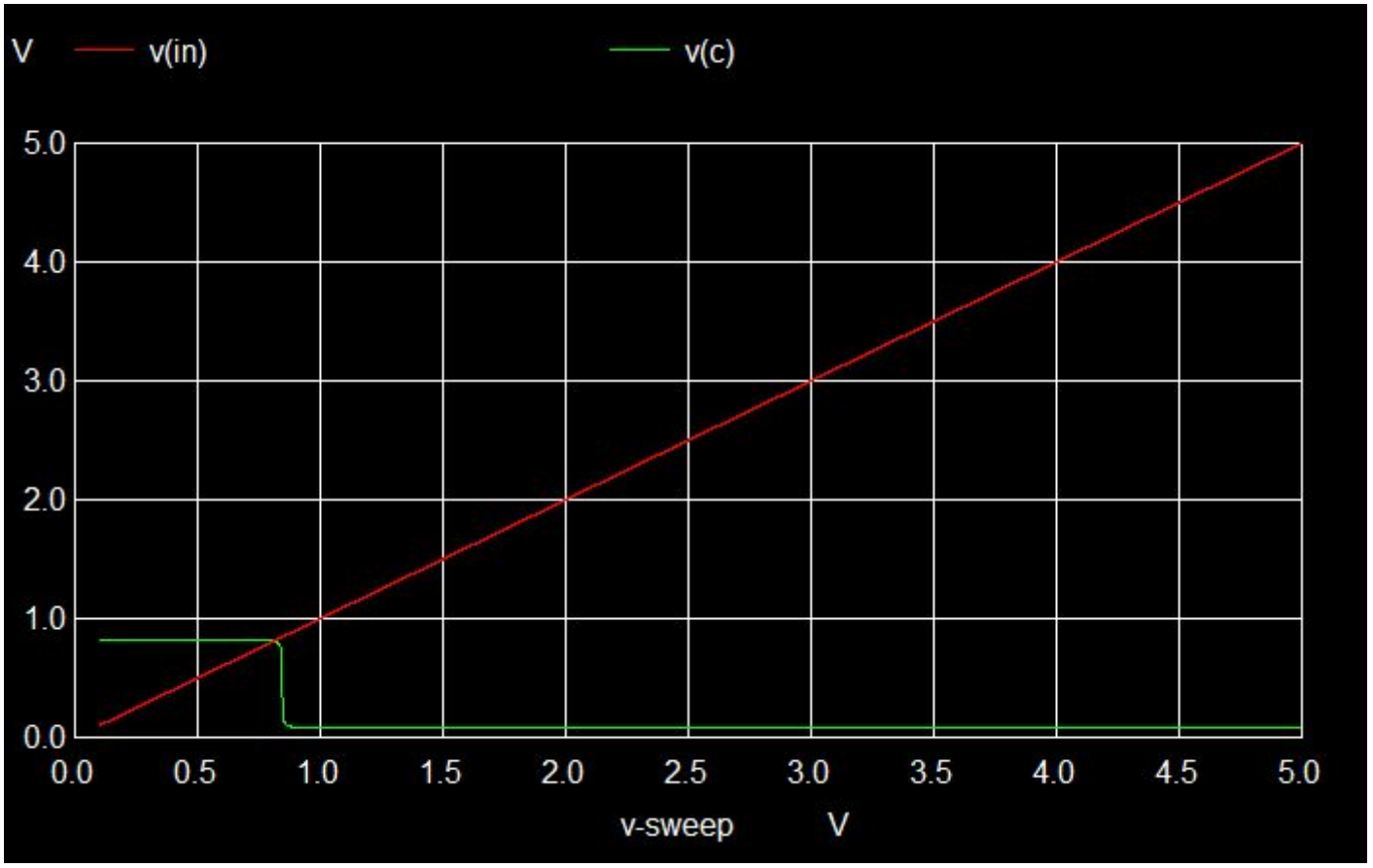
Propagation time= 7.25 ps

TTL inverter Fan-out

Code:

```
**ttl inverter fan out***

.model q1 npn BF=20
q10 c 3 0 q1
q11 3 2 in q1
rc 1 c 1.4k
rb 1 2 4k
vcc 1 0 5
vin in 0 5

.subckt ttl v in1 0 out
q20 out 3a 0 q1
q21 3a 2a in1 q1
```

```
rcc v out 1.4k
rbb v 2a 4k
.ends ttl

x1 1 c 0 out1 ttl
x2 1 c 0 out2 ttl
x3 1 c 0 out3 ttl
x4 1 c 0 out4 ttl
x5 1 c 0 out5 ttl
x6 1 c 0 out6 ttl
x7 1 c 0 out7 ttl
x8 1 c 0 out8 ttl
x9 1 c 0 out9 ttl
x10 1 c 0 out10 ttl
x11 1 c 0 out11 ttl
x12 1 c 0 out12 ttl
x13 1 c 0 out13 ttl
*x14 1 c 0 out14 ttl

.dc vin 0.1 5 0.001
.control
run
plot v(c) v(in)
.endc
.end
```



Calculation:

At 13^{th} subcircuit, VOH = VIH
Therefore, fanout =13

RESULTS:

Parameters	**TTL**	**RTL**
Propagation delay	7.25ps	1.9 ps
Noise margin	4.21 V	1.7V
Fan out	13	8

Conclusion: In the above experiment and simulation we verified inverter functionality Using RTL and TTL logic.