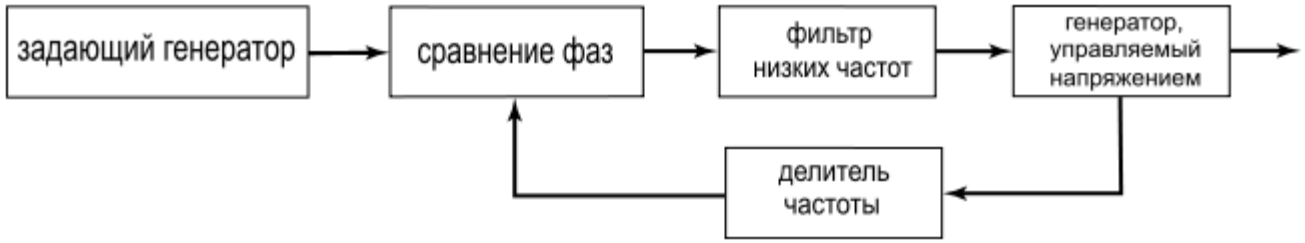
PLL

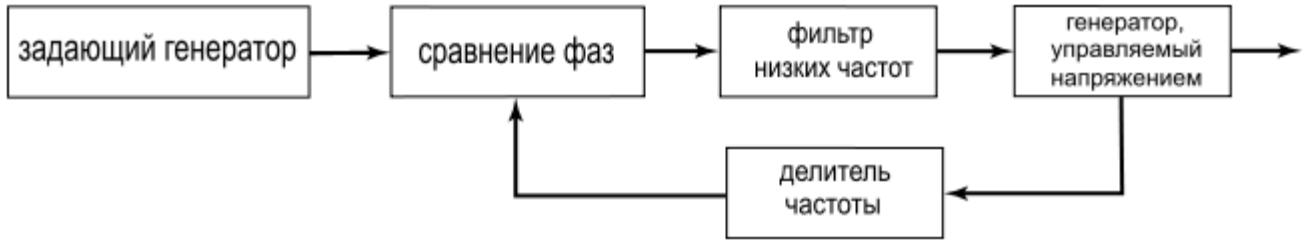
Использование

- Определение фазы сигнала
- Модуляция
- Генераторы
- Внутреннее распределение синхросигналов
- Clock gating



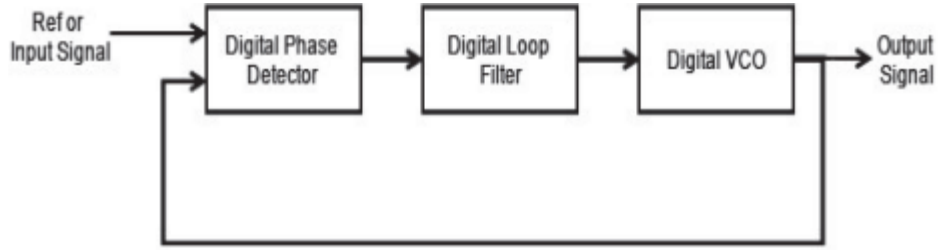
Структура

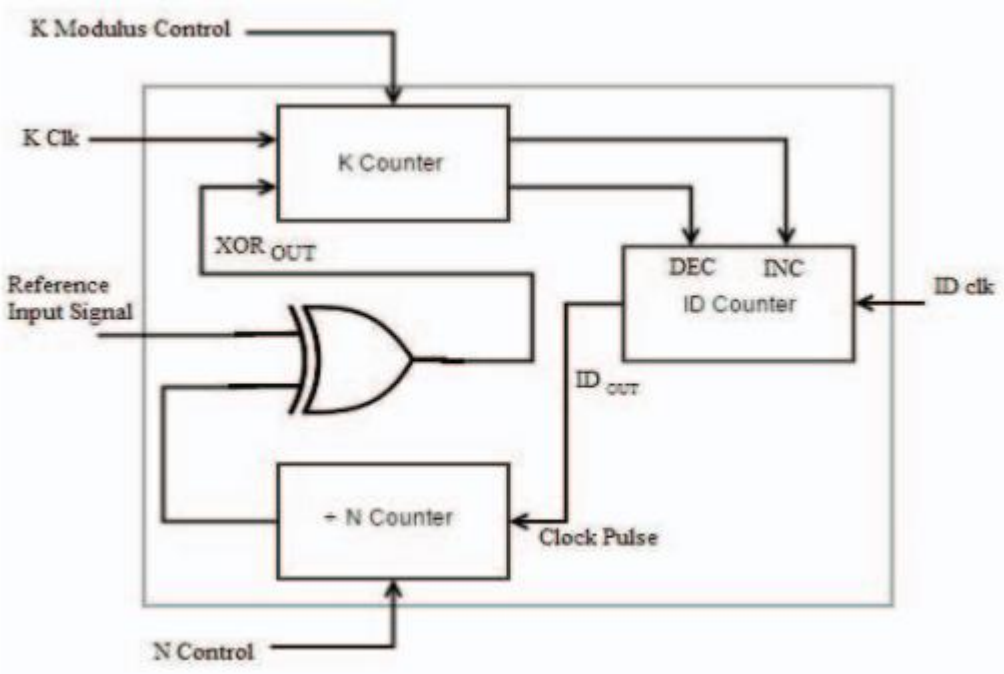
- Фазовый детектор
- Петлевой фильтр
- ГУН
- Делитель частоты



ADPLL

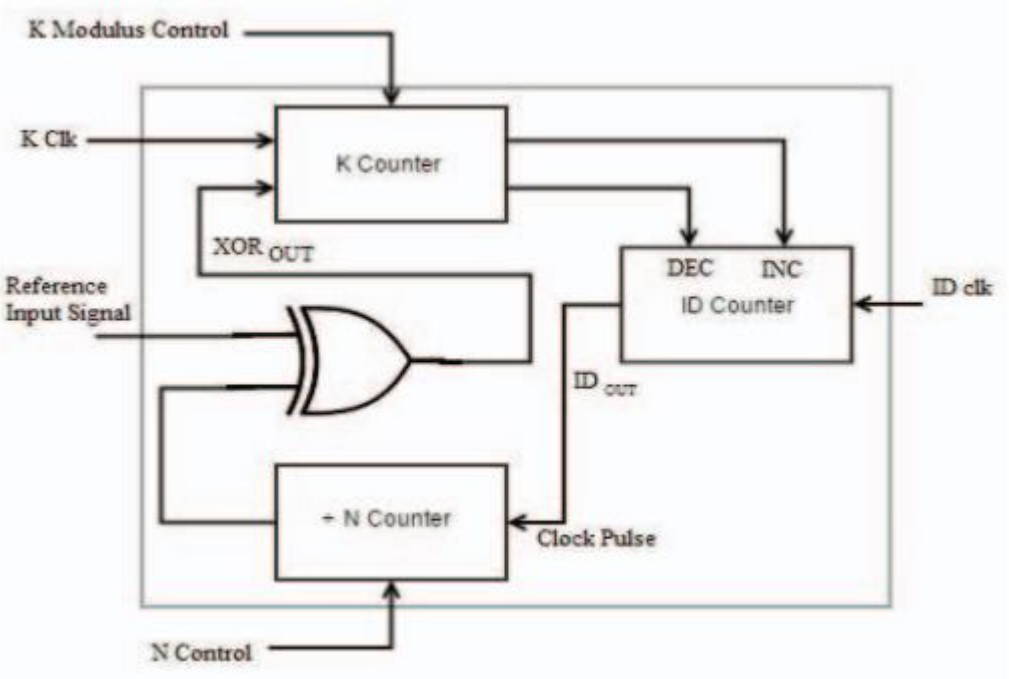
- Design of Power Efficient All Digital Phase Locked Loop (ADPLL)

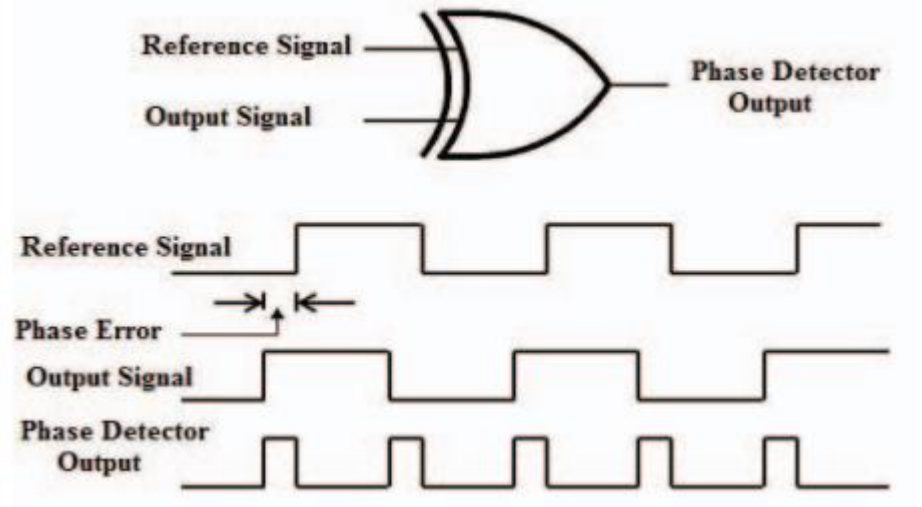




ADPLL

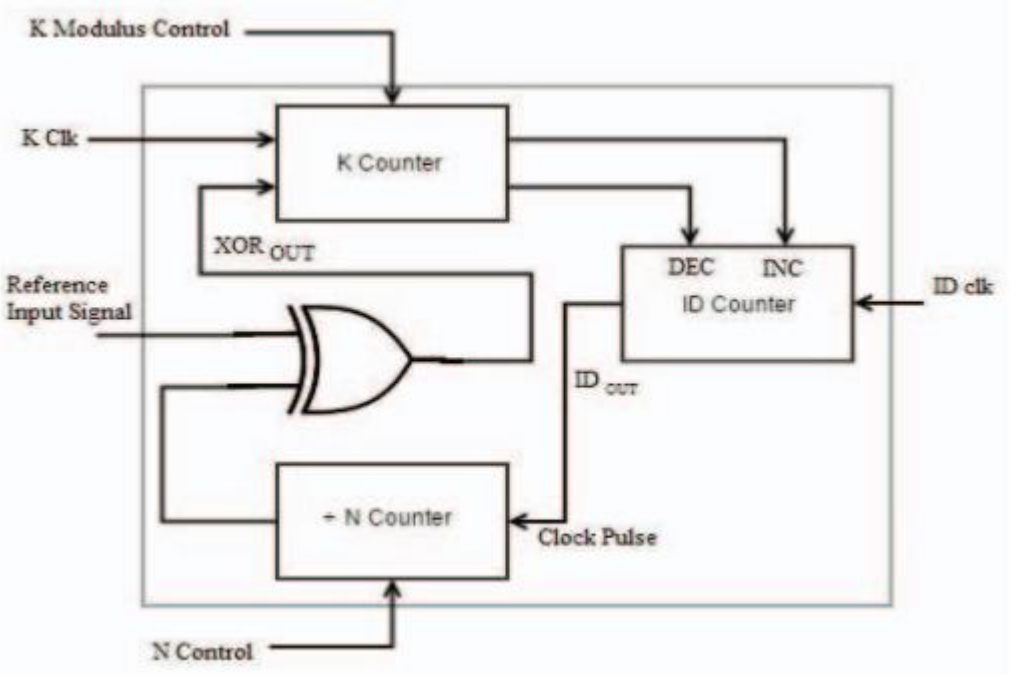
- Фазовый детектор

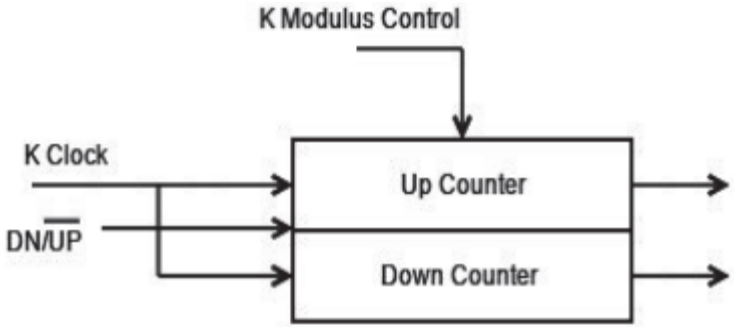


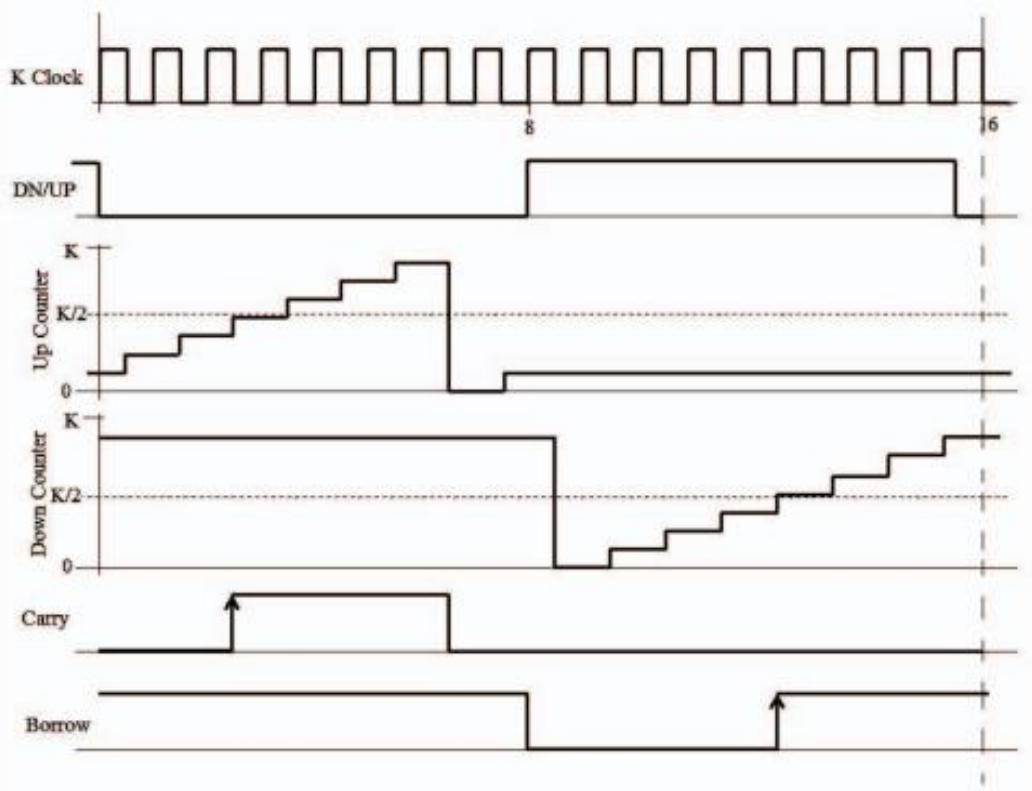


ADPLL

- Петлевой фильтр

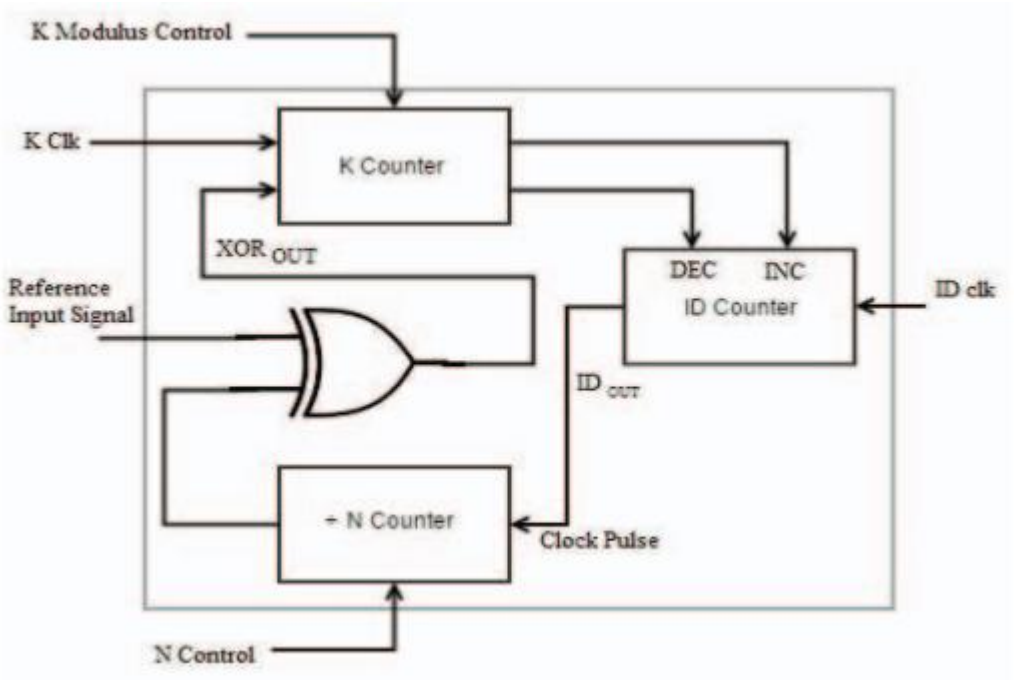


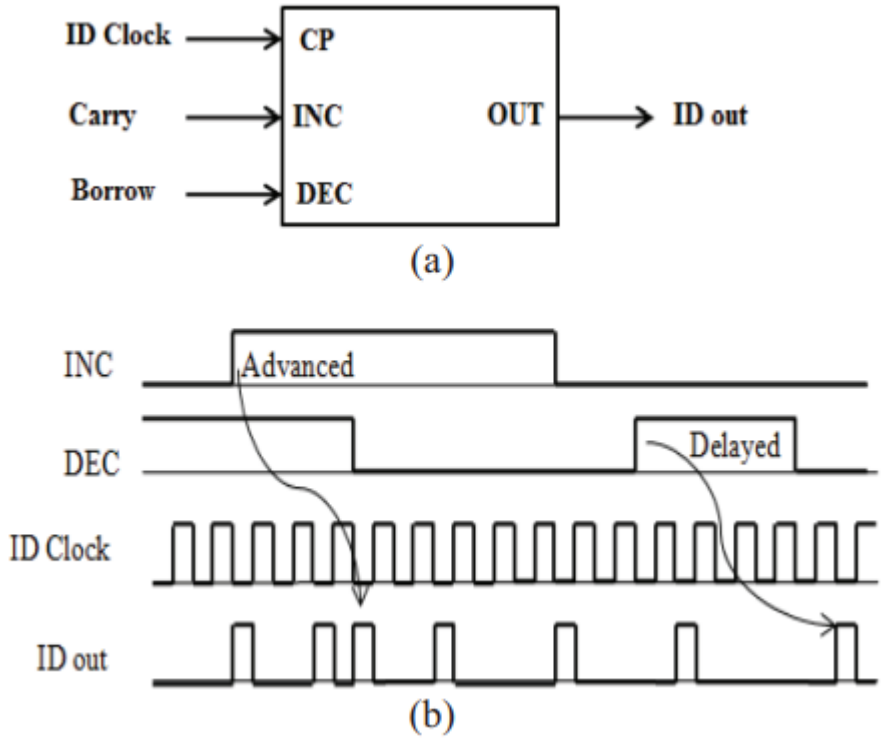




ADPLL

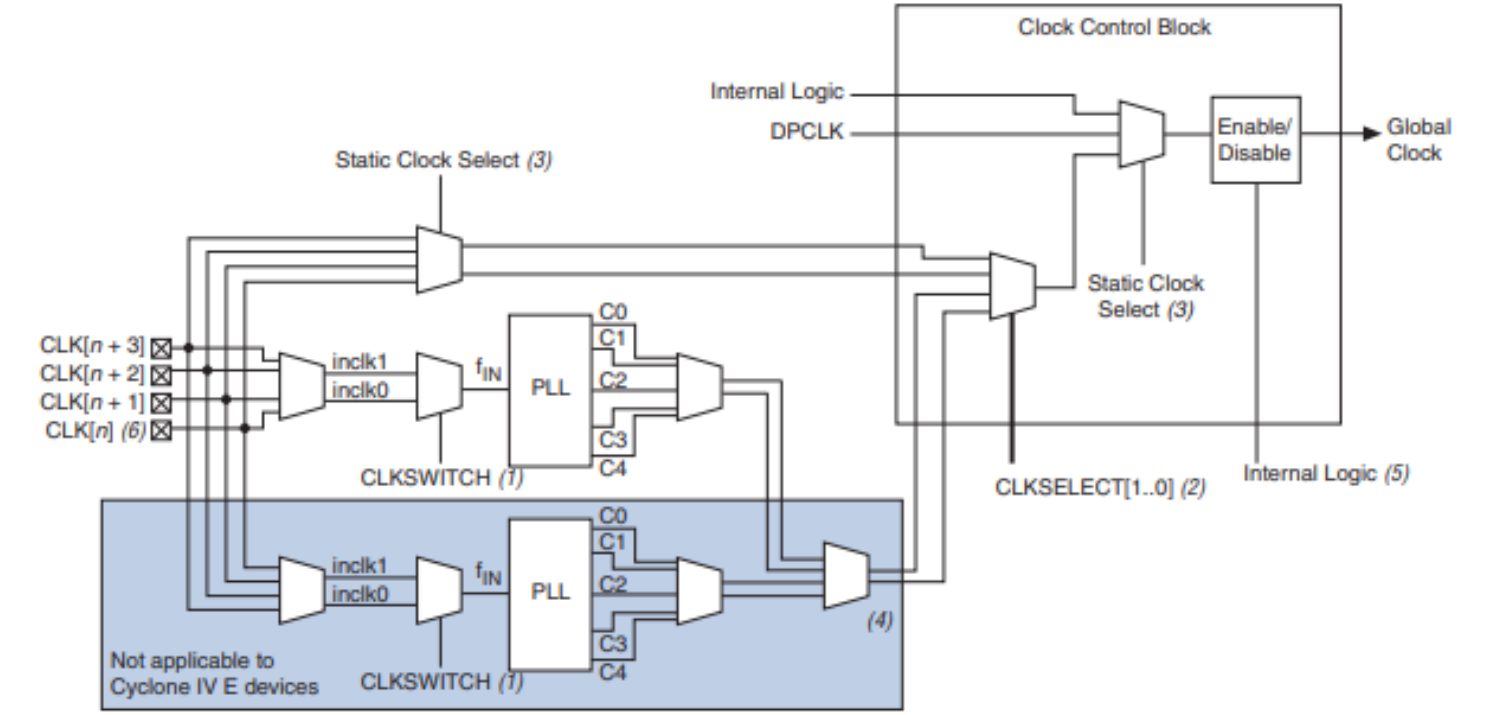
- DCO


K Modulus Control
K Clk
K Counter
XOR OUT
Reference
Input Signal
DEC
INC
ID Counter
ID clk
ID OUT
÷ N Counter
Clock Pulse
N Control


ID Clock
Carry
Borrow
CP
INC
DEC
OUT
ID out
(a)
INC
DEC
ID Clock
ID out
Advanced
Delayed
(b)

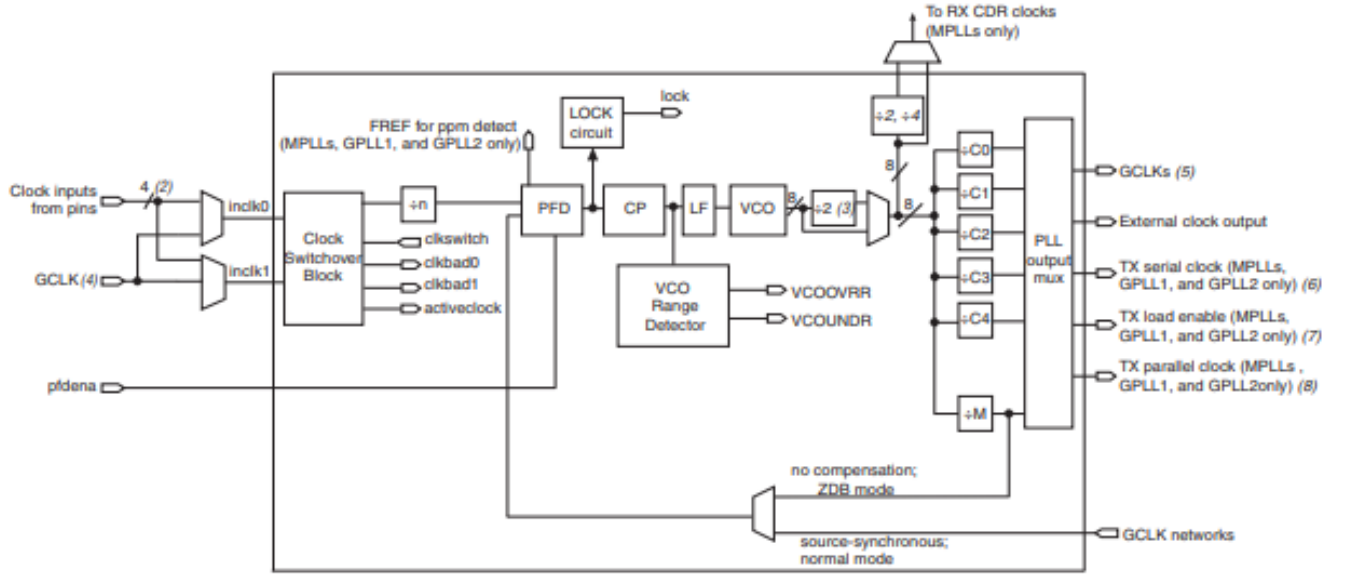
PLL CYCLONE IV

Figure 5–1. Clock Control Block

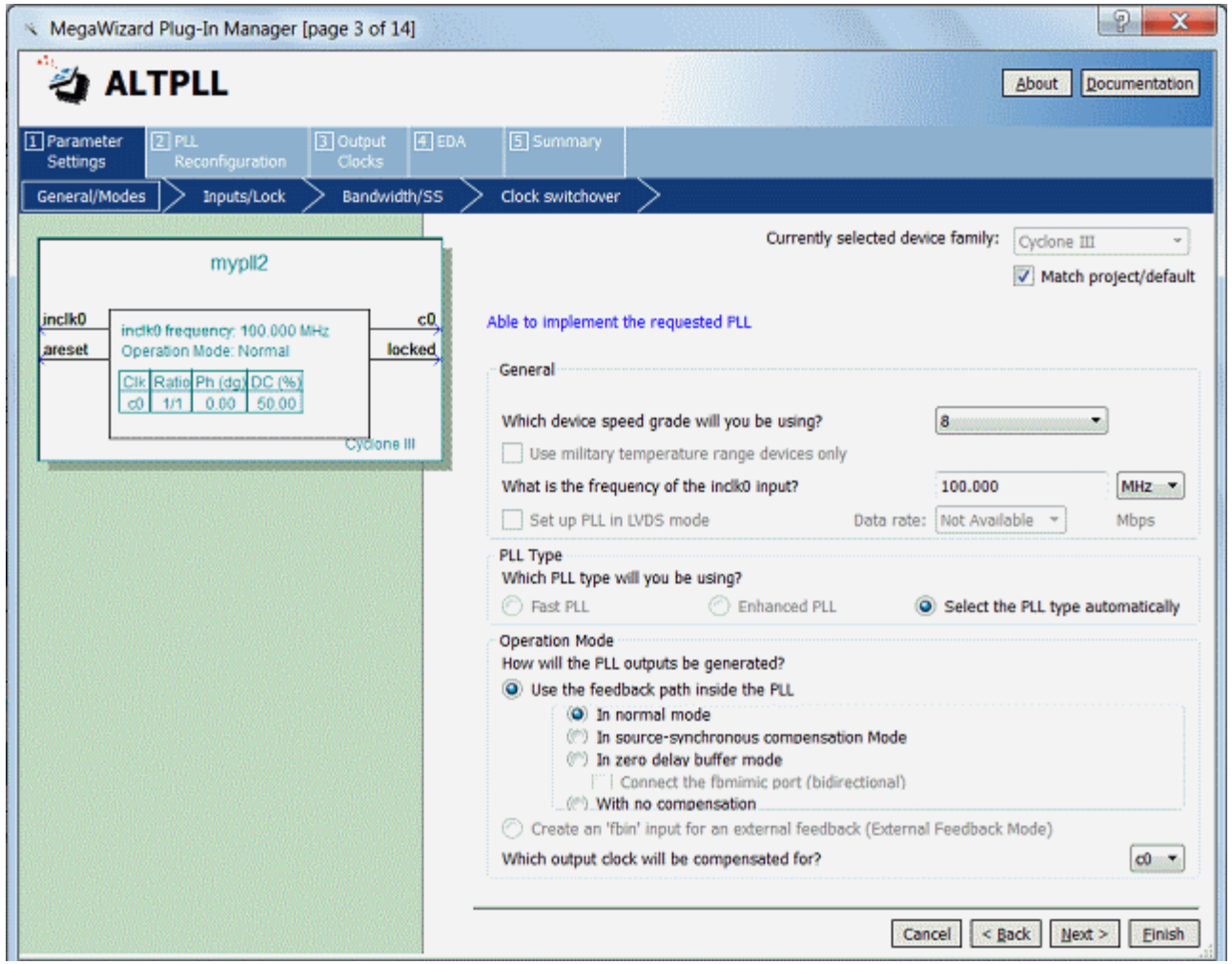


PLL CYCLONE IV

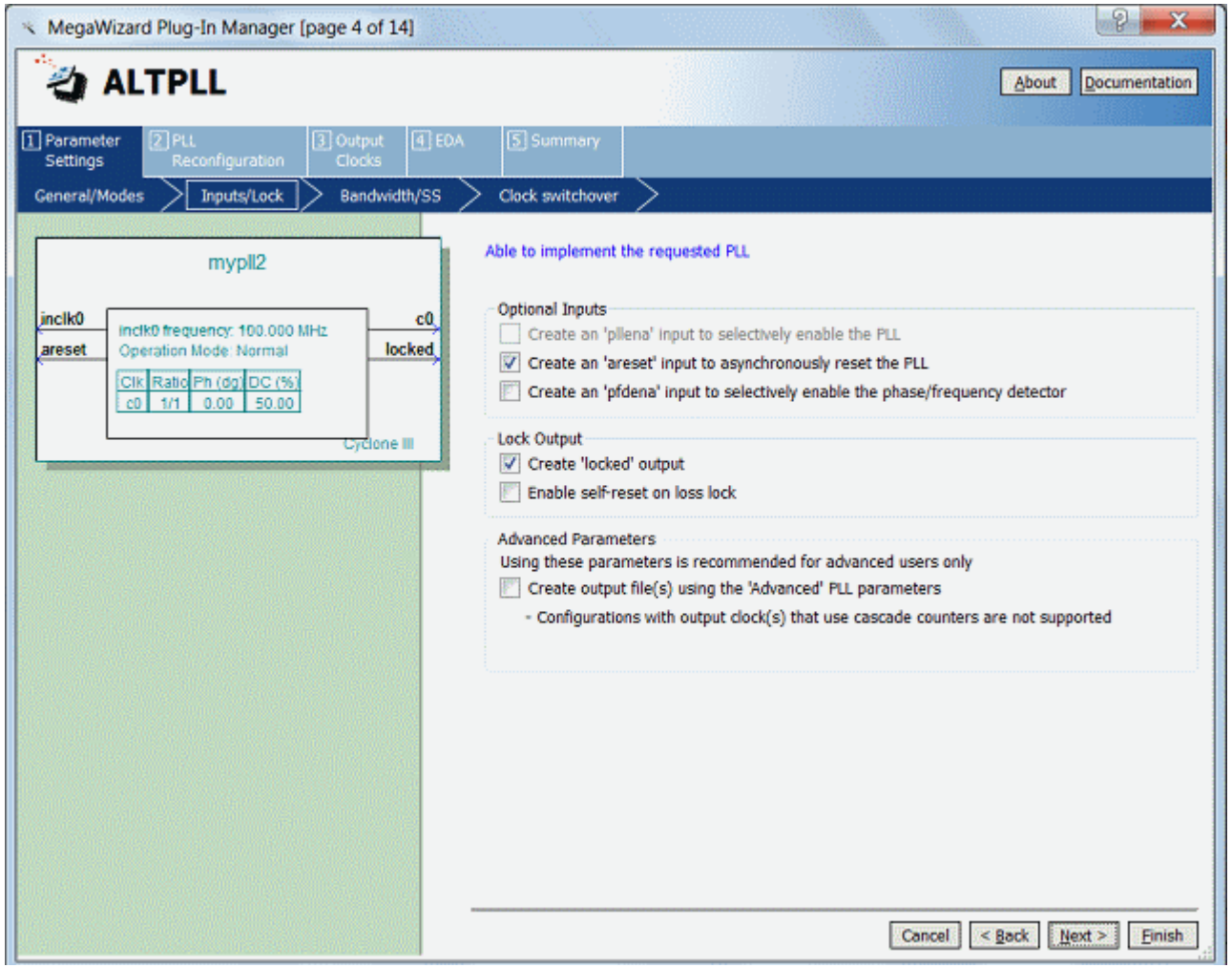
Figure 5–9. Cyclone IV GX PLL Block Diagram *(1)*



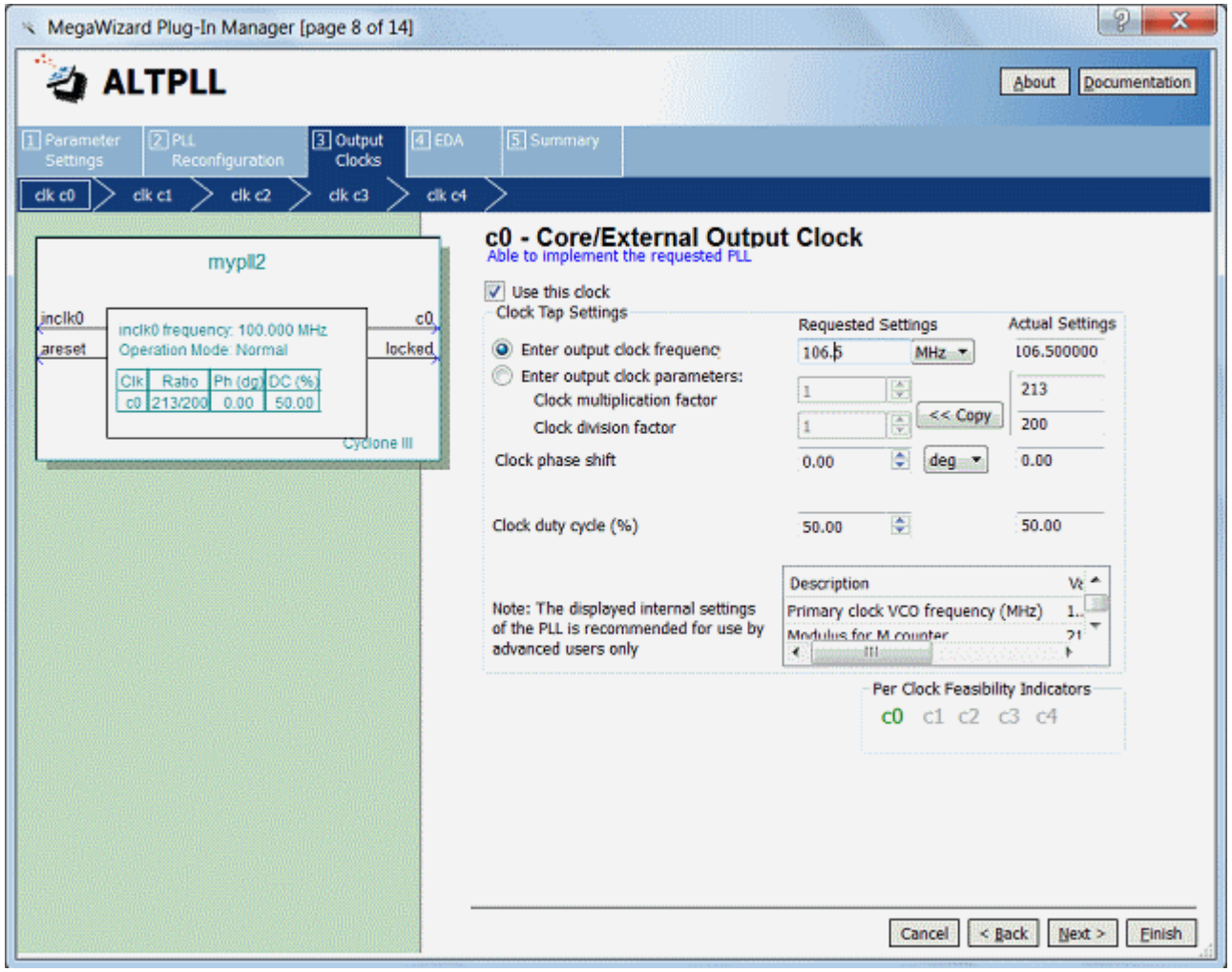
PLL CYCLONE IV



PLL CYCLONE IV



PLL CYCLONE IV



PLL CYCLONE IV