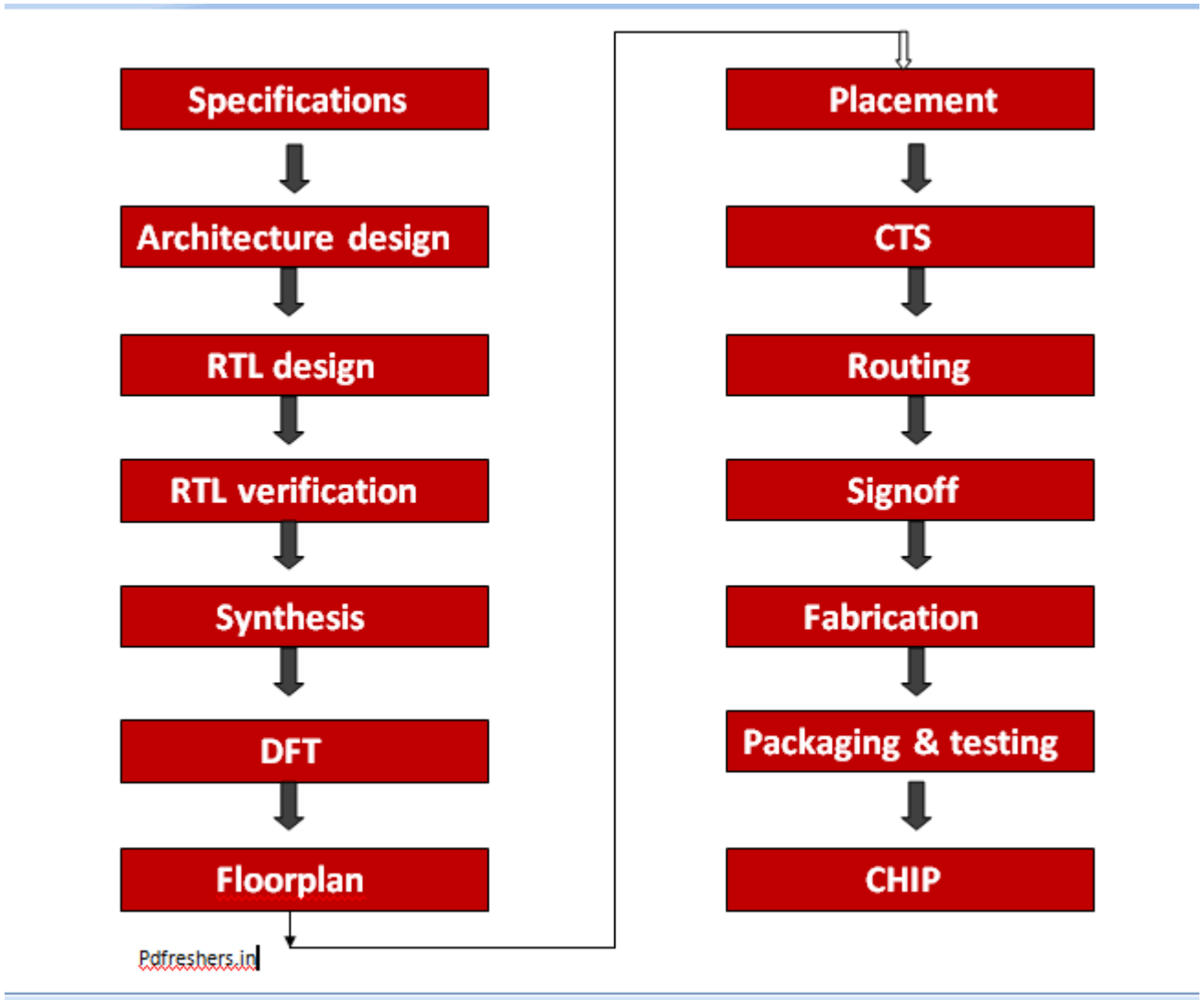
Маршруты проектирования, верификация, тестирование

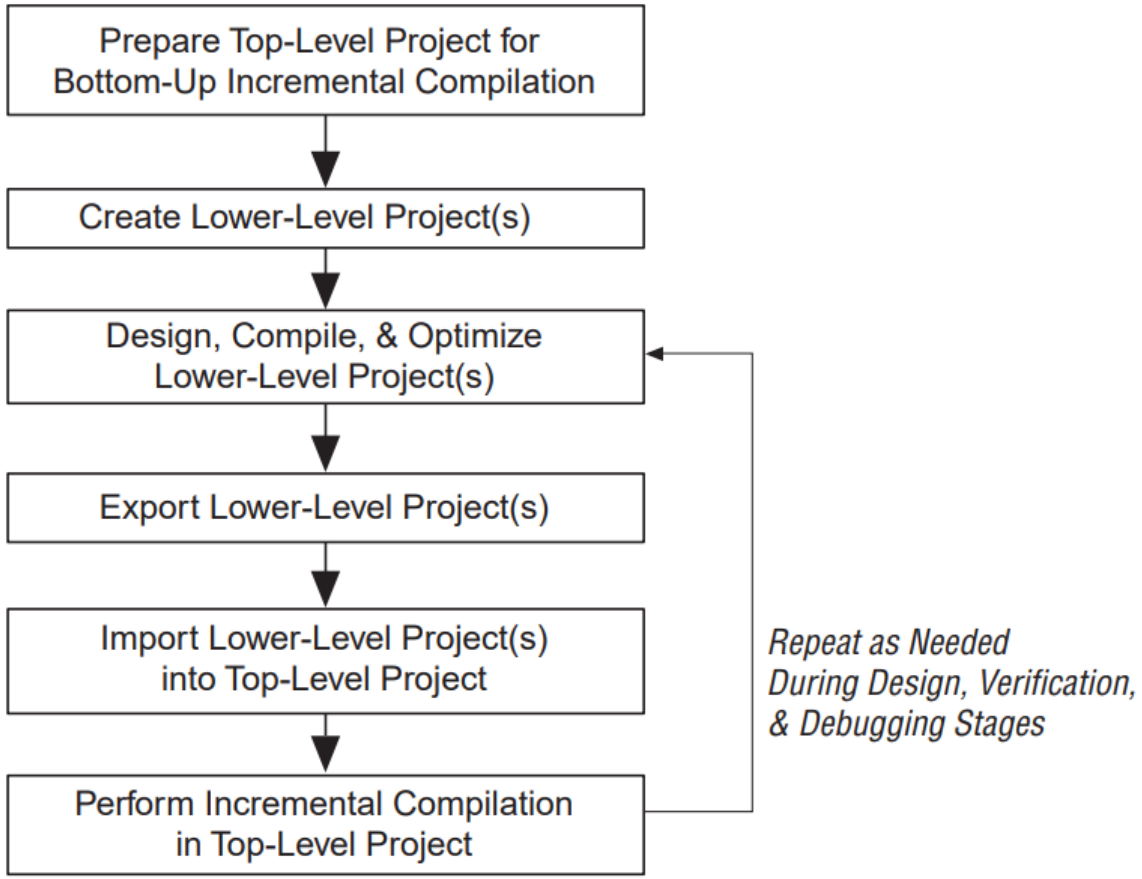
Маршрут проектирования

- Top-down
- Bottom-up



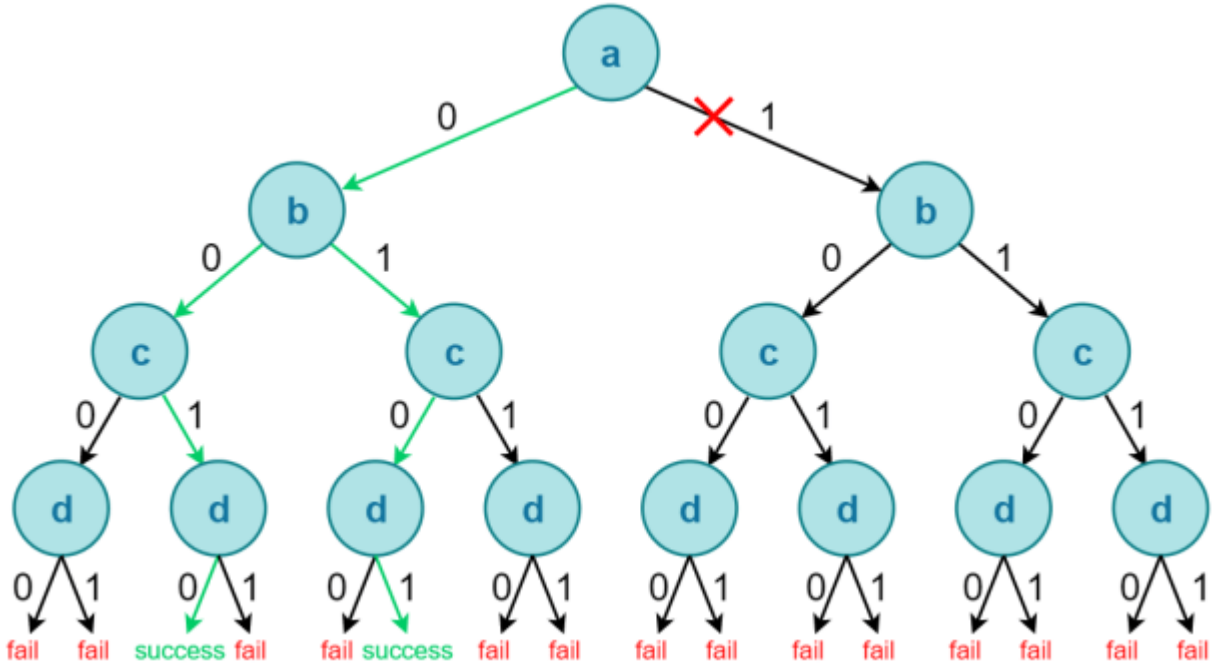
Bottom-up

Figure 2–12. Summary of Bottom-Up Incremental Compilation Flow

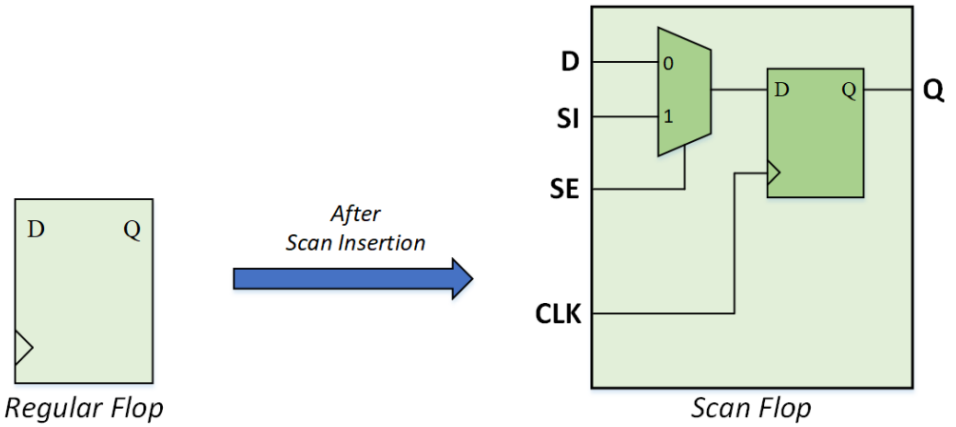


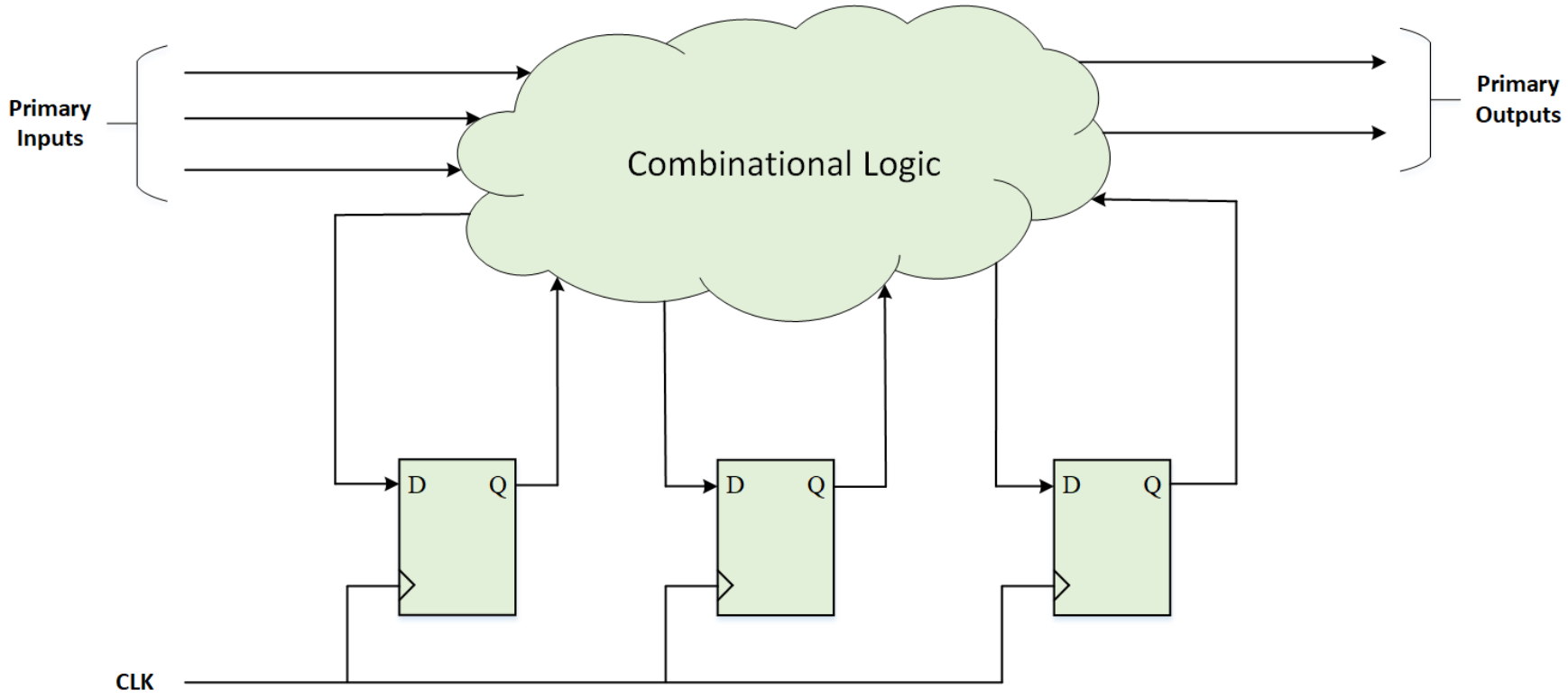
DFT

- ATPG
- Scan chains
- Boundary
- JTAG

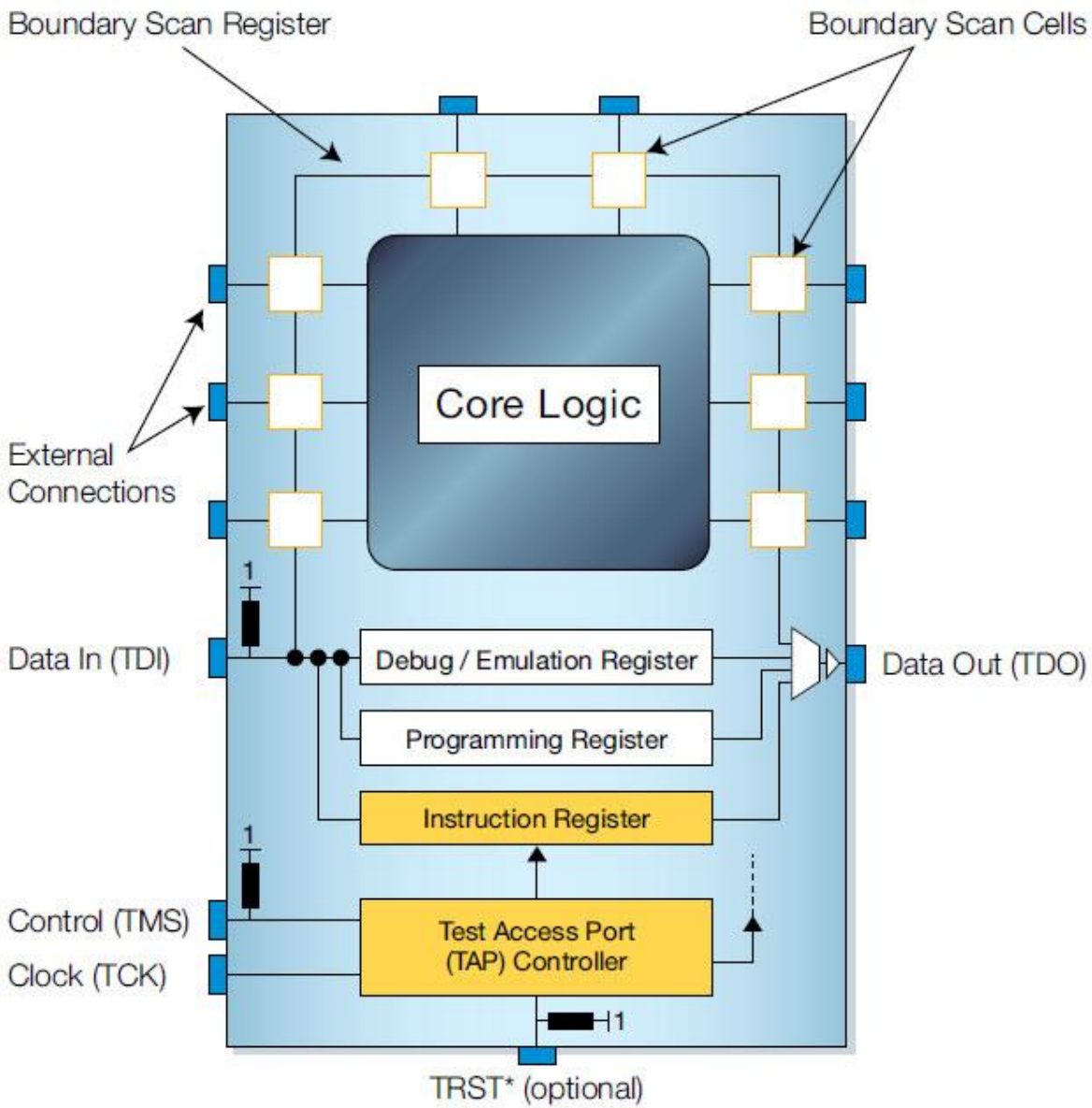


Scan chains


D
Q
Regular Flop
After
Scan Insertion
D
SI
SE
CLK
0
1
D
Q
Q
Scan Flop


Primary
Inputs
Combinational Logic
Primary
Outputs
D
Q
D
Q
D
Q
CLK

Boundary


Boundary Scan Register
Boundary Scan Cells
Core Logic
External
Connections
1
Data In (TDI)
Debug / Emulation Register
Data Out (TDO)
Programming Register
Instruction Register
1
Control (TMS)
Clock (TCK)
Test Access Port
(TAP) Controller
1
TRST* (optional)

Constraints

create_constraint_mode -name <NAME> -sdc_files <SDC_FILES>
set_case_analysis <VALUE> <PORTS>

Поведенческие модели

- Симуляция аналоговых блоков
- Симуляция внешних блоков
- Временные модели: симуляция временных параметров на уровне RTL

```
module behave;
reg [1:0]a,b;

initial
begin
   a = 'b1;
   b = 'b0;
end

always
begin
   #50 a = ~a;
end

always
begin
   #100 b = ~b;
end
End module
```

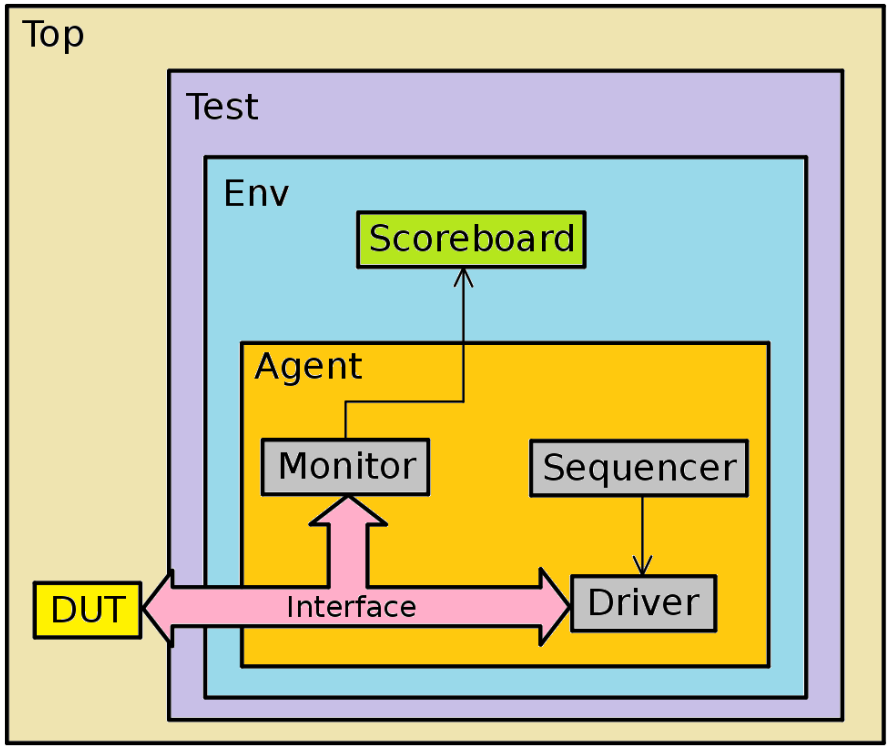
Временные модели

```
specify
    specparam tpd_CK_Q_posedge_r = 0.240558:0.544685:1.16364;
    specparam tpd_CK_Q_posedge_f = 0.226402:0.497838:0.99056;
    specparam tpd_CK_QN_posedge_r = 0.314371:0.600496:1.21156;
    specparam tpd_CK_QN_posedge_f = 0.320749:0.561028:1.02143;
    specparam tsetup_D_CK_posedge_posedge = 0.243168:0.490477:0.862879;
    specparam thold_D_CK_posedge_posedge = -0.01163:0.271283:0.592782;
    specparam tsetup_D_CK_negedge_posedge = 0.243168:0.490477:0.862879;
    specparam thold_D_CK_negedge_posedge = -0.01163:0.271283:0.592782;
    specparam tpw_CK_adacond_D_posedge = 0.138864:0.528814:1.50024;
    specparam tpw_CK_adacond_D_negedge = 0.138864:0.528814:1.50024;
    specparam tpw_CK_adacond_NOT_D_posedge = 0.199546:0.553530:1.50024;
    specparam tpw_CK_adacond_NOT_D_negedge = 0.199546:0.553530:1.50024;

    (posedge CK => (Q+:D)) = ( tpd_CK_Q_posedge_r , tpd_CK_Q_posedge_f );
    (posedge CK => (QN-:D)) = ( tpd_CK_QN_posedge_r , tpd_CK_QN_posedge_f );
    $setuphold (posedge CK, posedge D,
         tsetup_D_CK_posedge_posedge,
         thold_D_CK_posedge_posedge, notifier,,, delayed_CK, delayed_D);
    $setuphold (posedge CK, negedge D,
         tsetup_D_CK_negedge_posedge,
         thold_D_CK_negedge_posedge, notifier,,, delayed_CK, delayed_D);
    $width (posedge CK &&& adacond_D, tpw_CK_adacond_D_posedge, 0, notifier);
    $width (negedge CK &&& adacond_D, tpw_CK_adacond_D_negedge, 0, notifier);
    $width (posedge CK &&& adacond_NOT_D, tpw_CK_adacond_NOT_D_posedge, 0, notifier);
    $width (negedge CK &&& adacond_NOT_D, tpw_CK_adacond_NOT_D_negedge, 0, notifier);
endspecify
```

UVM

- Стандарт IEEE 1800.2
- Принцип в реализации базовых классов
- Верификация RTL и STA



ПАРА-ПАРА-ПАМ

ВСЁ!

(ПОЧТИ)