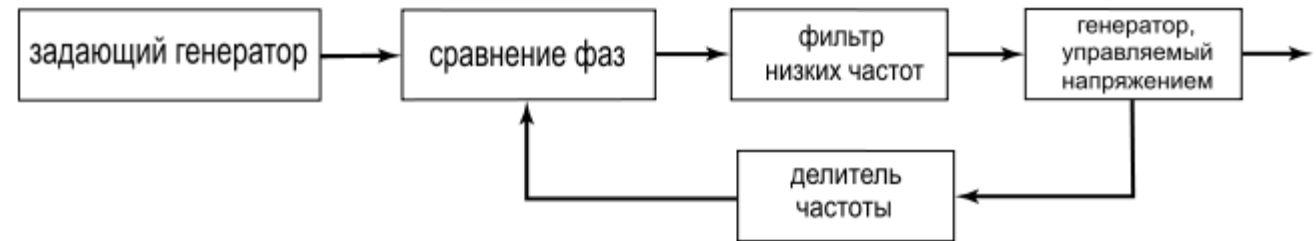


PLL

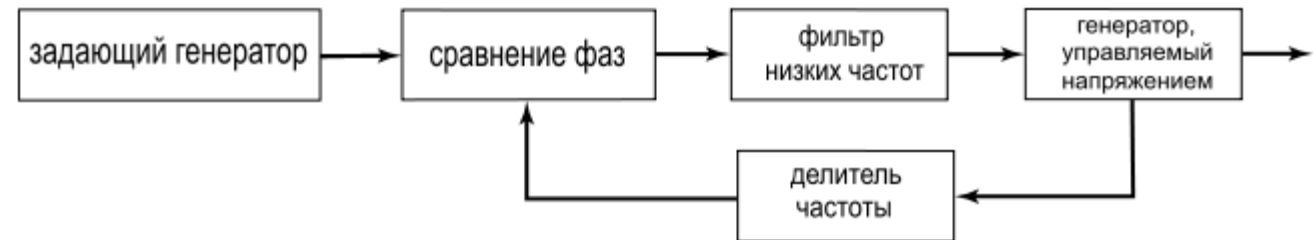
Использование

- Определение фазы сигнала
- Модуляция
- Генераторы
- Внутреннее распределение синхросигналов
- Clock gating



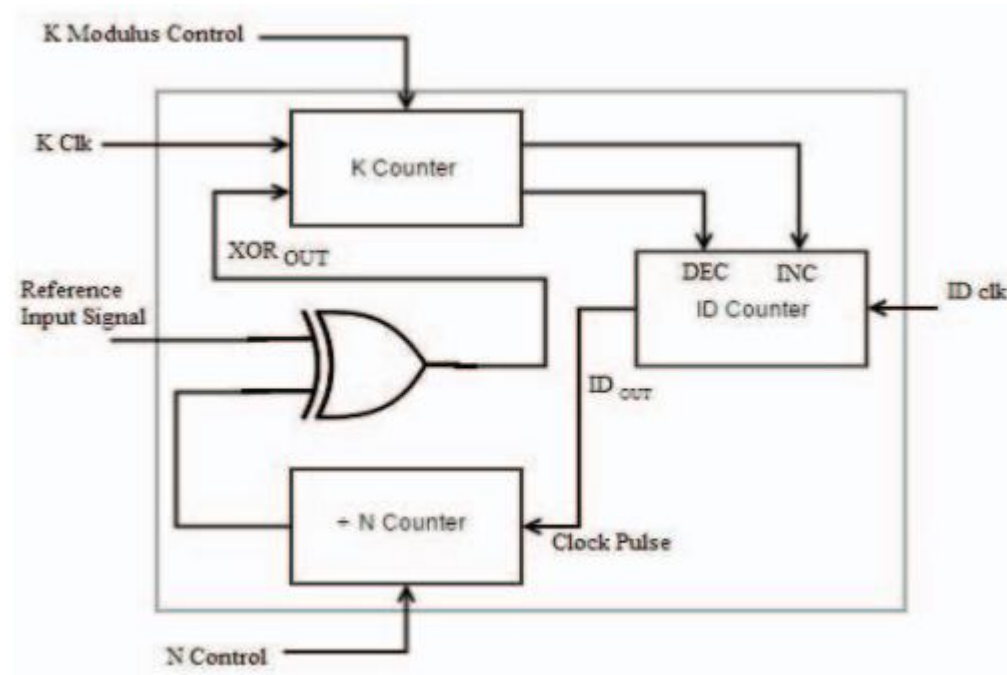
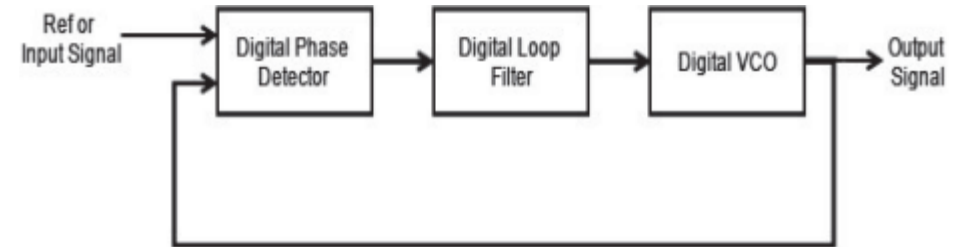
Структура

- Фазовый детектор
- Петлевой фильтр
- ГУН
- Делитель частоты



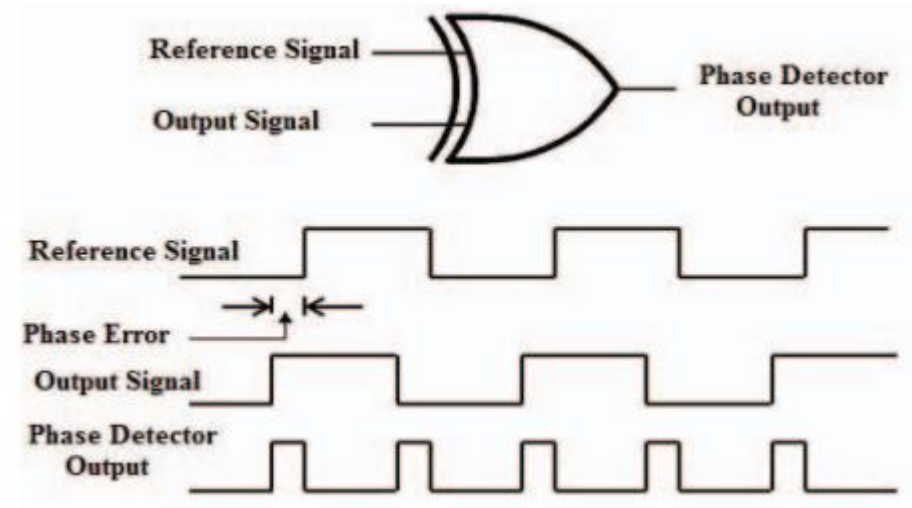
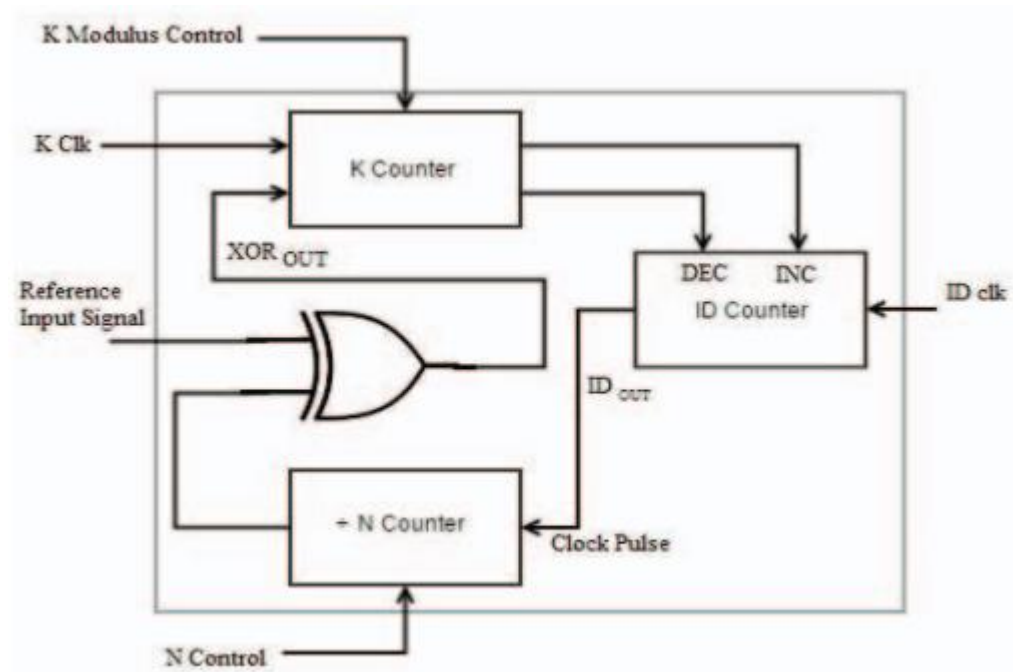
ADPLL

- Design of Power Efficient All Digital Phase Locked Loop (ADPLL)



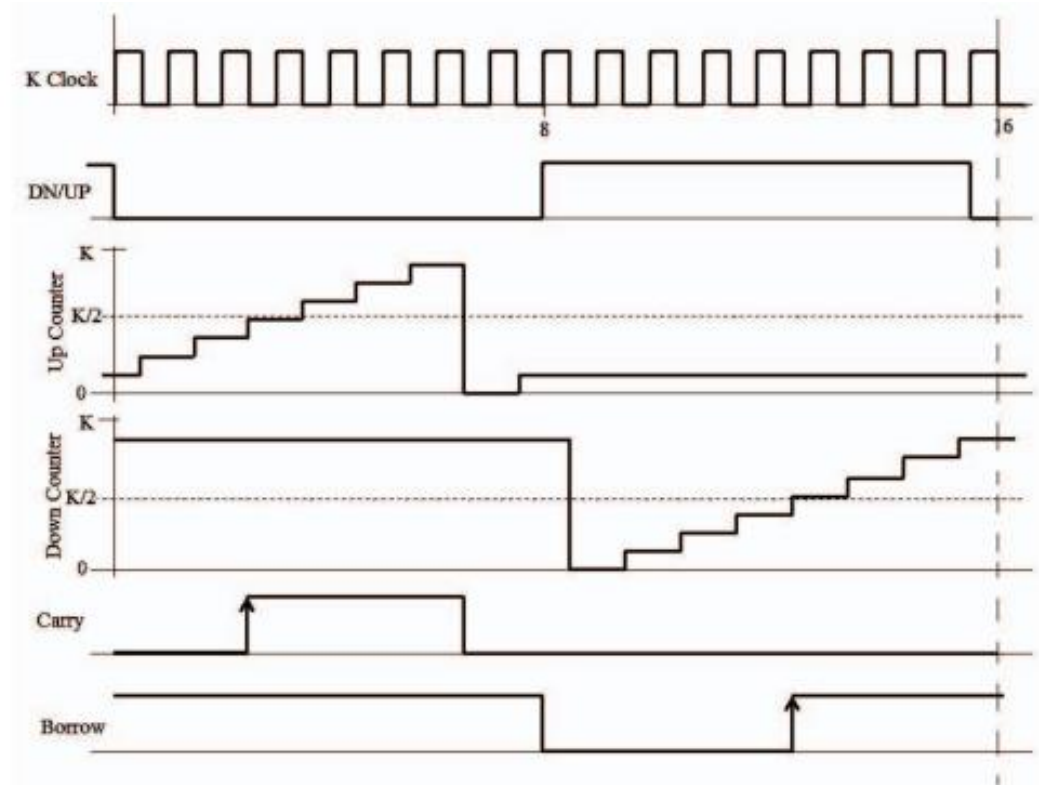
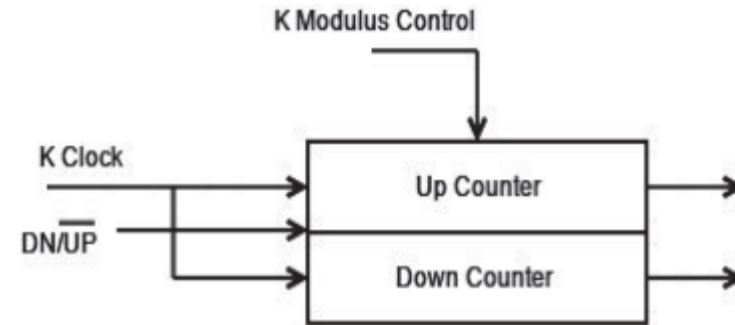
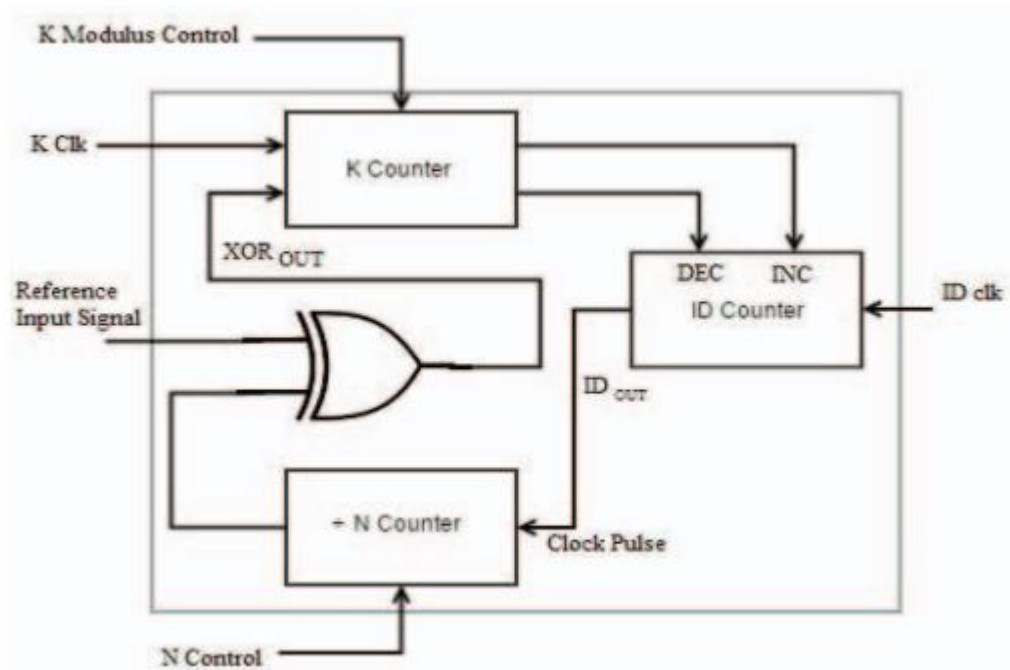
ADPLL

- Фазовый детектор



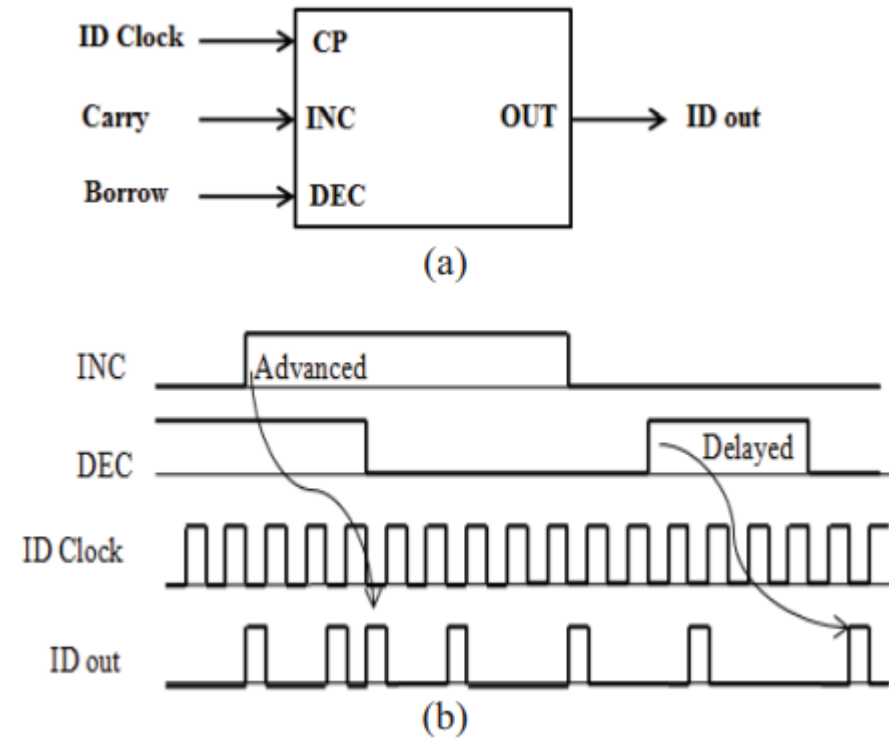
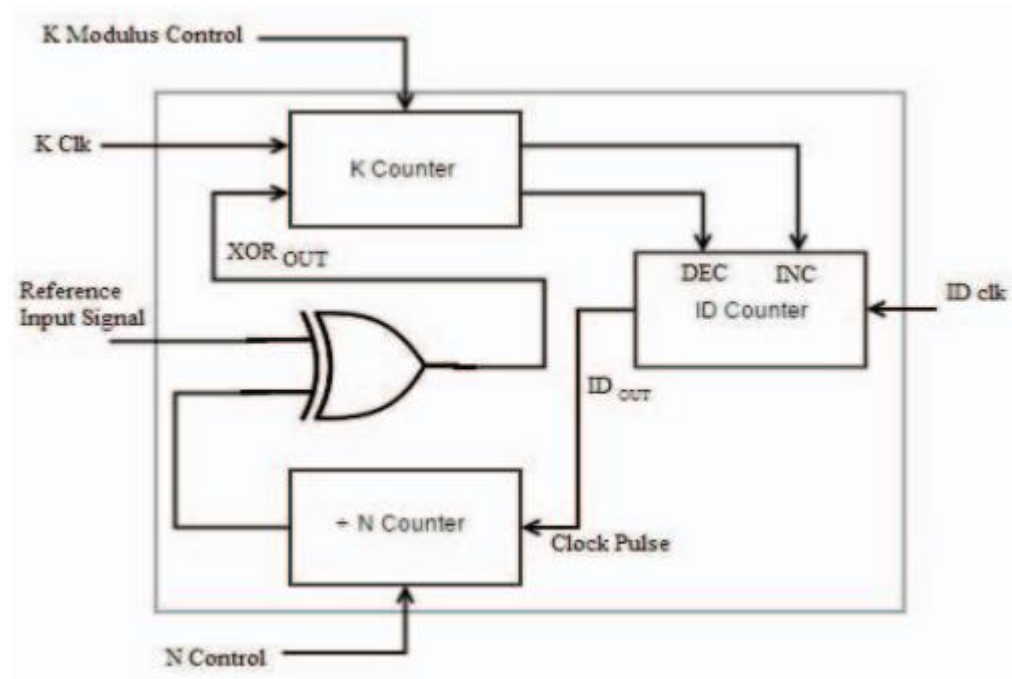
ADPLL

- Петлевой фильтр



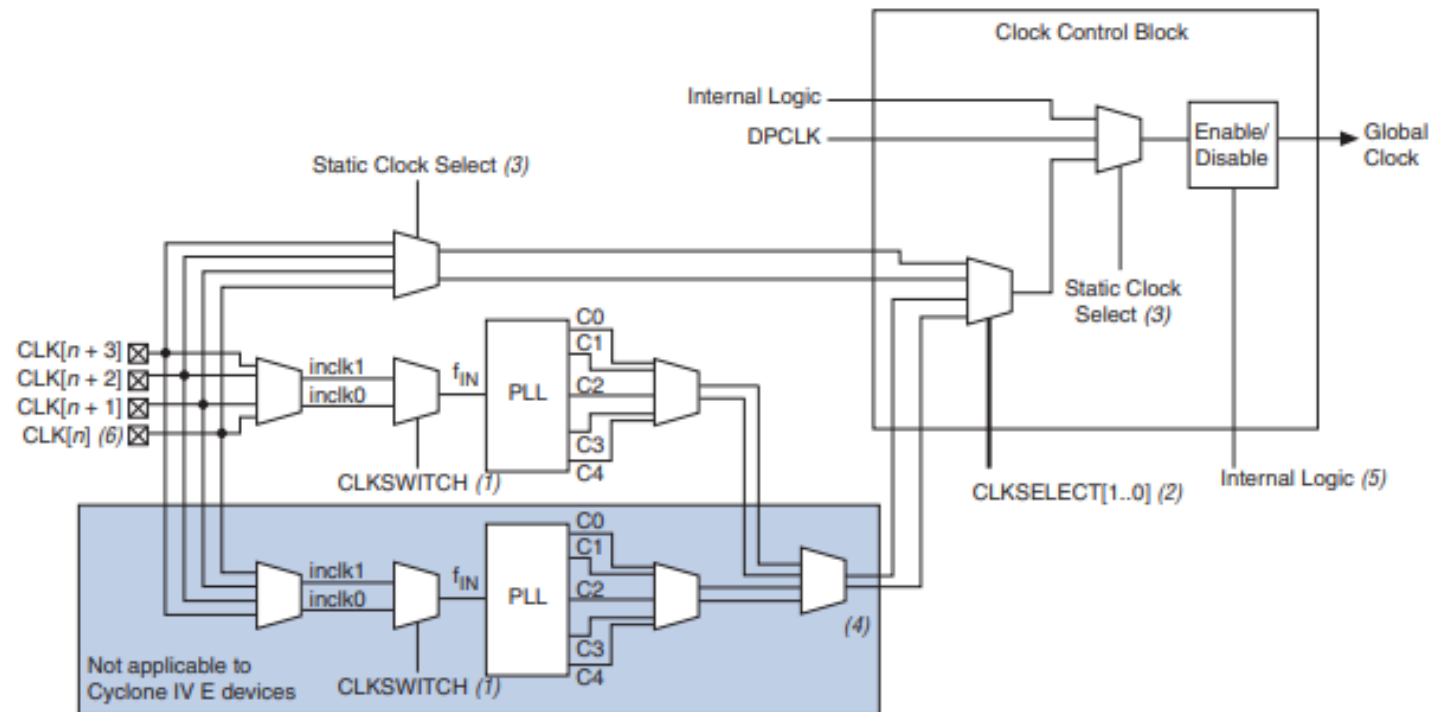
ADPLL

- DCO



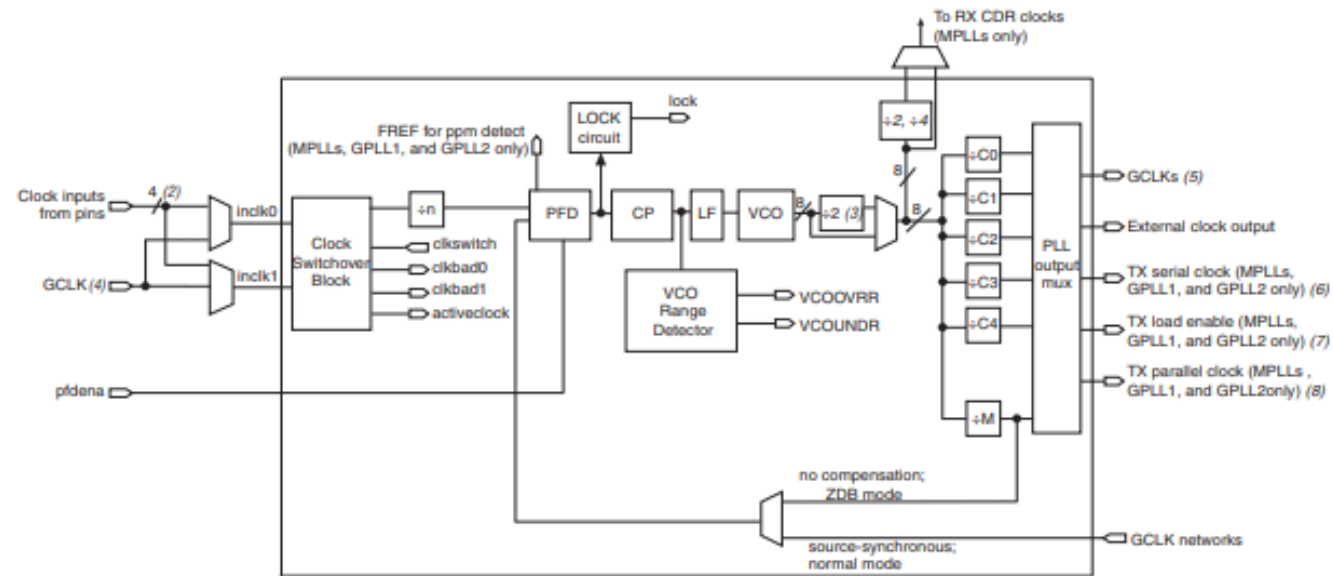
PLL CYCLONE IV

Figure 5–1. Clock Control Block



PLL CYCLONE IV

Figure 5–9. Cyclone IV GX PLL Block Diagram ⁽¹⁾



PLL CYCLONE IV

MegaWizard Plug-In Manager [page 3 of 14]

ALTPLL

About Documentation

1 Parameter Settings 2 PLL Reconfiguration 3 Output Clocks 4 EDA 5 Summary

General/Modes Inputs/Lock Bandwidth/SS Clock switchover

Currently selected device family: Cyclone III

☒ Match project/default

mypll2

inclk0
areset
c0
locked

inclk0 frequency: 100.000 MHz
Operation Mode: Normal

Clk	Ratio	Ph (deg)	DC (%)
c0	1/1	0.00	50.00

Cyclone III

Able to implement the requested PLL

General

Which device speed grade will you be using? 8

☐ Use military temperature range devices only

What is the frequency of the inclk0 input? 100.000 MHz

☐ Set up PLL in LVDS mode Data rate: Not Available Mbps

PLL Type

Which PLL type will you be using?

☐ Fast PLL ☐ Enhanced PLL ☒ Select the PLL type automatically

Operation Mode

How will the PLL outputs be generated?

☒ Use the feedback path inside the PLL

☒ In normal mode
☐ In source-synchronous compensation Mode
☐ In zero delay buffer mode
Connect the fbimic port (bidirectional)
☐ With no compensation

☐ Create an 'fbim' input for an external feedback (External Feedback Mode)

Which output clock will be compensated for? c0

Cancel < Back Next > Finish

PLL CYCLONE IV

MegaWizard Plug-In Manager [page 4 of 14]

ALTPLL

About Documentation

1 Parameter Settings 2 PLL Reconfiguration 3 Output Clocks 4 EDA 5 Summary

General/Modes Inputs/Lock Bandwidth/SS Clock switchover

mypll2

inclk0
areset

inclk0 frequency: 100.000 MHz
Operation Mode: Normal

CLK	Ratio	Ph (deg)	DC (%)
c0	1/1	0.00	50.00

c0
locked

Cyclone III

Able to implement the requested PLL

Optional Inputs

- ☐ Create an 'pllana' input to selectively enable the PLL
- ☒ Create an 'areset' input to asynchronously reset the PLL
- ☐ Create an 'pfdena' input to selectively enable the phase/frequency detector

Lock Output

- ☒ Create 'locked' output
- ☐ Enable self-reset on loss lock

Advanced Parameters

Using these parameters is recommended for advanced users only

- ☐ Create output file(s) using the 'Advanced' PLL parameters
 - Configurations with output clock(s) that use cascade counters are not supported

Cancel < Back Next > Finish

PLL CYCLONE IV

MegaWizard Plug-In Manager [page 8 of 14]

ALTPLL

About Documentation

1 Parameter Settings 2 PLL Reconfiguration 3 Output Clocks 4 EDA 5 Summary

clk c0 > clk c1 > clk c2 > clk c3 > clk c4

mypll2

inclk0
areset
c0
locked

inclk0 frequency: 100.000 MHz
Operation Mode: Normal

Clk	Ratio	Ph (deg)	DC (%)
c0	213/200	0.00	50.00

Cyclone III

c0 - Core/External Output Clock

Able to implement the requested PLL

☒ Use this clock

Clock Tap Settings

☒ Enter output clock frequency:
☐ Enter output clock parameters:

Requested Settings	Actual Settings
106.5 MHz	106.500000
1	213
1	200
0.00 deg	0.00
50.00	50.00

Copy

Note: The displayed internal settings of the PLL is recommended for use by advanced users only

Description
Primary clock VCO frequency (MHz) 1.0
Modulus for M counter 213

Per Clock Feasibility Indicators
c0 c1 c2 c3 c4

Cancel < Back Next > Finish

PLL CYCLONE IV

MegaWizard Plug-In Manager [page 14 of 14]

ALTPLL [About](#) [Documentation](#)

1 Parameter Settings 2 PLL Reconfiguration 3 Output Clocks 4 EDA 5 Summary

mypll2

inclk0
areset
c0
locked

inclk0 frequency: 100.000 MHz
Operation Mode: Normal

Clk	Ratio	Ph (deg)	DC (%)
c0	213/200	0.00	50.00

Cyclone III

Turn on the files you wish to generate. A gray checkmark indicates a file that is automatically generated, and a green checkmark indicates an optional file. Click Finish to generate the selected files. The state of each checkbox is maintained in subsequent MegaWizard Plug-In Manager sessions.

The MegaWizard Plug-In Manager creates the selected files in the following directory:
C:\Altera\mesohod2\cyclone3_first\

File	Description
<input checked="" type="checkbox"/> mypll2.v	Variation file
<input checked="" type="checkbox"/> mypll2.ppf	PinPlanner ports PPF file
<input type="checkbox"/> mypll2.inc	AHDL Include file
<input type="checkbox"/> mypll2.cmp	VHDL component declaration file
<input type="checkbox"/> mypll2.bsf	Quartus II symbol file
<input type="checkbox"/> mypll2_inst.v	Instantiation template file
<input checked="" type="checkbox"/> mypll2_bb.v	Verilog HDL black-box file

Cancel < Back Next > Finish