This is a subset of Atmels AVR instruction set to be implemented in our processor. Please feel free to add additional AVR-instructions to this list.

NOP	0000 0000 0000 0000
LSL Rd	0000 11dd dddd dddd
ADD Rd, Rr	0000 11rd dddd rrrr
CP Rd, Rr	0001 01rd dddd rrrr
SUB Rd, Rr	0001 10rd dddd rrrr
ROL Rd	0001 11dd dddd dddd
ADC Rd, Rr	0001 11rd dddd rrrr
AND Rd, Rr	0010 00rd dddd rrrr
EOR Rd, Rr	0010 01rd dddd rrrr
OR Rd, Rr	0010 10rd dddd rrrr
MOV Rd, Rr	0010 11rd dddd rrrr
CPI Rd, K	0011 KKKK dddd KKKK
SUBI Rd, K	0101 KKKK dddd KKKK
ORI Rd, K	0110 KKKK dddd KKKK
ANDI Rd, K	0111 KKKK dddd KKKK
LD Rd, Z	1000 000d dddd 0000
ST Z, Rr	1000 001r rrrr 0000
COM Rd	1001 010d dddd 0000
ASR Rd	1001 010d dddd 0101
DEC Rd	1001 010d dddd 1010
INC Rd	1001 010d dddd 0011
LSR Rd	1001 010d dddd 0110
RJMP k	1100 kkkk kkkk kkkk
LDI Rd, K	1110 KKKK dddd KKKK
BRBS s, k	1111 00kk kkkk ksss
BRBC s, k	1111 01kk kkkk ksss
SEC	1001 0100 0000 1000
CLC	1001 0100 1000 1000
PUSH	1001 001d dddd 1111
POP	1001 000d dddd 1111
RCALL	1101 kkkk kkkk kkkk
RET	1001 0101 0000 1000

The AVR Studio assembler outputs the result in Intel-Hex format. Use the converter to convert the appropriate file into VHDL (see folder in Lab).