ELEN 21 Lab 4: Multiplexer Design
Pre-Lab

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II. Pre-Lab

Problem Statement:
You will design a 2 to 1 Multiplexer (MUX) then use it as a building block to design an 8:1 MUX.

A 2 to 1 MUX is a switch that allows you to select one of two inputs to appear at the output. A 2 to 1 MUX has three inputs and one output. Two of the inputs, w_0 and w_1, are **data inputs**. The third input, s, the **select input**, determines which of the data inputs, w_0 or w_1 will appear on the output z. If s is "0", then the output z is w_0. If s is "1", then the output z is w_1.

Part 1: Circuit 1 - Multiplexer as a switch

Design a **2-to-1 *multiplexer*** with a select input s, two data inputs w_0 and w_1, and output z.

Show the truth table for this multiplexer:

s	w_0	w_1	z
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

Table 1: Truth Table for the 2-to-1 Multiplexer

Draw the sum-of-products logic implementation for the circuit.

	00	01	11	10
0	0 0	0 1	1 3	1 2
1	0 4	1 5	1 7	0 6

Figure 1: Sum-of-products Schematic for the Circuit

Part 2: Circuit 2 - Hierarchical design of Multiplexers

*Design and build an **8-to-1** multiplexer using **2-to-1** multiplexers in a hierarchical manner.*

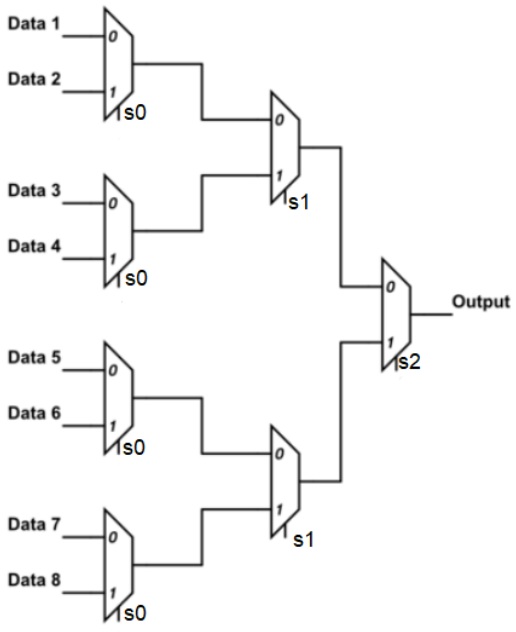

Figure 2: An 8-to-1 multiplexer using 2-to-1 multiplexers

How many 2:1 MUXes are needed?

From the diagram, we see that we need 7 2:1 MUXes. Draw the schematic clearly showing the hierarchical design and clearly indicate in your block diagram the select inputs and the ordering of the data inputs.

Show what the output of each 2:1 MUX in your design will be if,

$s_2\ s_1\ s_0 = 1\ 0\ 0.$

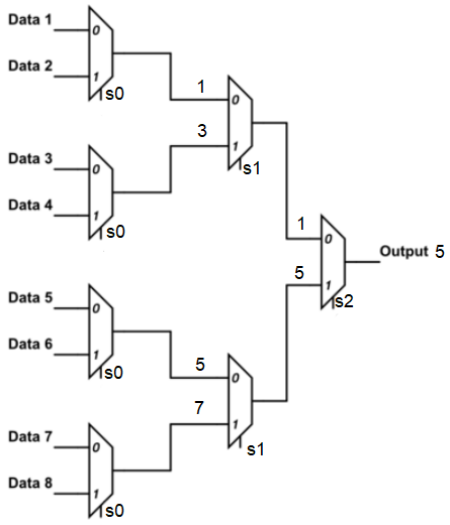

Figure 3: Outputs of each MUX when $s_2\ s_1\ s_0 = 1\ 0\ 0$

Show what the output of each 2:1 MUX in your design will be if,

$s_2\ s_1\ s_0 = 0\ 1\ 1.$

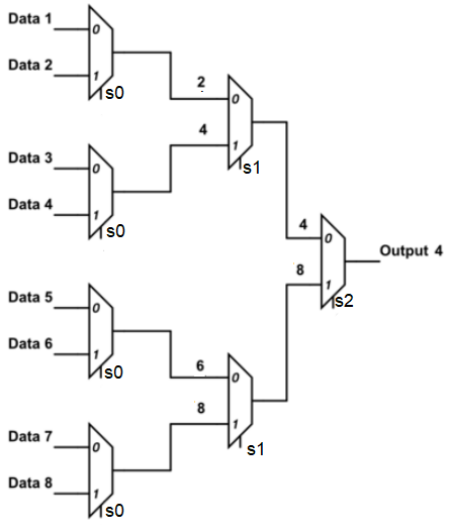

Figure 4: Outputs of each MUX when $s_2\ s_1\ s_0 = 0\ 1\ 1$

Part 3: Circuit 3 - Multiplexer as a logic building block

A multiplexer can be used as a standard building block to implement any desired logic function without requiring any minimization techniques. Further, if the specification of the logic function changes, the circuit can be modified by simply changing the MUX data inputs corresponding to the changed truth table values.

A majority circuit is to be built whose output F is high when the majority of its three inputs A, B, and C are one.

Draw the truth table for the majority circuit with the three bits A, B, and C as the inputs and F as the output.

	A	B	C	f
0	0	0	0	0
1	0	0	1	0
2	0	1	0	0
3	0	1	1	1
4	1	0	0	0
5	1	0	1	1
6	1	1	0	1
7	1	1	1	1

Figure 5: Truth table for the majority circuit with three bits A, B, and C

Design the majority circuit using only an 8 to 1 MUX.

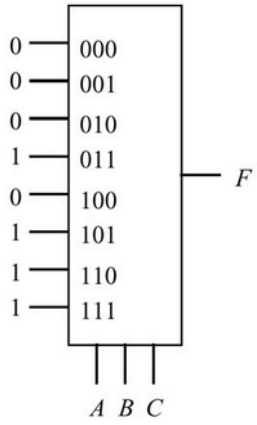

Figure 6: 8:1 MUX design for the Majority function