ELEN 21 HW #5

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Question #1. Given a register file with 32 registers

a. How many bits of MUX select would we need for the MUX that would allow any register value to be transferred onto a single bus?

The MUX select size is based off of how many registers there are in the register file. Since there are 32 registers, we find that $log_2 32 = 5$, so we need 5 MUX selects.

b. If we used tri-state buffers instead of a MUX, how many logically distinct enables would we need to control these buffers?

We need 32 enables to match the 32 registers we have.

c. If we had two separate buses and we wanted to be able to independently control which register value we wanted to transfer on each bus, how many MUX select signals would we need?

Two busses, both of which access and change 32 registers on their own means that we have 5 selects per bus, or 10 total selects.

d. If we had another bus connected to the D input of all 32 registers, how many logically distinct load enables would we need to control updates (i.e. writes) to the register file?

If we wanted to have a load enable on both the input and write functions for a register (input D, read/write $Enable$), we would need 64 total unique enables.

Question #2.

a. If we were to write out the truth table for a function with 5 input variables, how many rows would be in the table?

There would be 2^5 amount of rows, or 32 unique permutations.

b. So how many possible minterms would there be?

If we were to assume that the function basically resulted in always 1s (all outputs are 1), there can be 32 minterms, where the SOP solution is $f = 1$.

c. How many outputs would a 5-bit decoder have?

A decoder with N bits has 2^N outputs, which is the same as 32 outputs.

d. Draw a circuit, using a 5-bit decoder, that implements the function $f(A, B, C, D, E) = \sum 6, 17, 19$

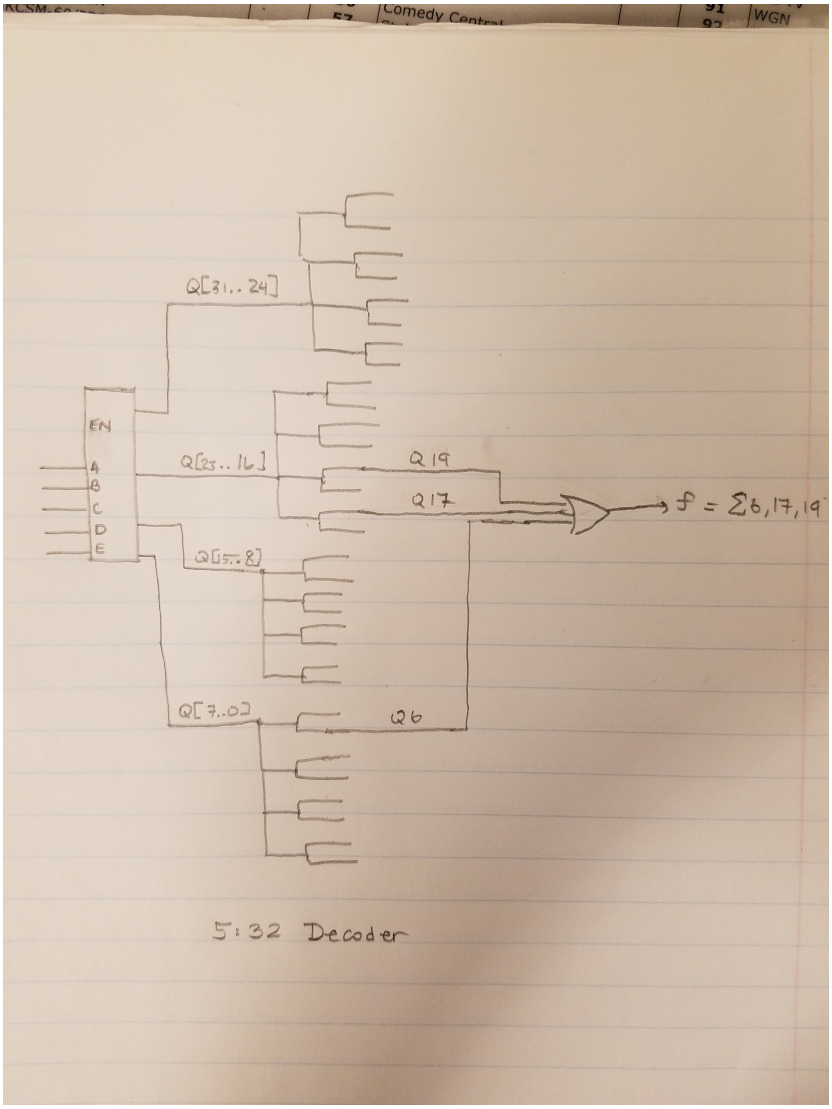

Figure 1: A 5-bit (5:32) decoder with SOP solution of $\sum 6, 17, 19$