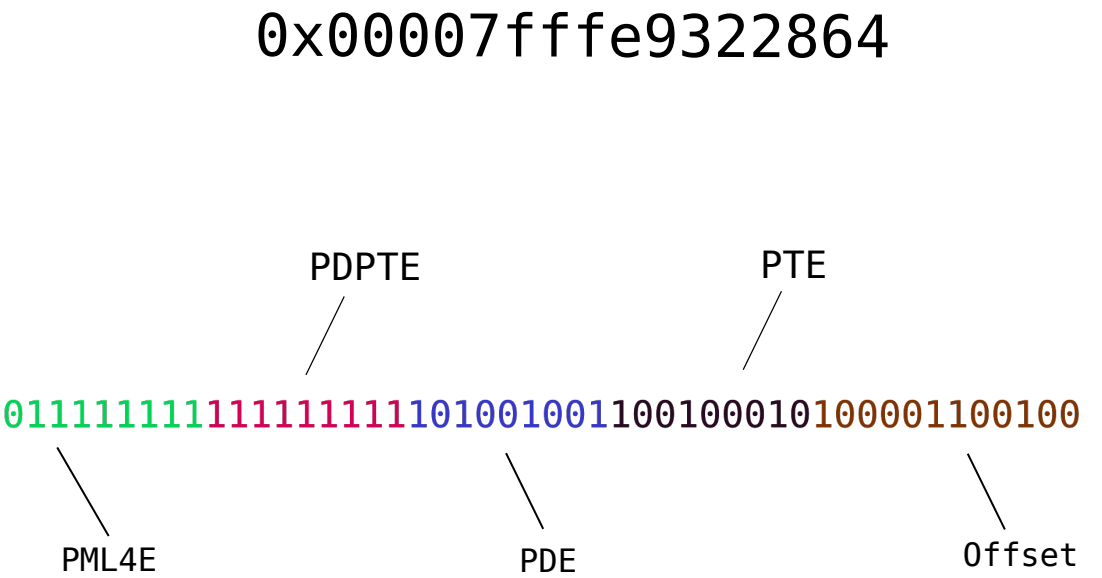
Anatomy of a virtual address[1]



The translation of a virtual memory address into a physical memory takes place transparently in the hardware of modern CPUs nowadays. In a 64-bit machine the hardware uses 4-level page tables, each capable of holding up to 512 entries.

The outer most table is named *Page-Map Level 4 (PML4)*. The following levels are named *Page-Directory Pointer Table (PDPT)*, *Page-Directory (PD) and Pointer Table (PT)* respectively.

The drawing above shows how the CPU interprets the virtual memory address for a 4 KiB page. Bits 64:49 are always a copy of bit 48, in this case 0s. From bit 48:12, every 9 bits represents an index in the page table of the respective level. Bits 12:1 are the offset on the page of the address.

Huge pages needs to be set explicitly by the OS when mapping a new entry in the page tables, signaling to the CPU that the entry points to a page, instead of a table. The remaining bits are interpreted as an offset. As of today, most hardware support 2 MiB and 1 GiB huge pages.

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[1] 64-bit address