Jetson AGX Xavier Series HDMI Tuning Guide

Application Note

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Document History

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Version	Date	Description of Change
1.0	December 2, 2019	Initial Release

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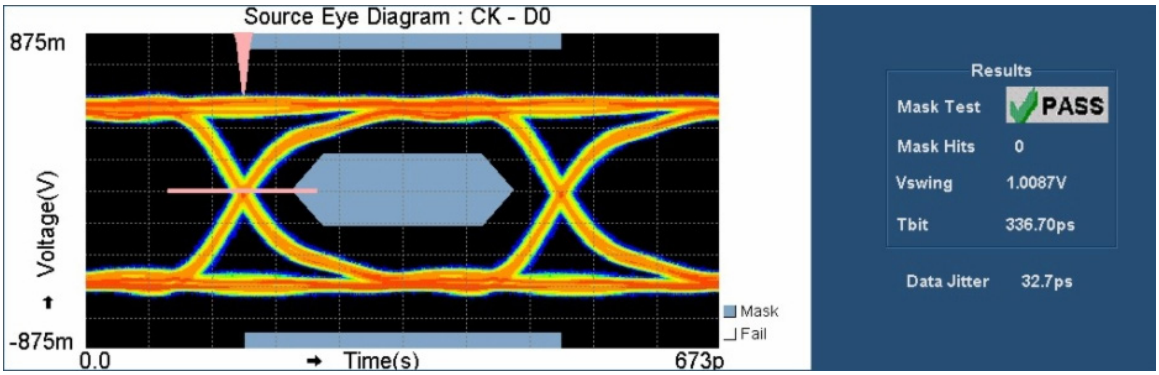
Overview

The NVIDIA® Jetson AGX Xavier™ includes HDMI™ technology; this application note describes the registers and steps needed to tune the HDMI signals output from the NVIDIA® Xavier™ system on chip (SoC).

In order to meet HDMI compliance, tuning may be required to adjust the TMDS signal such that the voltage swing is close to 500 mV ± 100 mV single-ended, or 1000 mV ± 200 mV differentially. This is to ensure the signal integrity is clean, meets the HDMI specifications, and the device is optimized for low power consumption.

Note: Prior to any tuning, scope and probes must be calibrated. Refer to the documentation for your scope and probe for instructions on how to calibrate.

Figure 1. Source Eye Diagram: CK-D0



Abbreviations and Definitions

Table 1 lists the abbreviations that may be used throughout this application note and their definitions.

Table 1. Abbreviations and Definitions

Abbreviation	Definition
CTS	Compliance Test Specification
DUT	Device Under Test
EMI	Electromagnetic Interference
HDMI	High-Definition Multimedia Interface
HPD	Hot Plug Detect
PVT	Process, Voltage, and Temperature
RF	Radio Frequency
Sink	Any type of receiver, such as a display or panel
SOR	Serial Output Resource – Module naming referring to the HDMI block
Source	Any type of transmitter, such as Xavier
TMDS	Transition-Minimized Differential Signaling

Setup

Required Equipment

There are many tools currently available to perform the HDMI tuning. The following components are required:

- Test fixture
- Oscilloscope
- Probes
- DC power supply
- Software
  - HDMI compliance software
  - Tools to access register space in Xavier

The following subsections list some of the acceptable equipment that may be used.

Note: The items highlighted with green in the following sections are the tools that NVIDIA used for validation and tuning. This guide will refer to those tools specifically for the rest of this application note.

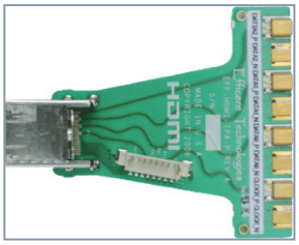
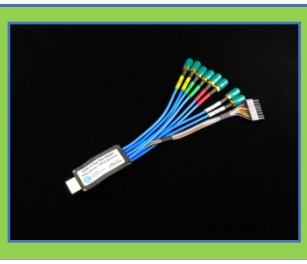
Test Fixture

Test fixtures are used to connect the probes to the output of the HDMI interface. The following example fixtures listed use the Type-A interface for HDMI 1.4b compliance. Fixtures of different interface types are available and are recommended instead of using adapters to convert the interface Type.

For HDMI 2.0 compliance, ensure that the test fixture can support the higher bitrate with minimal insertion loss.

The fixture selected must have SMA interconnects to avoid impedance mismatches due to discontinuities.

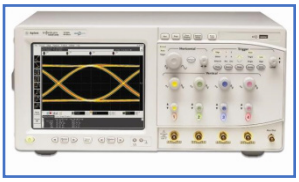
Table 2. Partial List of Acceptable HDMI Test Fixtures Type A

Efficere	EFF-HDMI-TPA-P	
Agilent	N1080A	
Wilder Tech	HDMI-TPA-P	

Oscilloscope

The scope is used to display and measure the signals. The HDMI 1.4 specification requires that the scope has at least 8 GHz of bandwidth and a sampling rate of at least 10 GS/s if the pixel clock is equal to or less than 165 MHz, or sampling rate of at least 20 GS/s if the pixel clock is greater than 165 MHz.

Table 3. Partial List of Acceptable Oscilloscopes for HDMI 1.4 Tuning

Tektronix	TDS6804B or better	
Agilent	DSO80000B or better	

For HDMI 2.0, a scope with at least 16 GHz of bandwidth is recommended.

Table 4. Partial List of Acceptable Oscilloscopes for HDMI 2.0 Tuning

Tektronix	DPO/MSO 70000 series 16 GHz or better	
Agilent	Infiniium 90000 series 16 GHz or better	

Probes

Probes are used to connect the scope to the test fixture. The probes must have at least 8 GHz of bandwidth for HDMI 1.4b testing and at least 12 GHz of bandwidth for HDMI 2.0 testing.

At least two (2) probes are required for tuning, four (4) probes are ideal.

Untested lanes must be terminated appropriately. See the "DC Power Supply" section for details.

Table 5. Partial List of Acceptable Probes

Tektronix	P7313SMA	
Agilent	1169A Requires Agilent N5380A	
Agilent	N5380A Used with Agilent 1169A	

DC Power Supply

Any power supply that can supply a constant voltage of 3.3V is needed to terminate the HDMI signals. Refer to the probe's instruction manual on how to supply this termination voltage to the probes.

Note: All untested lanes must be terminated to 3.3V using 50 Ω terminators. Irrespective of the tools used, it is important to make sure that they are calibrated and meet industry standards in order to obtain accurate measurements.

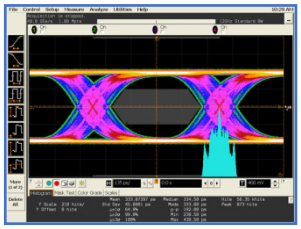
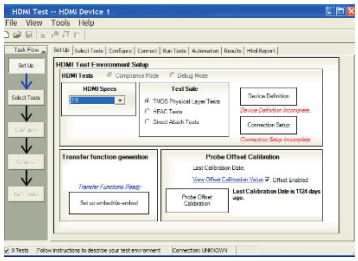
Software

This section describes the software used for HDMI tuning.

Compliance Test Software

NVIDIA recommends that the official compliance test software be used to ensure accurate results. Although manually measuring the signal may be as effective, it must ultimately pass with the compliance software at the compliance house.

Table 6. Partial List of Acceptable Test Software

HDMI 1.4b Testing		HDMI 2.0 Testing	
Tektronix TDSHT3 or later		TekExpress HDM or later	
Agilent N5399A or later		Agilent N5399C or later	

Xavier Software Tools

Consult your software team or contact your NVIDIA representative for assistance with software tools to access the register space in Xavier.

Method for Tuning

Tuning is done by running the eye diagram tests on each of the data lanes while shmoo'ing the applicable registers. The objective is to keep the differential voltage swing as close to 1000 mV as possible, while providing the eye diagram enough margin to meet HDMI specifications.

Internal Termination

To effectively shmoo for the correct voltage swing, the drive strength can be estimated by calculating the parallel resistance to AVDD_HDMI/AVcc, assuming exact 50 ohms to 3.3V in the receiver. The equivalent resistance can be calculated based on the internal resistance settings. Then refer to the register description section for the current per drive strength tap to calculate the voltage swing.

With the equivalent termination and current per drive strength, the approximate voltage swing can be calculated. However, for higher speeds and routing differences, increased drive strength and pre-emphasis may be needed to overcome signal loss due to routing or EMI damping components.

On Xavier, the internal termination has an internal calibration mechanism which calibrates the internal termination to 50Ω, depending on the external RSET value, silicon variation and temperature variation.

Procedures

Calibrate the scope and probes before you begin. Refer to your scope and probe user manuals for details on how to calibrate.

DUT

This guide does not cover setup of HDMI at any specific resolution. Work with your software team and NVIDIA representative to prepare the DUT for testing. Following are the general steps to set up the HDMI connection.

1. Disable Hot Plug Detect: The driver or OS may disable HDMI output if it detects the panel being disconnected. Try the following methods to prevent that:

a). **Method #1:** Disable the HPD interrupt via software by setting the HPD pin to TRISTATE.

b). **Method #2:** Disconnect the HPD circuit from the HDMI connector, manually rework HPD circuit to a desired voltage level to input to Xavier to make the software consider HDMI is still connected.
(Refer to the carrier I/O board schematics for how to do that. If this method is chosen, the circuit must be restored before performing the HDMI certification tests.)

2. Configure the DUT to drive HDMI at the supported resolutions: 480p (27 MHz), 720p (74.25 MHz), 1080p (148.5 MHz), 2160p/30 (297 MHz), or 2160p/60 (594 MHz).
3. Attach the test fixture to the DUT.
4. Attach the probe-ends to the test fixture, and properly connect the termination voltage to the probes. Untested lanes must be properly terminated.
5. Attach the probes to the scope.

Note: For using an HDMI converter (to GMSL/FPD link/MIPI, etc) design on board, HDMI CTS is not required. To check the HDMI signal quality from Xavier, probe the HDMI signals closest to the input of the HDMI converter to confirm if the signals meet the HDMI source electrical spec or HDMI converter's input electrical spec.

Oscilloscope

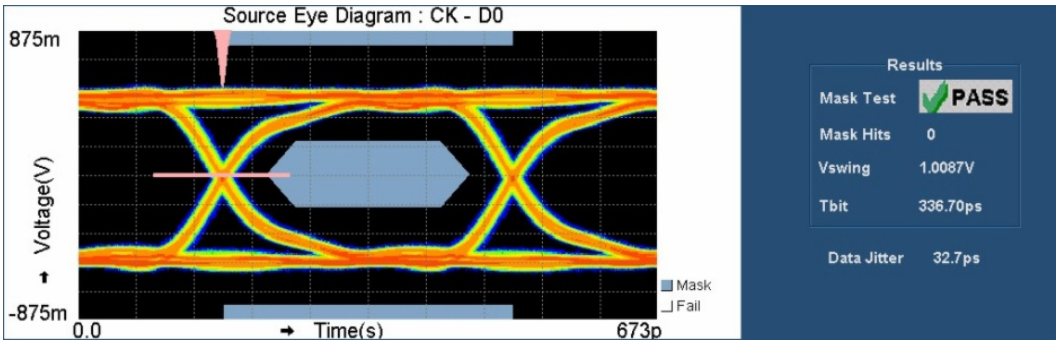
1. Ensure the probes are using the termination voltage of 3.3V.
2. Start the HDMI compliance software.
3. Set up the HDMI compliance software to take the Eye Diagram and configure the probes to the proper clock and data assignments.
4. Run the eye diagram test.
5. Check the voltage swing and margin result (see Figure 2).
6. Refer to Registers section and note the internal termination, drive strengths, and pre-emphasis settings.
7. Repeat for all data lanes, using different register settings, at all supported resolutions.

Tips:

When shmoo'ing drive strengths or pre-emphasis, keep the same value across each data lane. The HDMI pads for each of the data pairs and the clock are the same and should have very minor variation.

Since HDMI clock has less transitions than data, its settings can be weaker than the data lanes. This can save some power and lower possible noise or EMI.

Figure 2. Voltage Swing and Margin Results



Objectives

While there is no margin specification, a good rule of thumb is to provide:

- At least 40 mV of margin above and below the eye mask
- Voltage swing of around 1000 mV
- Find settings for:
  - 480p
  - 720p
  - 1080p
  - 2160p/30
  - 2160p/60

Tips:

- Lower drive strength, IO peak current, and pre-emphasis settings will lower the power consumption.
- The stronger the termination, more current is needed and therefore a higher power consumption.
- Fast rising/falling edges will contribute to increased EMI.

Voltage Swing Target

This guide targets a differential voltage swing of 1000 mV.

The target can be lowered to help reduce EMI and RF related issues.

CAUTION: Note that if the user lowers the differential voltage swing target, the user assumes complete responsibility for issues or consequences arising as a result. In addition, the user must test random parts to ensure HDMI compliance with the new differential voltage settings.

Registers

The Serial Output Resource (SOR) module can be configured to output HDMI or VESA® DisplayPort™ (DP). Jetson AGX Xavier has 3x instances of the SOR0~2 for HDMI_DP0~2 pins. SOR0 controls the HDMI_DP0 pins and SOR1 controls HDMI_DP1, and so forth.

The following table lists the detail registers to tune the Xavier Internal Termination Resistance, Drive Strength, Pre-Emphasis Controls, etc.

Table 7. HDMI_DP0~2 (SOR0~2) Registers

Register Name	Bit Fields	Description	Notes
SOR_NV_PDISP_SOR_PLL1_0 (Address: 0x15b005a8) SOR_NV_PDISP_SOR_PLL1_1 (Address: 0x15b405a8) SOR_NV_PDISP_SOR_PLL1_2 (Address: 0x15b805a8)			
RESERVED	31:16	RESERVED REGISTERS	Register field is RESERVED. Do not modify; preserve existing value.
TMDS_COMPOUT	15:15	Internal Termination Calibration Comparator Output	When calibrating the internal termination, this read-only register will output 0 if the termination is lower than 50Ω and 1 if the termination is higher.
RESERVED	14:14	RESERVED REGISTERS	Register field is RESERVED. Do not modify; preserve existing value.
TMDS_TERMADJ	12:09	Internal Termination Resistance Control	Requires TMDS_TERM to be enabled.
TMDS_TERM	08:08	Internal Termination Enable	Enables internal termination
RESERVED	07:00	RESERVED REGISTERS	Register field is RESERVED. Do not modify; preserve existing value.

Register Name	Bit Fields	Description	Notes
SOR_NV_PDISP_SOR_PLL3_0 (Address: 0x15b005b0) SOR_NV_PDISP_SOR_PLL3_1 (Address: 0x15b405b0) SOR_NV_PDISP_SOR_PLL3_2 (Address: 0x15b805b0)			
RESERVED	31:28	RESERVED REGISTERS	Register field is RESERVED. Do not modify; preserve existing value.
BG_VREF_LEVEL	27:24	Bandgap Voltage Level	Changes the reference voltage used to generate the current for the pads. Higher settings equate to higher current draw per tap for DRIVE_CURRENT and PREEMPHASIS.
RESERVED	23:00	RESERVED REGISTERS	Register field is RESERVED. Do not modify; preserve existing value.
SOR_NV_PDISP_SOR_LANE_DRIVE_CURRENT0_0 (Address: 0x15b00138) SOR_NV_PDISP_SOR_LANE_DRIVE_CURRENT0_1 (Address: 0x15b40138) SOR_NV_PDISP_SOR_LANE_DRIVE_CURRENT0_2 (Address: 0x15b80138)			
LANE3_DP_LANE3	31:24	Drive Strength Controls for the Clock Lane for HDMI and Lane 3 for DP/eDP	Each tap increases the drive strength by 0.400mA, with a base of 0.000mA. 000.0000 → 0.000mA 000.0001 → 0.400mA ... 011.0000 → 19.200mA (starting to borrow from pre-emphasis drivers) 100.0111 → 28.200mA (max) 100.1000 → 25.400mA
LANE2_DP_LANE0	23:16	Drive Strength Controls for Lane 2 for HDMI and Lane 0 for DP/eDP	
LANE1_DP_LANE1	15:08	Drive Strength Controls for Lane 1 for HDMI and Lane 1 for DP/eDP	
LANE0_DP_LANE2	07:00	Drive Strength Controls for Lane 0 for HDMI and Lane 2 for DP/eDP	
SOR_NV_PDISP_SOR_LANE_PREEMPHASIS0_0 (Address: 0x15b00148) SOR_NV_PDISP_SOR_LANE_PREEMPHASIS0_1 (Address: 0x15b40148) SOR_NV_PDISP_SOR_LANE_PREEMPHASIS0_2 (Address: 0x15b80148)			
LANE3_DP_LANE3	31:24	Pre-Emphasis Controls for the Clock Lane for HDMI and Lane 3 for DP/eDP	Pre-emphasis controls take lower precedence than drive strength and may not have any noticeable effect at higher drive strengths. Refer to the TRM for more detailed information.
LANE2_DP_LANE0	23:16	Pre-Emphasis Controls for Lane 2 for HDMI and Lane 0 for DP/eDP	
LANE1_DP_LANE1	15:08	Pre-Emphasis Controls for Lane 1 for HDMI and Lane 1 for DP/eDP	

LANE0_DP_LANE2	07:00	Pre-Emphasis Controls for Lane 0 for HDMI and Lane 2 for DP/eDP	
SOR_NV_PDISP_SOR_DP_PADCTL0_0 (Address: 0x15b005b8) SOR_NV_PDISP_SOR_DP_PADCTL0_1 (Address: 0x15b405b8) SOR_NV_PDISP_SOR_DP_PADCTL0_2 (Address: 0x15b805b8)			
RESERVED	31:24	RESERVED REGISTERS	Register field is RESERVED. Do not modify; preserve existing value.
PAD_CAL_PD	23:23	Pad Calibration Power Down	Set to 0 to enable calibration, 1 to disable
TX_PU	22:22	Transmitter pull-up resistors.	Enables the pull-ups for the current sources.
RESERVED	21:16	RESERVED REGISTERS	Register field is RESERVED. Do not modify; preserve existing value.
TX_PU_VALUE	15:08	TX pull-up current source drive	Provides additional current for the current drivers. Can help improve the transition edge speeds and overall voltage swings.
RESERVED	07:00	RESERVED REGISTERS	Register field is RESERVED. Do not modify; preserve existing value.

Xavier Register Settings

The following table describes the default settings that passed HDMI compliance on NVIDIA Jetson AGX Xavier Devkit across PVT. Refer to the previous tables for register descriptions.

Note: The settings may differ with customized carrier I/O board as the signal path differs (for example; different trace layout or connection through a flex cable).

Table 8. Xavier Register Settings

Pixel Clock Frequency	<54 MHz	54~111 MHz	112~223 MHz	224~300 MHz	301~600 MHz
SOR_NV_PDISP_SOR_PLL1_x					
TMDS_TERMADJ	0x8	0x8	0x8	0x8	0xc
TMDS_TERM	0x1	0x1	0x1	0x1	0x1
SOR_NV_PDISP_SOR_PLL3_x					
BG_VREF_LEVEL	0x8	0x8	0x8	0x8	0x8
SOR_NV_PDISP_SOR_LANE_DRIVE_CURRENT0_x					
LANE3_DP_LANE3	0x33	0x33	0x37	0x33	0x33
LANE2_DP_LANE0	0x3A	0x3A	0x3A	0x3D	0x3D
LANE1_DP_LANE1	0x3A	0x3A	0x3A	0x3D	0x3D
LANE0_DP_LANE2	0x3A	0x3A	0x3A	0x3D	0x3D
SOR_NV_PDISP_SOR_LANE_PREEMPHASIS0_x					
LANE3_DP_LANE3	0x00	0x00	0x00	0x00	0x00
LANE2_DP_LANE0	0x00	0x00	0x00	0x00	0x00
LANE1_DP_LANE1	0x00	0x00	0x00	0x00	0x00
LANE0_DP_LANE2	0x00	0x00	0x00	0x00	0x00
SOR_NV_PDISP_SOR_DP_PADCTL0_x					
TX_PU_VALUE	0x00	0x00	0x00	0x40	0x60

Pixel Clock Frequency	<54 MHz	54~111 MHz	112~223 MHz	224~300 MHz	301~600 MHz
TX_PU	0x1	0x1	0x1	0x1	0x1

Note: The "_x" in the register names represents 0~2 of SOR. See "Registers" chapter for details.

Final Check

Sanity Check

After tuning is completed, the settings should be sanity-checked to make sure they do not violate any other parts of the HDMI specifications and there is enough margin.

The DUT should go through the full set of electrical tests outlined in the HDMI Compliance Test Specifications (CTS) document to ensure that the DUT can pass HDMI certification.

If there are any failures, the settings must be tuned again until there is a passing result.

Note: Higher power consumption is expected if the new settings are stronger than the default settings. Stronger settings are required due to, but not limited to, longer traces, EMI chokes on the signal paths, or signal integrity issues.

Updating the Software

After the tuned settings have been verified, they need to be updated into the OS or the driver. Contact the appropriate software team, or your NVIDIA representative to update new tuned settings.

- The 480p settings apply to pixel clock resolutions ⩽ 54 MHz
- The 720p settings apply to pixel clock resolutions between > 54 MHz to ⩽ 111 MHz
- The 1080p settings apply to pixel clock resolutions between > 111 MHz to ⩽ 223 MHz
- The 2160p/30 settings apply to pixel clock resolutions between > 223 MHz to ⩽ 300 MHz
- The 2160p/60 settings apply to pixel clock resolutions between > 301 MHz to ⩽ 600 MHz

Note: Ranges can be adjusted according to design and use-cases. More ranges can also be defined as long as proper tuning and software implementation is performed.

Final Steps

After the settings have been updated in the driver, you must verify that the new tuned settings are really applied to each of the target resolutions.

A visual check-out is recommended as well. Connect the DUT to an HDMI panel and visually check that there is no corruption at any of the supported HDMI resolutions.

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