NVIDIA Jetson AGX Xavier USB 3.1 Compliance Test Guide

Application Note

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Introduction

This application note serves as a high-level guide to compliance testing of the USB 3.1 SuperSpeed (SS up to 5 Gbps) and SuperSpeed+ (SS+ up to 10 Gbps) PHY in host mode on the NVIDIA® Jetson AGX Xavier™ module. The NVIDIA Jetson AGX Xavier module has been tested for specification compliance and has passed under worst case scenarios. NVIDIA expects that no tuning will be required if customers follow the routing guidelines published in the relevant design guides.

Compliance Testing

The *Electrical Compliance Test Specification SuperSpeed Universal Serial Bus Rev 1.0a* provides the compliance criteria and test descriptions for SuperSpeed USB devices, hubs, and host controllers.

The *Electrical Compliance Test Specification Enhanced SuperSpeed Universal Serial Bus Rev 1.0a* provides the compliance criteria and test descriptions for SuperSpeed+ USB devices, hubs, and host controllers that conform to the *Universal Serial Bus 3.1 Specification, Rev 1.0*.

Refer to the test specification documents mentioned for a high-level overview of the tests that are performed to check the compliance criteria. Depending on the brand of equipment being used for the test, customers can then refer to the manufacturer's documentation for step-by-step procedure on how to perform the test.

Note: When the Jetson AGX Xavier module is in USB RCM mode, it may not be in compliance with the USB 3.1 specification.

Placing the Jetson AGX Xavier Module USB 3.1 Controller in Compliance Mode

To run the USB 3.1 TX electrical compliance test, the Jetson AGX Xavier module USB 3.1 controller must be placed in compliance mode.

For SuperSpeed TX Electrical Tests refer to sections TD.1.1, TD.1.3, and TD.1.4 in the *Electrical Compliance Test Specification SuperSpeed Universal Serial Bus* at the following link:

https://usb.org/sites/default/files/SuperSpeedPHYComplianceTest_Spec1_0a.pdf

For SuperSpeed+ TX Electrical Tests, refer to sections: TD 1.4, TD 1.5, and TD1.7 in the *Electrical Compliance Test Specification Enhanced SuperSpeed Universal Serial Bus* at the following link:

https://www.usb.org/sites/default/files/EnhancedSuperSpeedPHYComplianceTestSpec.pdf

Follow these steps to place the device under test into compliance mode:

1. Boot up the DUT. Ensure the USB 3.x (3.0 for SS or 3.1 for SS+) Host Test Fixture is not connected to the DUT.
2. Install the latest OS (Linux, for example) image for the Jetson AGX Xavier module.
3. Install the devmem2 tool (for the Linux installed in Step 2, for example) by running the following command.

```
$ sudo apt-get install devmem2
```

4. Launch the USB 3.1 Compliance Test Software on the scope.
5. Disable the auto suspend for the controllers:

```
$ echo on > /sys/bus/usb/devices/usb1/power/control
$ echo on > /sys/bus/usb/devices/usb2/power/control
```

6. Enter compliance test mode.

```
$ ./devmem2 0x03610420 w 0x10340
$ ./devmem2 0x03610440 w 0x10340
$ ./devmem2 0x03610450 w 0x10340
```

7. Plug in the USB 3.x Host test fixture to DUT. The other end of fixture should be connected to a scope such that DUT TX+/- with 50 ohm termination on the scope.

   For connection details refer to the "Transmitter Test Topologies" section in the document, *USB 3.0 Electrical Test Fixture Topologies*, at the following link:

   https://www.usb.org/sites/default/files/documents/superspeedtesttopologies.pdf

   For SuperSpeed+ Compliance testing, refer to the "TX Tests" section in the document, *USB3p1_fixture_topologies_11-8-2017_0.pdf*, at the following link for connection topology:

   https://www.usb.org/document-library/usb-31-electrical-test-fixture-topology

8. Use ./devmem2 0x3610420 (i.e. for port 0) command to read back the LTSSM state.

Note: The Jetson AGX Xavier module contains three USB 3.1 ports; their PORTSC offset and pin # are:

- UPHY_TX/RX1 (pins C22/C23/G22/G23), offset = 0x440
- UPHY_TX/RX6 (pins B17/B16/K16/K17), offset = 0x420
- UPHY_TX/RX11 (pins D13/D12/H13/H12), offset = 0x450

Writing 0x10340 will change the internal state of XUSB. Therefore, it is not expected to read back the same value. However, Bits[8:5] should be set to 0xA for compliance test mode, otherwise repeat Steps 1 through 7.

9. Connect RX+/- to external Ping.LFPS (20 MHz frequency; 2 periods) signal generator.

   Sending a **PING.LFPS** to the RX port of the DUT in compliance state will cause the compliance pattern to transition to next one. Contact generator vendor for support to provide required number of **Ping.LFPS** till controller pumps out the required compliance pattern.

10. Based on compliance pattern (CP) requirement for the current test, repeat Step 9 to pump out required CP pattern.
11. Let the test complete.

Placing the Jetson AGX Xavier Module USB 3.1 Controller in Loopback Mode

To run the RX electrical JTOL test, the Jetson AGX Xavier module must be trained to loopback mode.

For SuperSpeed RX Electrical Tests, refer to Sections: TD 1.2 and TD.1.5 in the document, *Electrical Compliance Test Specification SuperSpeed Universal Serial Bus Rev 1.0a*, at the following link:

https://usb.org/sites/default/files/SuperSpeedPHYComplianceTest_Spec1_0a.pdf

For SuperSpeed+ RX Electrical Tests, refer to Section TD 1.10 in the *Electrical Compliance Test Specification Enhanced SuperSpeed Universal Serial Bus* at the following link:

https://www.usb.org/sites/default/files/EnhancedSuperSpeedPHYComplianceTestSpec.pdf

Follow these steps to place the device under test into loopback mode:

1. Boot up the DUT. Make sure that the USB 3.x Host Test Fixture is not connected to the DUT.
2. Install the latest Linux image for Jetson AGX Xavier module.
3. Run the following script to disable power management for USB Host Controller.

```
#!/bin/sh
for hub in $(ls -d /sys/bus/usb/devices/usb?); do
echo on > $hub/power/control
done
```

4. Configure BERT to pump out the loopback training sequence, refer to Steps 5 through 11 in Section "TD.1.5 Receiver Jitter Tolerance Test" of the following specification:

   https://usb.org/sites/default/files/SuperSpeedPHYComplianceTest_Spec1_0a.pdf

   For SuperSpeed+, upon detecting DUT Power On, refer to Steps 14 through 18 in Section "TD.1.10 Receiver Jitter Tolerance Test at 10 GT/s" of the following specification:

   https://www.usb.org/sites/default/files/EnhancedSuperSpeedPHYComplianceTestSpec.pdf

5. Connect the USB 3.x Host Test Fixture to the DUT.

   For fixture topologies and connections for Superspeed RX testing, refer to the following: https://www.usb.org/document-library/usb-31-electrical-test-fixture-topology
6. Start JTOL test after the controller is in loopback or repeat Steps 1 through 5.
7. Let the test complete.

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