NVIDIA Jetson AGX Xavier Series PCIe Endpoint Design Guidelines

Application Note

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Document History

DA-09357-001_v1.3

Version	Date	Description of Change
1.0	February 21, 2019	Initial Release
1.1	June 14, 2019	• Updated to include all Jetson AGX Xavier series modules • Updated document to current NVIDIA standard
1.2	May 5, 2020	• Updated Figure 2 to show where board should be separated and added note • Added "Jetson AGX Xavier Developer Kit Configured as PCIe Card"
1.3	September 18, 2020	Removed mention of C0/C4 as possible Endpoints

Table of Contents

List of Figures

Overview

This application note contains design guidelines and example connections for using the NVIDIA® Jetson AGX Xavier™ series system with a PCIe interface configured as an Endpoint.

Notes: This application note provides information to enable our customers to develop a system with a PCIe interface configured as an Endpoint. Refer to the NVIDIA software documentation for support provided. Developers should feel free to select proper components and implement their software based on NVIDIA's design information.

References to Jetson AGX Xavier apply to any of the Jetson AGX Xavier series of modules except where explicitly noted.

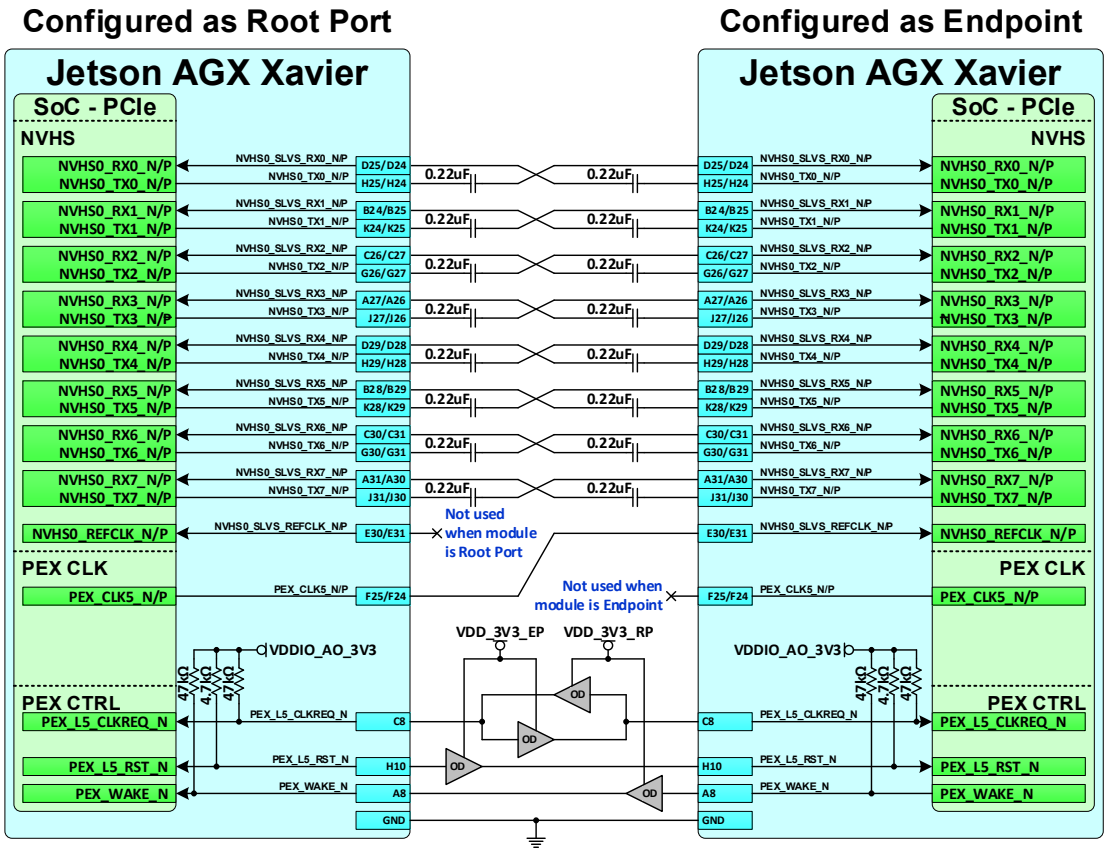
A Jetson AGX Xavier configured as an Endpoint can connect to another configured as Root Port. Endpoint support is only possible on the PCIe Controller C5 (x8). Figure 1 shows the basic connections required to connect two Jetson AGX Xavier modules with one configured as Root Port and the other as Endpoint. Instead of the Jetson AGX Xavier Root Port, a PCIe slot on a PC or similar system could be used.

The connections require that the TX lines of the Root Port are routed to the RX lines of the Endpoint and RX of Root Port routed to TX on the Endpoint. In addition, buffers are required on the control signals to ensure that the module pins are not driven prematurely as the two devices are powered up, which may not be simultaneously. These connections can be achieved in a variety of ways as follows.

- An NVIDIA Jetson AGX Xavier Developer Kit (or equivalent) and a custom PCIe board that includes a module connector and necessary power/control logic plus the necessary TX/RX swap and control signal buffers shown in the block diagram.
- A custom carrier board with two Jetson AGX Xavier connectors with the TX/RX swap and control signal buffers shown in the block diagram implemented on the carrier board itself.
- Two NVIDIA Jetson AGX Xavier Developer Kits (or equivalent) and a separate board (or board + cable) that has the TX/RX swap and control signal buffering. This configuration is described in the following sections. Care must be taken not to connect the powers on the two ends of the swap board.

The NVIDIA Developer Kit carrier board has a mux to select either **PEX_CLK5_P/N** or **NVHS_SLVS_REFCLK_P/N** to be routed to the PCIe connector **REFCLK** pins (A13 and A14). The mux should be set to select **PEX_CLK5_N/P** if the Jetson AGX Xavier will be the Root Port or **NVHS_SLVS_REFCLK_P/N** if it will be the Endpoint.

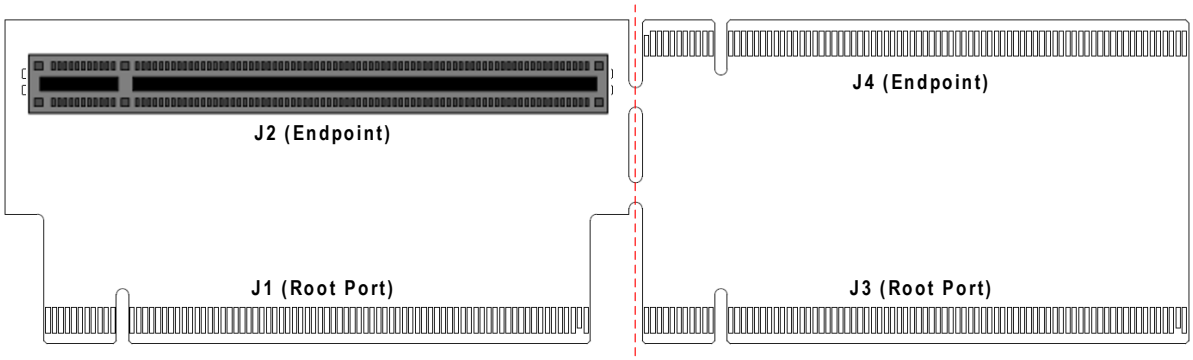
Figure 1. Jetson AGX Xavier Root Port Jetson AGX Xavier Endpoint



Note: If the two Jetson AGX Xavier devices shown in Figure 1 are on separate systems, then the power rails should not be connected between the two. The grounds for each system should be connected.

One example of a board that swaps the PCIe TX/RX lines and provides the proper buffering for the control signals is the NVIDIA E3317_A01. The schematics are attached to this application note. The E3317 provides two options in one design. One is for a PCIe x16 edge fingers on the Root Port side (J1 in Figure 2) and PCIe x16 edge connector on the Endpoint side (J2 in Figure 2). The other option is PCIe x16 edge fingers on both sides (J3 on bottom right is for the Root Port side and J4 on top right is for the Endpoint side, as shown in Figure 2.

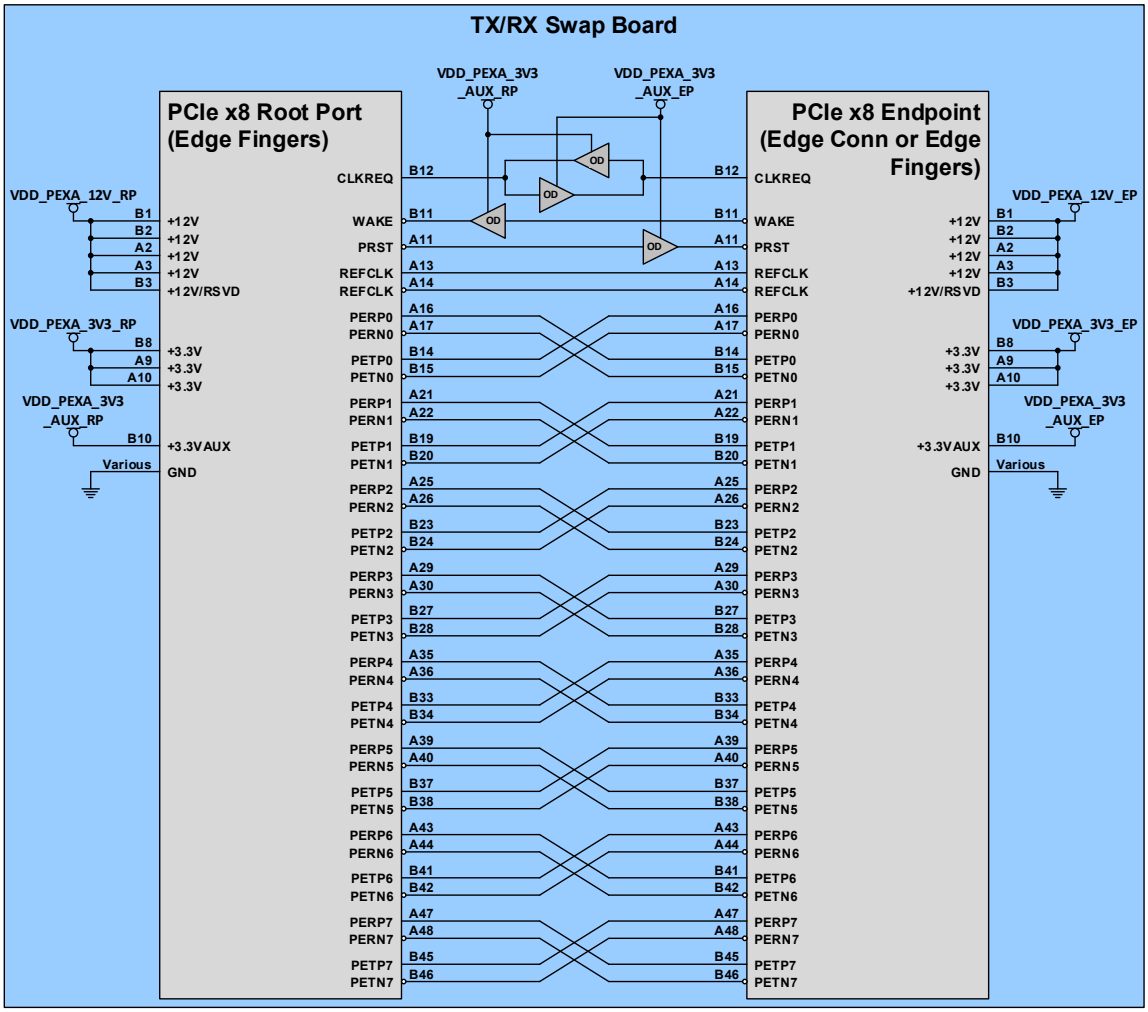
Figure 2. E3317_A01 RX/TX Swap Board



Note: The E3317 board shown in Figure 2 includes two options: Edge card to PCIe connector or edge card to edge card. These are separate options and the board should be separated at the center (dotted line).

The following figure shows the connections implemented on the TX/RX swap board. Note that the power rails of each connector have different net-names, so they are not connected. This can be seen in the attached schematics as well. The power rails for each end should not be tied together as they will likely come up at different times.

Figure 3. TX/RX Swap Board Connections



Note: The power rails are not connected since both the Root Port and Endpoint systems will provide power to their respective PCIe connectors. This will avoid possible issues with power being applied by the first system to power-up to pins in the other system that has not yet been powered up.

In the case where two NVIDIA Jetson AGX Xavier Developer Kit carrier boards (or equivalent) are to be connected via PCIe, the TX/RX swap board would be plugged into the available PCIe x16 edge connector on the platform to be configured as a PCIe Root Port. If the TX/RX swap board with a connector on one side is used, a PCIe x8 or x16 jumper cable with PCIe edge fingers on either end is plugged into the TX/RX swap board on one end, and the other Jetson AGX Xavier which is to be configured as the PCIe Endpoint. If the TX/RX swap board with edge fingers is used, the cable is not required, or a different cable with a connector on one end and edge fingers on the other is required. The TX/RX swap board with a connector and PCIe jumper cable are shown in the following figures.

Figure 4. TX/RX Swap Module and PCIe Male-to-Male x8 Cable Assembly – Top

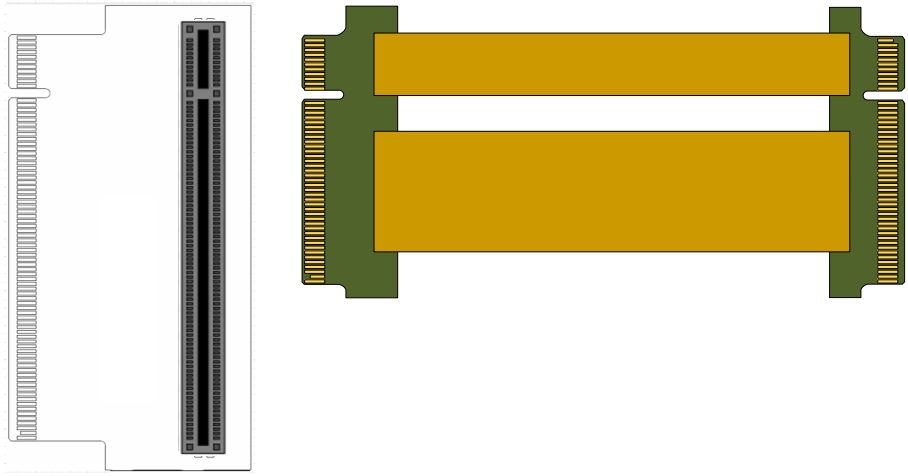


Figure 5. PCIe Male-to-Male x8 Cable Assembly – Side

Figure 6 shows two Jetson AGX Xavier Developer Kits connected together as described.

Figure 6. Jetson AGX Xavier Developer Kit-to-Developer Kit Connections (with Edge-to-Connector Board and Cable)

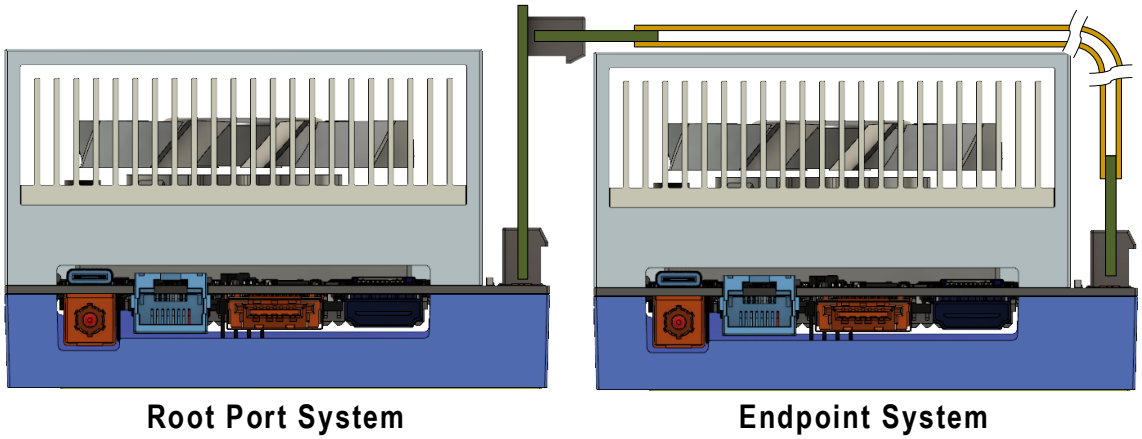
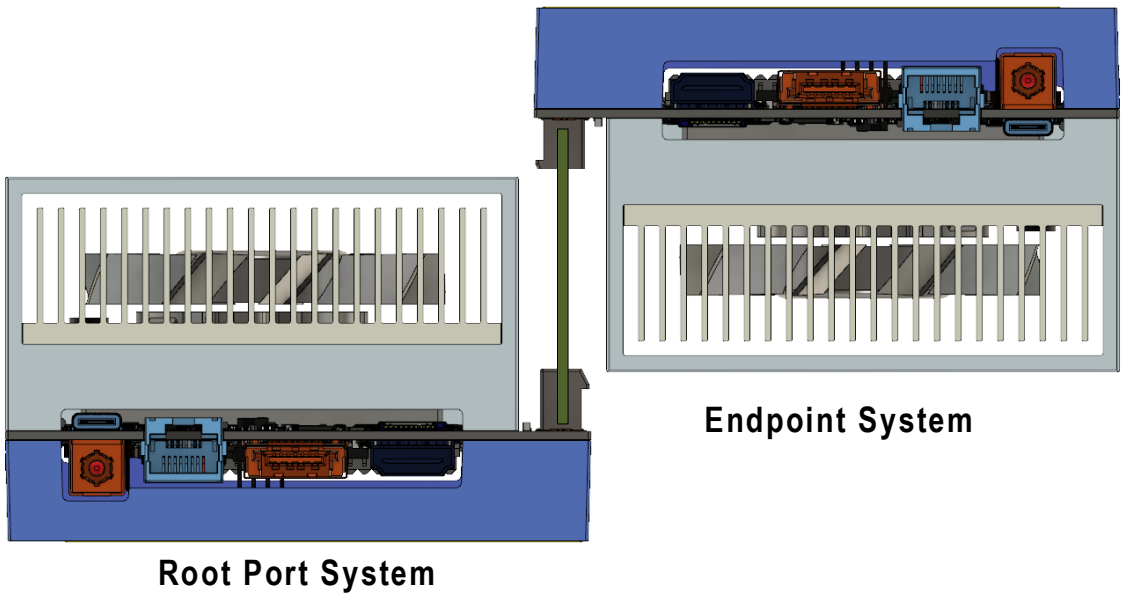


Figure 7. Jetson AGX Xavier Developer Kit-to-Developer Kit Connections (with Edge-to-Edge and no Cable)



Attachments

The following files are attached to this application note.

- Assembly drawing (242-83317-1000-A01#5.pdf)
- Schematics (602-83317-1000-A01.pdf)

To access the attached files, click the **Attachment** icon on the left-hand toolbar on this PDF (using Adobe Acrobat Reader or Adobe Acrobat). Select the file and use the Tool Bar options (**Open, Save**) to retrieve the documents. Files with the .nvzip extension can be extracted using 7-Zip file archive software, or may be renamed to .zip and extracted with other archive software

Software Considerations

A few software issues should be considered when configuring the Jetson AGX Xavier platform(s).

- If the approach used is to have two separate systems, with one of them being a Jetson AGX Xavier platform configured as an Endpoint, then the Endpoint system should be powered up first. This will allow the Endpoint to have been properly initialized before the Root Port system comes up and attempts to enumerate it. If the Endpoint is powered after the Root Port, then the Root Port system should be restarted to allow the proper enumeration to occur.
- If the Jetson AGX Xavier platform or platforms have the clock mux described previously, which is present on the NVIDIA Developer Kit carrier board, then it needs to be configured correctly after boot. This mux selects either **PEX_CLK5_P/N** (Root Port end) or **NVHS_SLVS_REFCLK_P/N** (Endpoint end) to be routed to the PCIe connector **REFCLK** pins (A13 and A14).

Jetson AGX Xavier Developer Kit Configured as PCIe Card

This chapter describes how to configure a Jetson AGX Xavier Developer Kit and TX/RX swap board to work as a PCIe add-in-card. The following description assumes a TX/RX board that is the equivalent of the E3317_A01 design attached to this application note.

Setup and Connections

The developer kit modifications listed are made on the Endpoint Developer Kit. The modifications to the TX/RX board refer to the reference designators on the E3317_A01 reference design. A PC is assumed as the Root Port system, but another Jetson AGX Xavier Developer Kit left in the default Root Port configuration can be used instead. If a PC is used, the PCIe slot should be a 75 W type to provide adequate power for the Endpoint Developer Kit.

1. Flash the developer kit to be used as Endpoint with latest software. See the "Jetson AGX Xavier PCIe Endpoint Mode" section of the NVIDIA Jetson Linux Developer Guide.
2. Rework the developer kit carrier board to connect the power source (DC Jack) to +12V rail on PCIe slot.
   a). Short VDD_12V (C506.1, C510.1, C513.1) with VCC_DCIN (J2.1)
   b). Short Q87.1, Q87.2 and Q87.3 together, to disable VDD_12V regulator U9 on carrier board and drive PRSNT2 low
3. Rework TX/RX board to enable +12V rail connection.
   a). Stuff R5 with a 0Ω resistor to enable the +12V connection
4. Connect reworked developer kit to a PC PCIe slot using the TX/RX swap board.
5. Connect a USB port on the PC system to the Endpoint Developer Kit debug port using a USB Type-A to Micro-B cable.
6. Power the PC then power up the Endpoint Developer Kit (press the power button S501). This powers the PC which provide the +12V supply to the Endpoint Developer Kit and then powers up the Endpoint Developer Kit.
7. Login into the developer kit from the Root Port system.
   a). (PC) # minicom -D /dev/ttyUSB3
8. Check if the clock mux selects NVHS_SLVS_REFCLK_P/N.

a). (Xavier) # grep 253 /sys/kernel/debug/gpio
gpio-253 (|pex-refclk-sel-high) out hi
If gpio-253 outputs low, run below command to set it high:

b). (Xavier) # echo 253 > /sys/class/gpio/export

c). (Xavier) # echo 1 > /sys/class/gpio/gpio253/value

Bring up Developer Kit as a Page of RAM

1. Run the following commands to configure and enable the PCIe endpoint mode:
   a). (Xavier) # cd /sys/kernel/config/pci_ep/
   b). (Xavier) # mkdir functions/pci_epf_nv_test/func1
   c). (Xavier) # echo 0x10de > functions/pci_epf_nv_test/func1/vendorid
   d). (Xavier) # echo 0x0001 > functions/pci_epf_nv_test/func1/deviceid
   e). (Xavier) # ln -s functions/pci_epf_nv_test/func1 controllers/141a0000.pcie_ep/
   f). (Xavier) # echo 1 > controllers/141a0000.pcie_ep/start
2. Reboot the PC to initialize the PCIE endpoint device. This asserts the PCI reset and re-enumerates the Endpoint.
   a). (PC) # reboot
   b). Reboot done.
   c). (PC) # lspci
   06:00.0 RAM memory: NVIDIA Corporation Device 0001

Bring up Developer Kit as an Ethernet IF over PCIe

1. Run the following commands to configure and enable the PCIe endpoint mode:
   a). (Xavier) # cd /sys/kernel/config/pci_ep/
   b). (Xavier) # mkdir functions/pci_epf_tvnet/func1
   c). (Xavier) # echo 16 > functions/pci_epf_tvnet/func1/msi_interrupts
   d). (Xavier) # ln -s functions/pci_epf_tvnet/func1 controllers/141a0000.pcie_ep/
   e). (Xavier) # echo 1 > controllers/141a0000.pcie_ep/start
2. Reboot the PC to initialize the PCIe Endpoint device.
   a). (PC) # reboot
   b). Reboot done.
   c). (PC) # lspci
   06:00.0 Network controller: NVIDIA Corporation Device 2296

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