NVIDIA Jetson AGX Xavier Series Pin and Function Names Guide

Application Note

DA-09115-001_v1.1 | June 2019

Document History

DA-09115-001_v1.1

Version	Date	Description of Change
1.0	September 25, 2018	Initial Release
1.1	June 14, 2019	• Updated to include all Jetson AGX Xavier series modules • Updated document to current NVIDIA standard

Table of Contents

List of Figures

List of Tables

Introduction

The NVIDIA® Jetson AGX Xavier™ series System on Module (SOM) is built around the NVIDIA® Xavier™ System on Chip (SoC). Jetson AGX Xavier series documentation often refers to names of interfaces, pins, functions, etc., from a SOM perspective, but other documentation (for example, the TRM) will necessarily take a SoC perspective. Some documentation will reference both SOM and SoC naming. It is important to understand whether a given document is using pin names/numbers, interface names/instances, and function names/instances with reference to the SOM or to the SoC.

Note: References to Jetson AGX Xavier apply to any of the Jetson AGX Xavier series of modules.

Various documents are provided to help customers design, lay out, build, and configure NVIDIA® Jetson™ module-based designs.

Table 1 lists the main documents that are focused on the hardware or contain references to hardware features.

Table 1. Hardware References and Features Documentation

Document Category	Document Name for Jetson AGX Xavier Designs	Description
Data Sheet	Jetson AGX Xavier Series Module Data Sheet	• Module overview • Power and system management • Interface and signal description • Electrical, package, and thermal specifications
Technical Reference Manual (TRM)	Xavier (SoC) Technical Reference Manual	• Address map • Chapters per block (functional description, programming guidelines, and registers)
Product OEM Design Guide	Jetson AGX Xavier Series OEM Product Design Guide	• Power • Interface chapters (connection figures and tables, and routing guidelines)
Carrier Board Specification	Jetson AGX Xavier Developer Kit Carrier Board Specification	• Developer Kit features and description • Expansion connector and interface descriptions • Power allocation

Document Category	Document Name for Jetson AGX Xavier Designs	Description
Pinmux	Jetson AGX Xavier Series Module Pinmux	• Module pin name and number, SoC ball name • SFIO and GPIO options • Wakes, straps POR state
Design files	Jetson AGX Xavier Developer Kit Carrier Board Design Files	• Schematics, layout, bill of materials (BOM) • Misc (Assy drawing, stack-up, gerbers, etc)

Pin and Function Names

There are different pin and interface names in many cases on the module vs. chip. Some documents are based on the chip, such as the TRM, while others are based on the module, or may have both chip and module terms and names. This can lead to confusion. It is important to use the right document and to understand whether a term or name is associated with a chip, module pin name or number, an interface name or instance, or a function name or instance.

Pinmux

The Jetson AGX Xavier module pinmux (pin multiplexing) spread sheet has the module pin names and pin numbers in the first two columns, and the SoC ball name in the 3rd column. The GPIOs and SFIO functions are covered in the pin muxing area. The portion of the pinmux in Table 2 includes one of the I2S interfaces.

Table 2. Pin Mux I2S and MCLK

		MPIO	Pin Muxing				
Signal Name	**Pin #**	**SoC Ball Name**	**GPIO**	**SFIO0**	**SFIO1**	**SFIO2**	**SFIO3**
I2S1_CLK	L14	DAP1_SCLK	GPIO3_PS.00	I2S1_SCLK	–	–	–
I2S1_SDOUT	C7	DAP1_DOUT	GPIO3_PS.01	I2S1_SDATA_OUT	–	–	–
I2S1_SDIN	H8	DAP1_DIN	GPIO3_PS.02	I2S1_SDATA_IN	–	–	–
I2S1_FS	D8	DAP1_FS	GPIO3_PS.03	I2S1_LRCK	–	–	–
MCLK01	H9	AUD_MCLK	GPIO3_PS.04	AUD_MCLK	–	–	–

In the case shown in Table 2, for one of the I2S interfaces that are available on the module pins, the following pin/function names exist:

- Module signal names: I2S1_xxx
- SoC chip pin names: DAP1_xxx
- SFIO 0 function names: I2S1_xxx

This shows that the module pin names, chip pin names, and function names can be different. When referring to the various documents, it is important to understand which name form is applicable. For instance, if the TRM is accessed for information on how to configure the pins or functions, it is necessary to know that the TRM is chip-focused. It will have SoC pin names when referring to the pins, such as in the "Pinmux Register" section, or function names if the function is being configured. In the case of the module data sheet, the module pin names are relevant. See the following "TRM" and "Data Sheet" sections for details.

Data Sheet

The module data sheet only uses the module pin names. If a programmer needed to know what SoC function to configure, it would be necessary to look at either the pinmux spreadsheet or OEM product design guide to know what SoC function is associated with that module pin.

Table 3. Data Sheet I2S1 and MCLK Pin Descriptions

Ball	Signal	Usage/Description	Wake	Strap	Group	Voltage	Direction
C7	I2S1_SDOUT	I2S Audio Port 1 Left/Right Clock			VDDIO_AUDIO	1.8	Bi-Dir
D8	I2S1_FS	I2S Audio Port 1 Data In			VDDIO_AUDIO	1.8	Input
H8	I2S1_SDIN	I2S Audio Port 1 Data Out			VDDIO_AUDIO	1.8	Output
L14	I2S1_CLK	I2S Audio Port 1 Clock			VDDIO_AUDIO	1.8	Bi-Dir
H9	MCLK01	Audio Codec Master Clock			VDDIO_AUDIO	1.8	Output

Technical Reference Manual

The technical reference manual (TRM) is based on the chip (for example, SoC X2). References to pin names (such as DAP1) will be chip pin names. There are also references to functions (such as I2S1). These should match the names of functions in the pinmux spreadsheet or OEM product design guide. To know what pin on the module an SoC pin is associated with, the pinmux spreadsheet is the best cross reference, although the OEM product design guide has that information as well.

PADCTL_AUDIO_DAP1_FS_0

Offset: 0x28
Read/Write: R/W
Parity Protection: N
SCR Protection: SCR_DAP1_FS_0
Reset: 0x00000454 (0bxxxx,xxxx,xxxx,xxxx,xxx0,x1x0,x1x1,0100)

1:0	I2S1	**PM**: **0** = I2S1 **1** = RSVD1 **2** = RSVD2 **3** = RSVD3

OEM Product Design Guide

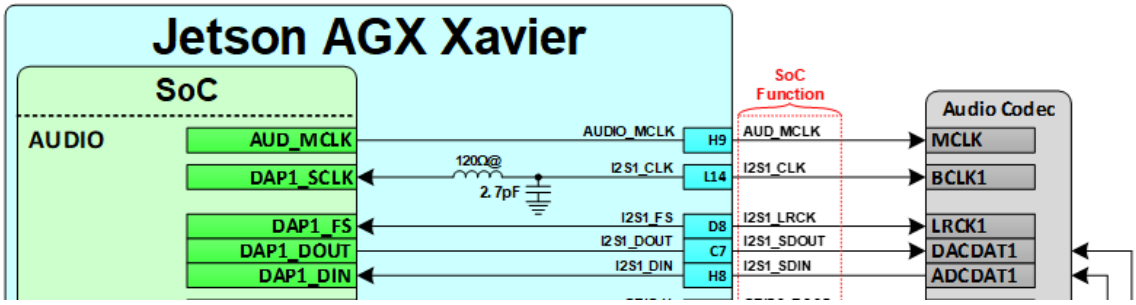
The OEM product design guide focuses on the module, but many of the figures and pin description tables also include the SoC signal associated with a module pin where applicable. The partial table (Table 4) contains the same I2S interface used as the example in the earlier document sections. Both the module (Jetson AGX Xavier) and SoC pin names are shown.

Table 4. OEM Design Guide Audio I2S and MCLK Pin Descriptions

Pin #	Module Pin Name	SoC Signal	Usage/Description	Usage on Carrier Board	Direction	Pin Type
H9	MCLK01	AUD_MCLK	Audio Codec Master Clock	Audio Codec	Output	CMOS – 1.8V
L14	I2S1_CLK	DAP1_SCLK	I2S Audio Port 1 Clock	Audio Codec	Bidir	CMOS – 1.8V
D8	I2S1_FS	DAP1_FS	I2S Audio Port 1 Data In	Audio Codec	Bidir	CMOS – 1.8V
H8	I2S1_SDIN	DAP1_DIN	I2S Audio Port 1 Data Out	Audio Codec	Input	CMOS – 1.8V
C7	I2S1_SDOUT	DAP1_DOUT	I2S Audio Port 1 Left/Right Clock	Audio Codec	Output	CMOS – 1.8V

Figure 1 also shows the I2S interface and includes the chip and module pin names. In addition, the reference schematic net names are used outside the module. The net names may match the form used for the chip pin names, as in the following example, but not in all cases.

Figure 1. I2S1 Interface



The following audio connections table contains only the module pin names, or function names in parenthesis if necessary, for clarity.

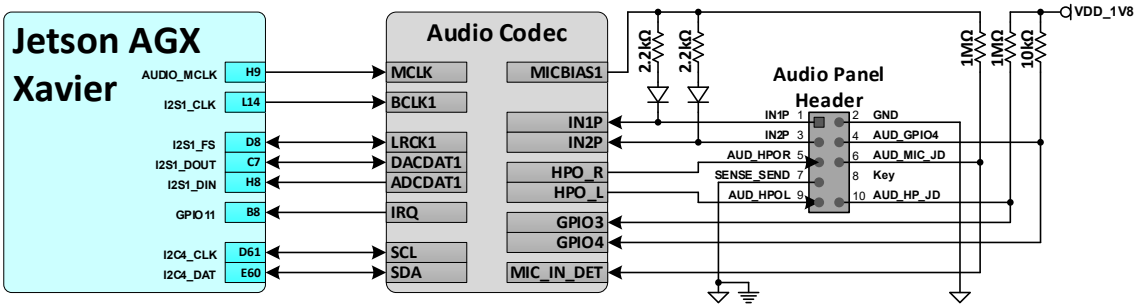
Table 5. OEM Design Guide Audio I2S and MCLK Signal Connections

Module Pin Name (SoC Function)	Type	Termination	Description
I2S1_SCLK (I2S1_CLK) I2S2_SCLK (I2S2_CLK) I2S3_SCLK (I2S4_CLK) GPIO21 (I2S6_CLK)	I/O	120Ω Bead in series and 2.7pF capacitor to GND (on module).	I2S Serial Clock: Connect to I2S/PCM CLK pin of audio device.
I2S1_FS (I2S1_LRCK) I2S2_FS (I2S2_LRCK) I2S3_FS (I2S4_LRCK) GPIO20 (I2S6_LRCK)	I/O		I2S Left/Right Clock: Connect to Left/Right Clock pin of audio device.
I2S1_DOUT (I2S1_SDOUT) I2S2_DOUT (I2S2_SDOUT) I2S3_DOUT (I2S4_SDOUT) GPIO05 (I2S6_SDOUT)	I/O		I2S Data Output: Connect to Data Input pin of audio device.
I2S1_DIN (I2S1_SDIN) I2S2_DIN (I2S2_SDIN) I2S3_DIN (I2S4_SDIN) GPIO04 (I2S6_SDIN)	I		I2S Data Input: Connect to Data Output pin of audio device.
AUD_MCLK	O		Audio Codec Master Clock: Connect to clock pin of Audio Codec.
GPIO20_AUD_INT	I		Audio Interrupt: Connect to interrupt pin of Audio Codec.

Developer Kit Carrier Board Specification

The developer kit specification uses module (Jetson AGX Xavier) pin names and net names from the carrier board reference design. If it is necessary to know the corresponding SoC name or function, the pinmux should be referenced (the OEM product design guide also contains this information).

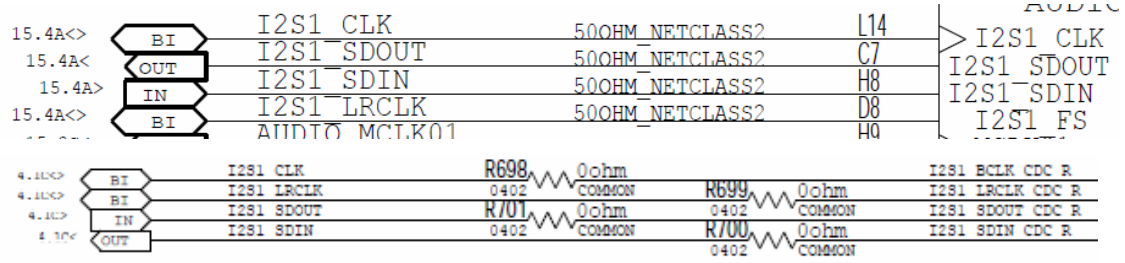
Figure 2. I2S and MCLK Connections to Audio Codec on Carrier Board



Design Files

The design files (schematics, layout, etc.) also contain only module pin names and net names. Look to the pinmux or OEM design guide if it is necessary to know which chip pin is associated with a module pin name.

Figure 3. Design Schematics



Chip, Module, and Carrier Board Pin Names and Numbers

The information provided in the following table can be found in various hardware documentation (as described within this application note). Table 6 provides a consolidation of this information for your convenience.

Table 6. Chip, Module, and Carrier Board Pinout

Conn. Pin #	Carrier Board Symbol Pin Name	Carrier Board Net Name	SoC Pin Name
A3	PRSNT0	na (GND)	–
A4	SDCARD_D2	SDMMC1_DAT2	SDMMC1_DAT2
A5	SDCARD_CMD	SDMMC1_CMD	SDMMC1_CMD
A6	UFS0_REF_CLK	UFS0_REF_CLK	UFS0_REF_CLK
A7	GPIO29	GPIO29_M2_KEYM_PEWAKE*	SOC_GPIO31
A8	PEX_WAKE_N	PEX_WAKE_N	PEX_WAKE_N
A9	GND	GND	–
A10	USB2_P	USB2_DP	USB2_DP
A11	USB2_N	USB2_DN	USB2_DN
A12	GND	GND	–
A13	GND	GND	–
A14	UPHY_RX8_N	SNN_UPHY_RX8_N	PEX_RX8_N
A15	UPHY_RX8_P	SNN_UPHY_RX8_P	PEX_RX8_P
A16	GND	GND	–
A17	GND	GND	–
A18	UPHY_RX4_P	UPHY_RX4_P	PEX_RX4_P
A19	UPHY_RX4_N	UPHY_RX4_N	PEX_RX4_N
A20	GND	GND	–
A21	GND	GND	–
A22	UPHY_RX0_P	UPHY_RX0_P	PEX_RX0_P
A23	UPHY_RX0_N	UPHY_RX0_N	PEX_RX0_N

Conn. Pin #	Carrier Board Symbol Pin Name	Carrier Board Net Name	SoC Pin Name
A24	GND	GND	–
A25	GND	GND	–
A26	NVHS0_SLVS_RX3_P	NVHS0_SLVS_RX3_P	NVHS0_RX3_P
A27	NVHS0_SLVS_RX3_N	NVHS0_SLVS_RX3_N	NVHS0_RX3_N
A28	GND	GND	–
A29	GND	GND	–
A30	NVHS0_SLVS_RX7_P	NVHS0_SLVS_RX7_P	NVHS0_RX7_P
A31	NVHS0_SLVS_RX7_N	NVHS0_SLVS_RX7_N	NVHS0_RX7_N
A32	GND	GND	–
A33	GND	GND	–
A34	NVHS1_SLVS_RX3_P	SNN_NVHS1_SLVS_RX3_P	–
A35	NVHS1_SLVS_RX3_N	SNN_NVHS1_SLVS_RX3_N	–
A36	GND	GND	–
A37	GND	GND	–
A38	NVHS1_SLVS_RX7_P	SNN_NVHS1_SLVS_RX7_P	–
A39	NVHS1_SLVS_RX7_N	SNN_NVHS1_SLVS_RX7_N	–
A40	GND	GND	–
A41	CSI2_D0_P	CSI_2_D0_P	CSI_C_D0_P
A42	CSI2_D0_N	CSI_2_D0_N	CSI_C_D0_N
A43	GND	GND	–
A44	CSI7_D0_P	CSI_7_D0_P	CSI_H_D0_P
A45	CSI7_D0_N	CSI_7_D0_N	CSI_H_D0_N
A46	GND	GND	–
A47	HDMI_DP1_TX0_P	DP1_TXP0	HDMI_DP1_TXDP0
A48	HDMI_DP1_TX0_N	DP1_TXN0	HDMI_DP1_TXDN0
A49	GND	GND	–
A50	HDMI_DP2_TX2_N	HDMI_DP2_TXN2	HDMI_DP2_TXDN2
A51	HDMI_DP2_TX2_P	HDMI_DP2_TXP2	HDMI_DP2_TXDP2
A52	GND	GND	–
A53	I2C5_CLK	I2C_GP5_CLK	DP_AUX_CH3_P
A54	GPIO17	GPIO17_40HEADER	SOC_GPIO21
A55	GPIO34	GPIO34_M2_KEYM_ALERT*	SOC_GPIO06
A56	SPI1_MISO	SPI1_MISO	SPI1_MISO
A57	UART2_CTS	UART2_CTS	UART2_CTS
A58	GPIO20	GPIO20_5V0_HDMI_EN	DAP6_FS
A59	GPIO05	GPIO05_VDD_12V_ENABLE	DAP6_DOUT
A60	JTAG_TCK	JTAG_TCK	JTAG_TCK
A61	SYSTEM_OC_N	SYSTEM_OC_N	BATT_OC

Conn. Pin #	Carrier Board Symbol Pin Name	Carrier Board Net Name	SoC Pin Name
A62	GPIO10	GPIO10_INC_INT_CCG2	CAN1_WAKE
A63	GND	GND	–
B3	SYS_VIN_HV	VCC_SRC	–
B4	GND	GND	–
B5	RGMII_TXC	RGMII_TXC	EQOS_TXC
B6	SDCARD_CLK	SDMMC1_CLK	SDMMC1_CLK
B7	GND	GND	–
B8	GPIO11	GPIO11_CODEC_INT	SOC_GPIO30
B9	PEX_L1_RST_N	PEX_L1_RST_N	PEX_L1_RST_N
B10	SATA_DEV_SLP	SNN_SATA_DEV_SLP	SATA_DEV_SLP
B11	GND	GND	–
B12	UPHY_RX10_P	UPHY_RX10_P	PEX_RX10_P
B13	UPHY_RX10_N	UPHY_RX10_N	PEX_RX10_N
B14	GND	GND	–
B15	GND	GND	–
B16	UPHY_RX6_P	UPHY_RX6_P	PEX_RX6_P
B17	UPHY_RX6_N	UPHY_RX6_N	PEX_RX6_N
B18	GND	GND	–
B19	GND	GND	–
B20	UPHY_RX2_N	UPHY_RX2_N	PEX_RX2_N
B21	UPHY_RX2_P	UPHY_RX2_P	PEX_RX2_P
B22	GND	GND	–
B23	GND	GND	–
B24	NVHS0_SLVS_RX1_N	NVHS0_SLVS_RX1_N	NVHS0_RX1_N
B25	NVHS0_SLVS_RX1_P	NVHS0_SLVS_RX1_P	NVHS0_RX1_P
B26	GND	GND	–
B27	GND	GND	–
B28	NVHS0_SLVS_RX5_N	NVHS0_SLVS_RX5_N	NVHS0_RX5_N
B29	NVHS0_SLVS_RX5_P	NVHS0_SLVS_RX5_P	NVHS0_RX5_P
B30	GND	GND	–
B31	GND	GND	–
B32	NVHS1_SLVS_RX1_N	SNN_NVHS1_SLVS_RX1_N	–
B33	NVHS1_SLVS_RX1_P	SNN_NVHS1_SLVS_RX1_P	–
B34	GND	GND	–
B35	GND	GND	–
B36	NVHS1_SLVS_RX5_N	SNN_NVHS1_SLVS_RX5_N	–
B37	NVHS1_SLVS_RX5_P	SNN_NVHS1_SLVS_RX5_P	–
B38	GND	GND	–

Conn. Pin #	Carrier Board Symbol Pin Name	Carrier Board Net Name	SoC Pin Name
B39	GND	GND	–
B40	MID4	SNN_MID_4	–
B41	GND	GND	–
B42	CSI2_CLK_N	CSI_2_CLK_N	CSI_C_CLK_N
B43	CSI2_CLK_P	CSI_2_CLK_P	CSI_C_CLK_P
B44	GND	GND	–
B45	CSI7_CLK_P	CSI_7_CLK_P	CSI_H_CLK_P
B46	CSI7_CLK_N	CSI_7_CLK_N	CSI_H_CLK_N
B47	GND	GND	–
B48	HDMI_DP1_TX1_N	DP1_TXN1	HDMI_DP1_TXDN1
B49	HDMI_DP1_TX1_P	DP1_TXP1	HDMI_DP1_TXDP1
B50	GND	GND	–
B51	HDMI_DP2_TX1_P	HDMI_DP2_TXP1	HDMI_DP2_TXDP1
B52	HDMI_DP2_TX1_N	HDMI_DP2_TXN1	HDMI_DP2_TXDN1
B53	GND	GND	–
B54	WDT_RESET_OUT_N	SNN_WDT_RESET_OUT_N	SOC_GPIO23
B55	GPIO30	GPIO30_M2_E_ALERT_R*	SOC_GPIO20
B56	SPI1_CS1_N	SPI1_CS1	SPI1_CS1
B57	GND	GND	–
B58	GPIO21	GPIO21_SD_POWER_SW_ON	DAP6_SCLK
B59	GPIO04	GPIO04	DAP6_DIN
B60	JTAG_TDI	JTAG_TDI	JTAG_TDI
B61	CAN1_DIN	CAN1_DIN	CAN1_DIN
B62	GPIO08	GPIO08_AO_DMIC_IN_DAT	CAN1_STB
B63	SYS_VIN_HV	VCC_SRC	–
C1	SYS_VIN_HV	VCC_SRC	–
C2	SYS_VIN_HV	VCC_SRC	–
C3	GND	GND	–
C4	RGMII_RD0	RGMII_RD0	EQOS_RD0
C5	RGMII_RXC	RGMII_RXC	EQOS_RXC
C6	UFS0_RST_N	SNN_UFS0_RST	UFS0_RST
C7	I2S1_SDOUT	I2S1_SDOUT	DAP1_FS
C8	PEX_L5_CLKREQ_N	PEX_L5_CLKREQ_N	PEX_L5_CLKREQ_N
C9	GND	GND	–
C10	USB1_N	USB1_DN	USB1_DN
C11	USB1_P	USB1_DP	USB1_DP
C12	GND	GND	–
C13	GND	GND	–

Conn. Pin #	Carrier Board Symbol Pin Name	Carrier Board Net Name	SoC Pin Name
C14	UPHY_RX9_N	SNN_UPHY_RX9_N	PEX_RX9_N
C15	UPHY_RX9_P	SNN_UPHY_RX9_P	PEX_RX9_P
C16	GND	GND	–
C17	GND	GND	–
C18	UPHY_RX5_N	UPHY_RX5_N	PEX_RX5_N
C19	UPHY_RX5_P	UPHY_RX5_P	PEX_RX5_P
C20	GND	GND	–
C21	GND	GND	–
C22	UPHY_RX1_N	UPHY_RX1_N	PEX_RX1_N
C23	UPHY_RX1_P	UPHY_RX1_P	PEX_RX1_P
C24	GND	GND	–
C25	GND	GND	–
C26	NVHS0_SLVS_RX2_N	NVHS0_SLVS_RX2_N	NVHS0_RX2_N
C27	NVHS0_SLVS_RX2_P	NVHS0_SLVS_RX2_P	NVHS0_RX2_P
C28	GND	GND	–
C29	GND	GND	–
C30	NVHS0_SLVS_RX6_N	NVHS0_SLVS_RX6_N	NVHS0_RX6_N
C31	NVHS0_SLVS_RX6_P	NVHS0_SLVS_RX6_P	NVHS0_RX6_P
C32	GND	GND	–
C33	GND	GND	–
C34	NVHS1_SLVS_RX0_P	SNN_NVHS1_SLVS_RX0_P	–
C35	NVHS1_SLVS_RX0_N	SNN_NVHS1_SLVS_RX0_N	–
C36	GND	GND	–
C37	GND	GND	–
C38	NVHS1_SLVS_RX6_N	SNN_NVHS1_SLVS_RX6_N	–
C39	NVHS1_SLVS_RX6_P	SNN_NVHS1_SLVS_RX6_P	–
C40	GND	GND	–
C41	CSI2_D1_N	CSI_2_D1_N	CSI_C_D1_N
C42	CSI2_D1_P	CSI_2_D1_P	CSI_C_D1_P
C43	GND	GND	–
C44	CSI5_CLK_P	CSI_5_CLK_P	CSI_F_CLK_P
C45	CSI5_CLK_N	CSI_5_CLK_N	CSI_F_CLK_N
C46	GND	GND	–
C47	CSI7_D1_P	CSI_7_D1_P	CSI_H_D1_P
C48	CSI7_D1_N	CSI_7_D1_N	CSI_H_D1_N
C49	GND	GND	–
C50	HDMI_DP2_TX3_N	HDMI_DP2_TXN3	HDMI_DP2_TXDN3
C51	HDMI_DP2_TX3_P	HDMI_DP2_TXP3	HDMI_DP2_TXDP3

Conn. Pin #	Carrier Board Symbol Pin Name	Carrier Board Net Name	SoC Pin Name
C52	GND	GND	–
C53	I2C5_DAT	I2C_GP5_DAT	DP_AUX_CH3_N
C54	GPIO33	GPIO33_CCG4_RST_IN*	SOC_GPIO05
C55	GPIO18	GPIO18_SLVS_HSYNC	SOC_GPIO40
C56	UART2_RX	UART2_RX	UART2_RX
C57	SPI3_CS0_N	PWM2_40PIN_BACKUP	SPI3_CS0
C58	UART2_TX	UART2_TX	UART2_TX
C59	I2S3_SCLK	I2S3_SCLK	DAP4_SCLK
C60	I2S3_FS	I2S3_FS	DAP4_FS
C61	GPIO09	GPIO09_CAN1_GPIO0	CAN1_EN
C62	GND	GND	–
C63	SYS_VIN_HV	VCC_SRC	–
C64	SYS_VIN_HV	VCC_SRC	–
C65	SYS_VIN_HV	VCC_SRC	–
D1	SYS_VIN_HV	VCC_SRC	–
D2	SYS_VIN_HV	VCC_SRC	–
D3	SYS_VIN_HV	VCC_SRC	–
D4	GND	GND	–
D5	RGMII_RX_CTL	RGMII_RX_CTL	EQOS_RX_CTL
D6	SDCARD_D3	SDMMC1_DAT3	SDMMC1_DAT3
D7	GND	GND	–
D8	I2S1_FS	I2S1_LRCLK	DAP1_DIN
D9	PEX_L1_CLKREQ_N	PEX_L1_CLKREQ_N	PEX_L1_CLKREQ_N
D10	PEX_L0_RST_N	PEX_L0_RST_N	PEX_L0_RST_N
D11	GND	GND	–
D12	UPHY_RX11_P	UPHY_RX11_P	PEX_RX11_P
D13	UPHY_RX11_N	UPHY_RX11_N	PEX_RX11_N
D14	GND	GND	–
D15	GND	GND	–
D16	UPHY_RX7_P	UPHY_RX7_P	PEX_RX7_P
D17	UPHY_RX7_N	UPHY_RX7_N	PEX_RX7_N
D18	GND	GND	–
D19	GND	GND	–
D20	UPHY_RX3_P	UPHY_RX3_P	PEX_RX3_P
D21	UPHY_RX3_N	UPHY_RX3_N	PEX_RX3_N
D22	GND	GND	–
D23	GND	GND	–
D24	NVHS0_SLVS_RX0_P	NVHS0_SLVS_RX0_P	NVHS0_RX0_P

Conn. Pin #	Carrier Board Symbol Pin Name	Carrier Board Net Name	SoC Pin Name
D25	NVHS0_SLVS_RX0_N	NVHS0_SLVS_RX0_N	NVHS0_RX0_N
D26	GND	GND	–
D27	GND	GND	–
D28	NVHS0_SLVS_RX4_P	NVHS0_SLVS_RX4_P	NVHS0_RX4_P
D29	NVHS0_SLVS_RX4_N	NVHS0_SLVS_RX4_N	NVHS0_RX4_N
D30	GND	GND	–
D31	GND	GND	–
D32	NVHS1_SLVS_RX2_N	SNN_NVHS1_SLVS_RX2_N	–
D33	NVHS1_SLVS_RX2_P	SNN_NVHS1_SLVS_RX2_P	–
D34	GND	GND	–
D35	GND	GND	–
D36	NVHS1_SLVS_RX4_P	SNN_NVHS1_SLVS_RX4_P	–
D37	NVHS1_SLVS_RX4_N	SNN_NVHS1_SLVS_RX4_N	–
D38	GND	GND	–
D39	GND	GND	–
D40	MID3	SNN_MID_3	–
D41	GND	GND	–
D42	CSI5_D0_P	CSI_5_D0_P	CSI_F_D0_P
D43	CSI5_D0_N	CSI_5_D0_N	CSI_F_D0_N
D44	GND	GND	–
D45	CSI5_D1_N	CSI_5_D1_N	CSI_F_D1_N
D46	CSI5_D1_P	CSI_5_D1_P	CSI_F_D1_P
D47	GND	GND	–
D48	HDMI_DP1_TX2_N	DP1_TXN2	HDMI_DP1_TXDN2
D49	HDMI_DP1_TX2_P	DP1_TXP2	HDMI_DP1_TXDP2
D50	GND	GND	–
D51	HDMI_DP2_TX0_P	HDMI_DP2_TXP0	HDMI_DP2_TXDP0
D52	HDMI_DP2_TX0_N	HDMI_DP2_TXN0	HDMI_DP2_TXDN0
D53	GND	GND	–
D54	GPIO03	GPIO03_AP_WAKE_BT_M2	SOC_GPIO52
D55	SPI1_MOSI	SPI1_MOSI	SPI1_MOSI
D56	SPI3_MISO	SLVS_XCLR	SPI3_MISO
D57	GND	GND	–
D58	JTAG_TDO	JTAG_TDO	JTAG_TDO
D59	CAN0_DOUT	CAN0_DOUT	CAN0_DOUT
D60	SPI2_CS0_N	SPI2_CS0	SPI2_CS0
D61	I2C4_CLK	I2C_GP4_CLK	GEN8_I2C_SCL
D62	SPI2_MISO	SPI2_MISO	SPI2_MISO

Conn. Pin #	Carrier Board Symbol Pin Name	Carrier Board Net Name	SoC Pin Name
D63	GND	GND	–
D64	SYS_VIN_HV	VCC_SRC	–
D65	SYS_VIN_HV	VCC_SRC	–
E1	SYS_VIN_HV	VCC_SRC	–
E2	SYS_VIN_HV	VCC_SRC	–
E3	GND	GND	–
E4	I2S2_FS	I2S2_FS	DAP2_FS
E5	RGMII_RD3	RGMII_RD3	EQOS_RD3
E6	RGMII_SMA_MDC	RGMII_SMA_MDC	EQOS_SMA_MDC
E7	RGMII_SMA_MDIO	RGMII_SMA_MDIO	EQOS_SMA_MDIO
E8	SDCARD_D0	SDMMC1_DAT0	SDMMC1_DAT0
E9	GND	GND	–
E10	GPIO12	GPIO12_M2_WAKE_AP	SOC_GPIO33
E11	PEX_L0_CLKREQ_N	PEX_L0_CLKREQ_N	PEX_L0_CLKREQ_N
E12	GND	GND	–
E13	GND	GND	–
E14	PEX_CLK0_N	PEX_CLK0_N	PEX_CLK0N
E15	PEX_CLK0_P	PEX_CLK0_P	PEX_CLK0P
E16	GND	GND	–
E17	GND	GND	–
E18	PEX_CLK2_N	SNN_PEX_CLK2_N	PEX_CLK2N
E19	PEX_CLK2_P	SNN_PEX_CLK2_P	PEX_CLK2P
E20	GND	GND	–
E21	GND	GND	–
E22	PEX_CLK4_N	SNN_PEX_CLK4_N	PEX_CLK4N
E23	PEX_CLK4_P	SNN_PEX_CLK4_P	PEX_CLK4P
E24	GND	GND	–
E25	GND	GND	–
E26	UPHY_REFCLK1_N	SNN_UPHY_REFCLK1_N	PEX_REFCLK1_N
E27	UPHY_REFCLK1_P	SNN_UPHY_REFCLK1_P	PEX_REFCLK1_P
E28	GND	GND	–
E29	GND	GND	–
E30	NVHS0_SLVS_REFCLK0_P	NVHS0_SLVS_REFCLK0_P	NVHS0_REFCLK_P
E31	NVHS0_SLVS_REFCLK0_N	NVHS0_SLVS_REFCLK0_N	NVHS0_REFCLK_N
E32	GND	GND	–
E33	GND	GND	–
E34	NVHS1_SLVS_REFCLK1_P	SNN_NVHS1_SLVS_REFCLK1_P	–
E35	NVHS1_SLVS_REFCLK1_N	SNN_NVHS1_SLVS_REFCLK1_N	–

Conn. Pin #	Carrier Board Symbol Pin Name	Carrier Board Net Name	SoC Pin Name
E36	GND	GND	–
E37	GND	GND	–
E38	CSI0_D1_N	CSI_0_D1_N	CSI_A_D1_N
E39	CSI0_D1_P	CSI_0_D1_P	CSI_A_D1_P
E40	GND	GND	–
E41	CSI0_D0_N	CSI_0_D0_N	CSI_A_D0_N
E42	CSI0_D0_P	CSI_0_D0_P	CSI_A_D0_P
E43	GND	GND	–
E44	CSI3_D0_N	CSI_3_D0_N	CSI_D_D0_N
E45	CSI3_D0_P	CSI_3_D0_P	CSI_D_D0_P
E46	GND	GND	–
E47	CSI4_D1_P	CSI_4_D1_P	CSI_E_D1_P
E48	CSI4_D1_N	CSI_4_D1_N	CSI_E_D1_N
E49	GND	GND	–
E50	HDMI_DP1_TX3_P	DP1_TXP3	HDMI_DP1_TXDP3
E51	HDMI_DP1_TX3_N	DP1_TXN3	HDMI_DP1_TXDN3
E52	GND	GND	–
E53	I2C3_DAT	I2C_GP3_DAT	CAM_I2C_SDA
E54	FAN_TACH	FAN_TACH	SOC_GPIO22
E55	SPI1_CS0_N	SPI1_CS0	SPI1_CS0
E56	SPI3_CS1_N	I2C_GP3_LVS_EN*	SPI3_CS1
E57	GND	GND	–
E58	JTAG_TMS	JTAG_TMS	JTAG_TMS
E59	GPIO06	GPIO06_PEX_REFCLK_SEL	CAN0_EN
E60	I2C4_DAT	I2C_GP4_DAT	GEN8_I2C_SDA
E61	SPI2_CLK	SPI2_SCK	SPI2_SCK
E62	GND	GND	–
E63	SYS_VIN_HV	VCC_SRC	–
E64	SYS_VIN_HV	VCC_SRC	–
E65	SYS_VIN_HV	VCC_SRC	–
F1	SYS_VIN_HV	VCC_SRC	–
F2	SYS_VIN_HV	VCC_SRC	–
F3	SYS_VIN_HV	VCC_SRC	–
F4	GND	GND	–
F5	I2S2_DOUT	I2S2_SDOUT	DAP2_DOUT
F6	I2S2_DIN	I2S2_SDIN	DAP2_DIN
F7	GND	GND	–
F8	SDCARD_D1	SDMMC1_DAT1	SDMMC1_DAT1

Conn. Pin #	Carrier Board Symbol Pin Name	Carrier Board Net Name	SoC Pin Name
F9	GPIO16	GPIO16_CAM1_RST	DAP5_DOUT
F10	GPIO15	GPIO15_CAM1_PWDN	DAP5_SCLK
F11	GND	GND	–
F12	USB0_P	USB0_DP	USB0_DP
F13	USB0_N	USB0_DN	USB0_DN
F14	GND	GND	–
F15	GND	GND	–
F16	PEX_CLK1_P	PEX_CLK1_P	PEX_CLK1P
F17	PEX_CLK1_N	PEX_CLK1_N	PEX_CLK1N
F18	GND	GND	–
F19	GND	GND	–
F20	PEX_CLK3_P	PEX_CLK3_P	PEX_CLK3P
F21	PEX_CLK3_N	PEX_CLK3_N	PEX_CLK3N
F22	GND	GND	–
F23	GND	GND	–
F24	PEX_CLK5_P	PEX_CLK5_P	PEX_CLK5P
F25	PEX_CLK5_N	PEX_CLK5_N	PEX_CLK5N
F26	GND	GND	–
F27	GND	GND	–
F28	UPHY_REFCLK2_P	SNN_UPHY_REFCLK2_P	PEX_REFCLK2_P
F29	UPHY_REFCLK2_N	SNN_UPHY_REFCLK2_N	PEX_REFCLK2_N
F30	GND	GND	–
F31	GND	GND	–
F32	NVHS0_SLVS_REFCLK1_P	SNN_NVHS0_SLVS_REFCLK1_P	–
F33	NVHS0_SLVS_REFCLK1_N	SNN_NVHS0_SLVS_REFCLK1_N	–
F34	GND	GND	–
F35	GND	GND	–
F36	NVHS1_SLVS_REFCLK0_P	SNN_NVHS1_SLVS_REFCLK0_P	–
F37	NVHS1_SLVS_REFCLK0_N	SNN_NVHS1_SLVS_REFCLK0_N	–
F38	GND	GND	–
F39	GND	GND	–
F40	MID2	SNN_MID_2	–
F41	GND	GND	–
F42	CSI0_CLK_N	CSI_0_CLK_N	CSI_A_CLK_N
F43	CSI0_CLK_P	CSI_0_CLK_P	CSI_A_CLK_P
F44	GND	GND	–
F45	CSI3_CLK_N	CSI_3_CLK_N	CSI_D_CLK_N
F46	CSI3_CLK_P	CSI_3_CLK_P	CSI_D_CLK_P

Conn. Pin #	Carrier Board Symbol Pin Name	Carrier Board Net Name	SoC Pin Name
F47	GND	GND	–
F48	CSI4_CLK_P	CSI_4_CLK_P	CSI_E_CLK_P
F49	CSI4_CLK_N	CSI_4_CLK_N	CSI_E_CLK_N
F50	GND	GND	–
F51	DP0_AUX_CH_N	DP_AUX_CH0_N	DP_AUX_CH0_N
F52	DP0_AUX_CH_P	DP_AUX_CH0_P	DP_AUX_CH0_P
F53	I2C3_CLK	I2C_GP3_CLK	CAM_I2C_SCL
F54	GPIO22	GPIO22_USB_VBUS_EN0	USB_VBUS_EN0
F55	SPI3_CLK	BT_WAKE_AP	SPI3_SCK
F56	GPIO36	GPIO36_CAM_AVDD_CAM_EN	SOC_GPIO53
F57	GND	GND	–
F58	CAN0_DIN	CAN0_DIN	CAN0_DIN
F59	GPIO07	GPIO07_CAN0_WAKE	CAN0_WAKE
F60	SPI2_MOSI	SPI2_MOSI	SPI2_MOSI
F61	VCOMP_ALERT_N	SNN_VMON	VCOMP_ALERT
F62	GND	GND	–
F63	SYS_VIN_HV	VCC_SRC	–
F64	SYS_VIN_HV	VCC_SRC	–
F65	SYS_VIN_HV	VCC_SRC	–
G1	SYS_VIN_HV	VCC_SRC	–
G2	SYS_VIN_HV	VCC_SRC	–
G3	GND	GND	–
G4	I2S2_CLK	I2S2_CLK	DAP2_SCLK
G5	RGMII_TD1	RGMII_TD1	EQOS_TD1
G6	RGMII_TD3	RGMII_TD3	EQOS_TD3
G7	GPIO13	SNN_GPIO13	DAP3_DIN
G8	PEX_L4_CLKREQ_N	SNN_PEX_L4_CLKREQ_N	PEX_L4_CLKREQ_N
G9	GND	GND	–
G10	USB3_N	USB3_DN	USB3_DN
G11	USB3_P	USB3_DP	USB3_DP
G12	GND	GND	–
G13	GND	GND	–
G14	UPHY_TX9_N	SNN_UPHY_TX9_N	PEX_TX9_N
G15	UPHY_TX9_P	SNN_UPHY_TX9_P	PEX_TX9_P
G16	GND	GND	–
G17	GND	GND	–
G18	UPHY_TX5_N	UPHY_TX5_N	PEX_TX5_N
G19	UPHY_TX5_P	UPHY_TX5_P	PEX_TX5_P

Conn. Pin #	Carrier Board Symbol Pin Name	Carrier Board Net Name	SoC Pin Name
G20	GND	GND	–
G21	GND	GND	–
G22	UPHY_TX1_N	UPHY_TX1_N	PEX_TX1_N
G23	UPHY_TX1_P	UPHY_TX1_P	PEX_TX1_P
G24	GND	GND	–
G25	GND	GND	–
G26	NVHS0_TX2_N	NVHS0_TX2_N	NVHS0_TX2_N
G27	NVHS0_TX2_P	NVHS0_TX2_P	NVHS0_TX2_P
G28	GND	GND	–
G29	GND	GND	–
G30	NVHS0_TX6_N	NVHS0_TX6_N	NVHS0_TX6_N
G31	NVHS0_TX6_P	NVHS0_TX6_P	NVHS0_TX6_P
G32	GND	GND	–
G33	GND	GND	–
G34	NVHS1_TX1_N	SNN_NVHS1_TX1_N	–
G35	NVHS1_TX1_P	SNN_NVHS1_TX1_P	–
G36	GND	GND	–
G37	GND	GND	–
G38	NVHS1_TX6_N	SNN_NVHS1_TX6_N	–
G39	NVHS1_TX6_P	SNN_NVHS1_TX6_P	–
G40	GND	GND	–
G41	CSI1_D0_P	CSI_1_D0_P	CSI_B_D0_P
G42	CSI1_D0_N	CSI_1_D0_N	CSI_B_D0_N
G43	GND	GND	–
G44	CSI3_D1_P	CSI_3_D1_P	CSI_D_D1_P
G45	CSI3_D1_N	CSI_3_D1_N	CSI_D_D1_N
G46	GND	GND	–
G47	CSI4_D0_N	CSI_4_D0_N	CSI_E_D0_N
G48	CSI4_D0_P	CSI_4_D0_P	CSI_E_D0_P
G49	GND	GND	–
G50	HDMI_DP0_TX1_N	DP0_TXN1	HDMI_DP0_TXDN1
G51	HDMI_DP0_TX1_P	DP0_TXP1	HDMI_DP0_TXDP1
G52	GND	GND	–
G53	DP2_AUX_CH_P	DP_AUX_CH2_P	DP_AUX_CH2_P
G54	DP2_AUX_CH_N	DP_AUX_CH2_N	DP_AUX_CH2_N
G55	GPIO23	GPIO23_PEX_3V3_EN	USB_VBUS_EN1
G56	SPI3_MOSI	SLVS_XCE	SPI3_MOSI
G57	GND	GND	–

Conn. Pin #	Carrier Board Symbol Pin Name	Carrier Board Net Name	SoC Pin Name
G58	UART2_RTS	UART2_RTS	UART2_RTS
G59	NC_03	SNN_CVM_COM_NC_03	–
G60	NVDBG_SEL	NVDBG_SEL	NVDBG_SEL
G61	JTAG_TRST_N	JTAG_TRST_N	JTAG_TRST_N
G62	GND	GND	–
G63	SYS_VIN_HV	VCC_SRC	–
G64	SYS_VIN_HV	VCC_SRC	–
G65	SYS_VIN_HV	VCC_SRC	–
H1	SYS_VIN_HV	VCC_SRC	–
H2	SYS_VIN_HV	VCC_SRC	–
H3	SYS_VIN_HV	VCC_SRC	–
H4	GND	GND	–
H5	ENET_RST_N	ENET_RST	SOC_GPIO09
H6	RGMII_RD2	RGMII_RD2	EQOS_RD2
H7	GND	GND	–
H8	I2S1_SDIN	I2S1_SDIN	DAP1_DOUT
H9	MCLK01	AUDIO_MCLK01	AUD_MCLK
H10	PEX_L5_RST_N	PEX_L5_RST_N	PEX_L5_RST_N
H11	GND	GND	–
H12	UPHY_TX11_P	UPHY_TX11_P	PEX_TX11_P
H13	UPHY_TX11_N	UPHY_TX11_N	PEX_TX11_N
H14	GND	GND	–
H15	GND	GND	–
H16	UPHY_TX7_P	UPHY_TX7_P	PEX_TX7_P
H17	UPHY_TX7_N	UPHY_TX7_N	PEX_TX7_N
H18	GND	GND	–
H19	GND	GND	–
H20	UPHY_TX3_P	UPHY_TX3_P	PEX_TX3_P
H21	UPHY_TX3_N	UPHY_TX3_N	PEX_TX3_N
H22	GND	GND	–
H23	GND	GND	–
H24	NVHS0_TX0_P	NVHS0_TX0_P	NVHS0_TX0_P
H25	NVHS0_TX0_N	NVHS0_TX0_N	NVHS0_TX0_N
H26	GND	GND	–
H27	GND	GND	–
H28	NVHS0_TX4_P	NVHS0_TX4_P	NVHS0_TX4_P
H29	NVHS0_TX4_N	NVHS0_TX4_N	NVHS0_TX4_N
H30	GND	GND	–

Conn. Pin #	Carrier Board Symbol Pin Name	Carrier Board Net Name	SoC Pin Name
H31	GND	GND	–
H32	NVHS1_TX3_P	SNN_NVHS1_TX3_P	–
H33	NVHS1_TX3_N	SNN_NVHS1_TX3_N	–
H34	GND	GND	–
H35	GND	GND	–
H36	NVHS1_TX7_P	SNN_NVHS1_TX7_P	–
H37	NVHS1_TX7_N	SNN_NVHS1_TX7_N	–
H38	GND	GND	–
H39	GND	GND	–
H40	MID1	SNN_MID_1	–
H41	GND	GND	–
H42	CSI1_CLK_N	CSI_1_CLK_N	CSI_B_CLK_N
H43	CSI1_CLK_P	CSI_1_CLK_P	CSI_B_CLK_P
H44	GND	GND	–
H45	CSI6_D1_N	CSI_6_D1_N	CSI_G_D1_N
H46	CSI6_D1_P	CSI_6_D1_P	CSI_G_D1_P
H47	GND	GND	–
H48	HDMI_DP0_TX0_N	DP0_TXDN0	HDMI_DP0_TXDN0
H49	HDMI_DP0_TX0_P	DP0_TXDP0	HDMI_DP0_TXDP0
H50	GND	GND	–
H51	GPIO26	GPIO26_BT_RST_M2*	SOC_GPIO51
H52	GPIO27	GPIO27_PWM2	SOC_GPIO54
H53	MCLK03	CAM1_MCLK03	EXTPERIPH2_CLK
H54	UART1_CTS	UART1_CTS	UART1_CTS
H55	MCLK04	CAM2_MCLK04	SOC_GPIO41
H56	GND	GND	–
H57	UART5_CTS	UART5_CTS	UART5_CTS
H58	UART5_RX	UART5_RX	UART5_RX
H59	NVJTAG_SEL	NVJTAG_SEL	NVJTAG_SEL
H60	GPIO31	GPIO31_UFS_DET	SAFE_STATE
H61	CAN1_DOUT	CAN1_DOUT	CAN1_DOUT
H62	UART3_TX_DEBUG	UART3_TX_DEBUG	UART3_TX
H63	GND	GND	–
H64	SYS_VIN_HV	VCC_SRC	–
H65	SYS_VIN_HV	VCC_SRC	–
J1	SYS_VIN_HV	VCC_SRC	–
J2	SYS_VIN_HV	VCC_SRC	–
J3	GND	GND	–

Conn. Pin #	Carrier Board Symbol Pin Name	Carrier Board Net Name	SoC Pin Name
J4	GPIO01	GPIO01_WIFI_DISABLE*	SOC_GPIO03
J5	ENET_INT	ENET_INT	SOC_GPIO08
J6	RGMII_TD0	RGMII_TD0	EQOS_TD0
J7	RGMII_TD2	RGMII_TD2	EQOS_TD2
J8	GND	GND	–
J9	PEX_L4_RST_N	SNN_PEX_L4_RST_N	PEX_L4_RST_N
J10	PEX_L3_CLKREQ_N	PEX_L3_CLKREQ_N	PEX_L3_CLKREQ_N
J11	PEX_L2_CLKREQ_N	SNN_PEX_L2_CLKREQ_N	PEX_L2_CLKREQ_N
J12	GND	GND	–
J13	GND	GND	–
J14	UPHY_TX8_P	SNN_UPHY_TX8_P	PEX_TX8_P
J15	UPHY_TX8_N	SNN_UPHY_TX8_N	PEX_TX8_N
J16	GND	GND	–
J17	GND	GND	–
J18	UPHY_TX4_P	UPHY_TX4_P	PEX_TX4_P
J19	UPHY_TX4_N	UPHY_TX4_N	PEX_TX4_N
J20	GND	GND	–
J21	GND	GND	–
J22	UPHY_TX0_P	UPHY_TX0_P	PEX_TX0_P
J23	UPHY_TX0_N	UPHY_TX0_N	PEX_TX0_N
J24	GND	GND	–
J25	GND	GND	–
J26	NVHS0_TX3_P	NVHS0_TX3_P	NVHS0_TX3_P
J27	NVHS0_TX3_N	NVHS0_TX3_N	NVHS0_TX3_N
J28	GND	GND	–
J29	GND	GND	–
J30	NVHS0_TX7_P	NVHS0_TX7_P	NVHS0_TX7_P
J31	NVHS0_TX7_N	NVHS0_TX7_N	NVHS0_TX7_N
J32	GND	GND	–
J33	GND	GND	–
J34	NVHS1_TX2_N	SNN_NVHS1_TX2_N	–
J35	NVHS1_TX2_P	SNN_NVHS1_TX2_P	–
J36	GND	GND	–
J37	GND	GND	–
J38	NVHS1_TX5_N	SNN_NVHS1_TX5_N	–
J39	NVHS1_TX5_P	SNN_NVHS1_TX5_P	–
J40	GND	GND	–
J41	CSI1_D1_P	CSI_1_D1_P	CSI_B_D1_P

Conn. Pin #	Carrier Board Symbol Pin Name	Carrier Board Net Name	SoC Pin Name
J42	CSI1_D1_N	CSI_1_D1_N	CSI_B_D1_N
J43	GND	GND	–
J44	CSI6_CLK_P	CSI_6_CLK_P	CSI_G_CLK_P
J45	CSI6_CLK_N	CSI_6_CLK_N	CSI_G_CLK_N
J46	GND	GND	–
J47	HDMI_DP0_TX2_P	DP0_TXP2	HDMI_DP0_TXDP2
J48	HDMI_DP0_TX2_N	DP0_TXN2	HDMI_DP0_TXDN2
J49	GND	GND	–
J50	HDMI_CEC	HDMI_CEC	HDMI_CEC
J51	GPIO24	GPIO24_SAR_TOUT	DP_AUX_CH3_HPD
J52	DP1_AUX_CH_P	DP_AUX_CH1_P	DP_AUX_CH1_P
J53	DP1_AUX_CH_N	DP_AUX_CH1_N	DP_AUX_CH1_N
J54	MCLK02	CAM0_MCLK02	EXTPERIPH1_CLK
J55	GPIO32	GPIO32_PWM01_40PIN_BACKUP	SOC_GPIO04
J56	GND	GND	–
J57	SPI1_CLK	SPI1_SCK	SPI1_SCK
J58	UART5_TX	UART5_TX	UART5_TX
J59	I2S3_DIN	I2S3_DIN	DAP4_DIN
J60	STANDBY_ACK_N	CVB_STBY	SOC_PWR_REQ
J61	I2C2_CLK	I2C_GP2_CLK	GEN2_I2C_SCL
J62	GND	GND	–
J63	SYS_VIN_HV	VCC_SRC	–
J64	SYS_VIN_HV	VCC_SRC	–
J65	SYS_VIN_HV	VCC_SRC	–
K3	SYS_VIN_HV	VCC_SRC	–
K4	GND	GND	–
K5	I2C1_CLK	I2C_GP1_CLK	GEN1_I2C_SCL
K6	RGMII_RD1	RGMII_RD1	EQOS_RD1
K7	RGMII_TX_CTL	RGMII_TX_CTL	EQOS_TX_CTL
K8	GND	GND	–
K9	PEX_L3_RST_N	PEX_L3_RST_N	PEX_L3_RST_N
K10	PEX_L2_RST_N	SNN_PEX_L2_RST_N	PEX_L2_RST_N
K11	GND	GND	–
K12	UPHY_TX10_N	UPHY_TX10_N	PEX_TX10_N
K13	UPHY_TX10_P	UPHY_TX10_P	PEX_TX10_P
K14	GND	GND	–
K15	GND	GND	–
K16	UPHY_TX6_N	UPHY_TX6_N	PEX_TX6_N

Conn. Pin #	Carrier Board Symbol Pin Name	Carrier Board Net Name	SoC Pin Name
K17	UPHY_TX6_P	UPHY_TX6_P	PEX_TX6_P
K18	GND	GND	–
K19	GND	GND	–
K20	UPHY_TX2_N	UPHY_TX2_N	PEX_TX2_N
K21	UPHY_TX2_P	UPHY_TX2_P	PEX_TX2_P
K22	GND	GND	–
K23	GND	GND	–
K24	NVHS0_TX1_N	NVHS0_TX1_N	NVHS0_TX1_N
K25	NVHS0_TX1_P	NVHS0_TX1_P	NVHS0_TX1_P
K26	GND	GND	–
K27	GND	GND	–
K28	NVHS0_TX5_N	NVHS0_TX5_N	NVHS0_TX5_N
K29	NVHS0_TX5_P	NVHS0_TX5_P	NVHS0_TX5_P
K30	GND	GND	–
K31	GND	GND	–
K32	NVHS1_TX0_P	SNN_NVHS1_TX0_P	–
K33	NVHS1_TX0_N	SNN_NVHS1_TX0_N	–
K34	GND	GND	–
K35	GND	GND	–
K36	NVHS1_TX4_P	SNN_NVHS1_TX4_P	–
K37	NVHS1_TX4_N	SNN_NVHS1_TX4_N	–
K38	GND	GND	–
K39	GND	GND	–
K40	MID0	SNN_MID_0	–
K41	GND	GND	–
K42	GND	GND	–
K43	CSI6_D0_N	CSI_6_D0_N	CSI_G_D0_N
K44	CSI6_D0_P	CSI_6_D0_P	CSI_G_D0_P
K45	GND	GND	–
K46	HDMI_DP0_TX3_P	DP0_TXP3	HDMI_DP0_TXDP3
K47	HDMI_DP0_TX3_N	DP0_TXN3	HDMI_DP0_TXDN3
K48	GND	GND	–
K49	GPIO25	GPIO25_VDD_SYS_EN	SOC_GPIO50
K50	DP2_HPD	DP_AUX_CH2_HPD	DP_AUX_CH2_HPD
K51	DP1_HPD	DP_AUX_CH1_HPD	DP_AUX_CH1_HPD
K52	DP0_HPD	CH0_HPD	DP_AUX_CH0_HPD
K53	UART1_TX	UART1_TX	UART1_TX
K54	UART1_RX	UART1_RX	UART1_RX

Conn. Pin #	Carrier Board Symbol Pin Name	Carrier Board Net Name	SoC Pin Name
K55	GND	GND	–
K56	GPIO19	GPIO19_SLVS_VSYNC	SOC_GPIO43
K57	PWM01	PWM01	SOC_GPIO44
K58	UART5_RTS	UART5_RTS	UART5_RTS
K59	I2S3_DOUT	I2S3_DOUT	DAP4_DOUT
K60	UART3_RX_DEBUG	UART3_RX_DEBUG	UART3_RX
K61	I2C2_DAT	I2C_GP2_DAT	GEN2_I2C_SDA
K62	FAN_PWM	FAN_PWM	TOUCH_CLK
K63	GND	GND	–
L3	GND	GND	–
L4	UART4_RTS	SNN_UART4_RTS	UART4_RTS
L5	UART4_TX	CAM0_RST	UART4_TX
L6	GPIO02	GPIO02_SD_DET	SOC_GPIO11
L7	GND	GND	–
L8	I2C1_DAT	I2C_GP1_DAT	GEN1_I2C_SDA
L9	GPIO28	GPIO28_BATLOW_N	SOC_GPIO02
L10	FORCE_RECOVERY_N	FORCE_RECOVERY*	SOC_GPIO00
L11	STANDBY_REQ_N	STABDBY_REQ_N	SOC_GPIO01
L12	GND	GND	–
L13	GND	GND	–
L14	I2S1_CLK	I2S1_CLK	DAP1_SCLK
L15	GPIO14	GPIO14_M2_EN	DAP3_FS
L16	GND	GND	–
L17	GND	GND	–
L18	NC_01	SNN_CVM_COM_NC_01	–
L19	NC_02	SNN_CVM_COM_NC_02	–
L20	GND	GND	–
L21	GND	GND	–
L22	SYS_VIN_MV_10	VDD_5V	–
L23	SYS_VIN_MV_9	VDD_5V	–
L24	GND	GND	–
L25	GND	GND	–
L26	SYS_VIN_MV_8	VDD_5V	–
L27	SYS_VIN_MV_7	VDD_5V	–
L28	GND	GND	–
L29	GND	GND	–
L30	SYS_VIN_MV_6	VDD_5V	–
L31	SYS_VIN_MV_5	VDD_5V	–

Conn. Pin #	Carrier Board Symbol Pin Name	Carrier Board Net Name	SoC Pin Name
L32	GND	GND	–
L33	GND	GND	–
L34	SYS_VIN_MV_4	VDD_5V	–
L35	SYS_VIN_MV_3	VDD_5V	–
L36	GND	GND	–
L37	GND	GND	–
L38	SYS_VIN_MV_2	VDD_5V	–
L39	SYS_VIN_MV_1	VDD_5V	–
L40	GND	GND	–
L41	VM_EN1_N	SNN_VM_EN1_N	–
L42	VM_EN0_N	SNN_VM_EN0_N	–
L43	GND	GND	–
L44	VM_I2C_SCK	SNN_VM_I2C_SCK	–
L45	VM_I2C_DAT	SNN_VM_I2C_DAT	–
L46	GND	GND	–
L47	VM_INT_N	SNN_VM_INT_N	–
L48	UART4_RX	SNN_UART4_RX	UART4_RX
L49	UART4_CTS	CAM0_PWDN	UART4_CTS
L50	GPIO35	GPIO35_PWM3	SOC_GPIO12
L51	UART1_RTS	UART1_RTS	UART1_RTS
L52	OVERTEMP_N	FORCE_SHUTDOWN	SOC_GPIO55
L53	VCC_RTC	BBAT	–
L54	MODULE_POWER_ON	MODULE_POWER_ON	–
L55	VDDIN_PWR_BAD_N	VDDIN_PWR_BAD_N	–
L56	TEMP_ALERT_N	SNN_TEMP_ALERT_N	–
L57	MCLK05	MCLK05	SOC_GPIO42
L58	PERIPHERAL_RESET_N	SNN_PERIPHERAL_RESET_N	–
L59	SAFETY_PROCESSOR_GPIO	SNN_SAFETY_PROCESSOR_GPIO	–
L60	SYS_RESET_N	SYS_RST_IN*	SYS_RESET_N
L61	POWER_BTN_N	POWER_BTN_ON*	POWER_ON
L62	CARRIER_POWER_ON	CARRIER_POWER_ON	–
L63	PRSNT1	CVM_PRSNT1	–

Notice

The information provided in this specification is believed to be accurate and reliable as of the date provided. However, NVIDIA Corporation ("NVIDIA") does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information. NVIDIA shall have no liability for the consequences or use of such information or for any infringement of patents or other rights of third parties that may result from its use. This publication supersedes and replaces all other specifications for the product that may have been previously supplied.

NVIDIA reserves the right to make corrections, modifications, enhancements, improvements, and other changes to this specification, at any time and/or to discontinue any product or service without notice. Customer should obtain the latest relevant specification before placing orders and should verify that such information is current and complete.

NVIDIA products are sold subject to the NVIDIA standard terms and conditions of sale supplied at the time of order acknowledgement, unless otherwise agreed in an individual sales agreement signed by authorized representatives of NVIDIA and customer. NVIDIA hereby expressly objects to applying any customer general terms and conditions with regards to the purchase of the NVIDIA product referenced in this specification.

Unless specifically agreed to in writing by NVIDIA, NVIDIA products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of the NVIDIA product can reasonably be expected to result in personal injury, death or property or environmental damage. NVIDIA accepts no liability for inclusion and/or use of NVIDIA products in such equipment or applications and therefore such inclusion and/or use is at customer's own risk.

NVIDIA makes no representation or warranty that products based on these specifications will be suitable for any specified use without further testing or modification. Testing of all parameters of each product is not necessarily performed by NVIDIA. It is customer's sole responsibility to ensure the product is suitable and fit for the application planned by customer and to do the necessary testing for the application in order to avoid a default of the application or the product. Weaknesses in customer's product designs may affect the quality and reliability of the NVIDIA product and may result in additional or different conditions and/or requirements beyond those contained in this specification. NVIDIA does not accept any liability related to any default, damage, costs or problem which may be based on or attributable to: (i) the use of the NVIDIA product in any manner that is contrary to this specification, or (ii) customer product designs.

No license, either expressed or implied, is granted under any NVIDIA patent right, copyright, or other NVIDIA intellectual property right under this specification. Information published by NVIDIA regarding third-party products or services does not constitute a license from NVIDIA to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property rights of the third party, or a license from NVIDIA under the patents or other intellectual property rights of NVIDIA. Reproduction of information in this specification is permissible only if reproduction is approved by NVIDIA in writing, is reproduced without alteration, and is accompanied by all associated conditions, limitations, and notices.

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS, AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS." NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY, OR OTHERWISE WITH RESPECT TO THE MATERIALS, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES OF NONINFRINGEMENT, MERCHANTABILITY, AND FITNESS FOR A PARTICULAR PURPOSE. Notwithstanding any damages that customer might incur for any reason whatsoever, NVIDIA's aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the NVIDIA terms and conditions of sale for the product.

ARM

ARM, AMBA and ARM Powered are registered trademarks of ARM Limited. Cortex, MPCore and Mali are trademarks of ARM Limited. All other brands or product names are the property of their respective holders. "ARM" is used to represent ARM Holdings plc; its operating company ARM Limited; and the regional subsidiaries ARM Inc.; ARM KK; ARM Korea Limited.; ARM Taiwan Limited; ARM France SAS; ARM Consulting (Shanghai) Co. Ltd.; ARM Germany GmbH; ARM Embedded Technologies Pvt. Ltd.; ARM Norway, AS and ARM Sweden AB.

Trademarks

NVIDIA, the NVIDIA logo, Jetson, Jetson AGX Xavier, and Xavier are trademarks and/or registered trademarks of NVIDIA Corporation in the U.S. and other countries. Other company and product names may be trademarks of the respective companies with which they are associated.

Copyright

NVIDIA Corporation | 2788 San Tomas Expressway, Santa Clara, CA 95051
http://www.nvidia.com