NVIDIA Jetson AGX Xavier Series USB 2.0 Tuning Guide

Application Note

DA-09493-001_v1.1 | June 2019

Document History

DA-09493-001_v1.1

Version	Date	Description of Change
1.0	May 29, 2019	Initial Release
1.1	June 14, 2019	Updated to include all Jetson AGX Xavier series modules

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Overview

This application note describes the registers and steps needed to tune the USB 2.0 high speed eye diagram for the NVIDIA® Jetson AGX Xavier™ series module. USB IF provides complete test specification and instructions on their website for high speed host and device mode testing.

Note: References to Jetson AGX Xavier apply to any of the Jetson AGX Xavier series of modules.

NVIDIA typically uses Tektronix oscilloscopes for USB characterizations. The following test procedures for Tektronix oscilloscopes are available.

- Host Mode Testing
  - Procedure for using Tektronix scopes:

    http://www.usb.org/developers/docs/Host_test_procedure.pdf
- Device Mode Testing
  - Procedure for using Tektronix scopes:

    http://www.usb.org/developers/docs/DeviceTestProcedure.pdf

Customers are free to use oscilloscopes from other vendors to do USB characterization.

Required Equipment

The following equipment is required:

- Tektronix TDS694C or faster digital sampling oscilloscope
- Tektronix P6247 or P6248 or equivalent differential probe * 1
- High-speed USB Electrical Test Fixture
- Oscilloscope USB test software
- Tool to access register/memory space in NVIDIA® Xavier™ or build a special image to force USB test mode enabled

Registers for Host Mode Testing

Toggle the Jetson AGX Xavier module USB registers listed in Table 1 to force Test J, Test K, Test SE0 NAK, and Test Packet on the respective USB port.

Table 1. Host Mode Test Registers

Description	Register Name and Setting
Normal Operations	T_XUSB_XHCI_OP_PORTPMSCHS_x[31:28] = 0000b
Test J	T_XUSB_XHCI_OP_PORTPMSCHS_x[31:28] = 0001b
Test K	T_XUSB_XHCI_OP_PORTPMSCHS_x[31:28] = 0010b
Test SE0 NAK	T_XUSB_XHCI_OP_PORTPMSCHS_x[31:28] = 0011b
Test Packet	T_XUSB_XHCI_OP_PORTPMSCHS_x[31:28] = 0100b
Force Enable	T_XUSB_XHCI_OP_PORTPMSCHS_x[31:28] = 0101b

The xUSB USB 2.0 port register addresses are as follows:

- Port 0: 0x03610464: T_XUSB_XHCI_OP_PORTPMSCHS_4
- Port 1: 0x03610474: T_XUSB_XHCI_OP_PORTPMSCHS_5
- Port 2: 0x03610484: T_XUSB_XHCI_OP_PORTPMSCHS_6
- Port 3: 0x03610494: T_XUSB_XHCI_OP_PORTPMSCHS_7

Test Mode Programming Sequence

The programming sequence for enabling USB 2.0 test mode is as follows:

Note: The output of USB 2.0 test pattern is only supported for point to point connections.

1. Connect any USB device to the port (this will prevent the controller from entering power down mode).

Note: "Any USB device" refers to any real device, such as HS uDISK or LS mouse.

2. Disable the auto suspend for the controllers:

   a). For example: the following command under Linux Kernel:
   echo on > /sys/bus/usb/devices/usb1/power/control

Note: The "usb1" here is the XHCI USB2 controller; it may map to "usb2" if there is another USB controller on the board. The XHCI bus number can be found under /sys/devices/3610000.xhci/.

3. Set PP (Port Power) to Disabled state by T_XUSB_XHCI_OP_PORTSC[9] = 0.
   Port 0: 0x03610460: T_XUSB_XHCI_OP_PORTSC_4
   Port 1: 0x03610470: T_XUSB_XHCI_OP_PORTSC_5
   Port 2: 0x03610480: T_XUSB_XHCI_OP_PORTSC_6
   Port 3: 0x03610490: T_XUSB_XHCI_OP_PORTSC_7
4. Set RS (Run/Stop) bit in the T_XUSB_XHCI_OP_USBCMD_0[0] = 0.
   0x03610020: T_XUSB_XHCI_OP_USBCMD_0
5. Wait for the HCHalted (HCH) bit in the T_XUSB_XHCI_OP_USBSTS_0[0] = 1.
   0x03610024: T_XUSB_XHCI_OP_USBSTS_0
6. Set the xUSB Port Test Control registers in PORTPMSCHS register (see Section "Register for Host Mode Testing").

Note: Per "USB 2.0 Specification," only a single downstream facing port can be in test_mode at a given time.

7. Disable Pad PD (power down) by clearing the T_XUSB_PADCTL_USB2_OTG_PADx_CTL_0_0[26] = 0.
   Port 0: 0x03520088: T_XUSB_PADCTL_USB2_OTG_PAD0_CTL_0_0
   Port 1: 0x035200C8: T_XUSB_PADCTL_USB2_OTG_PAD1_CTL_0_0
   Port 2: 0x03520108: T_XUSB_PADCTL_USB2_OTG_PAD2_CTL_0_0
   Port 3: 0x03520148: T_XUSB_PADCTL_USB2_OTG_PAD3_CTL_0_0
8. Plug in the test fixture to start the USB 2.0 eye diagram test.

Note: In Steps 3, 6, and 7, Port 0 is USB0_DP/DN (F12/F13), Port 1 is USB1_DP/DN (C11/C10), Port 2 is USB2_DP/DN (A10/A11), and Port 3 is USB3_DP/DN (G11/G10).

Registers to Adjust USB 2.0 Eye Diagram

Table 2 lists the Jetson AGX Xavier module USB registers that are needed to tune the USB 2.0 eye diagram. Refer to the "Tuning Procedure" section on how to use these registers during characterization.

Table 2. Xavier USB Registers

Register Name	Bit Field	Description
XUSB_PADCTL_USB2_OTG_PAD0_CTL_0_0 (Address 0x03520088) for Port 0 XUSB_PADCTL_USB2_OTG_PAD1_CTL_0_0 (Address 0x035200C8) for Port 1 XUSB_PADCTL_USB2_OTG_PAD2_CTL_0_0 (Address 0x03520108) for Port 2 XUSB_PADCTL_USB2_OTG_PAD3_CTL_0_0 (Address 0x03520148) for Port 3		
HS_SLEW[1]	8:6	HSSLEW (high speed slew rate control)
HS_CURR_LEVEL[2]	5:0	Setup (high speed drive strength control)
XUSB_PADCTL_USB2_OTG_PAD0_CTL_1_0 (Address 0x0352008C) for Port 0 XUSB_PADCTL_USB2_OTG_PAD1_CTL_1_0 (Address 0x035200CC) for Port 1 XUSB_PADCTL_USB2_OTG_PAD2_CTL_1_0 (Address 0x0352010C) for Port 2 XUSB_PADCTL_USB2_OTG_PAD3_CTL_1_0 (Address 0x0352014C) for Port 3		
RPD_CTRL	30:26	RPD_CTRL (15K host pull down)
TERM_RANGE_ADJ	6:3	ATERM (high speed termination control)
XUSB_PADCTL_USB2_BIAS_PAD_CTL_0_0 (Address 0x03520284)		
HS_SQUELCH_LEVEL	2:0	HSSQUELCH (squelch level control for device RX testing)

Register Name	Bit Field	Description
XUSB_PADCTL_USB2_OTG_PAD0_CTL_3_0 (Address 0x03520094) for Port 0 XUSB_PADCTL_USB2_OTG_PAD1_CTL_3_0 (Address 0x035200D4) for Port 1 XUSB_PADCTL_USB2_OTG_PAD2_CTL_3_0 (Address 0x03520114) for Port 2 XUSB_PADCTL_USB2_OTG_PAD3_CTL_3_0 (Address 0x03520154) for Port 3		
HS_RXEQ[3]	8:6	HS_RXEQ (device RX testing)
HS_TXEQ[3]	3:1	HS_TXEQ (device TX testing)

Notes:

[1]HS_SLEW where 0'b000 = slowest and 0'b111 = fastest

[2]HS_CURR_LEVEL where 0'b000000 = highest current level and 0'b111111 = lowest current level

[3]If system has inner cable, consult with AE for recommendations and perform certificate/functional test verification

Table 3. TXEQ and RXEQ Pre-Emphasis

HS_TXEQ[2:0]	AC Gain	HS_RXEQ[2:0]	SQ Level
00	+0 dB (default)	00	-0 dB (default)
01	+1.3 dB	01	-1.2 db
10	+2.5 dB	10	-2.0 dB
11	+3.5 dB	11	-3.5 dB

Table 4. HS_SQUELCH Level

HS_SQUELCH[2:0]	EL17
000	140 mV (default)
001	90 mV
010	102.5 mV
011	115 mV
100	127.5 mV
101	152.5 mV
110	165 mV
111	177.5 mV

Tuning Procedure

During production, each NVIDIA Jetson AGX Xavier module is calibrated based on the silicon process, the corresponding USB drive strength (HS_CURR_LEVEL), HS termination (TERM_RANGE_ADJ), and 15K host pull down (RPD_CTL) fuses are burnt on each chip.

Table 5 lists the registers that are used to find the default drive strength and HS termination value by reading from the FUSE_USB_CALIB fuse and the FUSE_USB_CALIB_EXT fuse.

Table 5. FUSE_USB Registers

Register Name	Bit Field	Description
FUSE_USB_CALIB (Address 0x038201F0)		
USB_CALIB	28:23	HS_CURR_LEVEL for USB Port 3
USB_CALIB	22:17	HS_CURR_LEVEL for USB Port 2
USB_CALIB	16:11	HS_CURR_LEVEL for USB Port 1
USB_CALIB	10:7	TERM_RANGE_ADJ for all USB ports
USB_CALIB	5:0	HS_CURR_LEVEL for USB Port 0
FUSE_USB_CALIB_EXT (Address 0x03820350)		
USB_CALIB_EXT	4:0	RPD_CTRL for all USB ports

During the characterization stage, manually adjusting the HS_CURR_LEVEL value should be enough to fulfill compliance requirements. It is possible to try and increase termination as a last resort.

Note: NVIDIA does not recommend customers adjusting termination values. Note that if the TERM_RANGE_ADJ needs to be adjusted, it may result in an impedance mismatch on the board and further attention might be needed.

If modification to HS_CURR_LEVEL is absolutely necessary, it must be done as an offset to the default fused value to account for silicon process differences.

> **!** CAUTION: Do not apply a global overwrite HS_CURR_LEVEL value for all silicon. There is a mechanism provided in software to read fuse USB drive strength and add an offset to it.
> Consult NVIDIA SWPM/CE for additional information

- To change high speed slew rate, write directly to: XUSB_PADCTL_USB2_OTG_PADx_CTL_0_0 bits 8:6
- To change receive squelch level, write directly to: XUSB_PADCTL_USB2_BIAS_PAD_CTL_0_0 bits 2:0
- To compensate for long cable loss, use the XUSB_PADCTL_USB2_OTG_PADx_CTL_3_0 HS_TXEQ/HS_RXEQ bit directly.

HS_CURR_LEVEL Offset Adjustment Procedure

If the default value does not fit customer design, adjust the HS_CURR_LEVEL register in order to pass the USB HS eye diagram.

Follow this procedure:

1. Obtain default value; read register FUSE_USB_CALIB (Address 0x038201F0)
   a). USSB_CALIB[5:0] USB pad HS_CURR_LEVEL[5:0] for Port 0
   b). USSB_CALIB[16:11] USB pad HS_CURR_LEVEL[5:0] for Port 1
   c). USSB_CALIB[22:17] USB pad HS_CURR_LEVEL[5:0] for Port 2
   d). USSB_CALIB[28:23] USB pad HS_CURR_LEVEL[5:0] for Port 3
2. Calculate the offset from fused HS_CURR_LEVEL value and desired value to pass eye mask.
   a). For example, if default value is 0x20 and desired value is 0x1C, then offset = -4
   b). For example, if default value is 0x10 and desired value is 0x14, then offset = +4
3. Adjust HS_CURR_LEVEL register as described in the "Tuning Procedure" section (Note: maximum allowable offset: +/-6 steps).
4. Provide the "tuned offset value" to software team.

Software Verification

NVIDIA recommends a functional check. Connect the DUT to USB hosts and devices to perform a check on functionality.

To check if software has implemented the tuned offset step properly, load new software with offset included into another DUT and check to ensure:

HS_CURR_LEVEL = USB_CALIB + tuned offset steps

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