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Senior Mask Design Layout Engineer | SoC & Full-Chip | Custom & Compiler-Based Memory | Analog & Mixed-Signal

PROFESSIONAL SUMMARY

Layout Design Engineer with 20+ years of experience in SoC, full-chip, custom and compiler-based memory, and analog/mixed-signal layout, delivering robust, high-quality semiconductor designs.

TECHNICAL SKILLS

EDA & Physical Verification Tools:

Cadence: Virtuoso Layout Suite (including Virtuoso Layout Editor (VLE) and Virtuoso XL Editor (VXL))
Synopsys: IC Compiler I, IC Compiler II, Fusion Compiler, Embed-It! Integrator
Physical Verification: DRC, LVS, ERC, RV (Calibre), EM/IR (RedHawk), Various Internal Tools – Project Dependent

Scripting and Automation:

Languages: Basic working knowledge of Perl, TCL, and Python
Scripting: Familiar with writing basic scripts and modifying existing ones to support layout automation.

Version Control Systems:

Tools: Experience with Git, SVN, and Perforce for version control and design repository management

Operating Systems:

UNIX/Linux: Proficient in command-line operations and scripting
Windows: MS Office (Word, Excel, PowerPoint, Outlook)

Process Nodes:

Intel: 22nm, 14nm, 10nm, 7nm, 18A
TSMC: N7, N5

Design and Verification Techniques:

Design Techniques: Standard cell library design, high-density arrayed CMOS analog/mixed-signal layout, custom and compiler SRAM physical layout, SoC and full-chip layout cleanup and optimization
Verification: DRC (Design Rule Checking), LVS (Layout vs. Schematic), ERC (Electrical Rule Checking), RV (Reliability Verification), other quality checks as determined by project/process

Physical Design Summary:

SoC and Full-Chip Design: Extensive experience in SoC and full-chip mask design cleanup and optimization, including partition work, HIP (Hard IP) integration, and complex layout tasks
Memory Design: Proficient in designing and optimizing SRAM, RF, and other memory layouts, ensuring high performance and reliability
Analog and Mixed-Signal: Layout experience developed through early-career roles and project-based support

PROFESSIONAL EXPERIENCE

Intel Corporation, Austin, TX
Mask Designer | November 2008 – November 2024

XDC PHYS & MD LAYOUT / DATA CENTER & AI GROUP
Primary Role: Provided SoC and Full-Chip Mask Design support

- **Physical Design Gage Keeper (PDGK):** Oversaw layout quality, enforcing design standards compliance across multiple projects.
- **Layout Owner Lead:** Coordinated SoC project updates, facilitating issue resolution and efficient team communication.
- **Layout Management:** Tracked partition layout statuses, performed quality checks on HardIPs, documented waivers, and provided actionable feedback to partition owners.
- **Verification Expertise:** Ensured layouts met industry standards through DRC, LVS, and ERC checks; participated in LV Convergence Work Group to test flows for new and existing nodes.
- **EDA Collaboration:** Partnered with internal EDA teams and Synopsys to address tool challenges and improve usability for IC Compiler and Embed-It! Integrator.
- **Cross-Functional Debugging:** Resolved verification issues, supporting seamless integration and compliance with design rules across SoC teams.
- **Leadership & Mentorship:** Led critical design efforts in analog and SoC layouts, mentoring junior designers and sharing best practices.

Key Accomplishments:

- Supported layout for 9+ SoC projects/steppings, contributing from initial design through successful tape-out.
- Supported analog block physical design for integration into SoC floorplans, guided layout review and coordination with junior designers.
- Facilitated the integration of a new memory team using TSMC technology nodes, introducing Intel's memory compiler methodologies to enhance team productivity.
- Established systems for LV reviews and MD cleanup Mode of Work, guiding partition owners on layout quality; led LV reviews and supported tape-in for complex partitions.
- Executed full-chip cleanup for long pole partitions, achieving timely and high-quality tape-in.

CMO (Corporate Memory Organization) / TD (TECHNOLOGY DEVELOPMENT)

Primary Role: Led physical design of custom SRAM EBBs & compiled memory arrays, ensuring high-quality layouts across multiple process nodes.

- **Layout Quality Control:** Ensured high standards in layout quality through all verification flows and integration guidelines.
- **Custom Design:** Designed memory bit arrays, I/O logic cells, control blocks, decoder logic, and transition/halo cells; implemented top-level interconnects for seamless integration.
- **Cross-Functional Collaboration:** Worked with circuit designers and layout teams across locations to deliver top-tier custom and compiled memory arrays.
- **SRAM Compiler Collaboration:** Partnered with SRAM compiler developers to create collateral content, addressing timing, noise, and RV/IR drop challenges.
- **Version Control & Regression Testing:** Managed physical design exports to version-controlled repositories and implemented compiler regressions to streamline workflows.
- **TMG Approval Process:** Collaborated with TMG's SRAM team on bitcell collateral approvals, developing specifications for unique requests.
- **Standard Cell Support:** Assisted the Standard Cell Library team, creating new logic families and performing critical DFM and DR cleanup.

Key Accomplishments:

- Led layout efforts for complex transition rings and halo cells, enabling the assembly of multiple SRAM blocks.
- Improved SRAM array efficiency by reducing level shifter size, optimizing supercell dimensions for area savings.
- Spearheaded approval and release of new bitcell transition collateral, producing specifications in collaboration with senior designers.
- Solved complex layout integration and HIP issues by creating SRAM transition cells and methodologies to enhance compiler functions.
- Owned layout compaction for word line decoders on the 14nm cross-site project, ensuring quality and readiness for tape-in.

DEG (Digital Enterprise Group)

Primary Role: Supported layout of custom mixed-signal circuits under guidance of senior analog designers.

- **Mixed-Signal Support**: Contributed to layout efforts for support blocks in power management and analog interface circuits.
- **Verification & Compliance:** Conducted DRC, LVS, and ERC checks, ensuring layouts met stringent quality and compliance standards.
- **Cross-Disciplinary Collaboration:** Worked closely with analog design engineers to translate requirements into efficient, high-quality layouts.
- **Performance Optimization:** Enhanced layouts for optimal performance, matching accuracy, and parasitic reduction.
- **Documentation & Reporting:** Maintained comprehensive documentation and provided clear reports to stakeholders, supporting transparency and project alignment.
- **Continuous Improvement:** Actively supported team objectives and demonstrated a commitment to expanding technical skills.

Key Accomplishments:

- Provided reliable support for analog layout tasks while building foundational skills in physical design.
- Implemented layout optimizations that minimized parasitic effects, improving circuit performance and reliability.

Universal CADWorks, Inc., Dallas, TX

Analog Mask Designer | January 2008 – November 2008

Supported analog layout design for Texas Instruments projects, including cell and block-level layout using Cadence Virtuoso, VXL, and VCR. Generated and verified regression cells for DRC deck testing, contributing to quality assurance for internal physical verification flows.

Cirrus Logic, Inc., Austin, TX

Analog IC Layout Designer | April 2005 – April 2007

Designed custom analog layouts at the cell and block level using Cadence Virtuoso, VXL, and VCAR. Completed full layout flows from schematic through tape-out, including two all-layer chip revisions. Performed DRC, LVS, and ERC verification while optimizing layouts for area, matching, electro-migration compliance, and parasitic reduction. Developed and maintained four new standard cell libraries to support evolving place-and-route technologies.

U.S. Navy / Naval Reserve

Aircraft Engine Mechanic / Naval Aircrew (Loadmaster) | May 1990 – April 1997

Performed advanced mechanical and electromechanical maintenance on aircraft propulsion systems including the Allison T-56-A-14 turboprop and Rolls Royce MK611-8 turbofan. Maintained critical fuel, lubrication, electrical, and hydraulic subsystems, applying engineering principles in high-stakes operational environments. Conducted inspections and diagnostics on P-3 Orion and C-20G Gulfstream IV aircraft, resolved complex system faults using technical schematics and manuals, and ensured readiness through systems-level troubleshooting. Served as a Naval Aircrew Loadmaster during deployment, managing cargo calculations and aircraft safety protocols.

EDUCATION & MILITARY EXPERIENCE

United States Navy
Rating: Aviation Machinist's Mate (AD)
Years of Service: 1990 – 1994
Combat Veteran – Operation Desert Storm

United States Naval Reserve
Rating: Aviation Machinist's Mate (AD) & Naval Aircrewman (Loadmaster)
Years of Service: 1994– 1997

Integrated Circuit Layout & Design Specialization
Austin Community College, Austin, TX
Completed coursework toward specialization before being hired into industry