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Senior Layout Engineer | SoC | Custom & Compiler-Based Memory | Analog & Mixed-Signal

PROFESSIONAL SUMMARY

Senior Layout Engineer with 20+ years of experience delivering high-quality semiconductor designs across SoC, full-chip, memory, and analog/mixed-signal domains. Proven contributor to top-level integration and block-level physical implementation, with hands-on experience in ICC-based PnR environments contributing to cleanup, congestion debug, and SoC-level integration. Currently transitioning into a Physical Design Engineering role, building on a foundation of hands-on integration, quality ownership, and close collaboration with RTL, CAD, and circuit design teams.

TECHNICAL SKILLS

EDA & Physical Verification Tools

Cadence

- Virtuoso Layout Suite, including Virtuoso Layout Editor (VLE) and Virtuoso XL Editor (VXL)

Synopsys

- IC Compiler I / II, Fusion Compiler (GUI-based layout support for cleanup, congestion debug, and constraint review)

Physical Verification

- Calibre DRC, LVS, ERC, Reliability Verification (RV)
- RedHawk (IR/EM debug and reliability handoff support)
- STAR-RC (used in parasitic extraction checks and STA-driven layout fixes)
- CB2/Clock Health Checks, Analog Health Checks, and other project-specific verification flows/tools

Layout Design

- Device- and IP-level floorplanning and layout integration (e.g., Analog blocks, SRAM arrays)
- SoC-level layout cleanup and constraint-driven fixes across partition boundaries in collaboration with design and integration teams
- Applied constraint-driven fixes in collaboration with design and integration teams for clean physical handoff
- Layout experience across all levels: standard cell/leaf cell, block-level, Hard IP, partition-level, and full-chip (FCL/SoC)

Scripting and Automation

- TCL, Perl, Python – Edited existing scripts to support layout automation, implant fill, debug views, and flow integration

Version Control Systems

Tools

- Git, SVN, Perforce for version control and design repository management
- Windows and Linux tools for documentation and collaboration (Excel, Word, PowerPoint, OneNote, SharePoint)

PROFESSIONAL EXPERIENCE

Intel Corporation – SoC Mask Designer / SoC Layout Quality & Signoff Lead
XDC PHYS & MD LAYOUT / Data Center & AI Group | 2018 – 2024
Key Projects:
Supported multiple steppings of SNR, ICX, GNRIO, GNR, SRF, CWF, KNC, and DMR as SoC Mask Design support, Physical Design Gage Keeper (PDGK), and Layout Quality Reviewer for 1p0 tape-in milestones

- Served as Physical Design Gage Keeper (PDGK) for multiple SoC projects, leading partition-level layout signoff, constraint enforcement, and tape-in readiness reviews
- Implemented timing fixes through buffer insertion, routing optimization, and power-aware layout updates to resolve congestion and improve post-CTS layout quality
- Implemented IR/EM-driven layout fixes based on RedHawk feedback, including routing/via adjustments and strap improvements, generated heat maps to support partition debug and congestion analysis
- Diagnosed and fixed tool-generated layout issues during partition construction, manually inserting taps, diodes, and GNACs to resolve antenna violations, ensure coverage, and align with methodology requirements
- Identified layout issues caused by construction flow and tool misbehavior (e.g., via ladder misconfigurations); escalated to DA and flow owners for script and recipe updates to prevent recurring signoff violations
- Conducted post-verification layout reviews for partition-level violations; resolved interface DRCs and routing issues across block boundaries and hard IP to ensure clean handoff to SoC layout integration
- Managed SoC-level waiver documentation for tape-in, investigating violations across hierarchy boundaries, validating waiver applicability, and ensuring alignment with signoff criteria during final SoC review

- Analyzed and tracked milestone drops for Hard IPs delivered to SoC; reviewed stand-alone and integrated views to identify violations, interface issues, and gaps in documentation or waiver coverage

Intel Corporation – Senior Memory Mask Designer / CMO (Corporate Memory Organization) | 2010 – 2018

- Led layout of custom and compiled SRAM across multiple nodes, including arrays, control logic, halo/transition cells, and I/O
- Planned layout integration, power routing, and compaction across IP boundaries, aligned with copy-exact and foundry-defined constraints
- Designed transition rings to align non-lego arrays with standard cell pitch for SoC-level floorplan compatibility
- Validated compiler builds across corner cases, executed regressions, and resolved array-level DRCs with compiler and circuit teams
- Owned Calibre signoff flows (DRC, LVS, ERC, Antenna, Density) for memory collateral prior to SoC handoff
- Collaborated with TMG and litho teams on copy-exact cell updates to improve array compactness and routing

Intel Corporation – Senior Analog Mask Designer / DEG (Digital Enterprise Group) | 2008 – 2010

- Supported cell- and block-level custom layout for analog interface and power management circuits in a mixed-signal environment
- Performed DRC, LVS, and ERC verification and implemented fixes to meet physical design constraints
- Gained initial experience with Intel's internal block-level P&R tool (EDEN) for Hard IP layout implementation
- Built foundational skills in physical verification, constraint-driven layout, and schematic integration that supported later SoC-level physical design work

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Universal CADWorks, Inc. – Analog Layout Engineer
Dallas, TX | January 2008 – November 2008

- Supported analog IC layout for Texas Instruments projects at the cell and block level using Cadence Virtuoso (VXL and VCR)
- Performed layout verification using DRC and LVS flows, with iterative updates to meet project constraints and design rules
- Designed and validated regression cells to stress-test DRC rule decks; identified false violations and collaborated directly with deck authors to resolve mismatches between rule intent and implementation
- Gained experience in constraint-driven layout cleanup and collaborative debug of verification violations, building a foundation for structured physical design work

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Cirrus Logic, Inc. – Analog IC Layout Engineer
Austin, TX | April 2005 – April 2007

- Executed full custom layout flows from schematic to tape-out for analog and mixed-signal IP using Cadence Virtuoso (VXL/VCAR)
- Designed cell- and block-level analog layouts focused on area efficiency, matching, parasitic control, and EM reliability
- Developed layouts for integration into mixed-signal environments, ensuring compatibility with digital interfaces and top-level floorplans
- Collaborated with circuit designers to meet performance, integration, and design-for-reuse requirements across multiple chip revisions
- Performed DRC, LVS, and ERC signoff checks; supported QA efforts to ensure layout compliance and tape-in readiness
- Validated layout rule decks and implemented constraint-driven layout flows in coordination with EDA and CAD teams
- Developed and maintained four new standard cell libraries to support physical design enablement for digital-analog co-design

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U.S. Navy – Aviation Propulsion Systems Engineer
Rating: Aviation Machinist – AD, Naval Aircrew Loadmaster
Active Duty: 1990–1994 • Reserve: 1994–1997
Technical Training and Operational Systems Experience Equivalent to Formal Engineering Education

- Completed intensive military training in aircraft propulsion, power systems, hydraulics, fuel control, and electrical subsystems; applied this knowledge in high-reliability, mission-critical operational environments
- Served as a primary maintenance technician for turboprop and jet engine platforms (Allison T-56-A-14 and Rolls Royce MK611-8), performing diagnostics, system-level fault isolation, and full rebuild procedures
- Developed expertise in interpreting complex technical schematics, wiring diagrams, and system routing under performance-critical conditions
- Completed formal Loadmaster training and certified as Naval Aircrew; performed technical flight readiness procedures including aircraft weight and balance calculations, cargo configuration, and airborne safety planning in accordance with strict engineering and safety protocols
- Gained foundational experience in systems engineering, cross-disciplinary communication, and hands-on problem-solving in high-pressure environments

EDUCATION & MILITARY EXPERIENCE

United States Navy
Rating: Aviation Machinist's Mate (AD)
Years of Service: 1990 – 1994
Combat Veteran – Operation Desert Storm

United States Naval Reserve
Rating: Aviation Machinist's Mate (AD)
& Naval Aircrewman (Loadmaster)
Years of Service: 1994– 1997

Integrated Circuit Layout & Design Specialization
Austin Community College, Austin, TX
completed relevant coursework